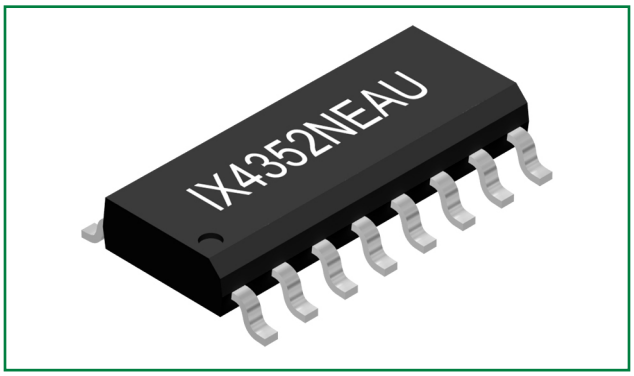
IX4352NEAU

9 A Low Side SiC MOSFET and IGBT Driver



Features

- AEC-Q100 qualified
- Separate 9A peak source and sink outputs
- Operating Voltage Range: V_{DD} - V_{SS} up to 35 V
- AEC-Q100 Operating Temperature Grade 1: −40 °C to +125 °C
- AEC-Q100 Human Body Model (HBM) ESD Classification 2: ±2 kV
- Internal charge pump regulator for selectable negative gate drive bias
- Desaturation detection with soft shutdown sink driver
- TTL and CMOS compatible input
- Under Voltage lockout (UVLO)
- Thermal shutdown
- Open drain FAULT output

Applications

- On-board chargers
- DC-DC converters
- Electric vehicle charging stations
- Motor controllers
- Power inverters

Description

The IX4352NEAU gate driver is designed specifically to drive SiC MOSFETs and high power IGBTs. Separate 9 A source and sink outputs allow for tailored turn-on and turn-off timing while minimizing switching losses. An internal negative charge regulator provides a user-selectable negative gate drive bias for improved dV/dt immunity and faster turn-off.

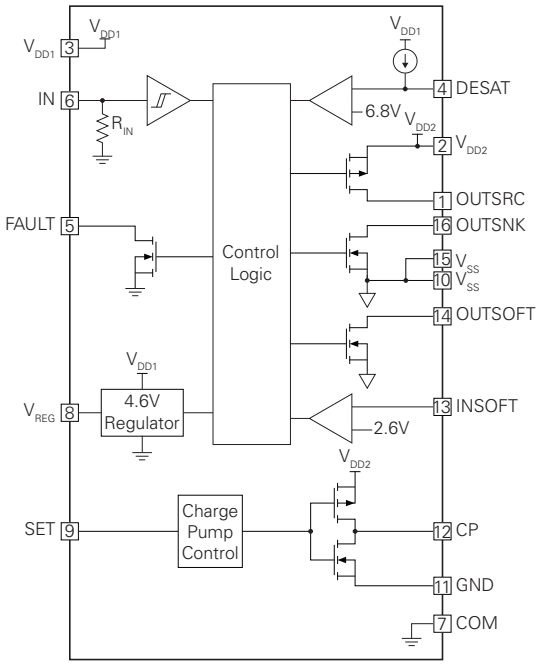
Desaturation detection circuitry senses an over-current condition of the SiC MOSFET and initiates a soft turn off, thus preventing a potentially damaging dV/dt event. The non-inverting logic input, IN, is TTL and CMOS compatible; internal level shifters provide the necessary bias to accommodate negative gate drive bias voltages. Additional protection features include UVLO detection and thermal shutdown. An open drain FAULT output signals a fault condition to the microcontroller.

The IX4352NEAU is AEC-Q100 Grade1 rated for an operational ambient temperature range of −40 °C to +125 °C, and is available in a thermally-enhanced 16-pin narrow SOIC package.

Ordering Information

Part Number	Description
IX4352NEAU	16-Pin narrow SOIC with exposed bottom side pad. In tubes: (50/Tube)
IX4352NEAUTR	16-Pin narrow SOIC with exposed bottom side pad. In Tape & Reel: (2000/Reel)

IX4352NEAU Functional Block Diagram



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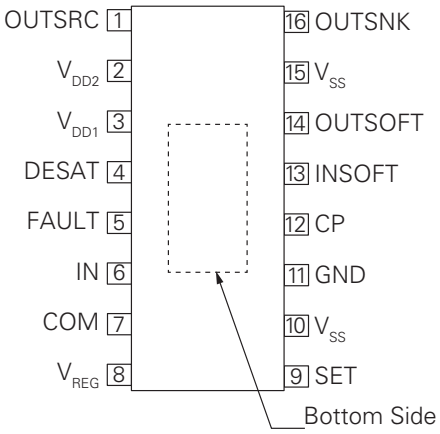
1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin	Name	Type	Description
1	OUTSRC	Output	Gate driver, source.
2	V_{DD2}	Power	Positive supply voltage for driver and charge pump outputs. Connect to pin 3 (V_{DD1}).
3	V_{DD1}	Power	Positive supply voltage for logic and control circuits. Connect to pin 2 (V_{DD2}).
4	DESAT	Input	Sense input for desaturation detection.
5	FAULT	Output	Fault status, Open-Drain, active low.
6	IN	Input	Logic input.
7	COM	Power	Common ground connection. Connect to GND.
8	V_{REG}	Output	4.6 V regulator output.
9	SET	Input	Charge pump control.
10, 15	V_{SS}	Power	Negative supply voltage. Connect pin 10 to pin 15 on the PCB.
11	GND	Power	Charge pump ground connection. Connect to COM.
12	CP	Output	Charge pump output.
13	INSOFT	Input	Soft Shutdown sense input.
14	OUTSOFT	Output	Gate driver, Soft Shutdown sink.
16	OUTSNK	Output	Gate driver, sink.
—	Exposed Pad	Thermal	It is highly recommended the exposed pad be connected to V_{SS}. Alternatively, it may be allowed to float, but must not be connected to any other signal or net.

1.3 Absolute Maximum Ratings

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Unless otherwise specified all voltages are with respect to COM, electrical ratings are over the operational ambient temperature range, and $V_{DD} = V_{DD1}$ connected to V_{DD2}.

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Positive Supply Voltage	V_{DD}	–0.3	32	V
Negative Supply Voltage	V_{SS}	V_{DD} - 40	0.5 [1]	V
Supply Voltage Range	V_{DD} - V_{SS}	-0.3	40	V
Ground Separation	V_{GND}	—0.3	+0.3	V
Gate Drive Output Voltage	V_{OUTSRC}, V_{OUTSNK}, $V_{OUTSOFT}$	V_{SS} - 0.3	V_{DD2} + 0.3	V
Gate Drive Output Current	I_{OUTSRC}, I_{OUTSNK}	—	±9	A_P
	$I_{OUTSOFT}$	—	1	
IN Input Voltage	V_{IN}	–0.3	7	V
DESAT Input Voltage	V_{DESAT}	–0.3	V_{DD1}+ 0.3	V
SET Input Voltage	V_{SET}	–1	7	V
FAULT Output Voltage	V_{FAULT}	–0.3	V_{DD1}+ 0.3	V
Regulator Output Voltage	V_{REG}	–0.3	7	V
ESD Rating Human Body Model (HBM)	V_{ESD}	–2	+2	kV
Junction Temperature	T_J	–55	+150	°C
Storage Temperature	T_{STG}	–55	+150	°C

[1] The current into V_{SS} must never exceed 1 mA.

1.4 Recommended Operating Conditions

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Positive Supply Voltage ($V_{DD1} = V_{DD2} = V_{DD}$)	V_{DD}	13	25	V
Negative Supply Voltage	V_{SS}	–3.5	–10	V
Input Voltage	V_{IN}	0	5.5	V
Operating Ambient Temperature	T_A	–40	+125	°C

1.5 Electrical Characteristics

Typical values are characteristic of the device at T_A = 25 °C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Unless otherwise specified, all voltages are referenced to COM, electrical characteristics are guaranteed at: $V_{DD1} = V_{DD2} = V_{DD} = 20V$, $V_{SS} = -5V$, $V_{GND} = 0V$, $V_{INH} = 5V$, $V_{INL} = 0V$, $C_{DD} = C_{REG} = 4.7\,\mu F$, $C_{SS} = 10\,\mu F$, and $-40\,°C \le T_A \le +125\,°C$.

1.5.1 V_{DD}

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Operating Supply Current	f_{IN} = 100 kHz, V_{SET} = 0.4 V, C_{LOAD} = 2.2 nF	I_{DD}	—	19	—	mA
Quiescent Supply Current	V_{IN} = 0 V, V_{SET} = −0.4 V, No load	I_{DDQ}	—	2.9	4.4	mA
UVLO Rising Threshold	V_{DD} Rising	V_{DDUV_th}	10	12	13	V
UVLO Hysteresis	V_{DD} Falling	V_{DDUV_hys}	—	2	—	V

1.5.2 V_{REG}

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Regulator Output Voltage	I_{REG} = −5 mA	V_{REG}	4.2	4.6	5	V
Line Regulation	15 V < V_{DD} < 25 V, I_{REG} = -5 mA	ΔV_{REG}	—	0.1	0.2	V
Load Regulation	−1 mA ≤ I_{REG} ≤ −10 mA		—	0.1	0.4	V

1.5.3 Charge Pump and V_{SS}

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
UVLO Negative Threshold	V_{SS} Increasing	V_{SSUV_th-}	−1	−2.2	−3.5	V
UVLO Positive Threshold	V_{SS} Decreasing	V_{SSUV_th+}	−2	−1.2	−0.1	
Average V_{SS} Current	C_{CP} = 68 nF, R_{CP} = 33 Ω	I_{SS}	—	—	50	mA
Charge Pump Frequency	V_{SET} = +0.4 V	f_{OSC}	90	125	160	kHz
Charge Pump Enable Threshold	—	V_{SET_th}	30	110	250	mV
SET Input Leakage Current	V_{SET} = 0 V, V_{SET} = 5 V	I_{SET}	—	<10	—	nA

1.5.4 Desaturation

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
DESAT Source Current	V_{DESAT} = 0 V	I_{DESAT}	400	570	750	µA
DESAT Detect Threshold Voltage	—	V_{DESAT_th}	6	6.9	8.2	V
Blanking Time	C_{BLANK} = 0 µF	t_{BLANK}	—	250	—	ns
DESAT Pull Down On-Resistance	V_{IN} = 0 V	R_{DESAT_on}	—	900	—	Ω

1.5.5 Thermal Shutdown

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Thermal Shutdown Temperature	—	T_{TSD_th}	—	160	—	°C
Thermal Shutdown Hysteresis	—	T_{TSD_hys}	—	20	—	

1.5.6 IN

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Input Voltage						
Logic Level High	—	V_{IH}	2.3	—	—	V
Logic Level Low		V_{IL}	—	—	1	
Hysteresis		V_{I_hys}	0.2	0.4	—	
Input Current						
High Level	V_{IH} = 5 V	I_{IH}	—	55	70	µA
Low Level	V_{IL} = 0 V	I_{IL}	—	—	—	
Input Pull-Down Resistance	V_{IN} = 5 V	R_{IN}	—	110	—	kΩ

1.5.7 FAULT

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Output Low Voltage	I_{FAULT_OL} = 20 mA	V_{FAULT_OL}	—	—	0.8	V
Output Leakage Current	V_{FAULT} = 20 V	I_{FAULT}	—	0.1	10	µA
DESAT Detect to FAULT Propagation Delay	—	t_{FAULT_pZL}	—	152	—	ns
MUTE Pulse Width	DESAT Detect = TRUE	t_{MUTE}	—	2	—	ms

1.5.8 Soft Shutdown

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Soft Shutdown Threshold Voltage	INSOFT Falling	V_{INSOFT_th}	2.3	2.6	3.2	V
Soft Shutdown Hysteresis	—	V_{INSOFT_hys}	—	0.4	—	V
OUTSOFT Peak Sink Current	—	$I_{OUTSOFT}$	—	900	—	mA
OUTSOFT On-Resistance	$I_{OUTSOFT}$ = 100 mA	$R_{OUTSOFT\_on}$	—	5.92	15	Ω
DESAT Detect to OUTSOFT Propagation Delay	—	$t_{OUTSOFT\_pZL}$	—	125	—	ns

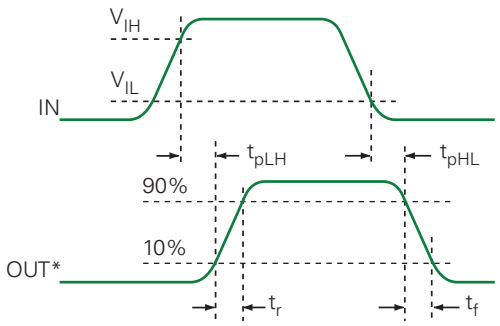
1.5.9 Gate Drive Output

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
High Level Output Voltage	I_{OUTSRC} = –100 mA	V_{OUTSRC}	V_{DD2} – 0.2	—	—	V
Low Level Output Voltage	I_{OUTSNK} = 100 mA	V_{OUTSNK}	—	—	V_{SS}+0.15	
OUTSRC On-Resistance	I_{OUTSRC} = –100 mA	R_{OUTSRC_on}	—	1.17	2	Ω
OUTSNK On-Resistance	I_{OUTSNK} = 100 mA	R_{OUTSNK_on}	—	0.79	1.5	
Turn-On Propagation Delay Time	C_{LOAD} = 1 nF	t_{pLH}	—	70	125	ns
Turn-Off Propagation Delay Time	C_{LOAD} = 1 nF	t_{pHL}	—	65	125	
Rise Time	C_{LOAD} = 1 nF	t_r	—	10	20	
Fall Time	C_{LOAD} = 1 nF	t_f	—	10	20	

1.6 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Impedance, Junction to Ambient	θ_{JA}	60	°C/W
Thermal Impedance, Junction to Case	θ_{JC}	28	°C/W

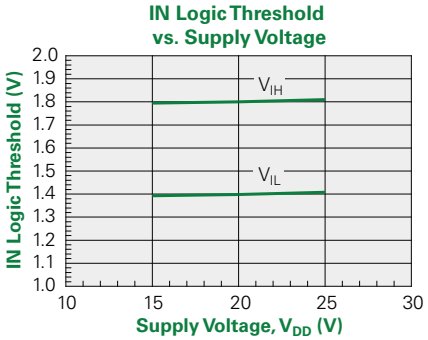
1.7 Timing Diagram

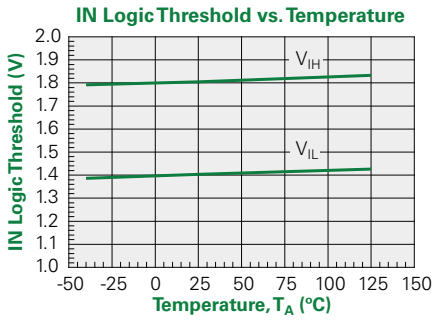


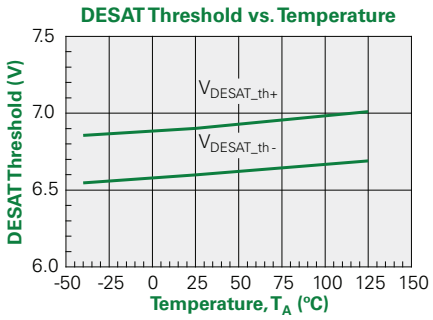
** OUT is the node formed by connecting OUTSRC, OUTSNK and OUTSOFT together.*

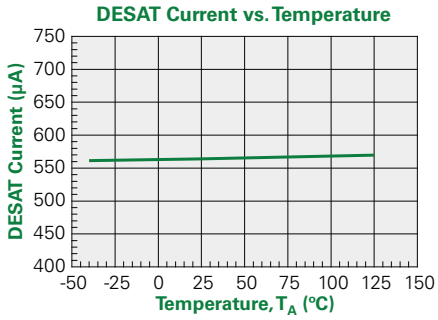
2 Performance Data

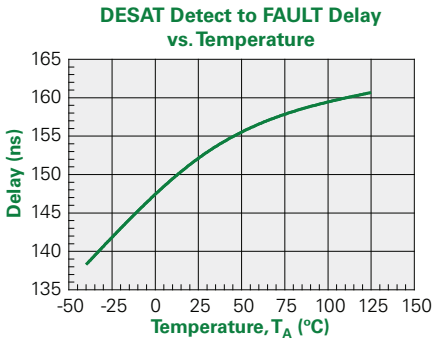
Unless otherwise noted, V_{DD} = 20 V, V_{IL} = 0 V, V_{IH} = 5 V, R1 = 40.2 kΩ, R2 = 44.2 kΩ, R_{CP} = 33 Ω, C_{CP} = 68 nF, T_A = 25 °C, and values are typical. Component locations are as shown in "Figure 1 IX4352NEAU Typical Application Circuit" on page 11. "V_{SS}(ext)" is the voltage applied to V_{SS} with the charge pump disabled and "V_{SS} (measured)" is at T_A = 25 °C.

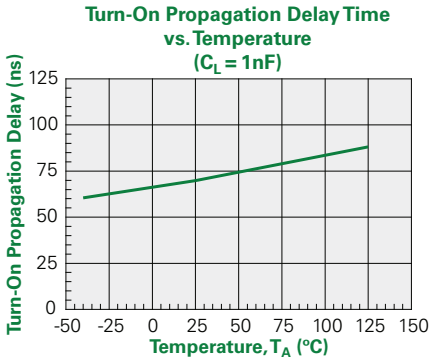


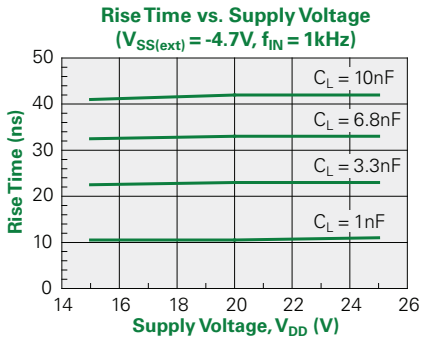


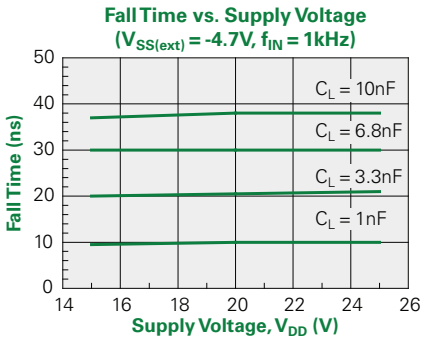


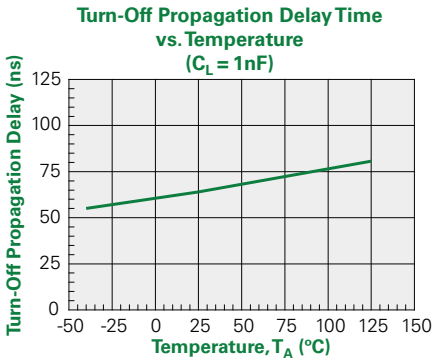


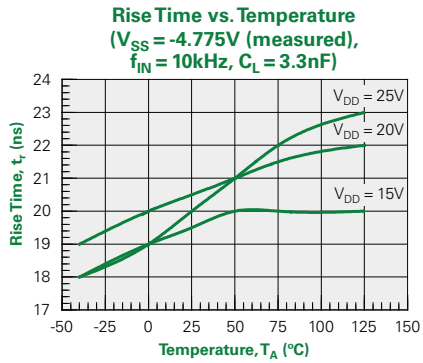


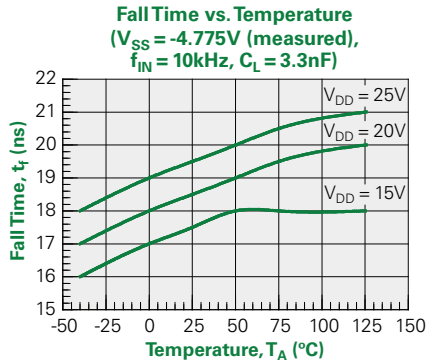




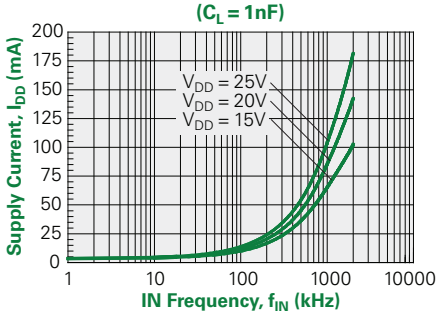




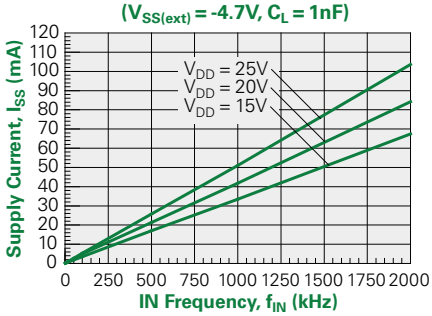




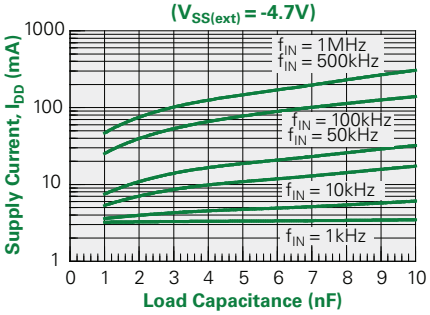
V_{DD} Supply Current vs. IN Frequency (C_L = 1nF)



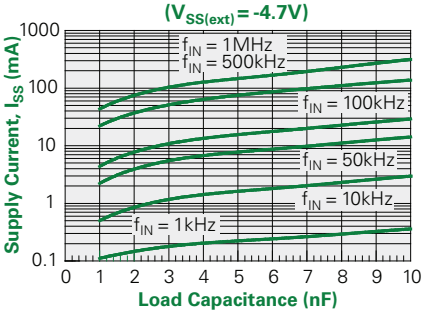
V_{SS} Supply Current vs. IN Frequency ($V_{SS(ext)}$ = -4.7V, C_L = 1nF)



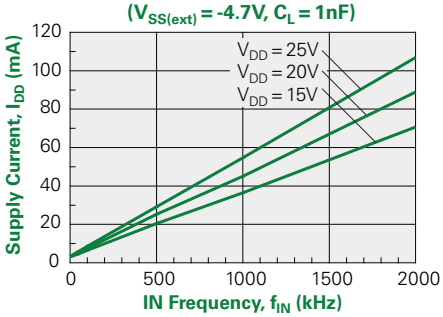
V_{DD} Supply Current vs. Load Capacitance ($V_{SS(ext)}$ = -4.7V)



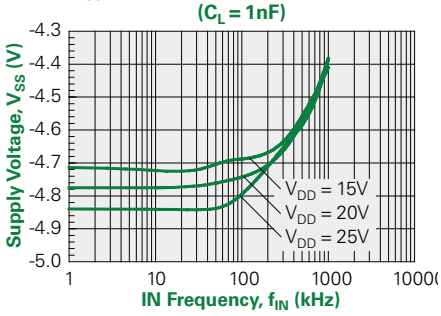
V_{SS} Supply Current vs. Load Capacitance ($V_{SS(ext)}$ = -4.7V)



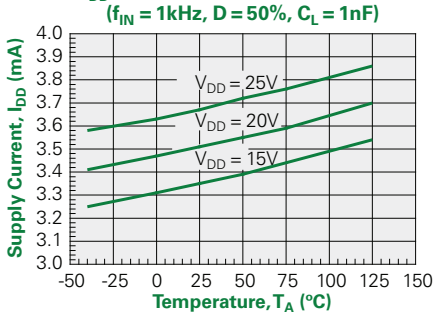
V_{DD} Supply Current vs. IN Frequency ($V_{SS(ext)}$ = -4.7V, C_L = 1nF)



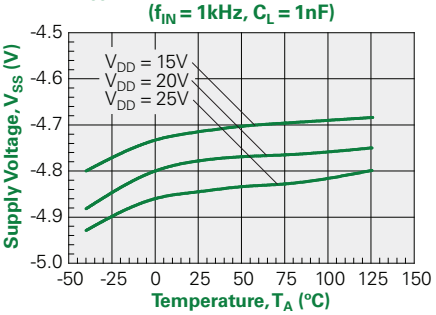
V_{SS} Supply Voltage vs. IN Frequency (C_L = 1nF)



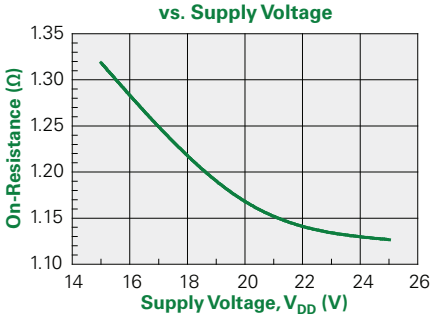
V_{DD} Supply Current vs. Temperature (f_{IN} = 1kHz, D = 50%, C_L = 1nF)



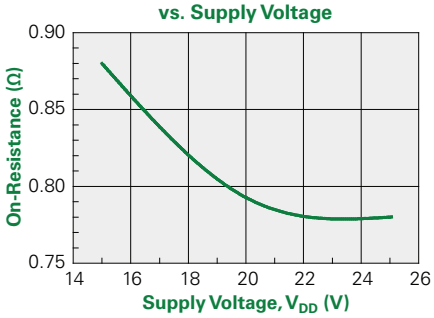
V_{SS} Supply Voltage vs. Temperature (f_{IN} = 1kHz, C_L = 1nF)



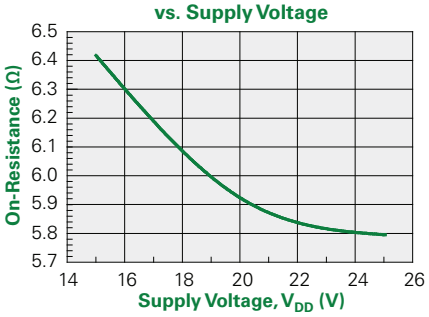
OUTSRC On-Resistance vs. Supply Voltage



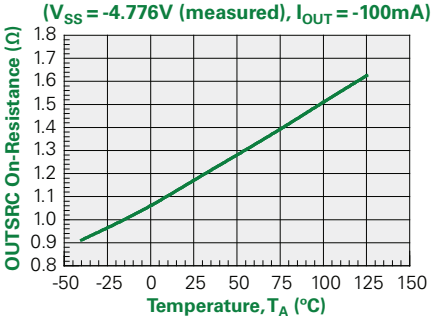
OUTSNK On-Resistance vs. Supply Voltage



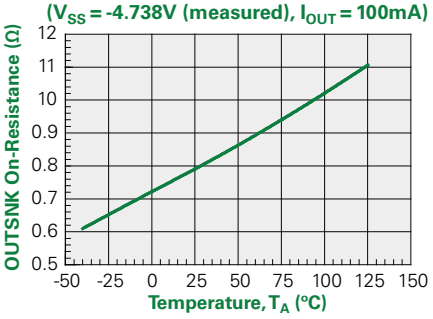
OUTSOFT On-Resistance vs. Supply Voltage



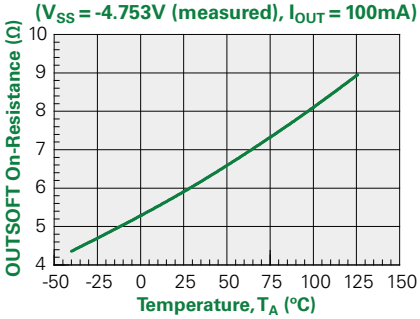
OUTSRC On-Resistance vs. Temperature (V_{SS} = -4.776V (measured), I_{OUT} = -100mA)



OUTSNK On-Resistance vs. Temperature (V_{SS} = -4.738V (measured), I_{OUT} = 100mA)



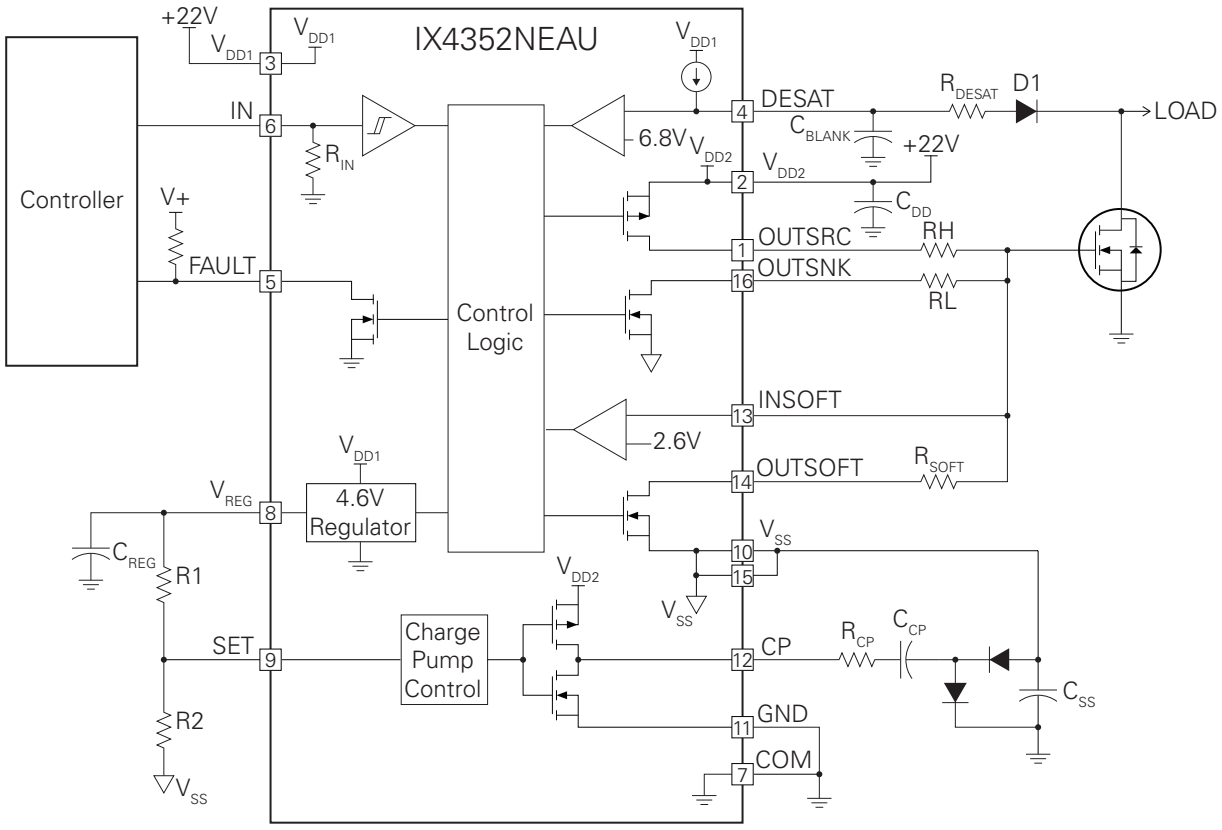
OUTSOFT On-Resistance vs. Temperature (V_{SS} = -4.753V (measured), I_{OUT} = 100mA)



3 Functional Description

The IX4352NEAU is designed to provide the gate drive for high power SiC MOSFETs and IGBTs.

Figure 1 IX4352NEAU Typical Application Circuit



3.1 Power Supplies

The IX4352NEAU requires only a single positive supply (V_{DD}) to provide SiC and IGBT gate driver functionality by generating the negative supply voltage (V_{SS}) required to efficiently turn off SiC and IGBT power switches. V_{DD} provides the supply voltage for both V_{DD1} at pin 3 and V_{DD2} at pin 2. V_{DD1} is the logic and control circuitry supply voltage while V_{DD2} is the positive supply for OUTSRC and the charge pump. In order to minimize coupling of the noise generated by transitions of OUTSRC and the charge pump to the logic and control circuits, V_{DD1} and V_{DD2} are not internally connected. Therefore it is important these two supply pins be tied together on the printed circuit board to ensure $V_{DD1} = V_{DD2}$. An on-board regulator provides the low voltage supply (V_{REG}) used by the internal control logic while the on-board charge pump generates the pulses necessary to create V_{SS}, the negative supply voltage.

3.2 Logic Input (IN)

IN, the gate driver logic input, is a TTL and CMOS logic level compatible high-speed Schmitt trigger buffer that controls the gate driver outputs: OUTSRC, OUTSNK, and OUTSOFT. The input voltage logic thresholds have a nominal 400 mV of hysteresis and are referenced to COM. On startup, after V_{DD} and V_{SS} exceed their Under Voltage Lock Out thresholds and under non-fault operating conditions, IN controls the state of the gate driver outputs according to the table below:

IN Gate Control Truth Table

IN	OUTSRC	OUTSNK	OUTSOFT
0	Off (Hi-Z)	On (Low)	On (Low)
1	On (High)	Off (Hi-Z)	Off (Hi-Z)

3.3 Gate Drive Outputs

The IX4352NEAU has three gate drive outputs. Two power outputs, OUTSRC and OUTSNK, are each rated for a maximum peak current of 9 A while the third output, OUTSOFT, is rated for a typical peak current of 900 mA. Separate source and sink high current outputs allow independent adjustment of the discrete power SiC MOSFET or IGBT turn-on and turn-off transactions by means of a single resistor for each output. An internal non-adjustable dead time prevents cross conduction of the

source and sink outputs.

During normal operation whenever IN, the gate control input, is driven to a logic low the lower rated current sink output, OUTSOFT, turns on concurrently with OUTSNK. These operations can be seen in "Figure 2 Logic Diagram" on page 13. In the logic diagram these normal operation transactions can be seen in the first high-to-low transition of IN.

3.4 Internal 4.6 V Regulator (V_{REG})

An internal 4.6 V regulator provides power for the IX4352NEAU low voltage control circuitry and requires an external 4.7 µF bypass capacitor (C_{REG}). Capable of sourcing up to 10mA, V_{REG} is utilized to set the negative supply voltage level and optionally to power the LED of an external optocoupler.

3.5 Negative Supply Voltage (V_{SS}) Generation

The IX4352NEAU voltage inverting charge pump circuitry outputs V_{SS}, a regulated negative supply voltage. Operating in a closed-loop mode, the charge pump generates V_{SS} from V_{DD} with regulation being achieved by sensing the V_{SS} voltage with respect to V_{REG} at the SET input by means of the resistor divider R1 and R2. See "Figure 1 IX4352NEAU Typical Application Circuit" on page 11 for the circuit configuration. The charge pump inverter requires five external components: two discrete diodes, two ceramic capacitors, and a peak output current limiting resistor (R_{CP}). For V_{DD} = 20 V, V_{SS} is set by the R1 and R2 resistor divider given in the following equation:

$$V_{SS} = -(V_{REG} - V_{SET}) \bullet \frac{R2}{R1} + V_{SET}$$

Setting V_{REG} = 4.66 V (the typical open circuit voltage) and V_{SET} = 0.11 V, the equation reduces to:

$$V_{SS} = -4.55 \bullet \left(\frac{R2}{R1}\right) + 0.11 \quad \text{(Where R1+R2 ~ 100kΩ)}$$

To improve efficiency, low leakage Schottky diodes may be used in the charge pump voltage inverter circuitry.

The recommended value of the charge pump inverter components is:

1. R_{CP} = 33 Ω
2. C_{CP} = 68 nF
3. C_{SS} = 10 µF

To prevent damaging the charge pump output and minimize power dissipation, the value of R_{CP} must not be reduced.

To ensure a negative voltage gate bias under all operating conditions, the charge pump is always active whenever the V_{DD} UVLO is cleared.

For applications where an external V_{SS} supply is available and preferred, the following steps need to be taken:

1. Connect the external negative supply to V_{SS} at pins 10 and 15.
2. Connect SET to COM to deactivate the charge pump.
3. Leave the charge pump output, CP, pin 12, open.

When using an external negative voltage supply, it is important not to exceed the V_{SS} voltage and current limitations.

3.6 Desaturation Detection and Protection

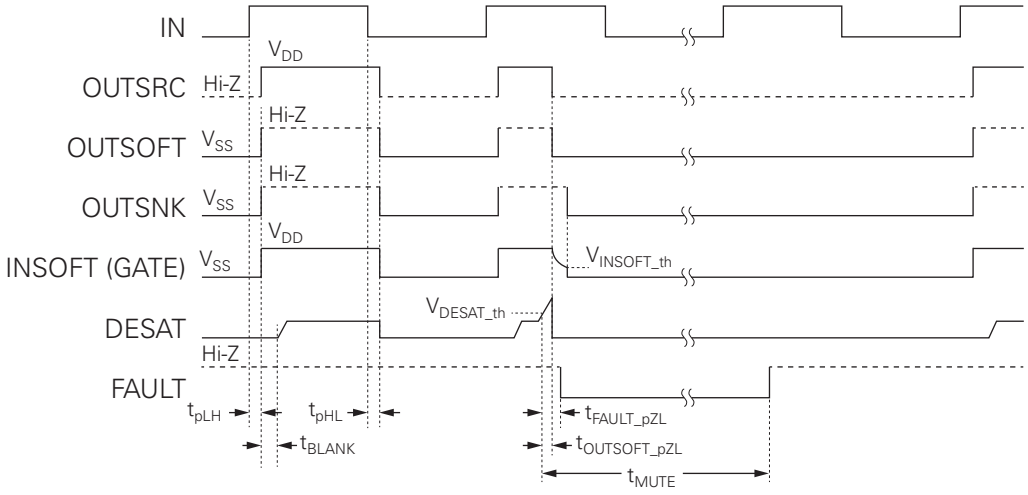
DESAT detection occurs when the SiC or IGBT power transistor goes into an over-current condition causing the voltage across the transistor to exceed a predetermined threshold chosen by the designer. When the power switch is in an overcurrent situation, the desaturation protection circuit ensures the safety of the external SiC MOSFET or IGBT during turn-off.

The DESAT pin monitors the voltage across the power transistor via the input circuitry between the DESAT input and the SiC MOSFET drain or the IGBT collector. When the sum of the drain or collector voltage plus the voltage drop of the DESAT input circuitry exceeds the DESAT Threshold Voltage (V_{DESAT_th}), typically 6.8 V, the FAULT output goes low, the internal MUTE function is activated and a controlled turn-off sequence is initiated. OUTSRC is turned off and OUTSOFT is turned on. The OUTSOFT 900 mA sink capability provides an initial slow turn-off of the external SiC MOSFET or IGBT. When the GATE voltage decreases to the Soft Shutdown Threshold Voltage (V_{INSOFT_th}), typically 2.6 V, OUTSNK turns on and quickly pulls the GATE to V_{SS}. This two-step turn-off avoids dangerous dV/dt transient over-voltage spikes across the external SiC MOSFET or IGBT.

When a DESAT fault is detected, the MUTE feature is activated. MUTE holds the FAULT output low and masks logic transitions applied to IN for a nominal 2 ms duration. Once the MUTE timer expires, FAULT is released and the input will begin normal operation with the next low to high transition of IN. During the DESAT fault event, transitioning IN from high to low anytime during MUTE will not affect the soft shutdown sequence or resumption of normal operation.

The DESAT detection and two-step turn-off sequence is illustrated in "Figure 2 Logic Diagram" on page 13. In the logic diagram, this sequence begins with the second rising edge of IN.

Figure 2 Logic Diagram



To avoid a false desaturation detect event when the external SiC MOSFET or IGBT is turned on, the IX4352NEAU provides a nominal 250 ns DESAT detect blanking time (t_{BLANK}) beginning when OUTSRC transitions from OFF
(Hi-Z) to ON (High) causing the gate drive output voltage to rise. While OUTSRC is off, the DESAT input is internally pulled low. To accomplish the fixed internal blanking time and to precondition the DESAT input for the fully turned on SiC MOSFET or IGBT, an internal pull down MOSFET at the DESAT input remains active for the duration of the blanking period.

For applications where the IX4352NEAU is not used to perform the DESAT fault detection voltage measurement, the DESAT input at pin 4 must be properly conditioned to prevent false detects and the subsequent shutdown procedure by the internal circuitry. The simplest solution is to use a low-value resistor from the DESAT input to COM that will ensure the voltage across the pull down resistor is sufficiently lower than the minimum detect threshold limit to provide noise immunity without the need for a noise suppression capacitor.

Although the nominal internal blanking duration is fixed at 250 ns it can be extended by means of an external capacitor, C_{BLANK}, installed from the DESAT input to COM. Once the internal pull down is released, the additional blanking duration is set by the time it takes to charge the total external capacitive loading of the DESAT input up to V_{DESAT_th}. The value of C_{BLANK} is the difference between the total capacitance required to obtain the desired blanking period less the capacitive loading of the other components on DESAT.

3.7 DESAT Input Component Selection

The value of R_{DESAT} is determined by the peak surge current permitted through diode D1 and the maximum voltage across the external power transistor. When IN is high and the power SiC MOSFET is on, the voltage at the DESAT input is calculated by the following equation:

$$V_{DESAT} = I_{DESAT} \bullet R_{DESAT} + V_f + V_{DS}$$

Substitute V_{CE} for V_{DS} when using an IGBT.

where V_f is the forward voltage drop of D1.

For a desired drain-to-source desaturation voltage detect threshold (V_{DS_th}), the equation is:

$$V_{DESAT\_th} - V_{DS\_th} = I_{DESAT} \bullet R_{DESAT} + NV_f$$

Substitute V_{CE_th} for V_{DS_th} when using an IGBT.

where "N" is the number of series diodes in the DESAT detection input circuit.

Using multiple series diodes improves DESAT detection consistency by minimizing R_{DESAT}. Larger values of R_{DESAT} lessens DESAT detection uniformity due to variations of I_{DESAT}. This of course assumes the diode is operating above its forward bias knee voltage with a forward current of I_{DESAT}.

3.8 DESAT Blanking Time Stretching

Extending the blanking period is easily accomplished by the addition of an external capacitor to the DESAT input. Blanking time extension is the difference between the nominal 250 ns fixed internal blanking period and the required total blanking time of the design. The equation for the total blanking time is given in the following equation:

$$t_{TOTAL} = 250ns + \frac{V_{DESAT\_th} \bullet C_{TOTAL}}{I_{DESAT}}$$

Where C_{TOTAL} is the total external capacitance seen by the DESAT input pin. For the design example shown in "Figure 1 IX4352NEAU Typical Application Circuit" on page 11, C_{TOTAL} is the sum of C_{BLANK} and C_J, the junction capacitance of D1. C_{BLANK} is calculated as follows:

$$C_{BLANK} = \frac{(t_{TOTAL} - 250ns) \bullet I_{DESAT}}{V_{DESAT\_th}} - \frac{C_J}{N}$$

Where "N" is the number of series diodes in the DESAT detection input circuit.

Optionally the total capacitance may include the junction capacitance of a protection zener diode from DESAT to COM. Because this additional junction capacitance is added to C_{TOTAL} it reduces the calculated value of C_{BLANK}.

Junction capacitance of reversed biased diodes is voltage dependent so it is important to consult the manufacturer's data sheets for the correct value.

3.9 Thermal Shutdown

Thermal protection circuity pulls FAULT low, turns off OUTSRC, turns on both OUTSNK and OUTSOFT when the IX4352NEAU internal junction temperature reaches a nominal +160°C. The charge pump remains active during thermal shutdown to ensure the power IGBT outputs are off. After the internal junction temperature decreases by approximately 20 °C, the device returns to normal operation.

3.10 FAULT Output

The FAULT output indicates the IX4352NEAU has detected a fault condition. An open-drain NMOS at the FAULT output pulls low whenever one of the four monitored fault conditions is detected. They are:

1. V_{DD} Under Voltage Lock Out.
   FAULT output goes low until V_{DD} UVLO clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump is disabled.
2. V_{SS} Under Voltage Lock Out.
   FAULT output goes low until V_{SS} UVLO clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump is unaffected by fault, continues to run.
3. DESAT detection.
   FAULT output goes low for a nominal 2 ms.
   OUTSRC is turned off.
   OUTSOFT goes low.
   Gate voltage crosses V_{INSOFT_th}
   OUTSNK goes low.
   Charge pump is unaffected by fault, continues to run.
4. Thermal Shut Down.
   FAULT output goes low until TSD clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump is unaffected by fault, continues to run.

When the UVLO and TSD faults clear, the IX4352NEAU returns to normal operation and the gate driver outputs immediately transition to comply with the current IN logic state.

When the DESAT fault clears, the FAULT output remains low until the 2 ms MUTE timer expires. The OUTSNK and OUTSOFT outputs remain low until the next low to high IN transition after the MUTE timer expires.

4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4352NEAU	MSL 1

4.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time (T_C – 5 °C). The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

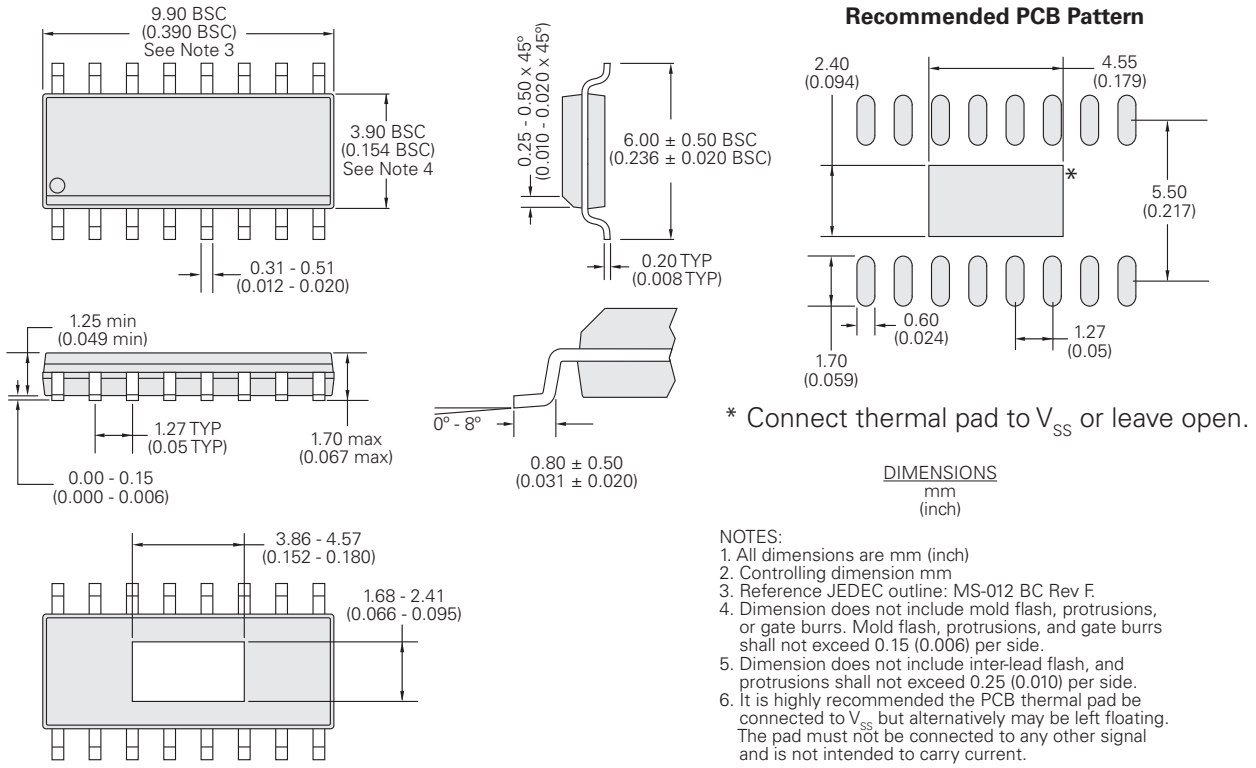
Device	Classification Temperature (T_C)	Dwell Time (t_P)	Maximum Reflow Cycles
IX4352NEAU	260 °C	30 seconds	3

4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce, or remove flux residue following the solder reflow process is acceptable, provided proper precautions are taken to prevent damage to the device. These precautions include, but are not limited to: Using a low pressure wash and providing a follow-up bake cycle sufficient to remove any moisture trapped within the device, due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning, or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

4.5 Mechanical Dimensions

4.5.1 16-Pin Narrow SOIC



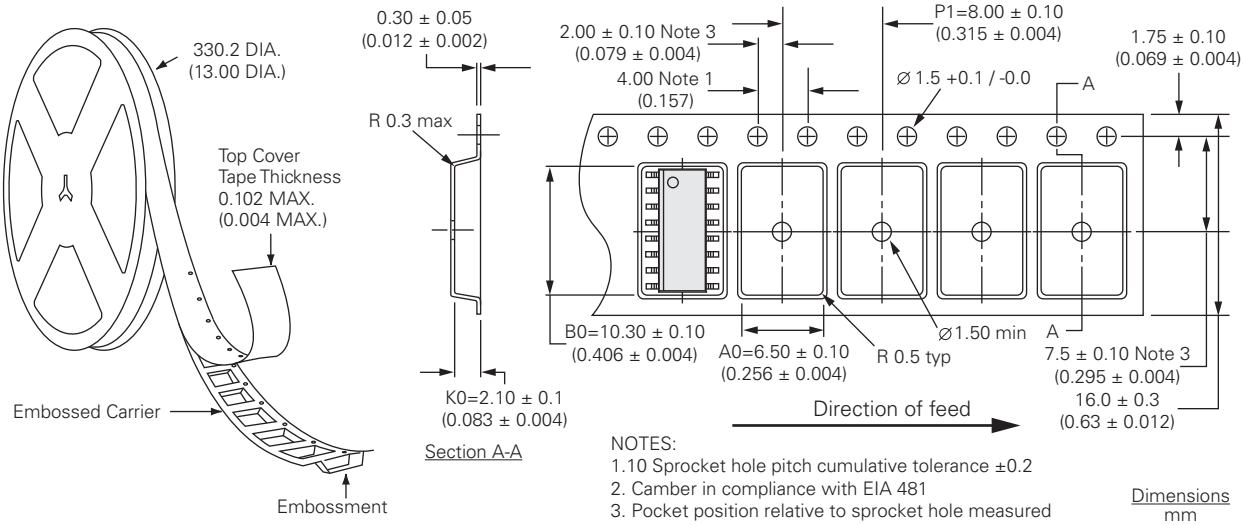
Recommended PCB Pattern

* Connect thermal pad to V_{SS} or leave open.

DIMENSIONS
mm
(inch)

NOTES:
1. All dimensions are mm (inch)
2. Controlling dimension mm
3. Reference JEDEC outline: MS-012 BC Rev F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 (0.006) per side.
5. Dimension does not include inter-lead flash, and protrusions shall not exceed 0.25 (0.010) per side.
6. It is highly recommended the PCB thermal pad be connected to V_{SS} but alternatively may be left floating. The pad must not be connected to any other signal and is not intended to carry current.

4.5.2 Tape and Reel Packaging



NOTES:
1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions
mm
(inches)