

# TP65H035G4YS

650V SuperGaN® FET in TO-247 (source tab)

## Description

The TP65H035G4YS 650V, 35 mΩ gallium nitride (GaN) FET is a normally-off device using Renesas's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

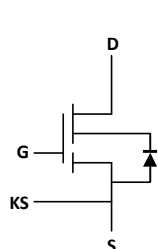
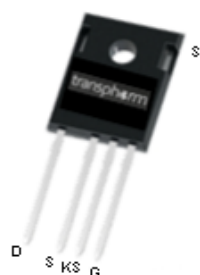
## Related Literature

- [Recommended External Circuitry for GaN FETs](#)
- [Printed Circuit Board Layout and Probing](#)

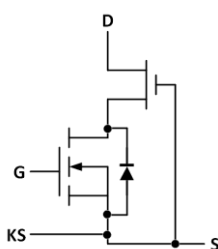
## Ordering Information

Part Number	Package	Package Configuration
TP65H035G4YS	4 lead TO-247	Source

TP65H035G4YS  
TO-247  
(top view)



Cascode Schematic Symbol



Cascode Device Structure

## Features

- JEDEC qualified GaN technology
- Dynamic  $R_{DS(on)eff}$  production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Enhanced inrush current capability
- Very low  $Q_{RR}$
- Reduced crossover loss

## Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

## Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor



## Key Specifications

$V_{DSS}$ (V)	650
$V_{DSS(TR)}(V)$	800
$R_{DS(on)eff}$ (mΩ) max*	41
$Q_{OSS}$ (nC) typ	142
$Q_G$ (nC) typ	42.7

\* Dynamic on-resistance; see Figures 19 and 20

**Absolute Maximum Ratings** ( $T_c=25^\circ\text{C}$  unless otherwise stated.)

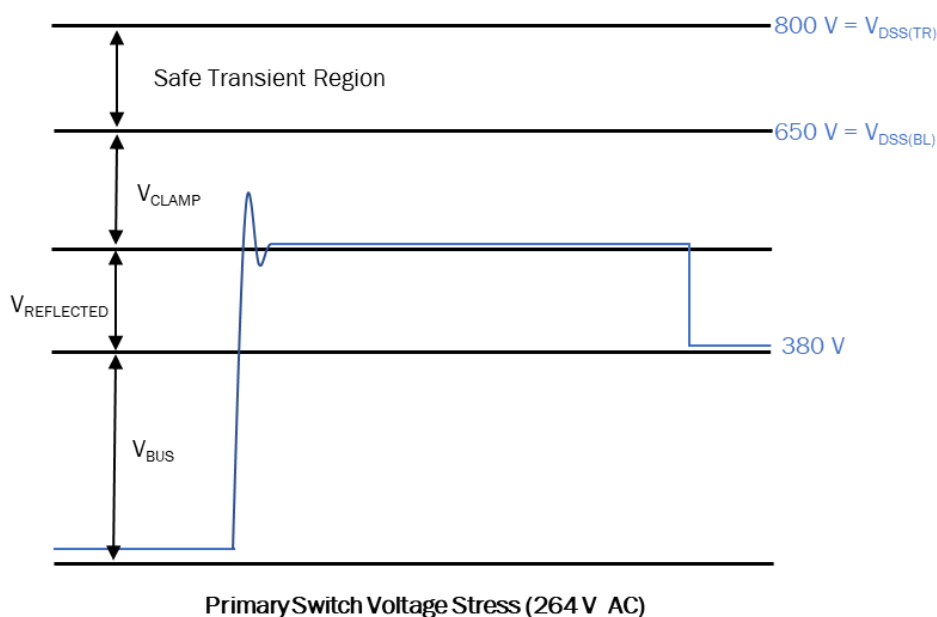
Symbol	Parameter		Limit Value	Unit
$V_{DSS}$	Drain to source voltage ( $T_J = -55^\circ\text{C}$ to $150^\circ\text{C}$ )		650	V
$V_{DSS(TR)}$	Transient drain to source voltage <sup>(a)</sup>		800	
$V_{GSS}$	Gate to source voltage		$\pm 20$	
$P_D$	Maximum power dissipation @ $T_c=25^\circ\text{C}$		156	W
$I_D$	Continuous drain current @ $T_c=25^\circ\text{C}$ <sup>(b)</sup>		46.5	A
	Continuous drain current @ $T_c=100^\circ\text{C}$ <sup>(b)</sup>		29.5	A
$I_{DM}$	Pulsed drain current (pulse width: 10 $\mu\text{s}$ )		240	A
$T_c$	Operating temperature	Case	-55 to +150	$^\circ\text{C}$
$T_J$		Junction	-55 to +150	$^\circ\text{C}$
$T_s$	Storage temperature		-55 to +150	$^\circ\text{C}$
$T_{SOLD}$	Soldering peak temperature <sup>(c)</sup>		260	$^\circ\text{C}$

Notes:

a. In off-state, spike duration <30 $\mu\text{s}$ , none repetitive.

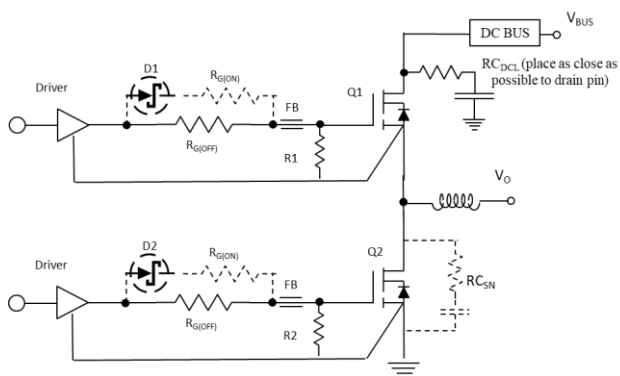
b. For increased stability at high current operation, see Circuit Implementation on page 3

c. For 10 sec., 1.6mm from the case

**Thermal Resistance**

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-case	0.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^\circ\text{C/W}$

## Circuit Implementation



**Simplified Half-bridge Schematic**  
( See also on Figure 15 )

For additional gate driver options/configurations, please see Application Note [Recommended External Circuitry for GaN FETs](#)

### Layout Recommendations for hard switching

#### Gate Loop:

- Gate Driver: SiLab Si823x/Si827x

- Keep gate loop compact

- Minimize coupling with power loop

#### Power loop: ( For reference see page 13 )

- Minimize power loop path inductance

- Minimize switching node coupling with high and low power plane

- Add DC bus noise filter (RC<sub>DCL</sub>) to reduce to voltage ringing

- Add Switching node snubber for high current operation

Parameter	Symbol	Value
Single Gate Resistor <sup>(d)</sup>	R <sub>G</sub> (R <sub>G(OFF)</sub> only)	18 Ω ( D1/D2/R <sub>G(ON)</sub> : NS)
Dual Gate Resistor <sup>(d)</sup>	Effective R <sub>G(ON)</sub> / R <sub>G(OFF)</sub>	18 Ω / 18 Ω
Operating frequency	F <sub>SW</sub>	<100 kHz
Steering Diode	D1/D2	Schottky diode ( Vr≥20V, Vf≤0.5V, Io≥1.5A)
Gate Ferrite Bead <sup>(d)</sup>	FB	180 – 270 Ω at 100MHz
Gate-to-source Resistor	R1/R2	10 kΩ
DC Link RC Noise Filter <sup>(d)</sup>	RC <sub>DCL</sub>	[4.7nF + 5Ω] x 2 or [10nF+ 2.3Ω]
Switching Node RC Snubber	RC <sub>SN</sub>	Not Necessary <sup>(e)</sup>
Gate Driver	Driver	Si823x/Si827x or similar

#### Note:

d. For every design and layout, a range of ferrite beads (FB), R<sub>G</sub> and DC link RC filter should be evaluated to help suppress any high frequency ringing and optimize performance.

e. RC<sub>SN</sub> (100pF + 10Ω) is needed if

- R<sub>G</sub> is smaller than recommended value;
- Layout is not optimized;
- Requires high current operation.

**Electrical Parameters** ( $T_J=25^\circ\text{C}$  unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Forward Device Characteristics</b>						
$V_{DS(BL)}$	Drain-source voltage	650	—	—	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	3.1	3.6	3.9	V	$V_{DS}=V_{GS}$ , $I_D=4.3mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-6.5	—	mV/ $^\circ\text{C}$	
$R_{DS(on)eff}$	Drain-source on-resistance <sup>(f)</sup>	—	35	41	m $\Omega$	$V_{GS}=10V$ , $I_D=30A$
		—	72	—		$V_{GS}=10V$ , $I_D=30A$ , $T_J=150^\circ\text{C}$
$I_{DSS}$	Drain-to-source leakage current	—	3	30	$\mu A$	$V_{DS}=650V$ , $V_{GS}=0V$
		—	20	—		$V_{DS}=650V$ , $V_{GS}=0V$ , $T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-source forward leakage current	—	—	400	nA	$V_{GS}=20V$
	Gate-to-source reverse leakage current	—	—	-400		$V_{GS}=-20V$
$C_{iss}$	Input capacitance	—	2680	—	pF	$V_{GS}=0V$ , $V_{DS}=400V$ , $f=1MHz$
$C_{oss}$	Output capacitance	—	137	—		
$C_{rss}$	Reverse transfer capacitance	—	11.2	—		
$C_{O(er)}$	Output capacitance, energy related <sup>(g)</sup>	—	191	—	pF	$V_{GS}=0V$ , $V_{DS}=0V$ to 400V
$C_{O(tr)}$	Output capacitance, time related <sup>(h)</sup>	—	354	—		
$Q_G$	Total gate charge	—	42.7	—	nC	$V_{DS}=400V$ , $V_{GS}=0V$ to 10V, $I_D=32A$
$Q_{GS}$	Gate-source charge	—	14.7	—		
$Q_{GD}$	Gate-drain charge	—	14.7	—		
$Q_{oss}$	Output charge	—	142	—	nC	$V_{GS}=0V$ , $V_{DS}=0V$ to 400V
$t_{D(on)}$	Turn-on delay	—	43	—	ns	$V_{DS}=400V$ , $V_{GS}=0V$ to 12V, $R_G=30\Omega$ , $I_D=32A$ , $Z_{FB}=240\Omega$ at 100MHz (See Figure 15)
$t_R$	Rise time	—	12.4	—		
$t_{D(off)}$	Turn-off delay	—	108	—		
$t_F$	Fall time	—	8	—		
$E_{off}$	Turn off Energy	—	26	—	$\mu J$	$V_{DS}=400V$ , $V_{GS}=0V$ to 12V, $R_G=18\Omega$ , $I_D=30A$ , $Z_{FB}=180\Omega$ at 100MHz
$E_{on}$	Turn on Energy	—	149	—	$\mu J$	

Notes:

f. Dynamic  $R_{DS(on)}$ , 100% tested; see Figures 19 and 20 for test circuit and conditionsg. Equivalent capacitance to give same stored energy as  $V_{DS}$  rises from 0V to 400Vh. Equivalent capacitance to give same charging time as  $V_{DS}$  rises from 0V to 400V

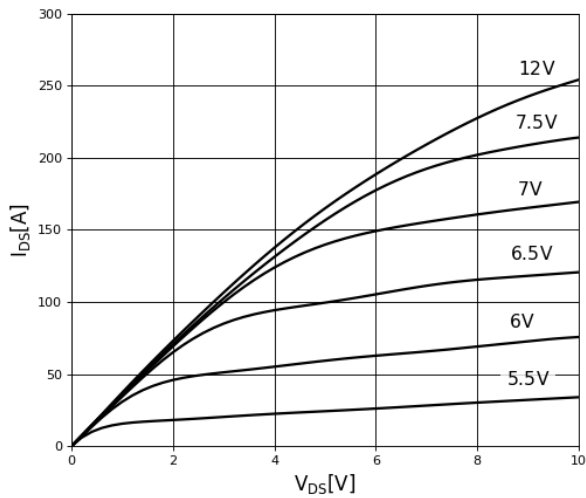
**Electrical Parameters** ( $T_J=25^\circ\text{C}$  unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Reverse Device Characteristics</b>						
$I_S$	Reverse current	—	—	29.5	A	$V_{GS}=0V$ , $T_C=100^\circ\text{C}$ $\leq 25\%$ duty cycle
$V_{SD}$	Reverse voltage <sup>(i)</sup>	—	1.8	—	V	$V_{GS}=0V$ , $I_S=32A$
		—	1.3	—		$V_{GS}=0V$ , $I_S=16A$
$t_{RR}$	Reverse recovery time	—	59	—	ns	$I_S=32A$ , $V_{DD}=400V$ , $di/dt=1000A/\mu s$
$Q_{RR}$	Reverse recovery charge <sup>(i)</sup>	—	0	—	nC	
$(di/dt)_{RM}$	Reverse diode $di/dt$ <sup>(k)</sup>	—	—	3200	A/ $\mu s$	Circuit implementation and parameters on page 3

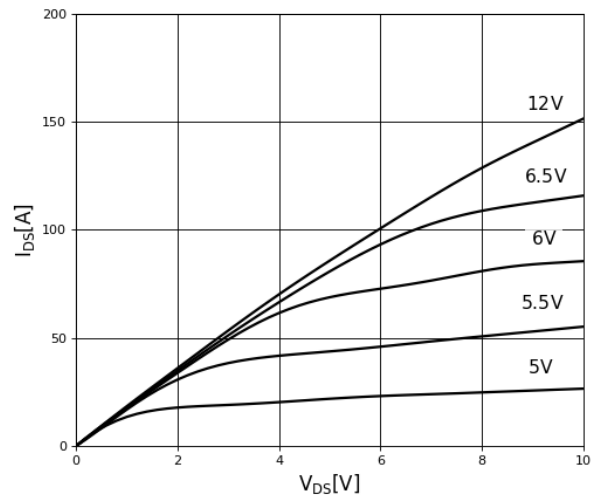
Notes:

i. Includes dynamic  $R_{DS(on)}$  effectj. Excludes  $E_{oss}$ k. Reverse conduction  $di/dt$  will not exceed this max value with recommended  $R_{\theta JA}$ .

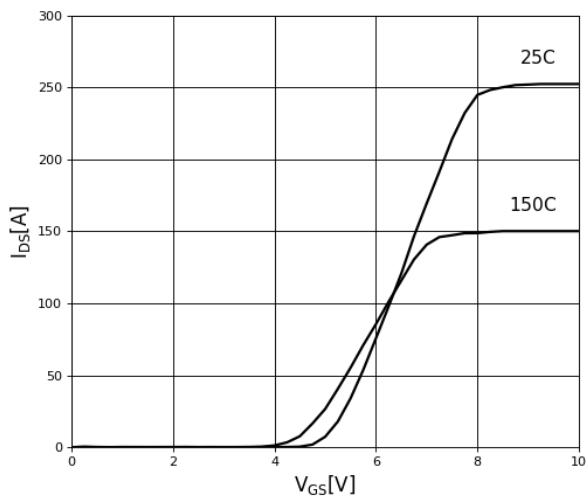
**Typical Characteristics** ( $T_c=25^\circ\text{C}$  unless otherwise stated)



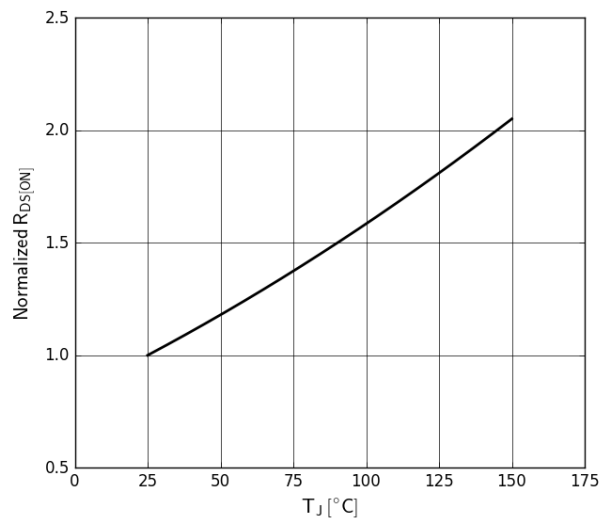
**Figure 1. Typical Output Characteristics**  $T_J=25^\circ\text{C}$   
Parameter:  $V_{GS}$



**Figure 2. Typical Output Characteristics**  $T_J=150^\circ\text{C}$   
Parameter:  $V_{GS}$

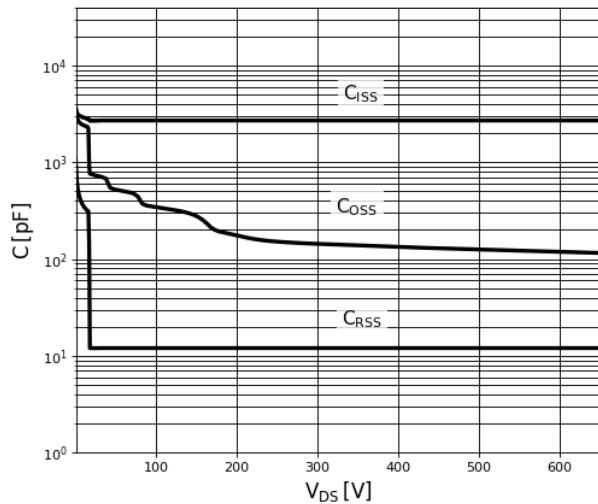


**Figure 3. Typical Transfer Characteristics**  
 $V_{DS}=20\text{V}$ , parameter:  $T_J$



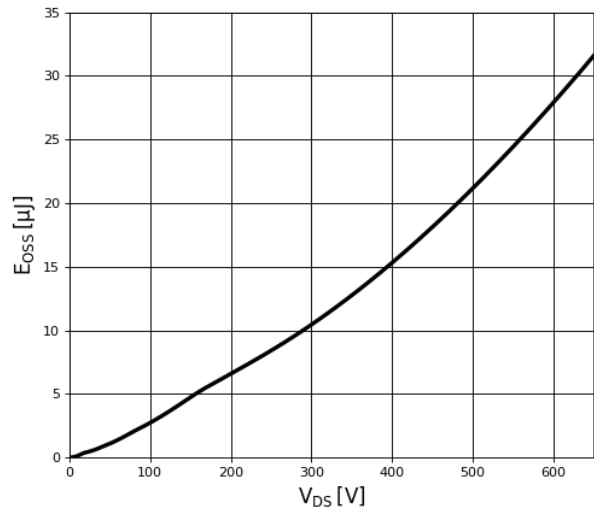
**Figure 4. Normalized On-resistance**  
 $I_D=30\text{A}$ ,  $V_{GS}=8\text{V}$

**Typical Characteristics** ( $T_c=25^\circ\text{C}$  unless otherwise stated)

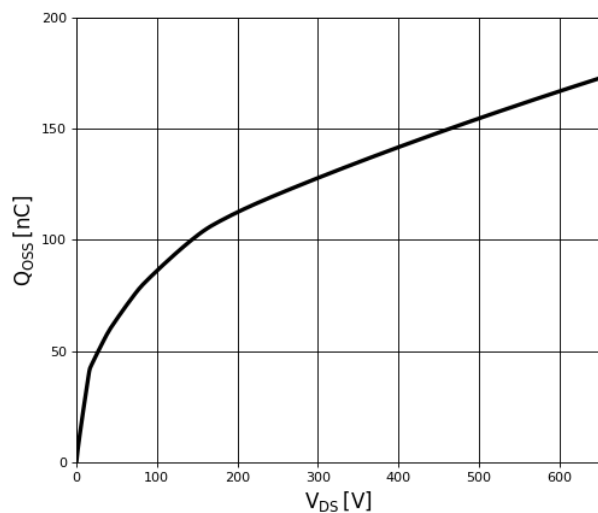


**Figure 5. Typical Capacitance**

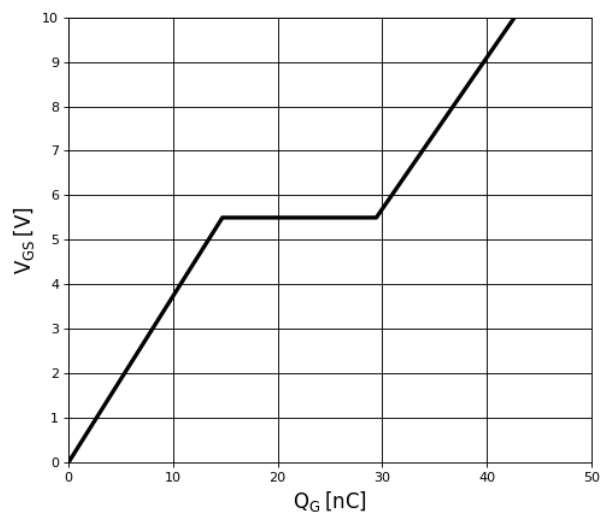
$V_{GS}=0V$ ,  $f=1MHz$



**Figure 6. Typical  $C_{oss}$  Stored Energy**



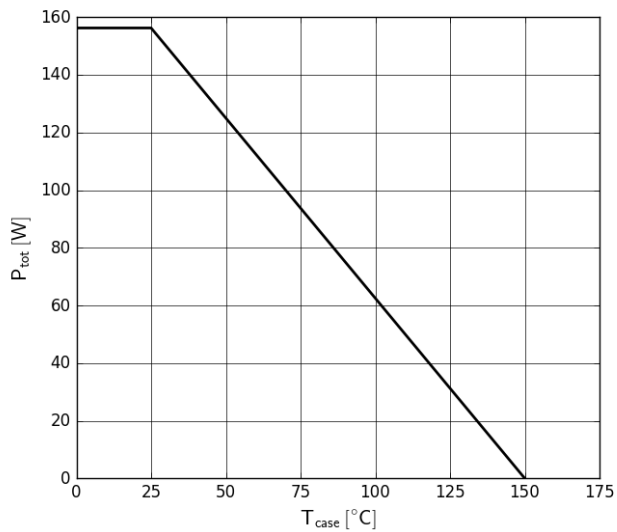
**Figure 7. Typical  $Q_{oss}$**



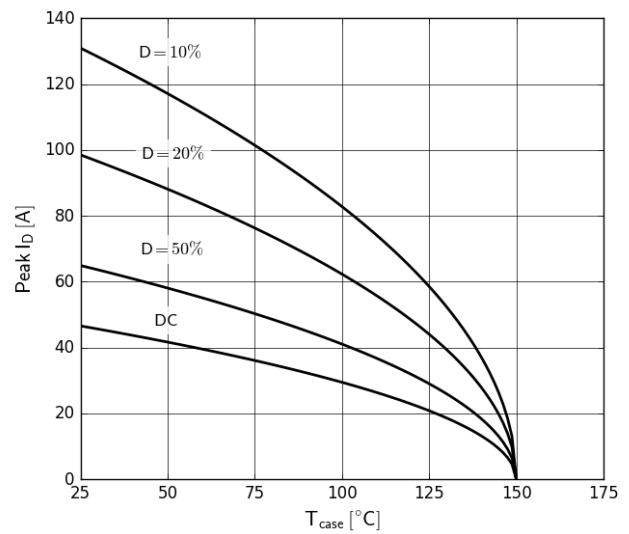
**Figure 8. Typical Gate Charge**

$I_{DS}=32A$ ,  $V_{DS}=400V$

# Typical Characteristics ( $T_c=25^\circ\text{C}$ unless otherwise stated)

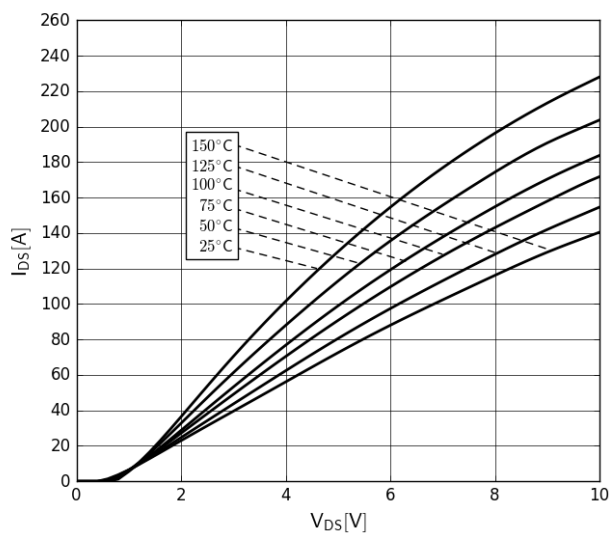


**Figure 9. Power Dissipation**



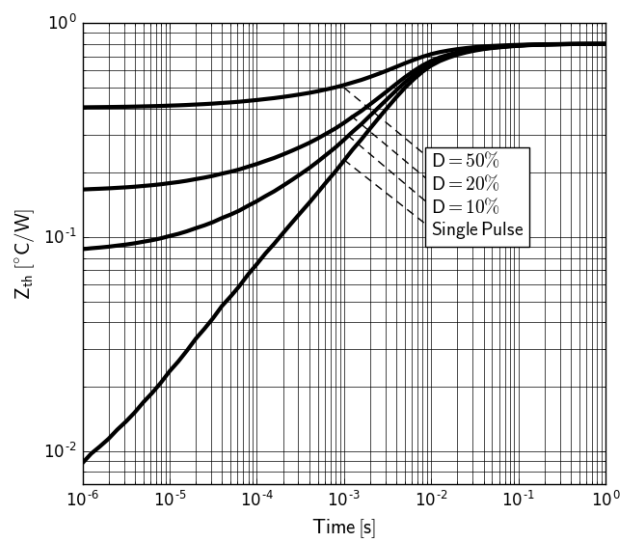
**Figure 10. Current Derating**

Pulse width  $\leq 10\mu\text{s}$ ,  $V_{GS} \geq 10\text{V}$



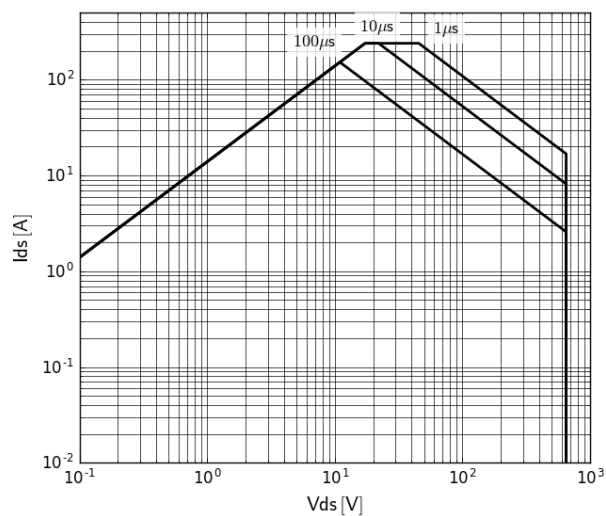
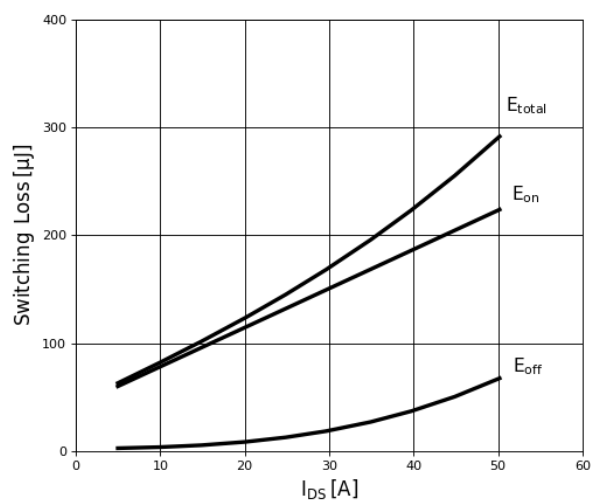
**Figure 11. Forward Characteristics of Rev. Diode**

$I_S=f(V_{SD})$ , parameter:  $T_J$



**Figure 12. Transient Thermal Resistance**



**Typical Characteristics** ( $T_c=25^\circ\text{C}$  unless otherwise stated)**Figure 13. Safe Operating Area  $T_c=25^\circ\text{C}$** **Figure 14. Inductive Switching Loss  $T_c=25^\circ\text{C}$   
 $R_g=18\Omega$ ,  $V_{DS}=400\text{V}$**

## Test Circuits and Waveforms

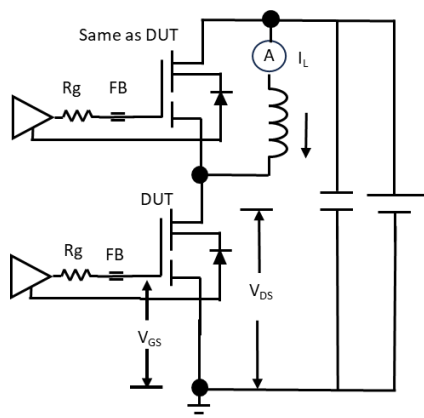


Figure 15. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

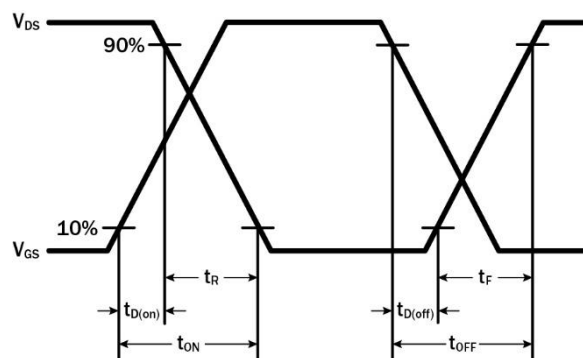


Figure 16. Switching Time Waveform

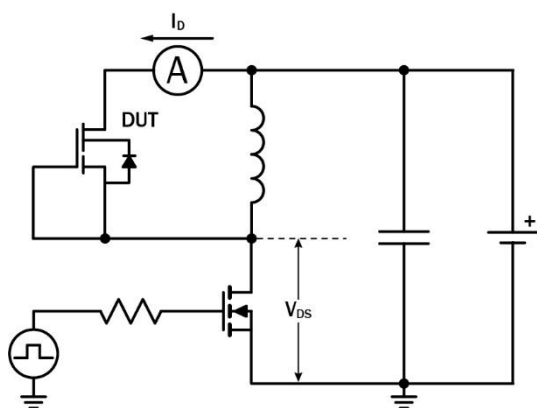


Figure 17. Diode Characteristics Test Circuit

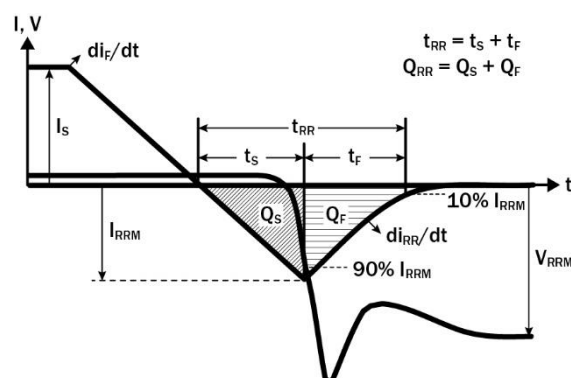
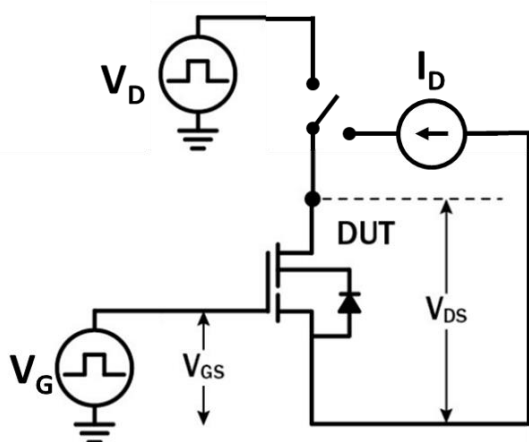
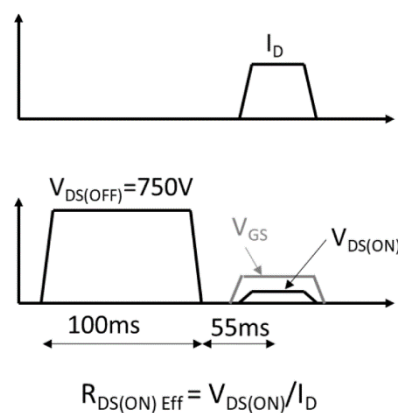


Figure 18. Diode Recovery Waveform

Figure 19. Dynamic  $R_{DS(on)eff}$  Test CircuitFigure 20. Dynamic  $R_{DS(on)eff}$  Waveform

## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

**When Evaluating Renesas GaN Devices:**

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See <a href="#">Printed Circuit Board Layout and Probing</a>	

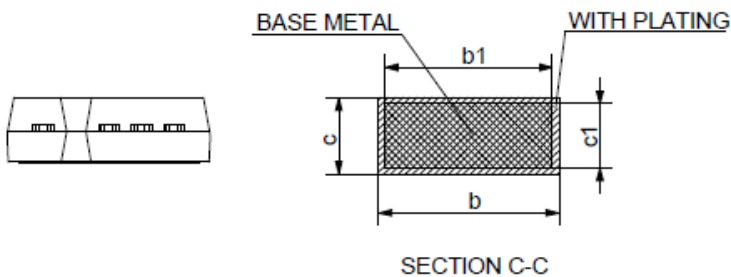
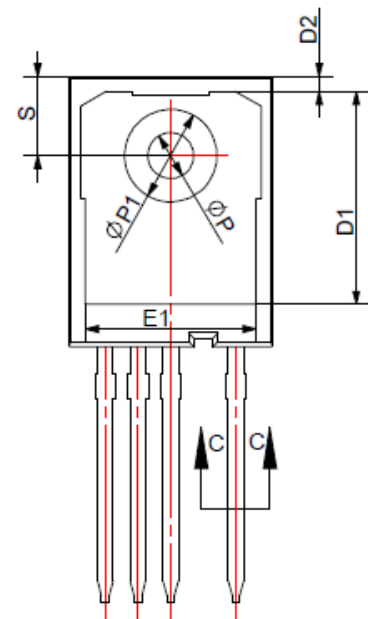
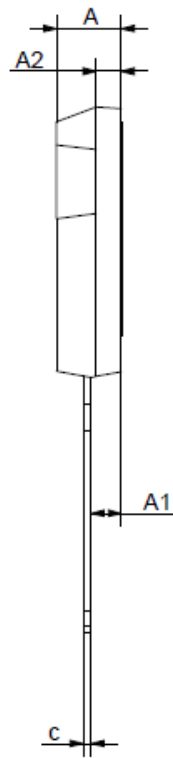
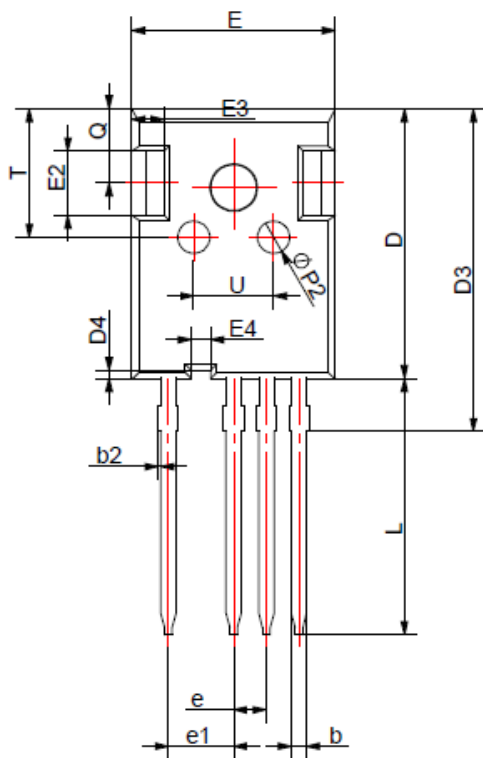
## GaN Design Resources

The complete technical library of GaN design tools can be found at [Renesasusa.com/design](https://www.renesas.com/design):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

## Mechanical

## 3 Lead TO-247 Package



DIM.	Millimeters.		
	MIN.	NOM.	MAX.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	—	1.29
b1	1.15	1.20	1.25
b2	0	—	0.20
c	0.59	—	0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
D4	0.55	0.65	0.75
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
E4	1.40	1.50	1.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1	—	—	7.40
P2	2.40	2.50	2.60
Q	5.60	—	6.00
S	6.15BSC		
T	9.80	—	10.20
U	6.00	—	6.40
TO-247-4L			
GaNext			
DATE: 2023.01		Rev. 01	

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