5A eFuse with Current Limit Control and Reverse Blocking FET Control

Features

- 4.5V to 18V Operating Voltage Range
- 20V Abs. Max. Rating at VIN
- 31mΩ typ. On-Resistance from VIN to OUT
- Adjustable Current Limit Protection (CLP)
  - 1A to 5A via R_{LIM}
- Soft-Start (SS) Limits Inrush Current
- Programmable OUT Slew Rate (dV/dT pin)
- Fast Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- Latched-off or Auto-retry Fault Response
- Reverse Current Blocking Support
- EN Enable Logic Input
- -40°C to 85°C Operating Temperature Range
- 10-pin VDFN 3mm x 3mm (0.5mm pitch)

Brief Description

KTS1630 is a low-resistance load switch with adjustable current limit, programmable output slew rate during soft-start, over-current protection, short-circuit protection, and over-temperature protection. It is optimized for applications that require adjustable output ramp rate for power sequencing and also need accurate output current limit for safety, such as eFuse protection in consumer appliances. The KTS1630 uses an external resistor to set the current limit and an external capacitor to set the output ramp rate.

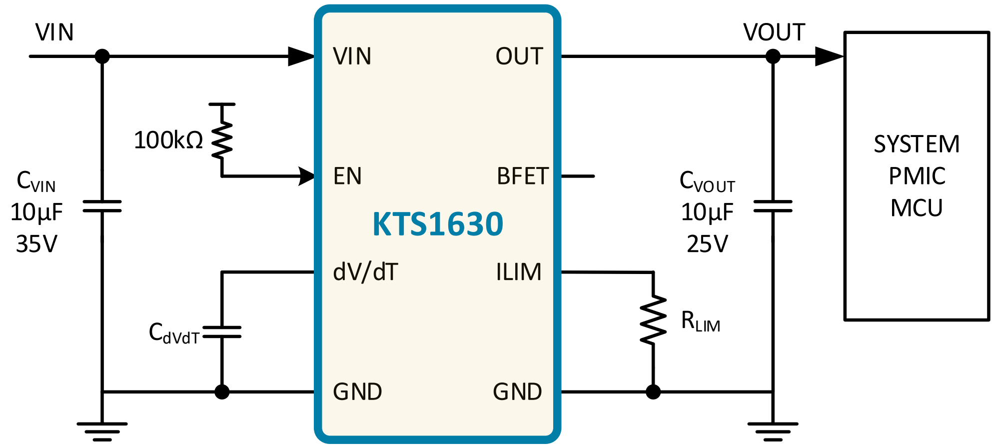
To prevent output capacitors being discharged back to input thru the internal body diode when power source at VIN is removed, an additional MOSFET can be connected to the output back-to-back, with its gate connected to BFET pin.

KTS1630 is packaged in advanced, fully "green" compliant, 3mm x 3mm x 0.85mm, 10-pin VDFN.

Applications

- Smart TV, Solid-State Drive (SSD), Set Top Box
- Industrial 5V/12V Power Rail

Typical Application

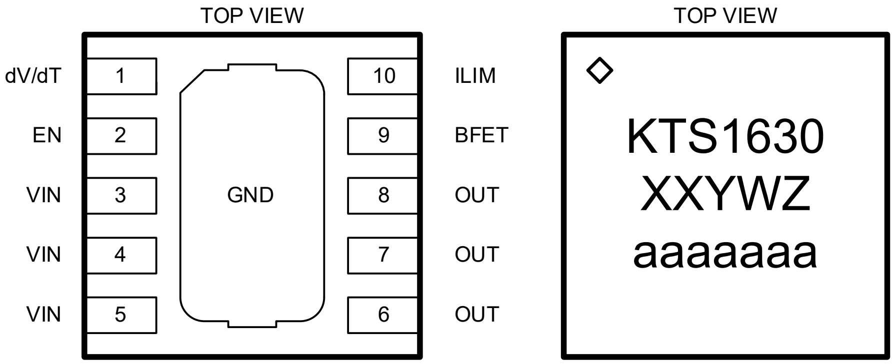


Ordering Information

Part Number	Marking[1]	Response to Fault	Operating Temperature	Package
KTS1630AEVAD-TB	TKYWZaaaaaaa	Auto-Retry	-40°C to +85°C	VDFN33-10
KTS1630BEVAD-TB	TLYWZaaaaaaa	Latched-off	-40°C to +85°C	VDFN33-10

Pinout Diagram

VDFN33-10



10-pin 3mm x 3mm x 0.85mm
VDFN Package, 0.5mm pitch
Top Mark: XX = TK or TL = Device ID, YW = Date Code, Z = Serial Number,
aaaaaaa = Assembly Lot Tracking Number

Pin Descriptions

Pin #	Name	Function
3, 4, 5	VIN	Power Switch Input and Device Power Supply.
6, 7, 8	OUT	Power Switch Output.
1	dV/dT	OUT Ramp Rate Setting – Adjust OUT ramp up rate during soft start using a capacitor from dV/dT pin to GND.
10	ILIM	Current Limit Setting – Adjust the current limit using a resistor from ILIM pin to GND.
2	EN	Active High Enable signal for VIN-OUT path. Bias this pin to logic high when it is not used.
9	BFET	External Reverse Blocking FET Control – Connect this pin to the gate of the reverse blocking FET. This pin can be floating (open) when it is not used.
Thermal Pad	GND	Ground. Connect this bottom pad to system ground.

---

[1] XX = TK or TL = Device ID, YW = Date Code, Z = Serial Number, aaaaaaa = Assembly Lot Tracking Number.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
V_{VIN}	VIN to GND	-0.3 to 20	V
	VIN 10ms Transient	22	
V_{OUT}	OUT to GND	-0.3 to 20	V
V_{BFET}	BFET to GND	-0.3 to 30	V
V_I and V_O	ILIM, dV/dT to GND	-0.3 to 7	V
V_{EN}	EN to GND	20	V
$I_{VIN\text{-}OUT}$	Maximum Switch Current (continuous)	6	A
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[3]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV

Thermal Capabilities[4]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	55.7	°C/W
P_D	Maximum Power Dissipation at 25°C (T_J = 125°C)	1.80	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-18.0	mW/°C

---

[2] Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

[3] ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

[4] Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{VIN}	VIN Supply Voltage	4.5 to 18	V
V_{OUT}	OUT Output Voltage	4.5 to 18	V
V_{BFET}	BFET Output Voltage	0 to VIN+6	V
V_I and V_O	ILIM, dV/dT Logic Input and Output Voltage	0 to 5.5	V
V_{EN}	EN to GND	0 to 18	V
C_{VIN}	Input Capacitance	1 to 10	µF
		35	V
C_{OUT}	Output Capacitance	1 to 10	µF
		25	V
$C_{dV/dT}$	Output Capacitance	1 to 1000	nF
		6.3	V
V_{ILIM}	ILIM Input Voltage	0 to 3	V
R_{LIM}	Current Limit Setting Resistance	10 to 162	kΩ
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Operating Temperature Range	-40 to 125	°C

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operating range of T_A = -40°C to +85°C, V_{IN} = 4.5V to 18V. Typical values are specified at T_A = +25°C with V_{IN} = 12V, EN = 2V, R_{LIM} = 100kΩ and C_{dVdT} = Open.

VIN Supply Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{VIN}	Input Voltage Operating Range			4.5		18	V
V_{UVLO_VIN}	Under-Voltage Lockout	V_{VIN} rising threshold		4.15	4.3	4.5	V
		Hysteresis			215		mV
I_{Q_VIN}	No-Load Supply Current	VOUT = open	EN = 2V		350	550	µA
			EN = GND		90	225	

VIN to OUT Switch Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
R_{ON_OUT}	Switch On-Resistance	I_{OUT} = 1A	T_A = 25°C		31	37	mΩ
		V_{VIN} = 5V/12V	T_J = 125°C		40	48	
I_{OFF_SYSA}	Switch Off Input Current at OUT	V_{VIN} = 12V, V_{OUT} = 0V, EN = GND		-5	0	1.2	µA
		V_{VIN} = 12V, V_{OUT} = 0.3V, EN = GND			1.5	12	
t_{DON_OUT}	Switch Turn-On Delay Time[6]	V_{VIN}>V_{UVLO}, EN = L→H			100		µs
		EN = H, V_{VIN} rising > V_{UVLO_VIN}			100		
t_{DOFF_DLY}	Switch Turn-Off Delay Time[7]	V_{VIN} > V_{UVLO}, EN = H→L			0.4		µs
		EN = H, V_{VIN} falling < V_{UVLO_VIN}			1		

Fault Recovery Timing Specifications [Auto-Retry Options only]

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{HICCUP}	Hiccup Retry Time after fault[8]	After OCP/OTP is triggered		64		ms

Current Limit Protection (CLP) Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
I_{CLP_OUT}	Current Limit Protection[9]	T_A = 25°C	R_{LIM} = 10kΩ		1.02		A
			R_{LIM} = 45.3kΩ	1.79	2.1	2.42	
			R_{LIM} = 100kΩ	3.3	3.7	4.2	
			R_{LIM} = 150kΩ[10]	4.5	5.1	5.7	
			R_{LIM} = Open		0.73		
			R_{LIM} = GND		0.84		
V_{ILIM_OPEN}	ILIM open resistor detect threshold	V_{ILIM} rising, R_{LIM} = Open			3.1		V

---

5. Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization and correlation with statistical process controls.
6. t_{DON_OUT} is time from the specified test condition until V_{OUT} = 10%*VVIN.
7. t_{DOFF_DLY} is time from the specified test condition and C_{BFET} = OPEN until BFET pin voltage first begin to fall.
8. t_{HICCUP} is time from protection triggers and restarts until Output voltage = 10%*Input voltage.
9. Min and Max tolerances are designed for V_{VIN}-$V_{OUT} \le$ 1V only.
10. Guaranteed by design and characterization; not production tested.

Electrical Characteristics (continued)[11]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operating range of T_A = -40°C to +85°C, V_{IN} = 4.5V to 18V. Typical values are specified at T_A = +25°C with V_{IN} = 12V, EN = 2V, R_{LIM} = 100kΩ and C_{dVdT} = Open.

Over Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP_OUT}	Over-Current Protection (OCP) Threshold			1.6 x I_{CLP_OUT}		A
t_{OCP_OUT}	OCP Response Time [12]			100		ns

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	IC Junction Over-Temperature Protection	T_J rising threshold		150		°C
		Hysteresis		20		

Reverse blocking FET Gate Driver (BFET) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{BFET}	BFET charging current	$V_{BFET} = V_{OUT}$		2		µA
V_{BFET}	BFET clamp voltage			V_{VIN} + 6.4		V
R_{BFET}	BFET discharging resistance	EN = GND, I_{BFET} = 100mA	12	19	37	Ω
t_{ON_BFET}	BFET Turn-On Time [13]	C_{BFET} = 1nF		8		ms
		C_{BFET} = 10nF		60		
t_{OFF_BFET}	BFET Turn-Off Time [14]	C_{BFET} = 1nF		0.4		µs
		C_{BFET} = 10nF		1.4		

Output Ramp Control (dV/dT) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$I_{dV/dT}$	dV/dT charging current	$V_{dV/dT}$ = 0V		220		nA
$R_{dV/dT}$	dV/dT discharging resistance	EN = GND, $I_{dV/dT}$ = 10mA sinking		160		Ω
$V_{dV/dT}$	dV/dT capacitor voltage			5.5		V
$G_{dV/dT}$	dV/dT to OUT Gain			5.0		V/V
$t_{dV/dT}$	Output ramp time [15]	C_{dVdT} = OPEN	0.7	1	1.3	ms
		C_{dVdT} = 1nF		12		

Logic Pin Specifications (EN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{EN}	EN Threshold Voltage	Rising voltage		1.40	1.46	V
		Falling voltage	1.27	1.35		
I_{EN}	EN Input Leakage Current	$0V \le V_{EN} \le 5V$	-0.1		0.1	µA

---

[11] Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization, and correlation with statistical process controls.

[12] t_{OCP_OUT} is time from I_{VIN} >> IOCP_OUT until switch turns off.

[13] t_{ON_BFET} is time from EN=L→H and the specified test condition until $V_{BFET} = V_{VIN}$.

[14] t_{OFF_BFET} is time from EN=H→L and the specified test condition until $V_{BFET} = 10\% * V_{VIN}$.

[15] $t_{dV/dT}$ is time from EN=L→H until $V_{OUT} = 97.5\% * V_{VIN}$.

Timing Diagrams

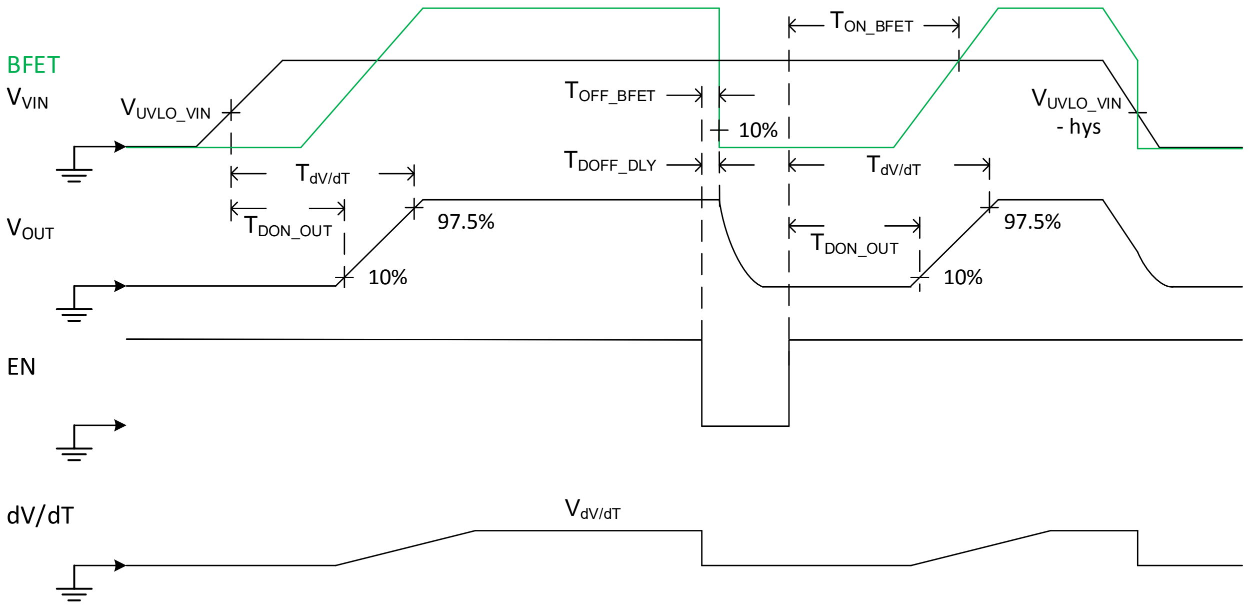


Figure 1. VIN Ramp-up, Ramp down and EN Toggling

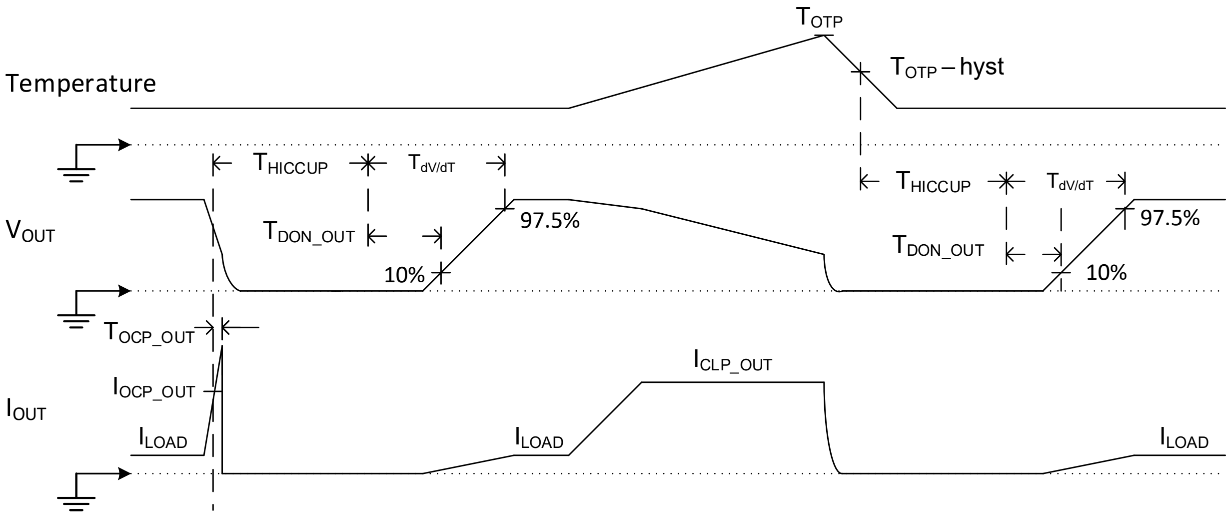


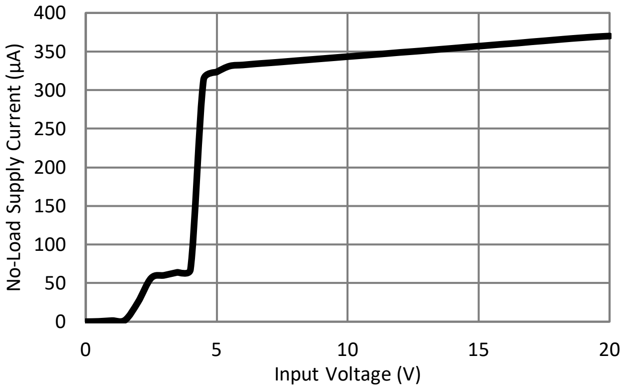
Figure 2. OCP, CLP and OTP Timing Diagram

Typical Characteristics

V_{IN} = 12V, EN = 2V, R_{LIM} = 100kΩ, CdVdT = Open, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C, unless otherwise specified.

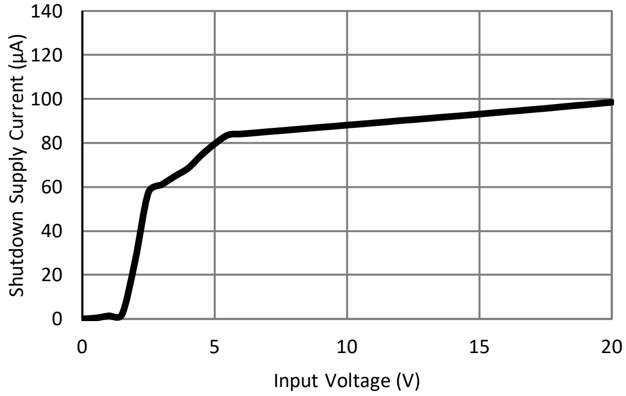
No-Load Supply Current vs. VIN Voltage

(EN = 2V)

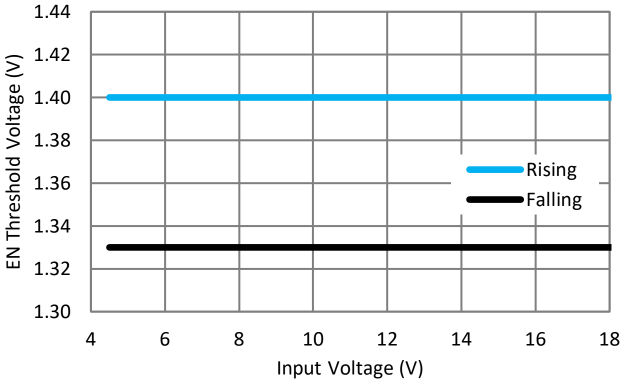


Shutdown Supply Current vs. VIN voltage

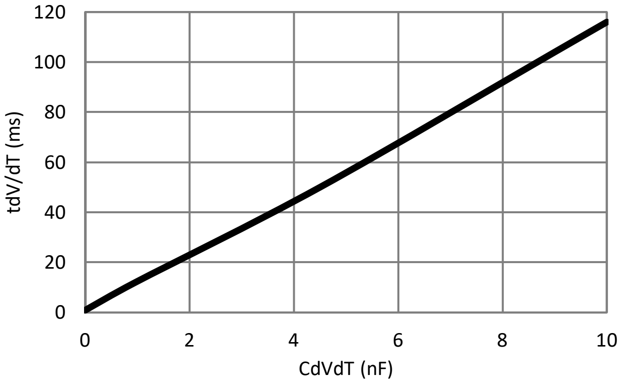
(EN = GND)



EN Logic Threshold vs. VIN

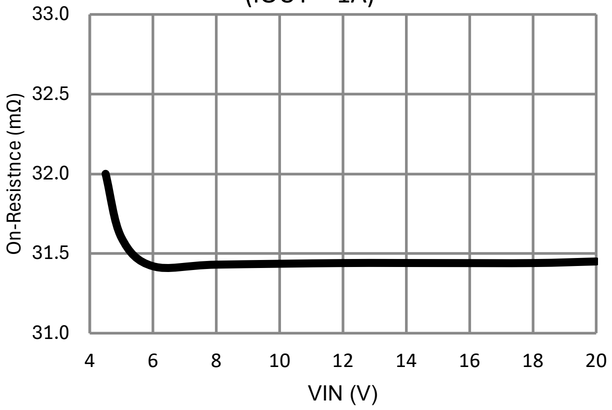


Output Ramp Time vs. CdVdT



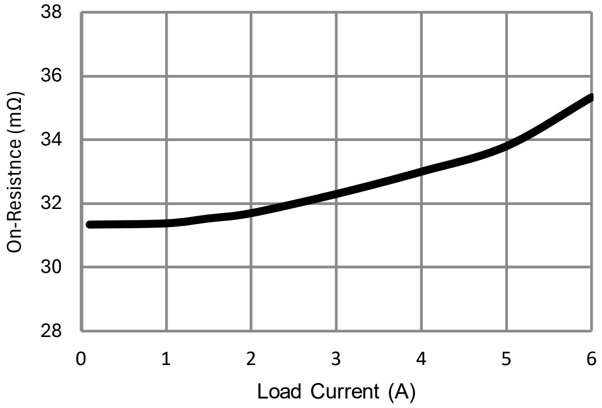
Switch On-Resistance vs. VIN

(IOUT = 1A)



Switch On-Resistance vs. Load Current

(VIN = 12V)



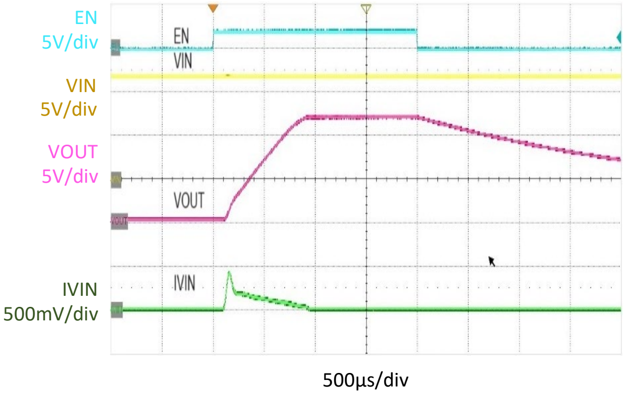
(continued next page)

Typical Characteristics (continued)

V_{IN} = 12V, EN = 2V, R_{LIM} = 100kΩ, CdVdT = Open, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C, unless otherwise specified.

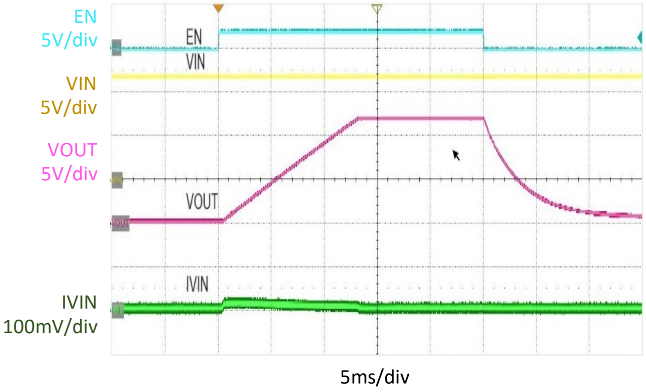
Enable Turn-on, Turn-off Response

(No load, Cout = 10µF, CdVdT = Open)



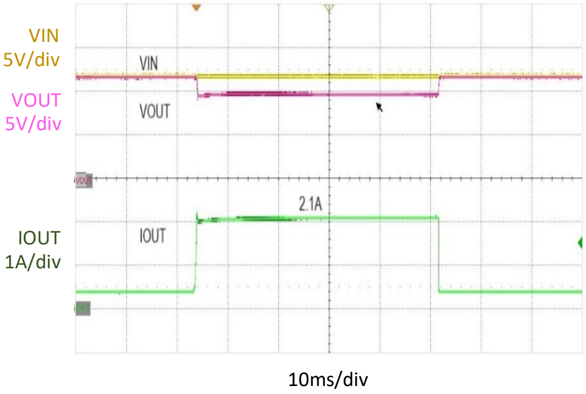
Enable Turn-on, Turn-off Response

(No load, Cout = 10µF, CdVdT = 1nF)



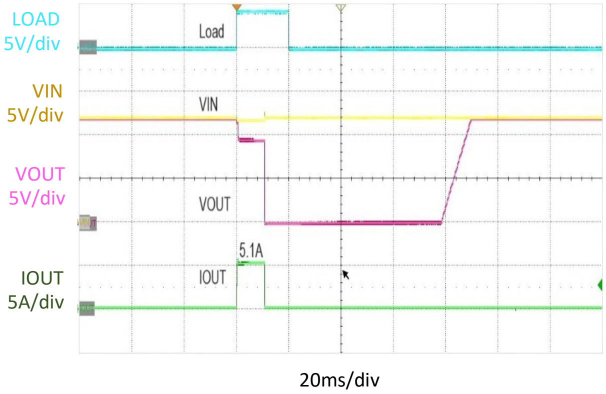
CLP Response

(2.1A Current Limit, Riset = 45.3kΩ)



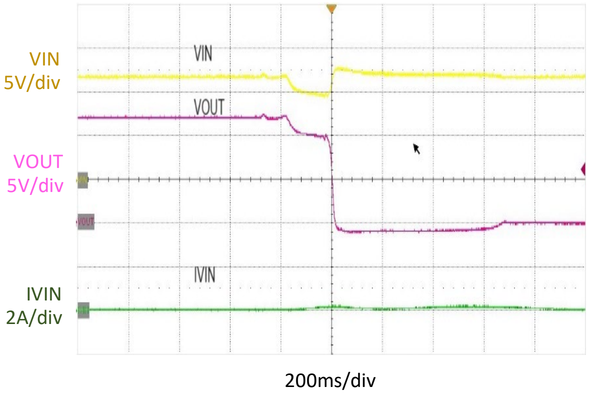
CLP followed by Thermal Shutdown and Restart

(5.1A Current Limit, Riset = 150kΩ)



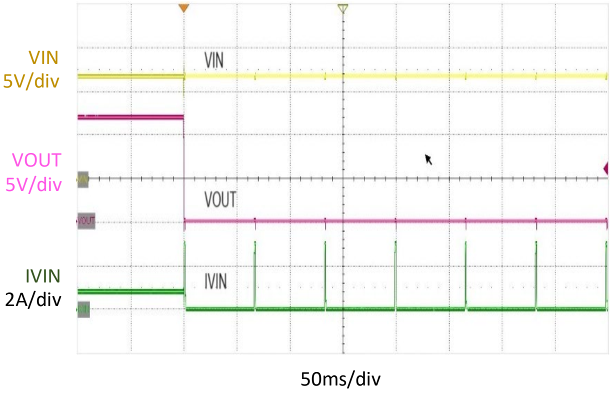
Short Circuit Response

CIN = 1000µF + 10µF, no COUT



Short Circuit Protection (SCP) Response with Hiccup-Retry

CIN = 1000µF + 10µF, ICLP_OUT = 3.2A, no COUT



Functional Block Diagram

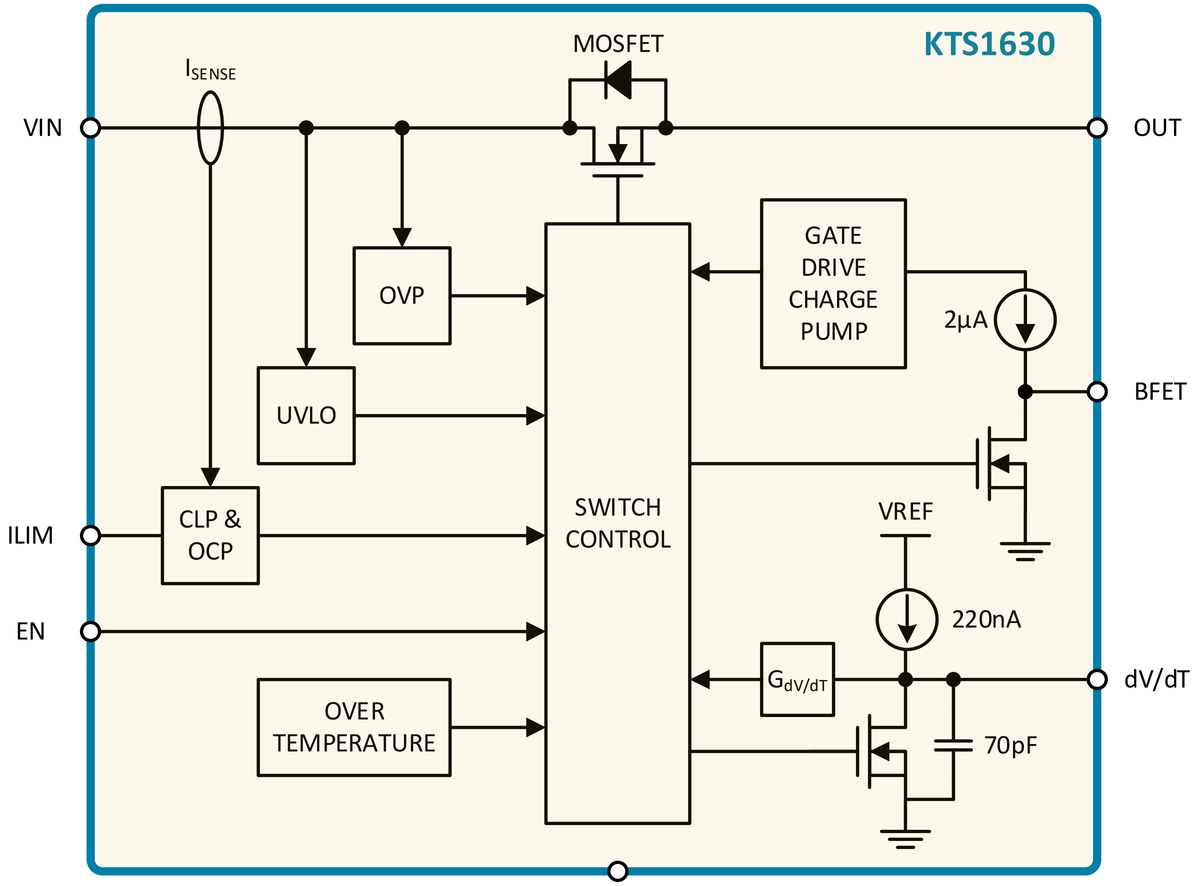


Figure 3. Functional Block Diagram

Functional Description

The KTS1630 is a low-resistance load switch with adjustable current limit, programmable output slew rate during soft start, over-current protection, short-circuit protection, and over-temperature protection. It is optimized for application that requires adjustable output ramp rate for power sequencing and provides accurate output current limit for safety, such as eFuse protection in consumer appliances. An external resistor connected between ILIM pin and GND allows to set the current limit. An external capacitor connected from dV/dT pin to GND sets the output ramp rate.

To prevent output capacitors from being discharged back to the input thru the internal body diode when VIN power source is removed (or a short to GND fault is applied at VIN), an additional N-channel MOSFET can be connected to the output back-to-back with its gate connected to BFET pin.

Under-Voltage Lockout (UVLO)

When $V_{VIN} < V_{UVLO\_VIN}$, the power switch is disabled. Once V_{VIN} exceeds V_{UVLO_VIN}, the power switch is controlled by the EN pin and fault detection circuits.

EN Enable Control

The EN pin is an active-high input, which disables the power switch when EN = Low (GND). When EN is set High, the power switch turns on after the switch turn on delay time. If the switch is expected to turn on whenever V_{VIN} > V_{UVLO_VIN}, EN input can be biased to V_{EN} rising threshold by dividing V_{VIN} or pulled up an external supply by a resistor. The EN pin should not be left floating.

On KTS1630B with Latched-off feature, the EN pin when toggled (from High to Low to High) allows to restart the device after Over-Current or Over-Temperature fault latch.

Reverse Blocking FET Control (BFET)

BFET pin, controlled by either VIN UVLO (V_{UVLO_VIN}) or EN pin, can be used to drive the gate of a N-channel MOSFET connected back-to-back in series to OUT, in order to prevent any reverse current to flow from OUT back to VIN when OUT voltage is higher than VIN.

The BFET pin can also be used to drive the gate of a P-channel MOSFET connected from OUT to GND, which helps to fast discharge any capacitance at OUT when the device is disabled. When EN input is higher than the enable rising threshold and VIN voltage is higher than UVLO, BFET pin sources up to 2µA to the connected gate channel. When either EN = Low or VIN is less than UVLO, BFET pin is pulled to GND internally via a discharging resistance of 21Ω typical.

Table 1. BFET Truth Table

V_{EN}	V_{VIN}	BFET pin
> V_{EN_rising}	> V_{UVLO_VIN}	2µA Current Source
X	< V_{UVLO_VIN}	Pull-down to GND (21Ω typ.)
< V_{EN_rising}	X	

Programmable Output Voltage Ramp (dV/dT)

The output voltage slew rate during startup can be programmed to a specific rate by connecting a capacitor from the dV/dT pin to GND.

The equation below determines the relationship between C_{dVdT}, VIN voltage and the desired time ($t_{dV/dT}$) to ramp up OUT to 97.5% of VIN when the input current is not limited by CLP:

$$t_{dV/dT}\ (s) = 10^6 \times V_{VIN} \times (C_{dVdT} + 70pF)$$

BFET pin has a 70pF capacitor connected internally to GND, so this pin can be floating if the minimum output ramp up time is needed.

ILIM Current Limit Protection (CLP)

KTS1630 switch current limit is set using an external resistor, R_{LIM}, which is connected between the ILIM pin and GND. The following equation shows the relationship between R_{LIM} and I_{ILIM}:

$$R_{LIM}\ (\Omega) = (I_{ILIM} - 0.7) / (3 \times 10^{-5})$$

Whenever the switch current reaches the programmed current limit, the current limit regulation loop takes control and reduces the gate drive to limit the switch current. During CLP, the switch acts as a constant current source, and the output voltage reduces depending on the load current. Once the load current reduces below the current limit, the output voltage rises back to V_{VIN} minus Rdson voltage drop. During CLP event, the die heats up due to high power dissipation, which can trigger thermal shutdown. When the chip temperature cools, the device recovers and turns back ON after hiccup time and switch turn on time.

Over-Current Protection (OCP)

During a sudden output short-circuit to ground event, the switch current may ramp up very quickly, faster than the bandwidth of the CLP regulation loop. For this reason, KTS1630 includes an additional over-current protection circuit (OCP). If the switch current exceeds I_{OCP_OUT}, OCP turns off the switch very quickly with 100ns (typ) response time. On KTS1630A with Auto-retry, once the fault is removed, the output voltage is restored automatically after hiccup time and the output ramp up time.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 150°C, the OTP circuit disables VIN to OUT switch.

On KTS1630A with Auto-retry, once the device junction temperature decreases below 130°C, and no other fault is detected, the power switch returns to its previous state after hiccup time and switch turn on time.

On KTS1630B with Latched-off, once the device junction temperature decreases below 130°C, and no other fault is detected, the power switch remains off. After the EN input is toggled, the device returns to its previous state after hiccup time and switch turn on time.

Recommended PCB Layout

Optimized trace routing and placement are important to assure KTS1630 protection features. The following guidelines are recommended for best system performance:

1. A good thermal printed circuit board design is recommended in order to support 5A fully loaded current. VIN, OUT and GND should have a reasonable size of copper pour, so that it can be used as a thermal dissipating interface. Additional thermal vias can also help to conduct the heat to the other side of PCB, with additional copper plate.
2. Place additional vias near the GND pad of the KTS1630, to connect to the ground plane on another layer. The ground plane layer should be referenced back to the system power source ground at one single point to avoid stray current paths through the ground plane.
3. Place the input bypass capacitor and output decoupling capacitor the closest to VIN and OUT pins respectively. Connect the ground terminal of the capacitor to the ground plane using multiple vias.
4. Place other components, R_{LIM} and C_{dVdT}, as close to ILIM and dV/dT pins respectively with the shortest traces. Minimize distance for the GND side end of these components to the GND pin of the device.

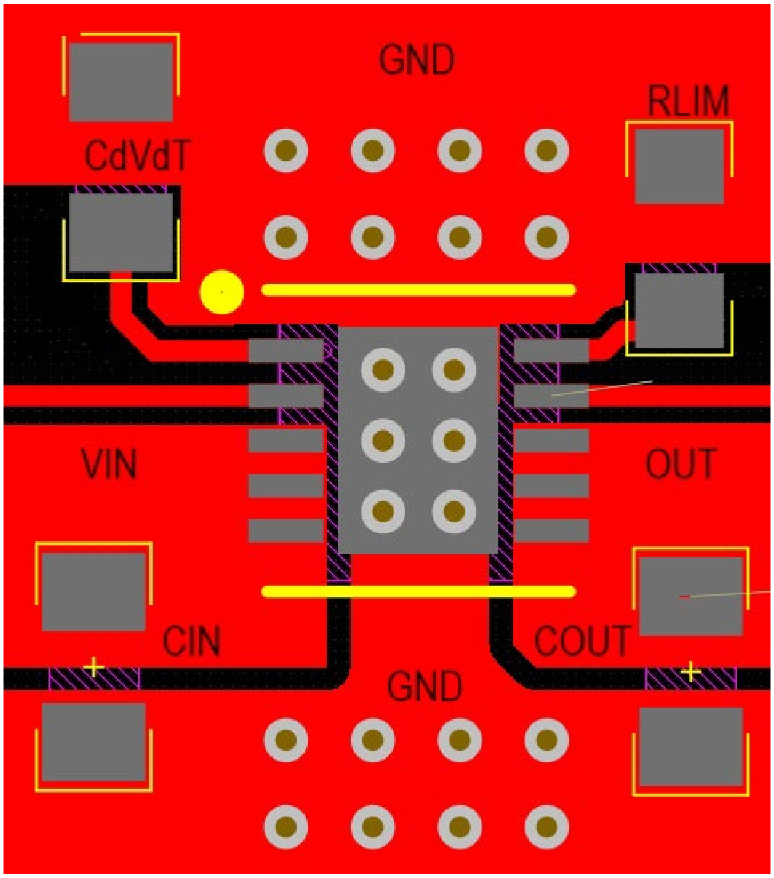
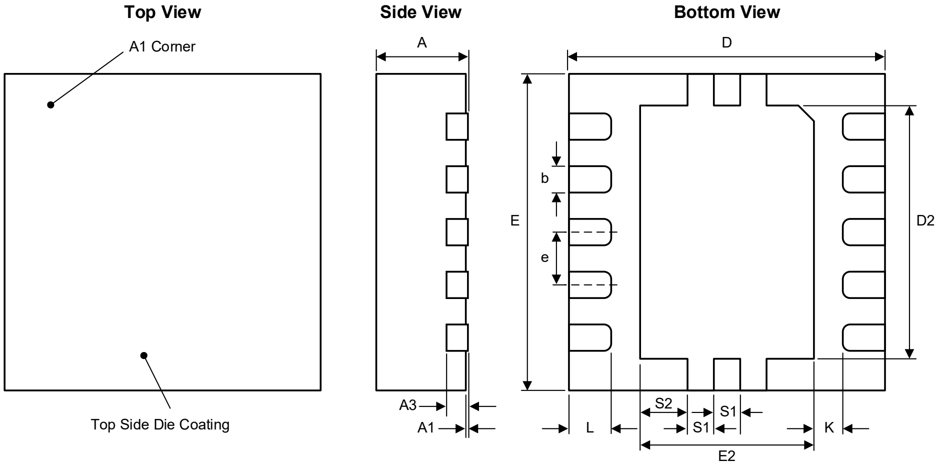


Figure 4. Recommended PCB Layout

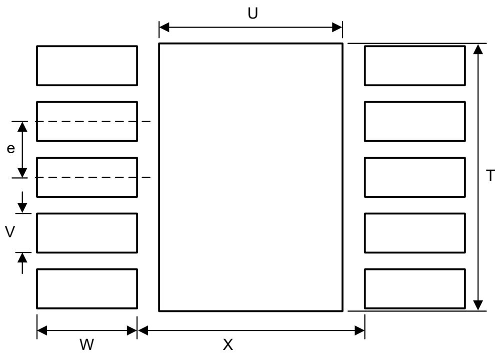
Packaging Information

VDFN33-10 (3.00mm x 3.00mm x 0.85mm)



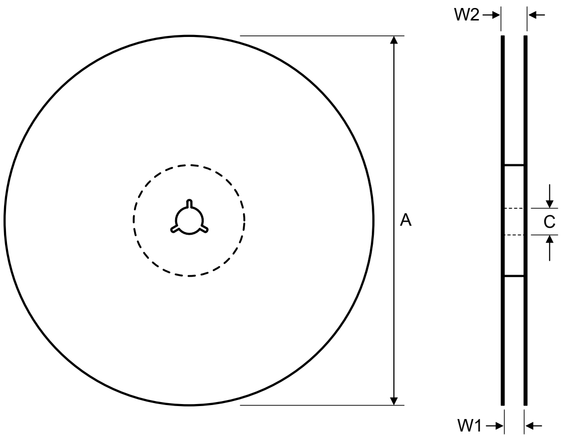
Dimension	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.35	2.40	2.45
E	2.90	3.00	3.10
E2	1.60	1.65	1.70
e	0.50 BSC		
K	0.20	–	–
L	0.35	0.40	0.45
S1	0.25 REF		
S2	0.45 REF		
T	2.40 BSC		
U	1.65 BSC		
V	0.35 BSC		
W	0.9 BSC		
X	2.05 BSC		

Recommended Footprint



Packaging Material Information

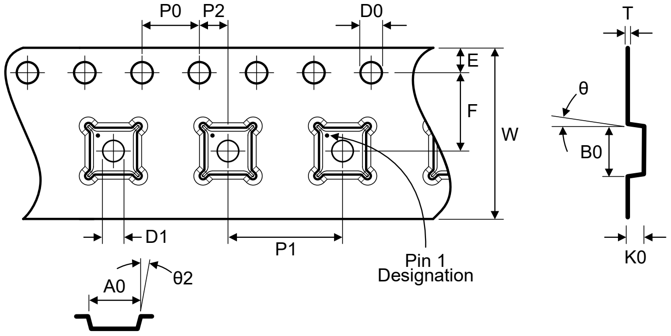
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	180
C	12.8	13.0	13.5
W1	12.4	12.4	14.4
W2	—	—	18.4

DWG-0261.01

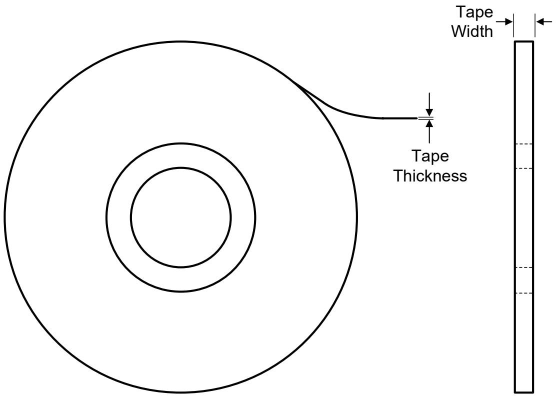
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1.00	1.10	1.20
P0	3.80	4.00	4.20
P1	7.90	8.00	8.10
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	1.50	1.50	1.60
E	1.65	1.75	1.85
F	5.45	5.50	5.55
10P0	39.8	40.0	40.2
W	11.90	12.00	12.30
T	0.25	0.30	0.35
ϴ	0°	—	5°
ϴ2	0°	—	5°

43-010X2-306

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.040	0.050	0.060
12mm	Tape Width	9.2	—	9.5

DWG-0259-01