IEEE 802.3bt-Compliant, PoE Powered Device with DC-DC Controller

Features

- Fully supports IEEE® Std. 802.3af/at/bt
- Supports input power levels up to 90W
- Supports Class 0-8 power (upto 72W) for PoE PD
- Integrated PWM peak current mode controller
- Dual gate driver with dead time adjustment
- High efficiency topologies:
  - Flyback, Forward
  - Flyback with synchronous rectification
  - Flyback with active clamp
  - Forward with active clamp
- Efficiencies upto 92.6%
- Internal slope compensation
- Internal pull-up resistor in feedback for optocoupler and isolated connection
- Robust Type 1, 2, 3 and 4 PSE detector with proprietary digital filtering line noise
- Auto-adjust Maintain Power Signature (MPS) for Type 1-4 PSE
- Supports up to 5 event classification
- Programmable DC current limit up to 2.2A for 90W applications
- Low R_{DSON} 100V hot-swap FET (typical 0.13Ω)
- IEC 61000-4-2/3/4/5/6 requirements for EMC Compliance
- Exceptional EMI performance
- Frequency dithering programming pin for spread-spectrum frequency operation
- Integrated Short-Circuit Protection (SCP) and OCP
- Over temperature protection (OTP)
- Seamless support for local power down to 9.5V
- Supports low power standby modes
- Auto class support
- 4x4mm, 32-lead WQFN Package
- -40°C to +125°C Junction Temperature Range

Brief Description

The KTA1142 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE) Powered Devices with a PWM controller that integrates all the circuitry required to design a smart and efficient converter for PoE and telecom mid-power applications up to 71Watt output load, include Voice over IP (VoIP) Phones, and 5G/LTE Base Stations, Wireless LAN Access Point, Security Cameras, and Notebook computers.

The KTA1142 implements all the physical layer Powered Device (PD) functionality, as required by IEEE® 802.3af-2003 and IEEE® 802.3at-2009 and IEEE® 802.3bt-2019 standards. This includes 8-event classification, Type 1-2 or 3-4 PSE detection indicator, PD detection, under-voltage lockout (UVLO), and Hot-Swap FET integration.

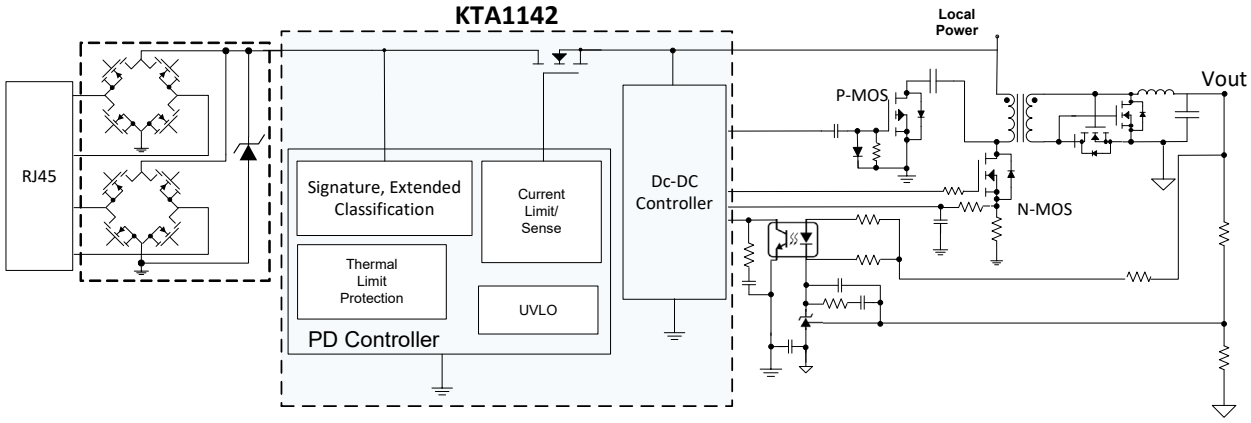
The integrated DC/DC controller features adjustable slope compensation, dual complementary low-side drivers with programmable dead time, programmable soft-start, soft-stop, and a programmable frequency dithering. The controller's main target is Flyback topology or Active Clamp Forward Converter for PoE.BT applications.

The KTA1142 has been architected to address EM emission concerns in PoE applications. The chip implements many design features that minimize transmission of system common-mode noise onto the Unshielded Twisted Pair (UTP). The device is designed to provide safe, low-impedance discharge paths directly to the earth ground, resulting in superior reliability and circuit protection.

Applications

- Voice over IP (VoIP) phones, and 5G/LTE Base Stations
- Pan, tilt and zoom (PTZ), security and web cameras
- Lighting and High-Power Wireless Data Systems
- Wireless LAN access points, WiMAX terminals
- Point-of-Sale (POS) terminals, RFID terminals
- Thin clients and notebook computers
- Fiber-to-the-home (FTTH) terminals

Typical Application

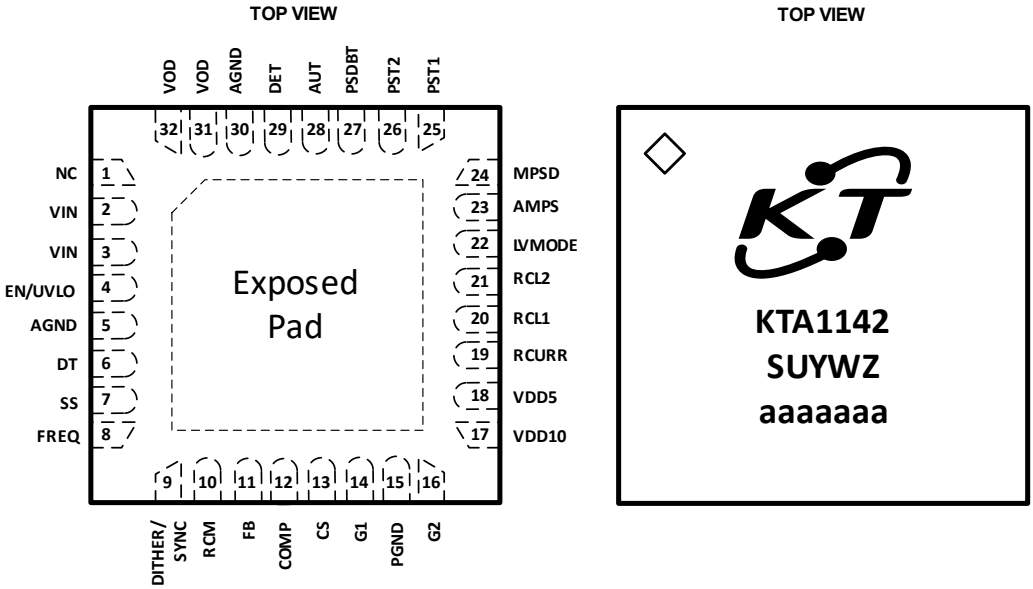


Ordering Information

Part Number	Marking[1]	Package
KTA1142EUAT-TB	SUYWZ aaaaaaa	WQFN44-32

Pinout Diagram

WQFN44-32



32-Lead 4mm x 4mm x 0.75mm
WQFN Package, 0.4mm pitch

Top Mark

SU = Device ID, YW = Date Code, Z = Serial Number
aaaaaaa = Assembly Lot Tracking Number

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Pin Descriptions

Pin #	I/O	Name	Function
1	-	NC	Not Connected.
2, 3	P	VIN	Positive bus pin fed by the output of the external diode bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to Detection Mode section.
4	A/I	EN/UVLO	Enable, and Undervoltage detection and protection pin.
5	A	AGND	Analog ground pin.
6	A/I	DT	Dead time set between two gate signals.
7	A/I	SS	Soft-start/Soft-stop set. A capacitor connected from this pin to AGND sets the converter soft-start/Soft-stop time. Use of stable ceramic capacitors is recommended.
8	A/I	FREQ	Switching frequency set. An external resistor connected from FREQ to AGND can set the oscillator frequency.
9	A/I	DITHER/SYNC	Frequency Dithering Programming or Synchronization Connection. DITHER: For spread-spectrum frequency operation and improve EMI using internal oscillator, connect a capacitor from DITHER to AGND and a resistor from DITHER to FREQ pins. SYNC: Use this pin to synchronize the internal oscillator to the externally applied frequency.
10	A/I	RCM	Slope compensation programming input and resistor. A resistor connected from this pin to AGND programs the amount of internal slope compensation. Can not be floated.
11	A/I	FB	If E/A is used for the part, this FB pin will be the input of E/A.
12	A/I	COMP	Comp pin to control the target output voltage. This pin will be output of E/A. Connect the compensation network between COMP and AGND for non-isolated applications. Connect optocoupler output to COMP directly for isolated applications.
13	A/I	CS	CS pin is used to sense the peak current utilized for current mode control and for current Limiting/protection functions.
14	O	G1	Main gate driver output of the PWM controller.
15	P	PGND	Power Ground Pin.
16	O	G2	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs.
17	O	VDD10	Output of the internal high-voltage regulator for 10V
18	O	VDD5	Output of the internal high-voltage regulator for 5V
19	A/I	RCURR	Current limit pin. RCURR =GND for AF, RCURR = 5kΩ for AT, RCURR = 10kΩ for BT1, RCURR = Open for BT2.
20	A/I	RCL1	Connect a resistor from RCL1 to GND to program the first classification current.
21	A/I	RCL2	Connect a resistor from RCL2 to GND to program the second classification current.
22	A/I	LVMODE	Local Voltage Mode. When above 1.7V, LVMODE opens the internal Hot-Swap FET and keeps the DC-DC controller active. This is a voltage-mode input pin. It should be pulled to GND when not in use.
23	A/I	AMPS	Automatic Maintain Power Signature (MPS) control pin. Connect a resistor with appropriate power rating (to support the MPS current) from AMPS to GND to program the MPS current amplitude. Leave AMPS open to disable the automatic MPS function.

Pin Descriptions (continued)

Pin #	I/O	Name	Function
24	A/I	MPSD	Maintain Power Signature (MPS) duty cycle select input, referenced to GND, internally driven by a precision current source with voltage limited to less than ~5.5V. A resistor connected to GND determines if the MPS duty cycle selected is either 5.4% (open), 8.1% (~60.4kΩ) or 12.5% (short).
25	O	PST1	PSE Type Indicator. Output, Open Drain active-low, Class result LSB output. This pin is referenced to GND
26	O	PST2	PSE Type Indicator2. Output, Open Drain active-low Class result MSB output. This pin is referenced to GND.
27	O	PSDBT	POE PSE TYPE/Power BT detects. This pin is also referenced to GND. Output, Open Drain active-low. Low level output indicates availability of PoE.BT higher system power level in Type 3 or 4
28	A/I	AUT	Auto-class enable input pin. Internally pulled-up to internal VDD rail during classification only, pulled down in other circumstances to minimize consumption. Pull low (to GND) to enable the Auto class function during classification. Leave open otherwise.
29	A/I	DET	Connect a 25.5kΩ resistor from DET to VIN to provide the PoE detection signature. Pull DET to GND to disable the pass MOSFET during powered operation. This pin cannot float.
30	A	AGND	Analog ground pin.
31, 32	P	VOD	Switched supply and Hot Swap output and Input source for DC/DC controller.
EP	-	Exposed Pad	Local ground. This is the negative output from the external diode bridge and is not isolated from the line input.

I = Input, O = Output, A = Analog Signal, P = Power

Absolute Maximum Ratings[2]

(T_A = 25˚C unless otherwise noted)

Symbol	Description	Value	Units
VIN, VOD, DET	High Voltage Pins	-0.3 to 100	V
VDD10, G1, G2		-0.3 to 16	V
EN/UVLO, VDD5, DT, SS, FREQ, DITHER/SYNC, RCM, FB, COMP, CS, RCURR, RCL1, RCL2, LVMODE, AMPS, MPSD, PST1, PST2, PSDBT, AUT	Low Voltage Pins	-0.3 to 6	V
TS	Storage Temperature Range	-55 to 165	°C
TJ	Die Junction Operating Temperature Range	-40 to 150	°C

ESD and Surge Ratings[3]

Symbol	Description	Value	Units
VESD_HBM	JEDEC JS-001-2017 Human Body Model (HBM)[4]	2	kV
VESD_CDM	JESD22-C101, Charged device model (CDM), All pins	0.5	kV
VESD_CD	IEC61000-4-2 Contact Discharge[5]	8	kV
VESD_AGD	IEC61000-4-2 Air Gap Discharge[5]	15	kV

Thermal Capabilities[6]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	34.35	°C/W
P_D	Maximum Power Dissipation	3.64	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-29.1	mW/°C

Recommended Operating Conditions

Symbol	Description	Min.	Typ.[7]	Max.	Units
$V_{IN-AF\ (Type\ 1\ PD)}$	Input Power Supply	37	48	57	V
$V_{IN-BT\ (Type\ 3,4\ PD)}$		42.5	48	57	V
V_{IN-LP}	Local Power Mode (VOD and GND)[8]	9.5		57	V
T_A	Ambient Operating Temperature Range	-40		+85	°C
T_J	Recommended Junction Operating Temperature	-40		+125	°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
4. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
5. Air Discharge, and Contact Discharge are specified at the system level.
6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
7. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.
8. Power transformer must be capable of handling the full voltage range.

Electrical Characteristics[9]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

PD (all PD voltage limits specified at the RJ45 Interface)

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{INRUSH_AF}	Inrush Current Limit (AF) – Type 1 PD	For V_{OUT} ≤ 16V during startup	50	120	240	mA
I_{INRUSH_AT}	Inrush Current Limit (AT) – Type 2 PD	For V_{OUT} ≤ 16V during startup	210	320	400	mA
I_{INRUSH_BT}	Inrush Current Limit (BT) – Type 3 PD	For V_{OUT} ≤ 16V during startup, (SINGLE-SIGNATURE)	300	410	500	mA
I_{INRUSH_BT2}	Inrush Current Limit (BT) – Type 4 PD	For V_{OUT} ≤ 16V during startup, (SINGLE-SIGNATURE)	380	530	630	mA
I_{IN_AF}	Operating Current – Type 1	R_{CURR} = GND; device configured for 13W operation			450	mA
I_{IN_AT}	Operating Current – Type 2	R_{CURR} = 5kΩ, device configured for 30W operation			800	mA
I_{IN_BT1}	Operating Current – Type 3	R_{CURR} = 10kΩ; device configured for 60W operation			1500	mA
I_{IN_BT2}	Operating Current – Type 4	R_{CURR} = left open; device configured for 90W operation			2200	mA
$I_{LIM\text{-}AF}$	PoE Current Limit– Type 1	R_{CURR} = GND; device configured for 13W operation	450	600		mA
$I_{LIM\text{-}AT}$	PoE Current Limit – Type 2	R_{CURR} = 5kΩ device configured for 30W operation	800	1000		mA
$I_{LIM\text{-}BT1}$	Operating Current – Type 3	R_{CURR} = 10kΩ; device configured for 60W operation	1500	1800		mA
$I_{LIM\text{-}BT2}$	Operating Current – Type 4	R_{CURR} = left open; device configured for 90W operation	2200	2700		mA
$R_{DS\text{-}ON}$	Hot-Swap FET On Resistance	I_{IN} = 2A		0.13	0.2	Ω
V_{DET_MIN}	Min Detection Signature voltage				2.7	V
V_{DET_MAX}	Max Detection Signature voltage		10.1	12.5	14.5	V
V_{CL_LOW}	Classification Lower Threshold	V_{IN} Rising, Classification turn on	11.0	12.5	14.5	V
$V_{CL\_LOW\_HY}$	Classification lower threshold hysteresis			1.4		V
V_{CL_HIGH}	Classification Upper Threshold	V_{IN} Rising, Classification turn off	20.5	22.0	25	V
$V_{CL\_HIGH\_HY}$	Classification Upper Threshold hysteresis			1.1		V
V_{MARK_MIN}	Min Mark Event Voltage				6.9	V
V_{MARK_MAX}	Max Mark Event Voltage		10.0	12.5	13.0	V
V_{CLMK_HYS}	Classification-Mark Hysteresis			1.5		V
V_{CL_RST}	Classification Reset Voltage		2.8		6.90	V
$I_{CLASS\_}$	Classification Current: signature 0 (RCL to VDD5 or NC)	For Voltage classification range: 12.5 < V_{CL} < 20.5	1		4	mA
	Classification Current: signature 1 (RCL = 280K)		9		12	
	Classification Current: signature 2 (RCL = 143K)		17		20	
	Classification Current: signature 3 (RCL = 90.9K)		26		30	
	Classification Current: signature 4 (RCL = 63.4k)		36		44	
$V_{IN\_UVLO\_R}$	Input UVLO Threshold	V_{IN} Rising	35.8	38	42	V
$V_{IN\_UVLO\_F}$		V_{IN} Falling	30	32	34	
T_{FLC}	First long class event timing		75.5	81.5	87.5	ms

9. It is guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[10]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

VDD5 Internal Regulator

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{VDD5}	Output Voltage	C_{VDD5} = 1µF		4.7		V

Detection Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{DET}	Detection Resistance		23.8	25.5	26.0	KΩ
V_{DOF}	Detection offset voltage				0.6	V

Maintain Power Signature (MPS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{MPS}	MPS Current Enable Threshold	Load current falling		70		mA
R_{AMPS}	Resistance options on AMPS pin to GND to program the MPS current amplitude.	R_{AMPS} = 237kΩ		10		mA
		R_{AMPS} = 150kΩ		16		
		R_{AMPS} = 118kΩ		20		

Local Power Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LV}	LVMODE Threshold LOW			1.2	1.3	V
V_{HV}	LVMODE Threshold HIGH		1.6	1.7		V

EN/UVLO Pin Threshold Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
EN	En Threshold	V_{EN} Rising		1.2		V
EN_H	En Hysteresis			150		mV

Feedback (FB)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage		1.176	1.2	1.224	V

VDD10

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{VDD10}[11]	VDD10 regulation	VIN = 48, I_{VDD} = 1mA	9	10	11.5	V
I_{VDD10}	Supply current			20		mA

10. It is guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

11. VDD10 provides bias for the internal gate drive.

Ramp/Slope Compensation

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SLOPE}	Slope Bias Current of RCM pin			10		µA
R_{SLOPE}	Slope resistor range		20		200	KΩ
	Slope Compensation ramp	For RCM = 100KΩ (slope = 5mV/µs per KΩ)		500		mV/µs

Current Limit/Protection

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CSD}	Current limit threshold		240	300	340	mV

Soft-Start/Soft Stop (SS)

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SSC}	Soft start charger current			10		µA
I_{SSD}	Soft-stop Dis-charger current			10		µA

Dithering Ramp Generator

Symbol	Description	Conditions	Min	Typ	Max	Units
$I_{DITHERC}$	Charging Current			50		µA
$I_{DITHERD}$	Discharging Current			50		µA
V_{RH}	Ramp High Trip			2		V
V_{RL}	Ramp Low Trip			0.4		V

Oscillator (FREQ)

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Freq Range		100		1200	KHz
D_{MAX}	Maximum duty cycle	VIN = 48V, DT = 0nS		82		%

Gates Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T_R	Rise Time	CLOAD = 2.0nF, VDD = 10V		15		ns
T_F	Fall Time	CLOAD = 2.0nF, VDD = 10V		15		ns
	Peak current Source			1.5		A
	Peak current Sink			1.5		A

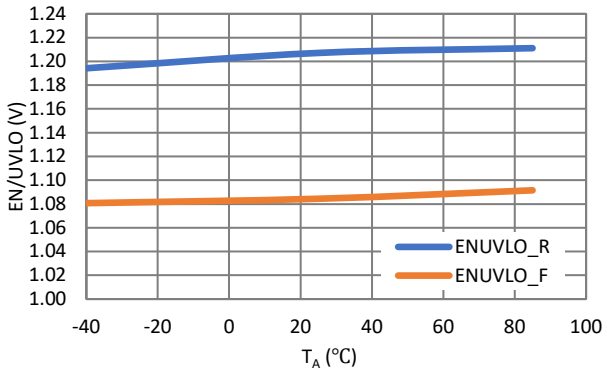
Thermal Protection Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{J_TS}	Thermal Shutdown Temperature			160		°C
T_{J_HYS}	Thermal Shutdown Hysteresis			30		°C

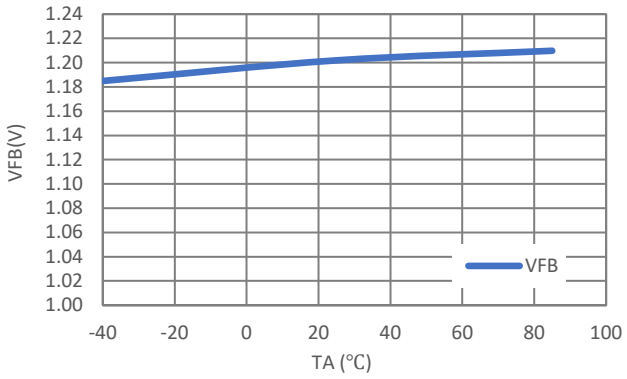
Typical Characteristics

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

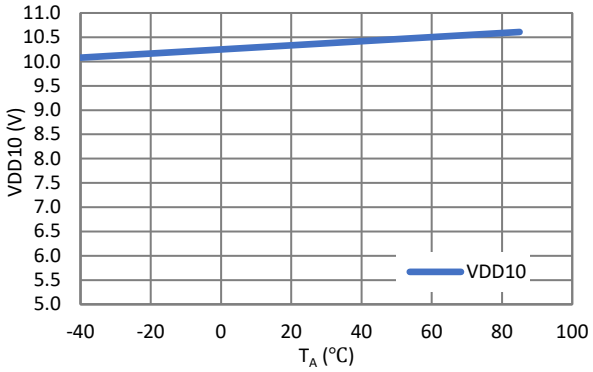
EN/UVLO vs. Temperature



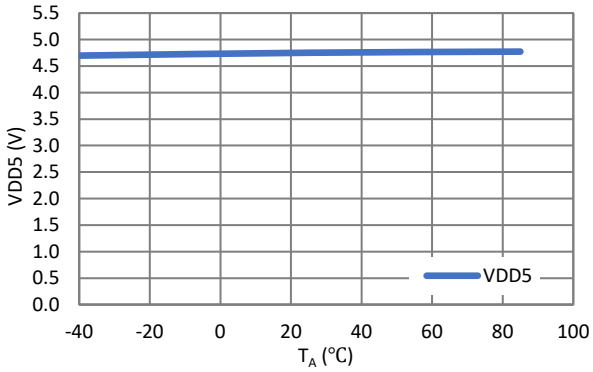
VFB vs. Temperature



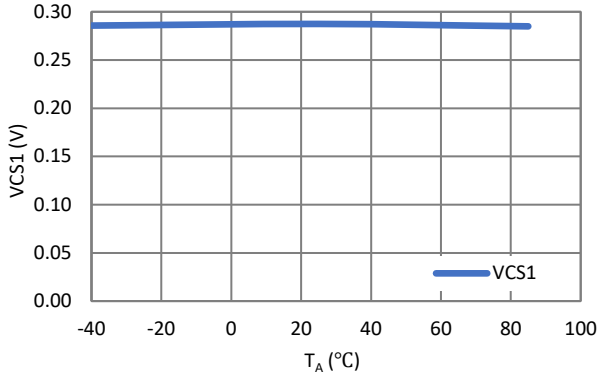
VDD10 vs. Temperature



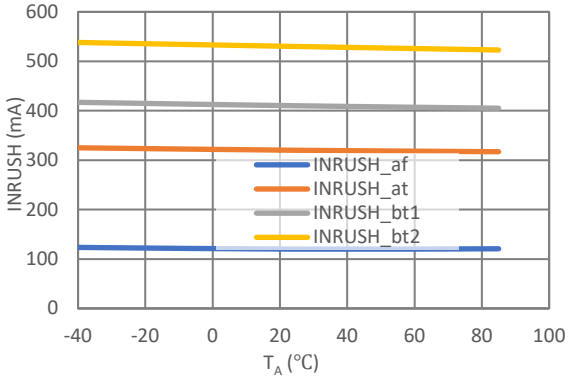
VDD5 vs. Temperature



VCS1 vs. Temperature



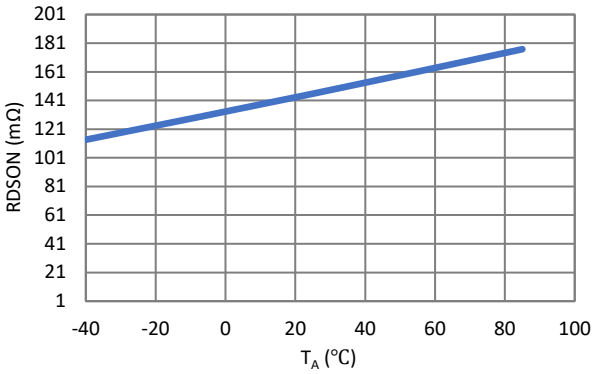
Inrush vs. Temperature



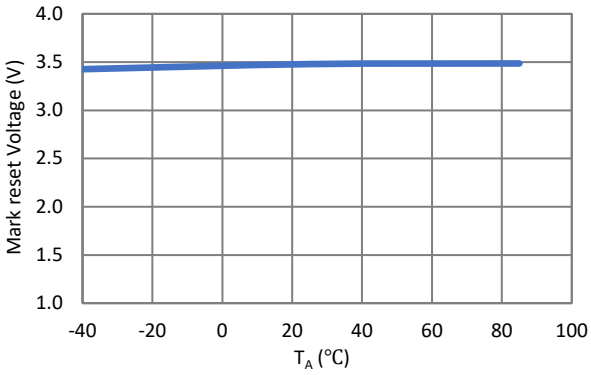
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

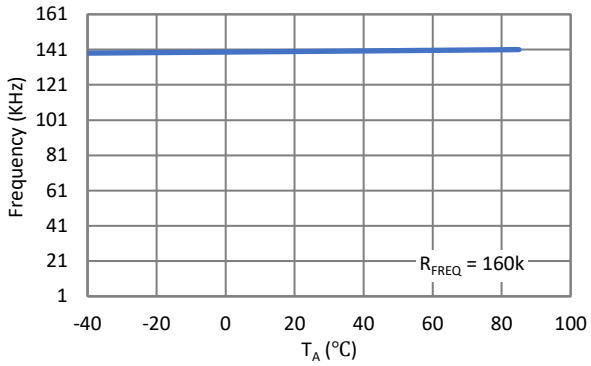
Hot-Swap FET R_{DSON} vs. Temperature



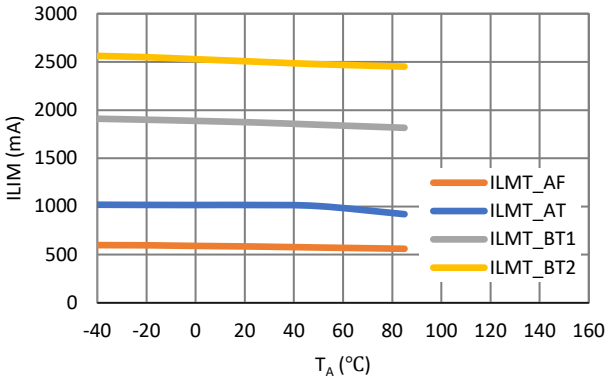
Mark Reset Voltage vs. Temperature



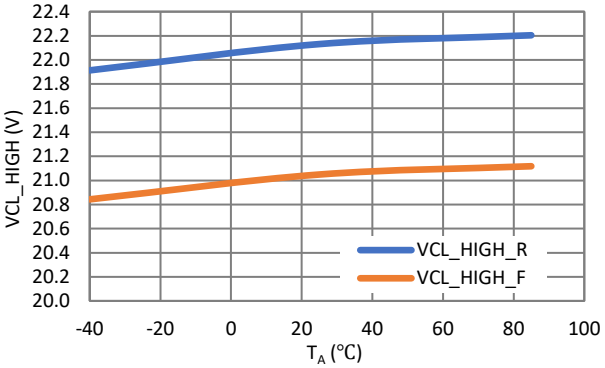
Frequency vs. Temperature



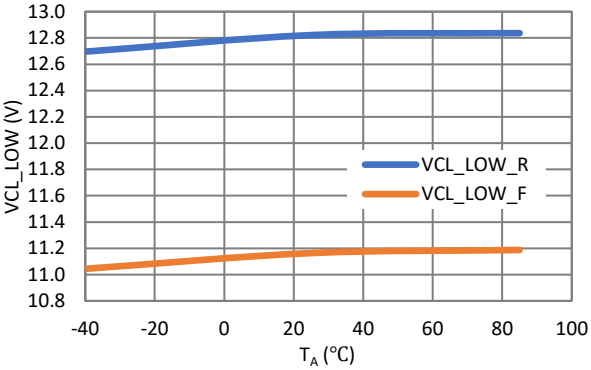
PD Current LIMIT vs. Temperature



Classification Upper Threshold vs. Temperature



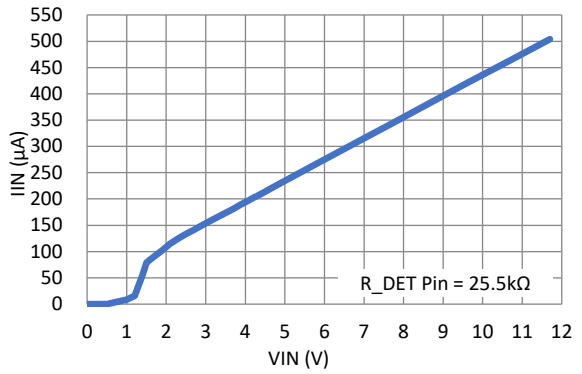
Classification Lower Threshold vs. Temperature



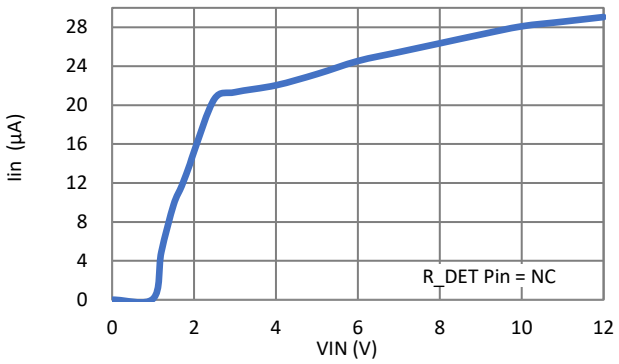
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

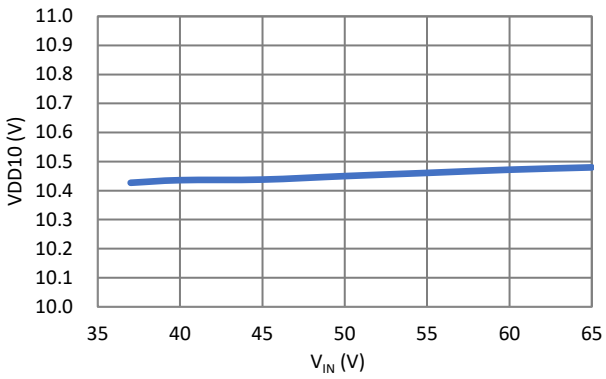
Detection Current vs. Input Voltage



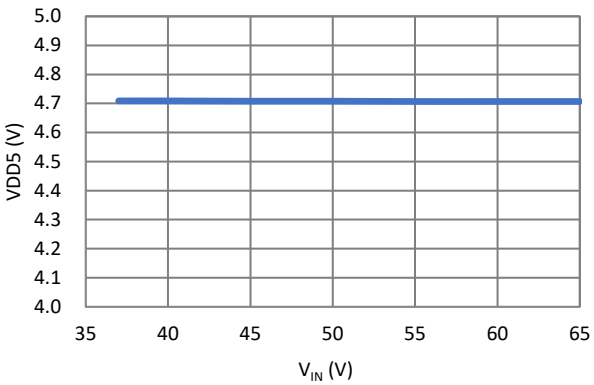
Quiescent Current vs. Input Voltage



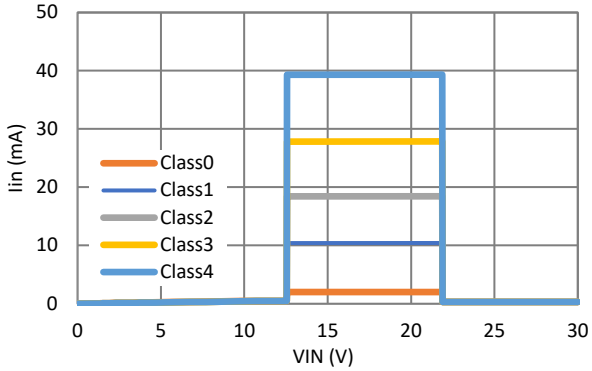
VDD10 vs. V_{IN}



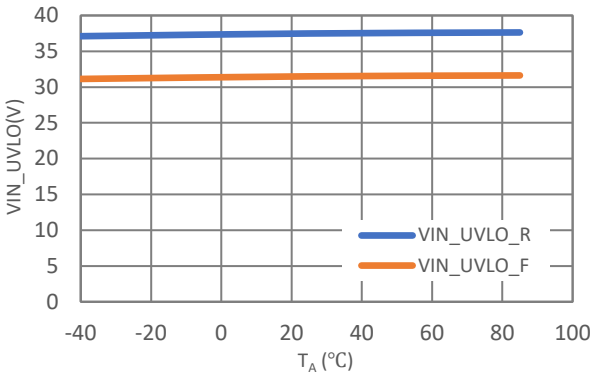
VDD5 vs. V_{IN}



Classification Current vs Input Voltage



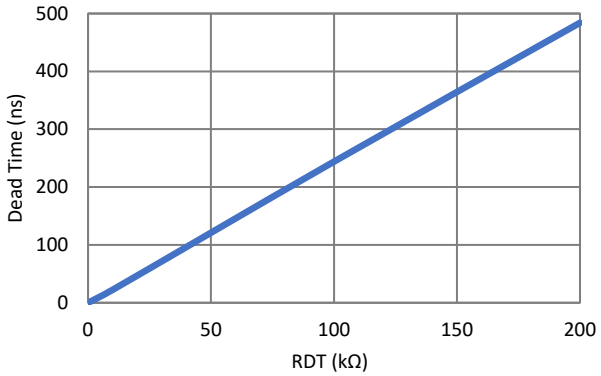
V_{IN_UVLO} vs. Temperature



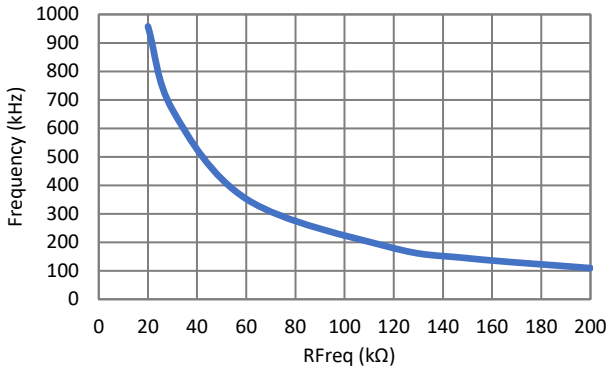
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

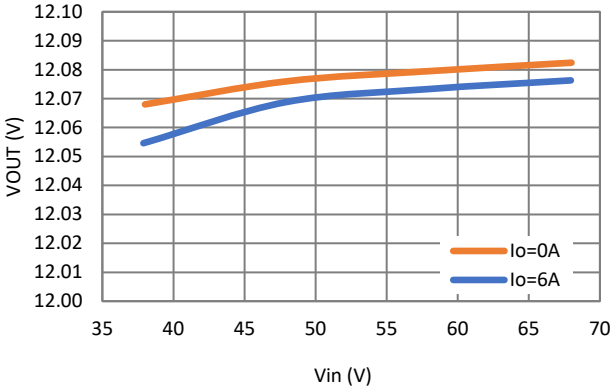
Dead Time vs. Programming Resistance



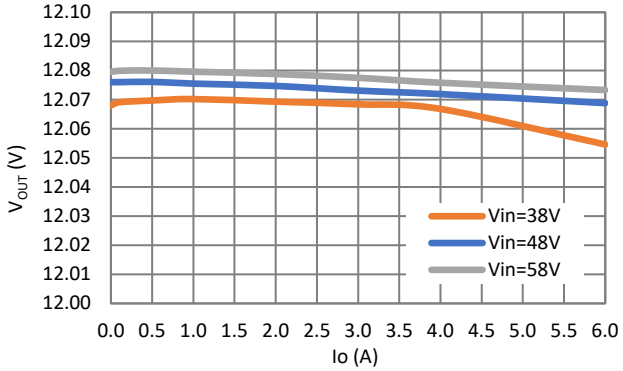
Switching Freq. vs. Programming Resistance



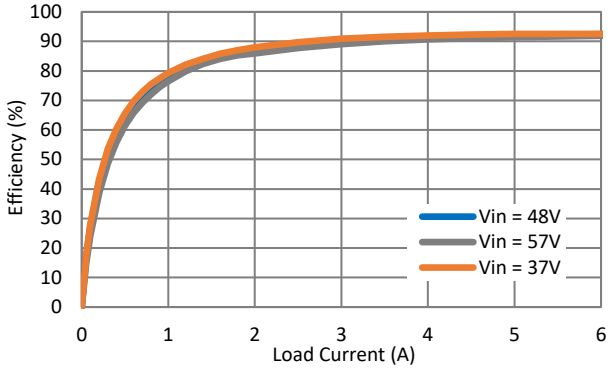
Line Regulation



Load Regulation



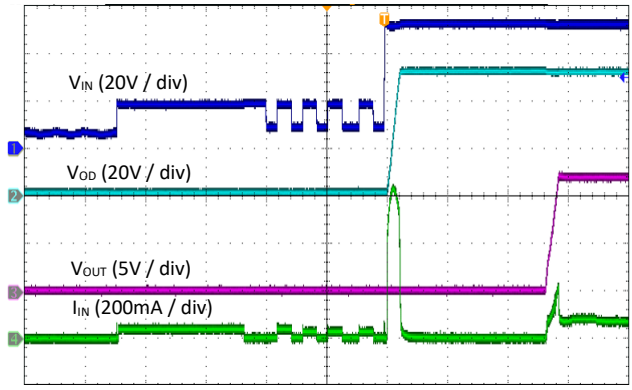
Efficiency vs Load Current



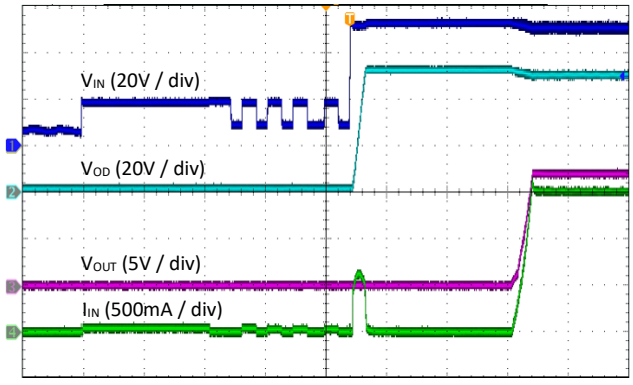
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

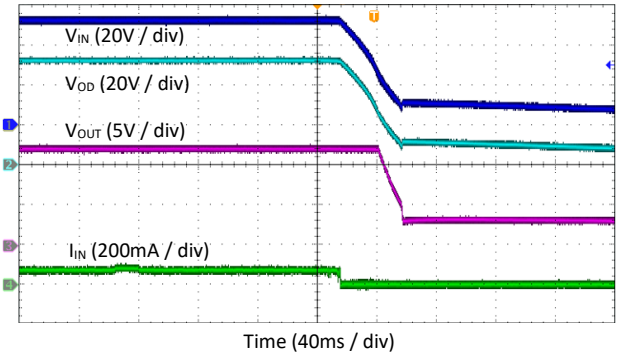
Startup with PSE Input at Downstream 12V-0A Load



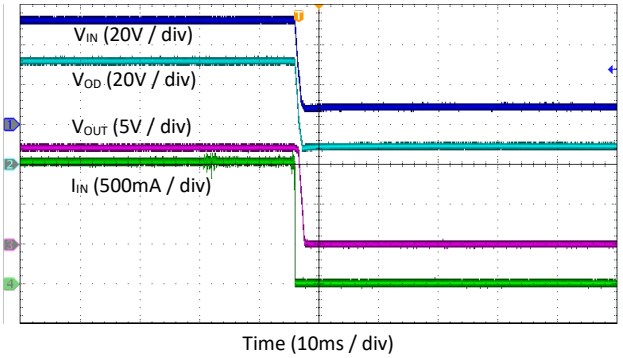
Startup with PSE Input at Downstream 12V-6A Load



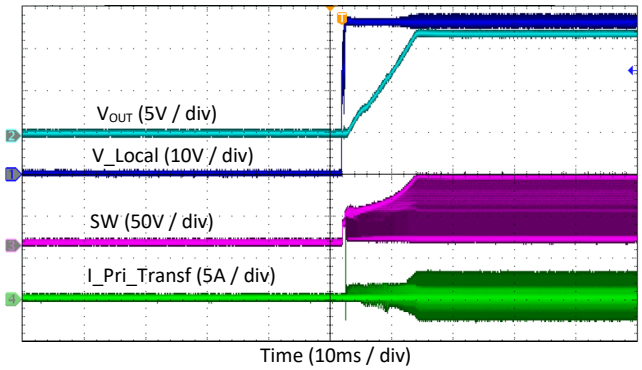
Shutdown by PSE at Downstream 12V-0A Load



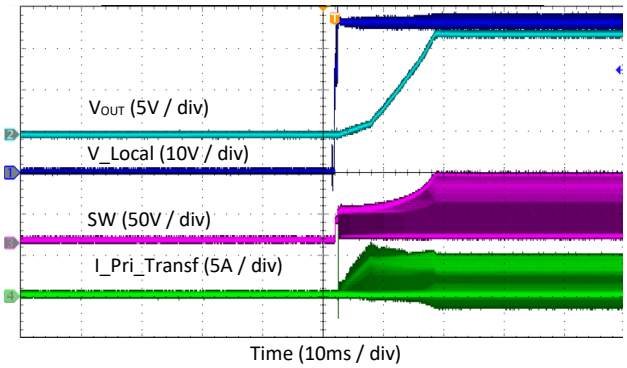
Shutdown by PSE at Downstream 12V-6A Load



Startup with Local Power at Downstream 12V-0A Load



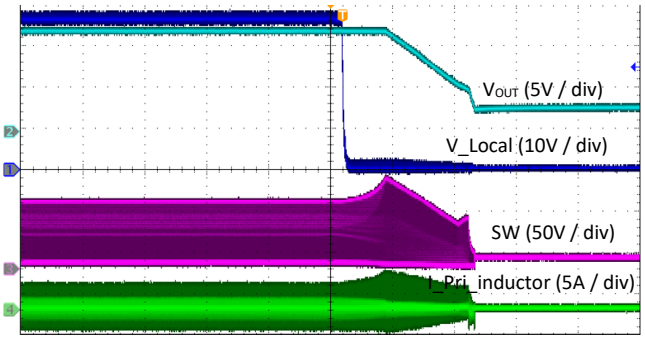
Startup with Local Power at Downstream 12V-6A Load



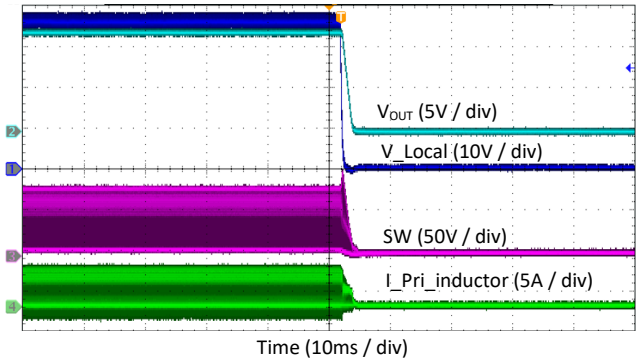
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

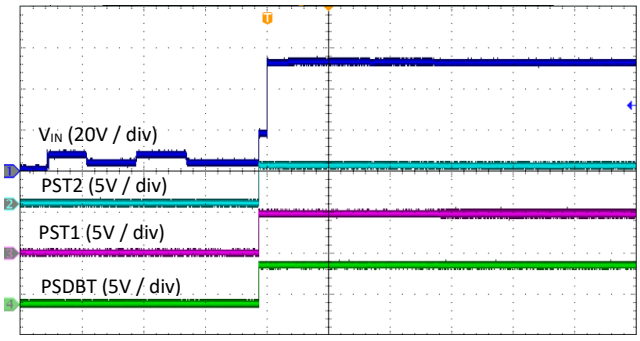
Shutdown with Local Power at Downstream 12V-0A Load



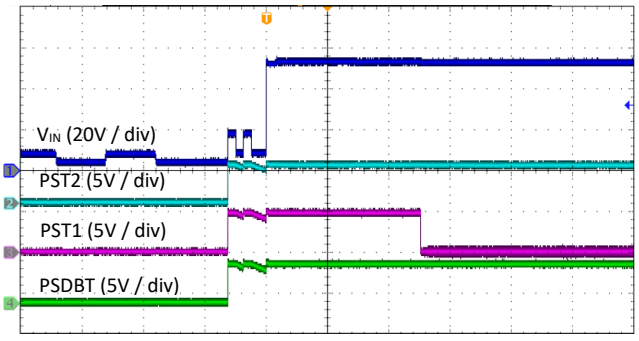
Shutdown with Local Power at Downstream 12V-6A Load



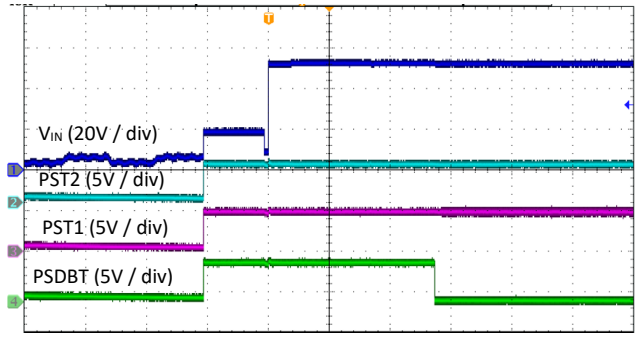
PSDBT PST Detect at PD Class0-3, af/at PSE



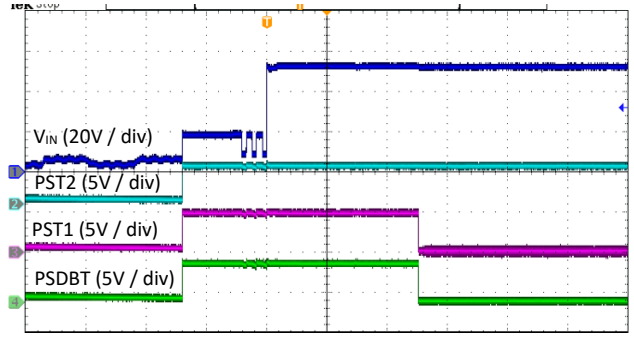
PSDBT PST Detect at PD Class4, af/at PSE



PSDBT PST Detect at PD Class0-3, bt PSE



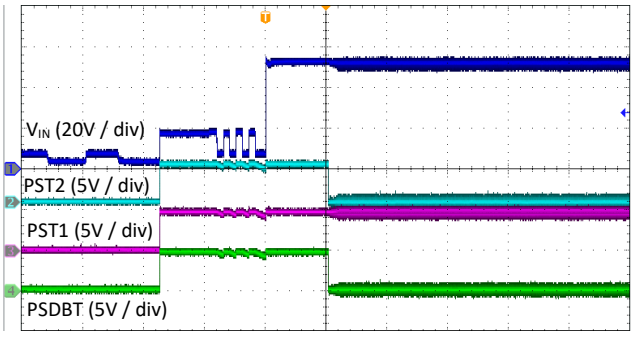
PSDBT PST Detect at PD Class4, bt PSE



Typical Characteristics (continued)

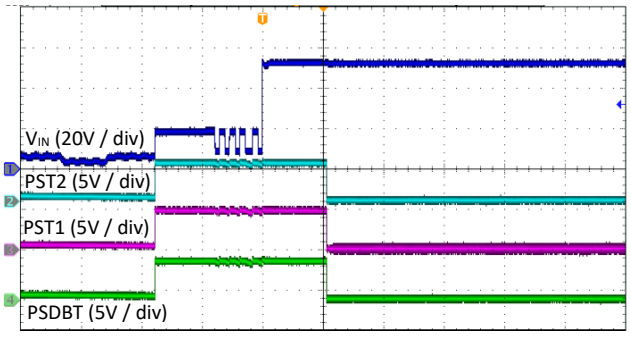
V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

PSDBT PST Detect at PD Class5-6, bt PSE



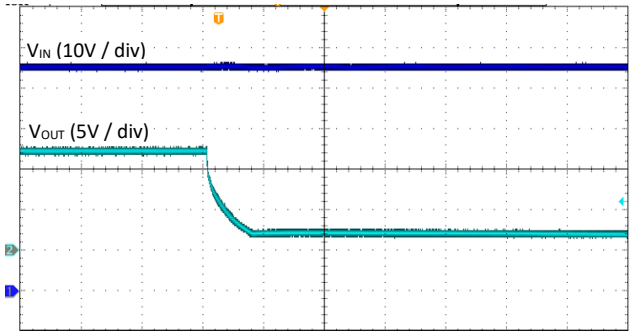
Time (100ms / div)

PSDBT PST Detect at PD Class7-8, bt PSE



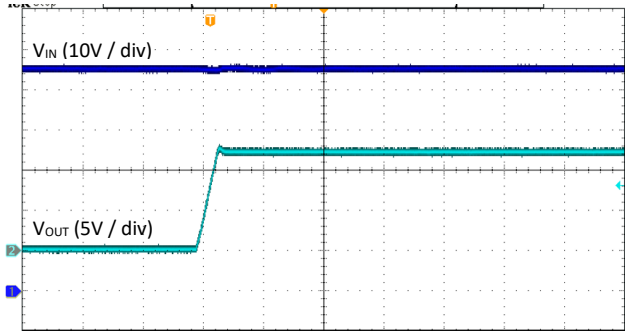
Time (100ms / div)

Over Temperature Protection



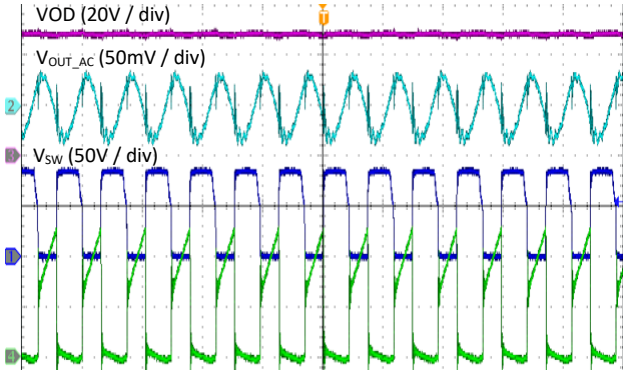
Time (20ms / div)

Over Temperature Protection Restart



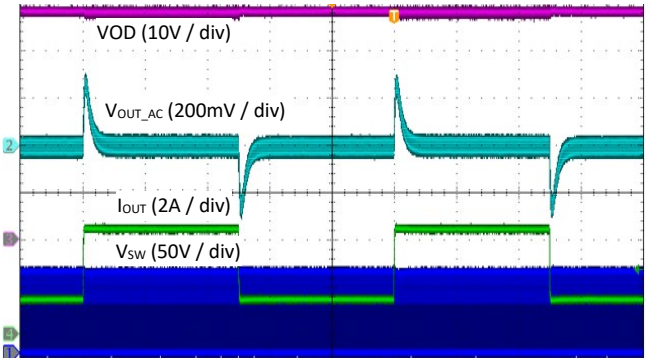
Time (20ms / div)

Steady State Switching (12V-6A load)



I_Primary-Transform (2A / div)

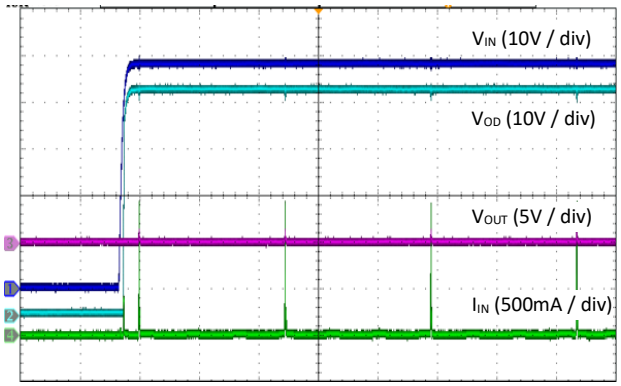
Transient Load Response (1.5A-4.5A load)



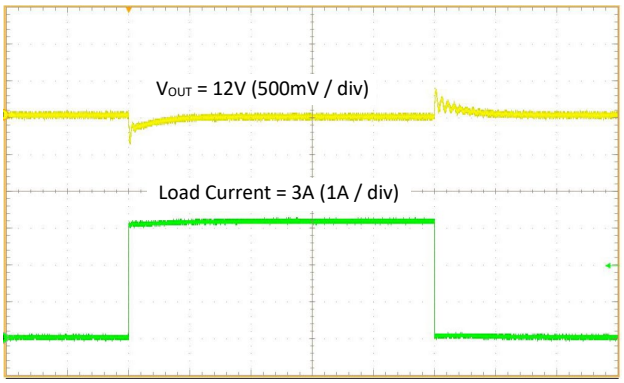
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

V_{OUT} Short Protection

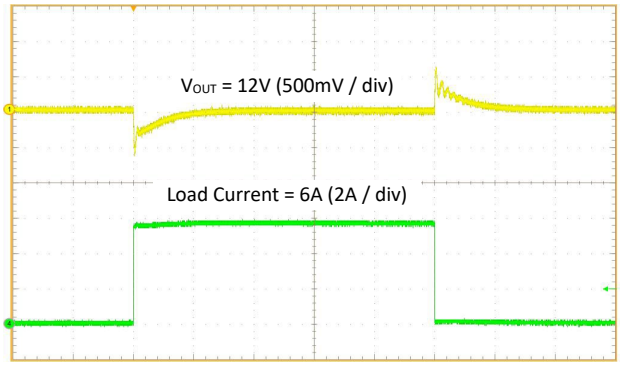


Load Transient Response (0A to 3A)



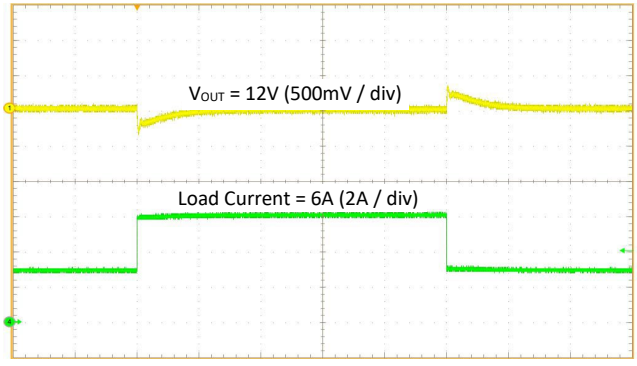
500µs / div

Load Transient Response (0A to 6A)



500µs / div

Load Transient Response (3A to 6A)



500µs / div

Functional Block Diagram

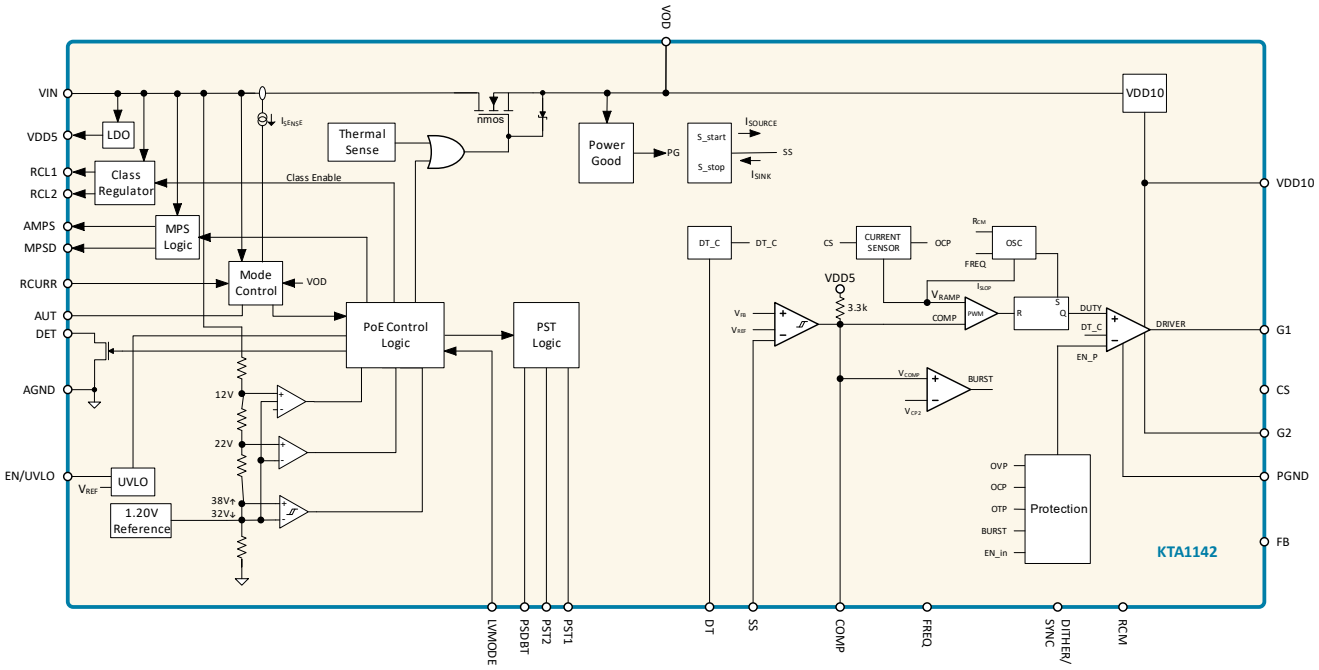


Figure 1. Functional Block Diagram

Functional Description

Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE® Std. 802.3af, 802.3at and 802.3bt are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and receives the agreed-upon power. IEEE® Std. 802.3af limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE® 802.3at allows for >13W power levels and up to <25.5W (Type 2 PD). There two higher power levels in IEEE® 802.3bt limit PSE power delivery to <51W (Type 3 PD) and <71.3 (Type 4 PD) at the PD input.

Table 1. Classification Settings for PoE Power Device

PD Requested Class	Standard	PD Power (Watt)	PSE Power (Watt)	PD Type	MAX Number of Events	2 or 4 Pair Power	Auto Class
0	802.3af	12.95	15.4	1	-	2 or 4 Pair	NO
1	802.3af	3.84	4	1	1	2 Pair Only	NO
2	802.3af	6.49	7	1	1	2 Pair Only	NO
3	802.3af	12.95	15.4	1	1	2 or 4 Pair	NO
4	802.3at	25.5	30	2	2	2 or 4 Pair	NO
5	802.3bt	38.25	45	3	4	4 Pair Mandatory	Optional
6	802.3bt	51	60	3	4	4 Pair Mandatory	Optional
7	802.3bt	62	75	4	5	4 Pair Mandatory	Optional
8	802.3bt	71.3	90	4	5	4 Pair Mandatory	Optional

The PSE uses the following sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

- **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
- **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
- **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available from the PSE.
- **On** — Operational state, during which the PSE provides the allocated power level to the PD.
- This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply listed in Table 2:

Table 2. PoE Requirements

Requirement	Value
Input voltage at Type 1 PD interface	37V-57V
Input voltage at Type 2 PD interface	42.5V-57V
Input voltage at Type 3 PD interface	42.5V-57V
Input voltage at Type 4 PD interface	41.1V-57V
Output voltage from Type 1 PSE	44V-57V
Output voltage from Type 2 PSE	50V-57V
Output voltage from Type 3 PSE	50V-57V
Output voltage from Type 4 PSE	52V-57V
Minimum operating current limit, Type 1 @ PSE min output voltage	350mA
Minimum operating current limit, Type 2 @ PSE min output voltage	600mA
Minimum operating current limit, Type 3 @ PSE min output voltage	600mA per pair
Minimum operating current limit, Type 4 @ PSE min output voltage	960mA per pair

KTA1142 Detailed Overview

The KTA1142 is a fully integrated PD with DC-DC controller that provides the functionality required for Power-over-Ethernet (PoE) applications with Active Clamp control for isolated DC/DC solution such as Flyback or Forward converter circuit configurations. The optimized architecture reduces external component cost in a small footprint while delivering high performance.

To meet PoE standards requirements, the KTA1142 includes a fully integrated PoE PD controller for Type1-4 PD implementations. The KTA1142 meets all system requirements for the IEEE® 802.3 standard for Ethernet and all power management requirements for IEEE® standard 802.3bt-2018.

The KTA1142 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External rectification bridges protect against polarity reversal, to provide alternative detection.

The KTA1142 also passes the 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of KTA1142-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions.

Rectification and Protection

To protect against polarity reversal, an external Rectification bridge is required. In conjunction with the external bridge, the KTA1142 provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The KTA1142 is implemented in a robust 100V process technology. By integrating robust input protection circuitry, Kinetic has produced a solution that provides much faster response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge paths directly to earth ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, voltages do not exceed critical breakdown and spark gap limits, protecting the PD from damage by the event. This enables system designers to achieve 15kV/8kV Air/Contact Discharge system ESD performance.

PD Controller

The KTA1142 PD Control Interface is designed to provide full PD functionality for IEEE® 802.3af/at/bt compliant systems, with programmable support for standard PD control functions.

The PD Controller provides the following major functions:

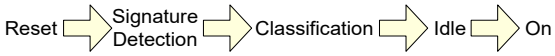
- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Type 4 (Class 8) Power capability for PD supply
- Power management and thermal protection override, including UVLO (Under Voltage Lock Out).
- PSE type indicator output signal pins
- PSDBT Output pin when connected to a PSE.BT that can deliver more than 30Watts.
- 5-Event Physical Layer classification.

Modes of Operation

The KTA1142 has five operating modes:

1. **Reset** — all blocks are disabled.
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via different number of Events Classification for IEEE® 802.3af/at/bt
4. **Idle** — this state is entered after Classification and remains until full-power input voltage is applied.
5. **On** — The PD is enabled and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the KTA1142 transitions through the modes of operation in this sequence:



If no PSE or local power supply is present, line voltage will be zero, which will hold the KTA1142 in the Reset state. The KTA1142 does not affect the Ethernet link function.

Reset

When the voltage supplied to the KTA1142 drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the Reset state. While in Reset, the power supply to the PD is disconnected, the KTA1142 consumes very little power and the device reverts to the pre-detection status.

Detection Mode

During the detection sequence, the PSE periodically applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltages, 1V or more apart, within the detection voltage range of 2.7V to 10.1V. It extracts a detection signature resistance value from the incremental I-V slope. Valid I-V slope resistance values are between 23.75kΩ and 26.25kΩ.

With the KTA1142, detection signature resistance is generated by an external resistor connected between VIN and GND on DET Pin. Typically, this is a 25.5kΩ, 1% resistor. With this value of RSIGNATURE, the PSE normally detects a total effective signature resistance of approximately 25kΩ, which is within the 802.3af/at/bt specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05µ to 0.12µF at 2.7V to 10.1V, and 1.9V maximum offset voltage, per the IEEE® 802.3bt standard, measured at the PD input connector. KTA1142 detection signature capacitance is generated by an external 68nF capacitor connected between VIN and GND. The offset voltage is mainly provided by the external bridge voltage drop.

Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE® Std. 802.3bt defines classes of power levels for PDs, listed in Table 1. The KTA1142 supports IEEE® Std. 802.3af/at and IEEE® Std. 802.3bt up to 5-Event Physical Layer classification, as shown in Figure 2 and Figure 3.

In real applications, noise or transient ringing on the line during classification phase can lead to false classification events or PSE type detection. To prevent such false positives, the KTA1142 integrates a proprietary digital filter to filter out noise events as long as 100µS during the classification phase, ensuring a very reliable BT Detection.

KTA1142 allows the user to program the classification current via external resistors. Each of the two external resistors connected between RCL1 and RCL2 pins and ground provide a distinct classification signature to the PSE, and are used to define the power class requested by the PD.

The current drawn by each resistor, combined with the internal circuit and leakage create the classification signature current. The number of classification cycles then determines how much power is allocated by the PSE. The current, power levels and programming resistor values for each class are shown in Table 3. For Class 0, the pin needs to be pulled up to VDD pin. This can be a direct short to VDD or using a resistor up to 100kΩ.

Use Equation 1 to determine the typical classification current:

$$I_{Class}\,[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \qquad \text{Equation 1}$$

Tolerance = Maximum of ±1.8mA or ±9%

Once the classification process is done, the PD removes the classification current to conserve power.

Table 3. Classification Settings Resistors Selection in RCL1 and RCL2 Pins

PD Class	PD Type	Power (W)	Class 1 Signature	Class 2 Signature	Number of Class Events for Max Power	R_{CL1} (kΩ), 1%	R_{CL2} (kΩ), 1%
0	1	0.44-12.95	0	0	1	Pull-up (0-100kΩ) to VDD pin	Pull-up (0-100kΩ) to VDD pin
1	1	0.44-3.84	1	1	1	280	280
2	1	3.84-6.49	2	2	1	143	143
3	1	6.49-12.95	3	3	1	90.9	90.9
4	2	12.96-25.5	4	4	2,3	63.4	63.4
5	3	25.5-38.25	4	0	4	63.4	Pull-up (0-100kΩ) to VDD pin
6	3	38.25-51	4	1	4	63.4	280
7	4	51-62	4	2	5	63.4	143
8	4	62-71.3	4	3	5	63.4	90.9

Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

On State

In the On state, the KTA1142 is supplying power across the Ethernet line(s) to the PD. Then, the PD turns on and full power is available via the KTA1142 to the DC-DC converter and the systems.

PoE Power-On Startup Waveform

Figure 2 represents the power-on sequence for PoE operation for af and at power level. Figure 3 represents the higher power level up to 5 classification events power-on sequence for PoE.bt operation. These waveforms reflect typical voltages present at the PD during signature, classification and power-on.

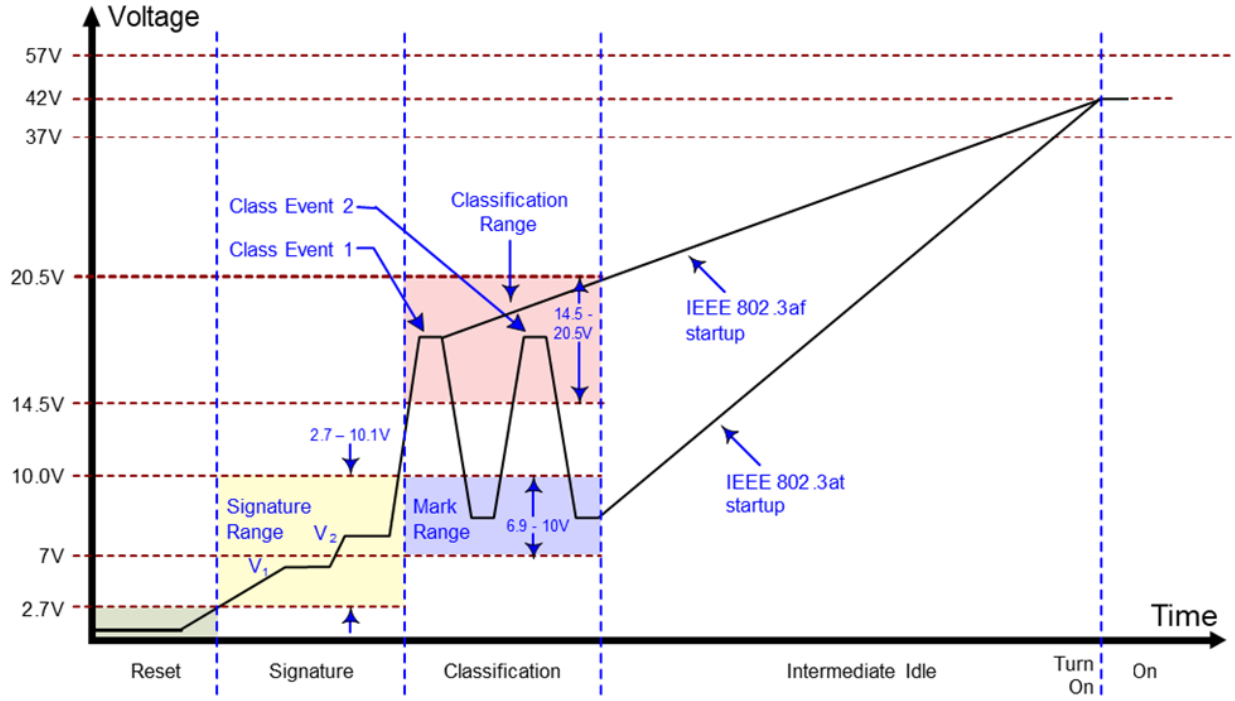


Figure 2. IEEE 802.3af/at Typical Power-On Waveform

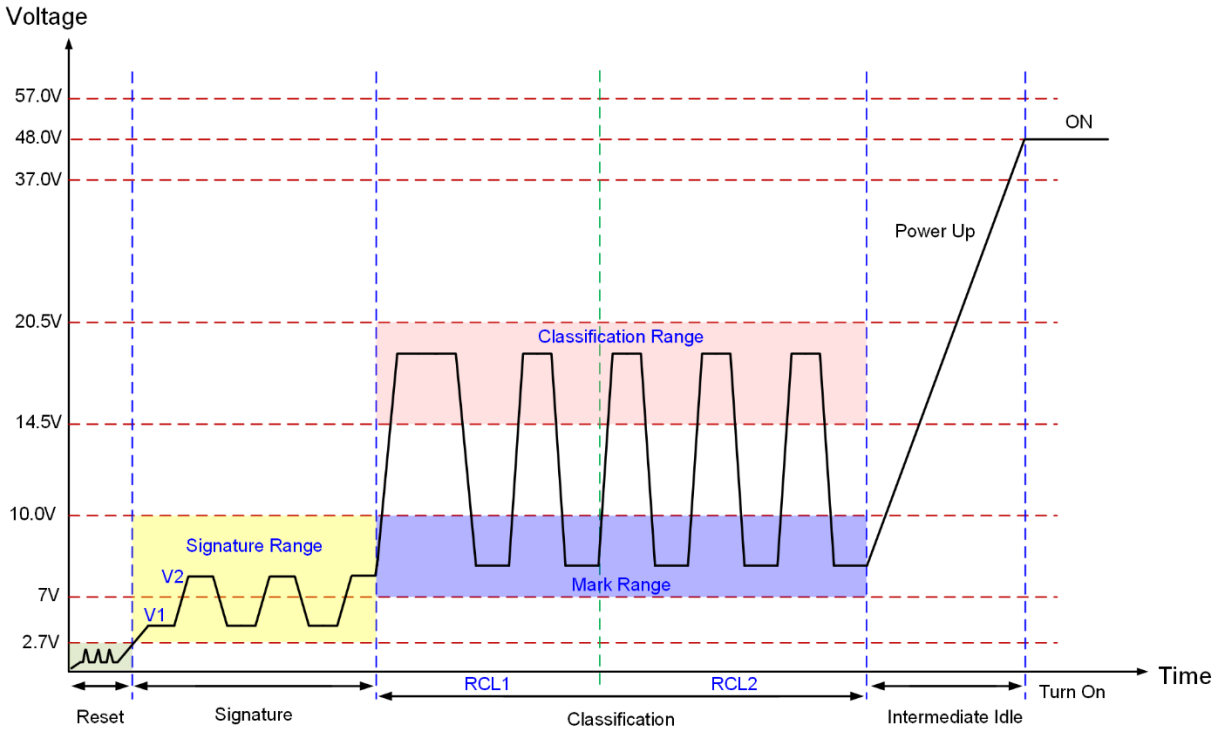


Figure 3. IEEE 802.3bt Typical Power-On Waveform

1. Voltages V1 and V2 with minimum 1V differences are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistances connected to the RCLASS pins (RCL1 and RCL2)
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a classification voltage (14.5V-20.5V). The PD responds by presenting a load current as determined by RCL1 and RCL2. After the PSE measures the PD load current during several class events and determines that it can deliver the requested power, it moves into the On state by raising the voltage to approximately 48V in PoE.BT power levels.

PST1, PST2 and PSDBT Pins

PST1 and PST2 are Open Drain active-low output pins that indicate PSE type and power level. PSDBT output pin provides an indicator when Type 3 or 4 PSE (bt PSE) is detected, PST1 and PST2 output pins indicate the allocated power level. The PSDBT, PST1, PST2 pins will be set low once the PD recognizes the related conditions and completion of internal PG signal set to high after V_{OD} power up, the pins will remain low and will only be reset high by the occurrence of a Reset or a power-down event.

The state of PST1, PST2 and PSDBT is used to provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. Table 4 lists the encoding corresponding to various combinations of PSE Type, PD Class and allocated power.

Demotion conditions also correspond to cases where the PSE allocated power is lower than what the PD is requesting. The allocated power is determined by the number of classification cycles having been received. KTA1142 power demotion details and PST1, PST2 and PSDBT status are provided in Table 5.

Table 4. KTA1142 Power LEVEL Details based on PST1, PST2 and PSDBT Pins Status

PSE Type	PD Class	# Class Events	PSE Power LEVEL	PST1	PST2	PSDBT
1 or 2	0	1	12.95	High	High	High
1 or 2	1	1	3.84	High	High	High
1 or 2	2	1	6.49	High	High	High
1 or 2	3	1	12.95	High	High	High
2	4	2	25.5	Low	High	High
3 or 4	0	1	12.95	High	High	Low
3 or 4	1	1	3.84	High	High	Low
3 or 4	2	1	6.49	High	High	Low
3 or 4	3	1	12.95	High	High	Low
3 or 4	4	2 or 3	25.5	Low	High	Low
3 or 4	5	4	38.25	High	Low	Low
3 or 4	6	4	51	High	Low	Low
4	7	5	62	Low	Low	Low
4	8	5	71.3	Low	Low	Low

Table 5. KTA1142 Power Demotion Details

PSE Type	PD Class	# Class Events	PSE Power LEVEL	PST1	PST2	PSDBT
1 or 2	0	1	12.95	High	High	High
1 or 2	1	1	3.84	High	High	High
1 or 2	2	1	6.49	High	High	High

Local Power Mode (LVMODE)

The LVMODE pin can be used in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local power adapter. The LVMODE pin is a voltage mode input pin with low and high thresholds as defined in the electrical characteristics for the PD. The LVMODE is asserted when the input exceeds the high threshold ~1.7V, and is de-asserted when the input voltage is below the low threshold ~1.2V threshold. If LVMODE operation is not desired, the LVMODE pin should be connected to GND.

A simplified internal implementation and external application circuit required to use the LVMODE feature. When power is applied at the local adapter input, the KTA1142 enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the internal DC-DC controller is in operation.

In this configuration, local power always takes priority, even in presence of PoE power, irrespective of their relative voltages. If local power is removed, the device will exit Local Voltage Mode operation and PoE power will be used, if available.

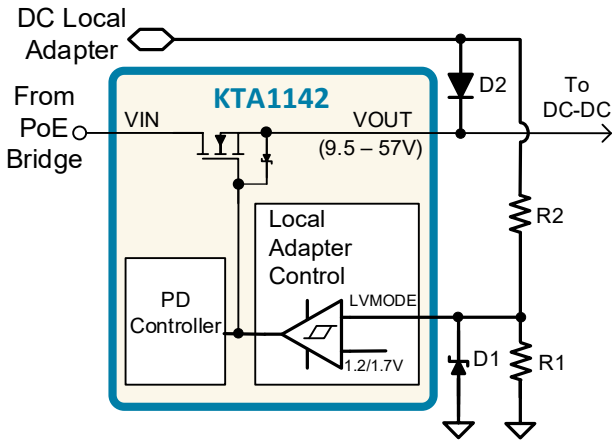


Figure 4. LVMODE Implementation

Local power is inserted at the VOUT node (VOD pin) through an external diode (D2). Use of a low reverse-leakage diode is recommended. This ensures that when there is no local power, PoE voltage at the VOUT node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode.

An appropriate ratio of R2 and R1 resistors should be used to ensure proper operation across all supply voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltages from 9.5V to 57V, using different value pairs, will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V, so a Zener diode (D1) is recommended to limit transient voltage excursions at the pin.

Since the input voltage at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an LED) that might draw current and voltage changes. LEDs or current-absorbing components may be driven directly from the Local Supply pin.

Table 6. LVMODE Configuration

Local Voltage Range	Recommended Local Adapters
9.5V-57V	12V, 18V
20V-57V	24V, 30V
32.4V-57V	36V, 48V

PD Controller Power and Thermal Protection

The KTA1142 provides the following PD controller power and thermal protection:

- Internal default Under Voltage Lock Out (UVLO) for hot swap FET
- EN/UVLO for external configurations for hot swap FET
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

Internal default Under Voltage Lock Out (UVLO) and external EN/UVLO configuration

The KTA1142 contains an internal default Under-Voltage Lock Out (UVLO) circuitry to determine when to power on the PD. The internal default UVLO power on point is 38v and power off point is 32V.

When EN/UVLO pin voltage rise to high logic (higher than 1.2V), it will enable the KTA1142 PD (power on the internal hot swap FET).

When EN/UVLO pin is programed by resistor divider from input voltage, the higher of the UVLO (Internal default UVLO and external programed UVLO) will take control. For example, if the external programed UVLO by EN/UVLO pin is programed at 46V(ON) and 38V(Off), then the KTA1142 PD will power on at 46V and power off at 38V. if the external programed UVLO by EN/UVLO pin is programed at 30V(ON) and 25V(Off), then the KTA1142 PD will power on and off follow the internal default UVLO, that is 38V on and 32V off.

If EN/UVLO is not used, connect it to VDD5, the KTA1142 PD will follow the internal default UVLO to power on (38v) and power off(32V).

The KTA1142 PD circuit controls power flow to the downstream DC-DC converter, to protect the PD from erratic operation or damage.

Inrush Current Limit / Current Sense

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes the PD on-chip temperature peaks by limiting both inrush and operating current.

During the PD startup sequence, VDS across the Hot-Swap FET is momentarily high as the VOUT output capacitance is charged up. During this state, the Hot-Swap FET experiences a high instantaneous power drop and heating. Therefore, it is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VOUT node, to minimize the startup time and associated power drop across the FET. There is a total 108ms time period for inrush. PD OCP will active after inrush time finished. There is a debounce time of 512µs for PD OCP.

Thermal Limit / Protection

The KTA1142 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent its pre-set thermal limits from being exceeded. Thermal current is implemented and disables the Hot swap MOSFET switch above 160˚C. Normal current limits in both cases are re-applied when the die temperature returns below 125˚C.

Maintain Power Signature and AMPS

To have PSE connected to PD controller a minimum amount of current is needed. This is referred to as the Maintain Power Signature (MPS). Depending on the PD assigned Class and PD signature configuration. To maintain PSE power in a very low current situation, the KTA1142 generates a pulsed current to reaches the required threshold to maintain the power. The pulsed current amplitude and period are automatically selected according to PSE Type (1-2, 3-4), to maintain PSE power while minimizing power consumption.

Table 7 shows the details for MPSD pin to select the MPS duty cycle select driven by a precision current source with voltage limited to less than ~5.5V.

Table 7. Maintain Power Signature Duty Cycle Selection Details

PSE Type	MPSD Pin Resistance Value	Duty Cycle	Ton	Toff
1, 2	-	-	88ms	224ms
3, 4	GND	12.5%	20ms	140ms
3, 4	60.4kΩ	8.1%	16ms	184ms
3, 4	Open	5.4%	12ms	210ms

Automatic Maintain Power Signature (AMPS) control can be assigned by AMPS pin with a resistor and appropriate power rating to support the MPS current.

Table 8. Maintain Power Signature Current Amplitude Selection Details

Conditions	AMPS Pin Resistance Value	MPS current Amplitude
1	237kΩ	10mA
2	150kΩ	16mA
3	118kΩ	20mA

Auto-Class

Auto-Class is a classification mechanism that allows a PD to communicate its effective maximum power consumption to the PSE. This happens in such a way that the PSE will be able to set the power budget to the effective maximum PD power. This new feature was introduced in the IEEE802.3bt standard to allow a more efficient use of the available power since only the effectively used power needs to be budgeted. A Type 3 or Type 4 PD may optionally support Auto-Class whereas a Type 3 or Type 4 PSE may make use of it to optimize its power management.

A PSE implementing Auto-Class uses the first-class event to inquire if the PD supports Auto-Class, looking for the class current to fall to class 0 current level. If it is the case, the PSE can then proceed to Auto-Class measurement immediately after power up, the PD being required to draw its highest power throughout the bounded period using sliding time window to calculate the power.

Pull KTA1142 AUT pin to AGND to enable the Auto-Class function during classification. Leave the pin open otherwise.

DC-DC Controller Details

The KTA1142 has a peak current mode active clamp PWM controller that integrates all the circuitry required to design a smart and efficient converter for PoE and telecom mid-power DCDC converter applications. KTA1142 features a programmable oscillator for the switching frequency, adjustable slope compensation, dual low-side drivers with programmable dead time, programmable soft-start, programmable frequency dithering, maximum duty limit, and a self-start internal high-voltage linear regulator.

The controller is mainly used for active clamp forward/flyback converter applications for small and mid-power devices.

The controller provides two control outputs, the main power switch control (G1) and the active clamp switch control (G2). The main output driver, G1, is designed for driving a forward/flyback converter primary MOSFET. The secondary output, G2, is designed for driving an active clamp circuit MOSFET, or a synchronous rectifier on the secondary side.

G1 / G2

The KTA1142 has two integrated MOSFET drivers with up to 1.5A peak source and sink current capability. G1 is intended for driving the main switching MOSFET, while G2 is used for an auxiliary function, depending on the topology selected. For typical application, G2 will control a P-channel auxiliary MOSFET referred to PGND in active clamp forward topologies. The dead time is controlled by the resistor value from DT pin connected to AGND pin of the controller. The rising edge dead time and the falling edge dead time are identical. DT can be adjusted to fine tune the relative switching times of the MOSFETs and to maximize the converter efficiency.

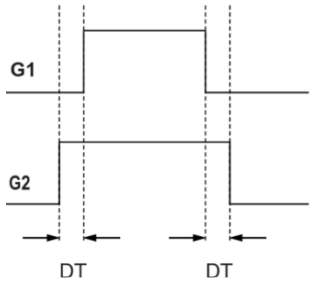


Figure 5. Time Relation between Output Drivers and DT

DT

The relative phase of the main switch gate driver G1 and active clamp gate driver G2 can be configured for multiple applications. For default, the active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase, with the active clamp output overlapping the main output. The dead time is controlled by the resistor value from DT pin connected to AGND pin of the controller. The rising edge dead time and the falling edge dead time are identical. The magnitude of the dead time can refer to the curve of Dead Time vs. Programming Resistance in the typical Characteristics section of this data sheet. The suggested DT resistance range is from 10K to approximately 200K. Please refer to Equation 2 below for the roughly programmed dead time vs resistor.

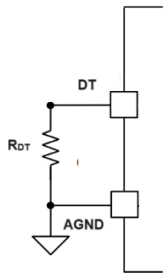


Figure 6. Dead time configuration

$$T_{DT}(\text{ns}) = 2.4 * R_{DT}(\text{K}\Omega) \qquad \text{Equation 2}$$

If DT pin is floating, the default dead time is around 60ns. The DT resistor should not be too far away from the chip.

FREQ

The oscillator frequency is set by the external resistance connected between the FREQ and AGND pins. When the DITHER/SYNC pin is connected to AGND pin with a 10nF capacitor or connected to a 3.3V or 5V high logic voltage, the frequency dithering function will be disabled, the controller will run the frequency right at the settled oscillator frequency by FREQ pin. Please refer to Equation 3 below for the roughly programmed frequency and resistor:

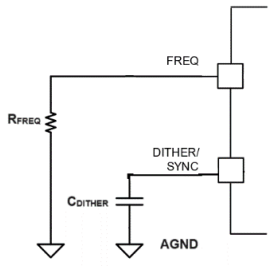


Figure 7. Frequency configuration

$$R_{freq} = \frac{1}{F_{freq}*4.2*10\hat{}-11} \qquad \text{Equation 3}$$

For the programmed frequency details, please refer to the Switching Frequency vs. Programming Resistance curve in the typical Characteristics section.

Soft Start /Soft Stop

The soft-start time is programmed by the capacitor (C_{SS}) from SS pin to AGND. During startup, this capacitor is charged by a constant 10μA (I_{SS})current, and its voltage rises accordingly. This slowly rising voltage in the SS pin (V_{SS}) will limit the COMP voltage during startup. The COMP voltage is clamped around 0.8V higher than SS pin voltage during startup ($V_{COMP} = V_{SS} + 0.8$). This slowly rising and clamped voltage on the COMP will achieve soft start for DC-DC converter applications during startup. Soft start begins when V_{SS} is around 0.1V. The soft start finishes when the clamped COMP voltage reaches a stable working voltage that is settled by the DC-DC converter.

Please refer to Equation 4 for the programmed capacitor (C_{SS}) and the soft startup time (T_{START}).

V_{SS} is the SS pin voltage that the soft start finished. For a typical application with 100nF C_{SS}, the soft startup time is around 10mS.

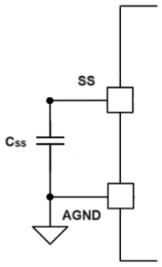


Figure 8. Soft start and soft stop configuration

$$C_{SS} = \frac{I_{SS} * T_{START}}{V_{SS}} \qquad \text{Equation 4}$$

To prevent oscillations in the self-driven synchronous rectifiers on the secondary side of the converter during turnoff, the KTA1142 has a soft stop feature. When a fault OCP, OTP, or turn off event occurs, the SS voltage falls slowly from 5V by a constant 10µA discharge current. When SS voltage drops to a certain voltage, it will start to clamp the COMP voltage (V_{COMP} = V_{SS} +0.8V). The COMP pin voltage is clamped around 0.8V higher than SS pin voltage during turn off which lets the COMP voltage slowly drop and the DC-DC converter can then achieve soft stop. The soft stop finishes when SS pin voltage (V_{SS}) drops to approximately 0.2V. Then the controller will fully turn off. The soft stop time is similar to the soft startup time if ignoring this 0.2V.

DITHER / SYNC

The KTA1142 has a Frequency Dithering Programming and Synchronization function. When DITHER/SYNC pin is configured to the Frequency Dithering Programming function, the switching frequency of the converter can be dithered by connecting a capacitor from DITHER/SYNC pin to AGND, and a resistor from DITHER/SYNC pin to FREQ pin. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor C_{DITHER} to 2V with 50µA (I_{DITHER}). Upon reaching this trip point, it discharges C_{DITHER} to 0.4V with 50µA. The charging and discharging of the capacitor generate a triangular waveform on DITHER/SYNC with bottom and peak levels at 0.4V and 2V. The triangular waveform frequency (modulation frequency) can be programmed by the capacitor from DITHER/SYNC pin to GND.

The resistor (R_{DITHER}) connected from DITHER/SYNC to FREQ determines the amount of dither frequency from FREQ pin settling the oscillator frequency. The approximate dither frequency range can be calculated using Equation 5 below. Please refer Equation 6 for the triangular waveform frequency (modulation frequency).
If setting R_{DITHER} to 5 times R_{FREQ}, it will generate around ±13.3% dither frequency of settled oscillator frequency. If setting C_{DITHER} to 10nF, it will generate 1.56K modulation frequency.

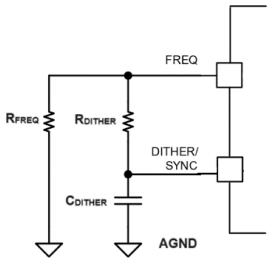


Figure 9. Frequency Dithering configuration

$$Freq_{DITHER\ Range}(+/-\%) = \frac{2}{3} * \frac{R_{FREQ}}{R_{DITHER}} * 100\% \qquad \text{Equation 5}$$

$$Freq_{Modulation} = \frac{1}{2} * \frac{I_{DITHER}}{C_{DITHER} * 1.6} \qquad \text{Equation 6}$$

When DITHER/SYNC is connected to AGND pin directly, there will exist a default Frequency Dithering function. The frequency dithering is fixed at ±7% of FREQ pin settled oscillator frequency. The default modulation frequency is 1/64 of FREQ pin settled oscillator frequency.

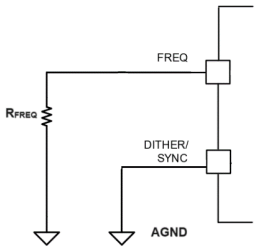


Figure 10. Frequency Dithering default configuration

When DITHER/SYNC is connected to AGND pin with a 10nF capacitor or connected to a 3.3V or 5V high logic voltage, the frequency dithering function will be disabled.

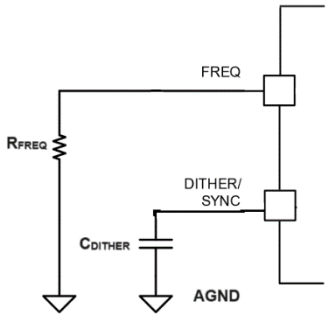


Figure 11. Frequency Dithering disable configuration

When DITHER/SYNC pin is configured to the Synchronization function this pin provides an input for an external-clock signal which synchronizes the internal oscillator of the controller. This pin should connect to external clock signal directly without any other components.

The external synchronizing frequency is suggested to be in the 110% to 130% range of the free-running frequency set by the FREQ pin resistor. The acceptable minimum pulse-width of the synchronization signal is approximately 400ns (positive logic). The synchronization signal high level should exceed 2.9V.

PWM Comparator and Slope Compensation

In a typical isolated flyback/forward topology application, the error amplifier is located outside the IC and the feedback signal is taken on the collector of an optocoupler, while the current is sensed through a current sense resistor Rcs connected between the source of the primary Main Switching MOSFET and the PGND.

The sensed voltage on the CS pin is then amplified and fed to the PWM comparator for current mode control. The current comparator takes this amplified current sensed voltage (plus slope compensation) as one of its inputs, then compares this value with the voltage of VCOMP-0.8V.

The COMP is internally pulled up to a fixed reference of 5V using an internal 3.3KΩ resistor. The PWM comparator start to output gate driver signals when the voltage at the COMP pin rise to approximately 1.0V. The comparator stop to output gate driver signals when the COMP pin voltage drops below 1.0V. For duty cycles greater than 50%, current mode control loops are subject to sub-harmonic oscillation. The controller fixes the maximum duty cycle at around 80% and implements a slope compensation technique consisting in adding a fixed slope voltage ramp to the signal sensed at the CS pin. This slope compensation is achieved by adding an external resistor from RCM pin to AGND (Refer to Figure 12).

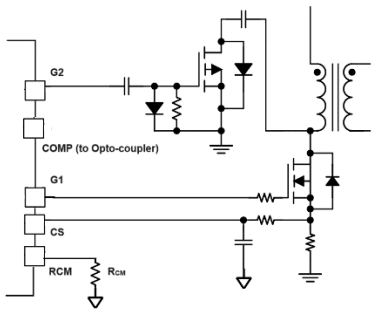


Figure 12. Slope Compensation configuration

CS

The CS pin input provides a control ramp for the pulse width modulator and current limit detection for overload protection.

The DC-DC controller of KTA1142 is a peak current mode active clamp controller. The current through the external Main MOSFET can be sensed through a current-sense resistor that is connected in series with the MOSFET's source. The sensed voltage on the CS pin is then amplified and fed to the PWM comparator for current mode control. The current comparator takes this amplified current sensed voltage (plus slope compensation) as one of its inputs, then compares this value with the VCOMP-0.8V. When the voltage exceeds VCOMP-0.8V, the comparator outputs low, and the power MOSFET turns off.

If the sensed voltage at CS exceeds 0.3V and stays around 32 cycles, the over-current protection will trigger and enter soft stop. A small RC filter, located near the controller, is recommended for the CS input pin. The blanking time is around 65ns at the start of each main switch cycle to attenuate the leading-edge spike in the current sense signal. After soft stop, the controller will restart after the hiccup time. The hiccup time is around (34,000) times of the oscillator switching cycle settled by the FREQ pin resistor.

VDD10

There is an internal high voltage start-up regulator in the KTA1142. The VDD10 voltage is regulated to approximately 10V. The VDD10 regulator provides power to internal gate drivers. The typical recommended capacitance for the VDD regulator is 1µF.

In order to save power loss in the internal start-up regulator and prevent the controller to be too hot, an external regulated voltage supply is suggested to be applied to the VDD pin. This external voltage regulator is usually from the auxiliary transformer winding. The external regulated voltage at the VDD pin is suggested to be greater than 11.5V to shut off the internal start-up regulator and not exceed 15V to prevent going over the maximum rating of the VDD10 pin.

Startup Sequences

When EN/UVLO pin is not used, the internal PoE UVLO (Undervoltage Lock Out) circuit holds the Hot-Swap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification.

The PSE drives the primary voltage to the operating range once it has decided to power up the PD. When Vin rises above the UVLO turn-on threshold (approximately 38V), KTA1142 enables the Hot-Swap MOSFET with inrush current limit.

During inrush period, the DC/DC Controller is also turned off, providing no low supply voltage to the PWM controller, to avoid additional loading that could prevent successful PD and subsequent converter start up. After inrush finished (typical around 10ms, depends on inrush current and VOD capacitor value), the VOD voltage is charged to VIN, and with some delay time, then the DC/DC Controller start to work and downstream DC-DC converter start loading from VOD. This always happens around 100ms later from the inrush start point. The PD OCP is also valid at this moment.

PCB Layout Guidelines

Thermal De-Rating and Board Layout Considerations

The KTA1142 is capable of operating to an industrial temperature range of 85°C in ambient air and up to 125°C junction temperature, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In higher power applications, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

Besides the layout for thermal consideration, the following layout guidelines are recommended for optimum system performance.

1. Keep below DCDC converter power stage loops area as small as possible for minimal noise and ringing.
    a. Input power loop: Input capacitors (VOD net), Primary of Transformer, Main MOSFET, Current sense resistor.
    b. Output power loop: Secondary of Transformer, Output capacitors, Rectifier Diodes or MOSFETs.
    c. Active-clamp loop: Input capacitors (VOD net), Primary of Transformer, active-clamp MOSFET and Capacitor.
2. The KTA1142 has an analog/signal ground, AGND, and a power ground, PGND. AGND is used for analog/signal connections such as FREQ, DT and other signal pins. PGND is used for high power

connections such as the output drivers, G1 and G2 pins. All the analog/signal ground tracks should be connected in common near the IC AGND, and then a single connection made from the KTA1142 signal ground to the DCDC converter power ground (sense resistor ground point).

3. The DCDC converter current-sense circuit usually employs a sense resistor. The sense resistor is connected between the Source of Main MOSFET and the power ground terminal. A low inductance resistor should be used. The negative terminal of the DCDC input power capacitor, the ground return of the MOSFET, and current-sensing resistor should be close together. The filter network for the current-sense circuit should be located close to the IC.
4. The gate drive outputs of the KTA1142 should have short direct paths to the MOSFETs to minimize inductance in the PCB traces, wider trace is suggested for these gate drive loops.
5. Place all the components (VDD5 and VDD10 pin capacitor, DT pin resistor, etc.) to their respective grounds and place these components close to the IC to decouple noise. These components and traces should keep far away from the noise nodes (such as primary Main MOSFET switching node).

Applications Circuits

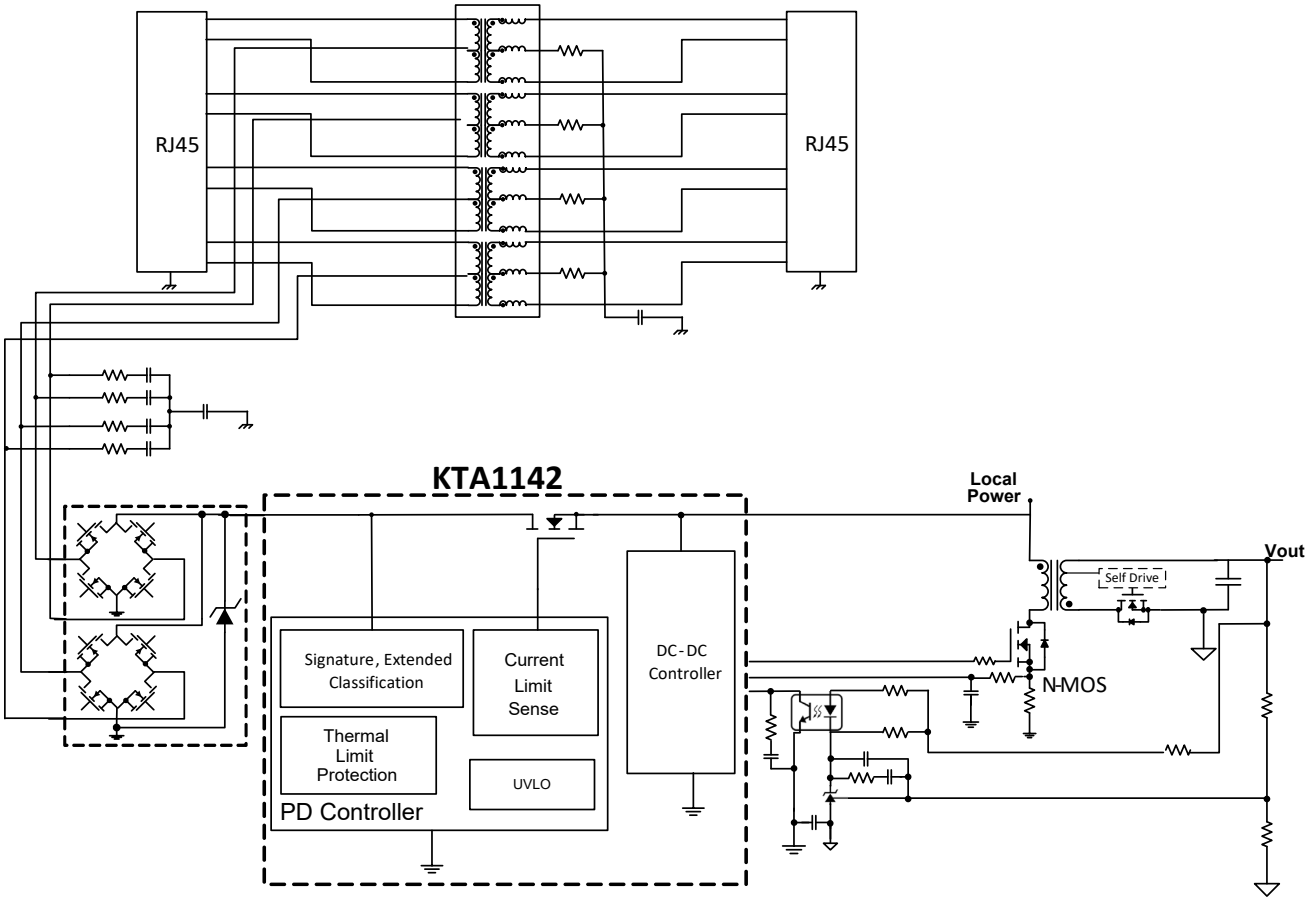


Figure 13. KTA1142 High-Efficiency Flyback DC-DC Solution with Self Drive Synchronization

Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information.

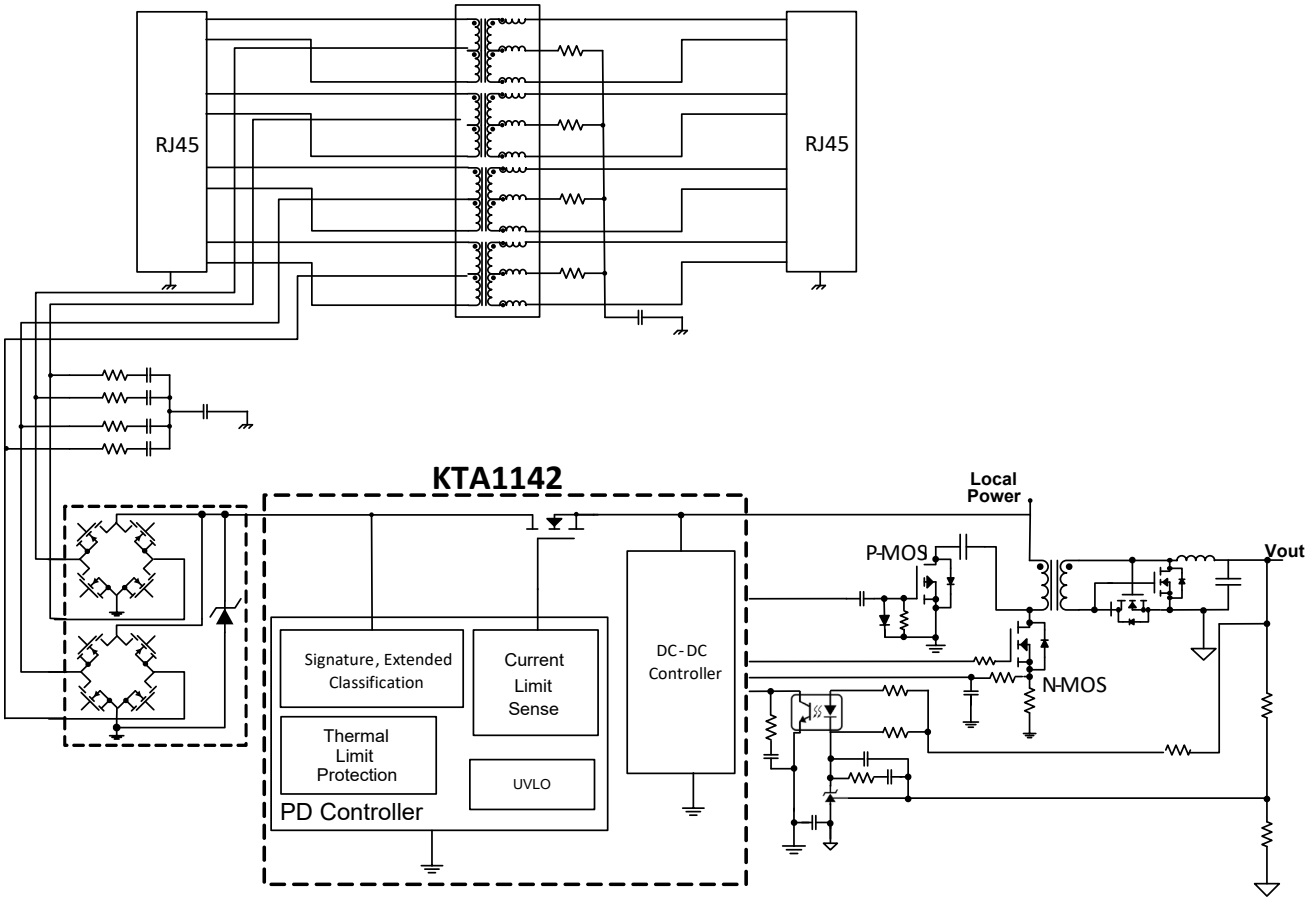
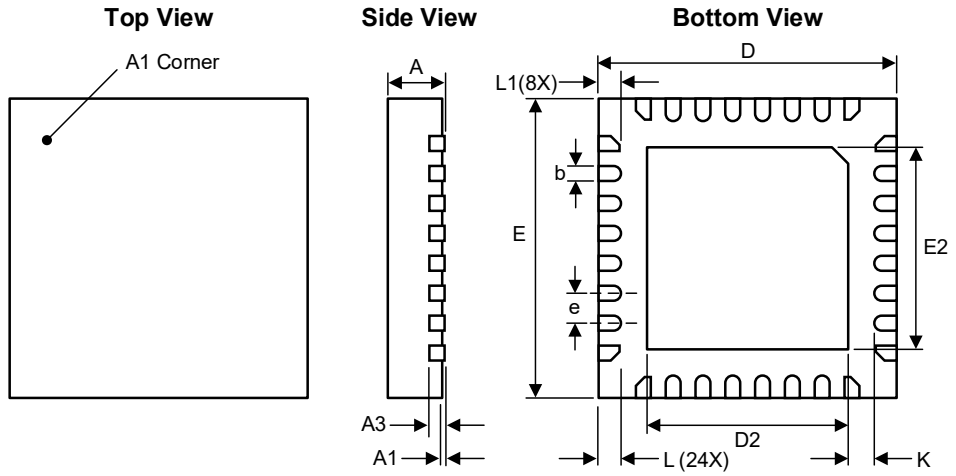


Figure 14. KTA1142 High-Efficiency Active Clamp Forward Solution for Higher Current Applications

Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information.

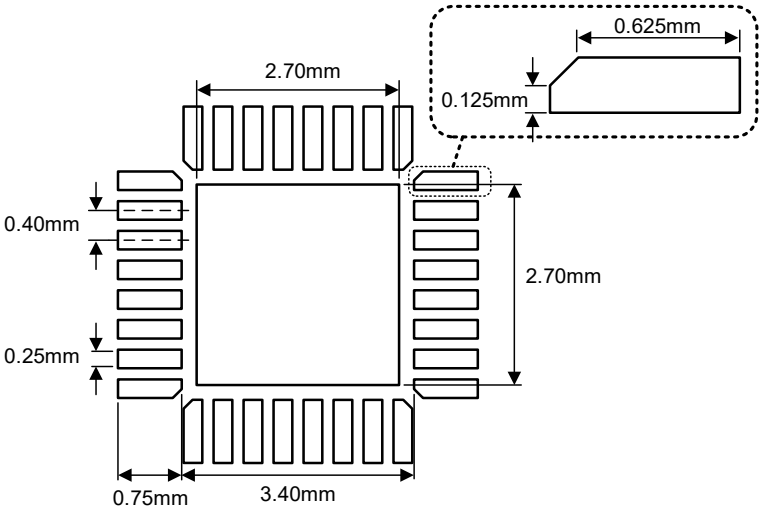
Packaging Information

WQFN44-32 (4.00mm x 4.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	0.40 BSC		
K	0.20	–	–
L	0.25	0.30	0.35
L1	0.33	0.28	0.33

Recommended Footprint



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