



PESD2CANFD36LQC-Q

Extremely low clamping bidirectional ESD protection diode

5 January 2024

Product data sheet

1. General description

ESD protection device in an ultra-small DFN1412D-3 (SOT8009) leadless Surface-Mounted Device (SMD) plastic package with side wettable flanks, designed to protect two automotive in-vehicle network bus lines from the damage caused by Electro-Static Discharge (ESD) and other transients.

2. Features and benefits

- Reverse stand-off voltage: $V_{RWM} = 36$ V
- Low clamping voltage: typical $V_{CL} = 42$ V at $I_{pp} = 1$ A
- ESD protection up to 20 kV (IEC 61000-4-2)
- ESD protection up to 20 kV (ISO 10605; $C = 330$ pF, $R = 330$ Ω)
- Low capacitance: $C_d = 10$ pF
- ISO 7637-2 pulse 3a/3b = ± 300 V
- ISO 7637-2 pulse 2a = 65 V
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

ESD protection for in-vehicle network lines in automotive environments

- 24 V board net / truck systems
- CAN / CAN-FD
- FlexRay
- SENT

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|--------------------------|--|---------|-----|-----|-----|------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25$ °C | | - | - | 36 | V |
| I_{PPM} | rated peak pulse current | $t_p = 8/20$ μ s | [1] [2] | - | - | 2.9 | A |
| V_{CL} | clamping voltage | $I_{PP} = 16$ A; $t_p = 100$ ns; $T_{amb} = 25$ °C | [3] [2] | - | 52 | - | V |

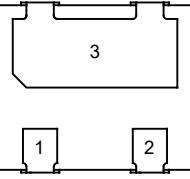
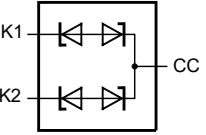
[1] According to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|---|--|
| 1 | K1 | cathode (diode 1) |  Transparent top view |  006aaa155 |
| 2 | K2 | cathode (diode 2) | | |
| 3 | CC | common cathode | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------------|------------|--|---------|
| | Name | Description | Version |
| PESD2CANFD36LQC-Q | DFN1412D-3 | plastic, leadless ultra small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body | SOT8009 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------------|--------------|
| PESD2CANFD36LQC-Q | Q2 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|---|---------|-----|-----|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | [1] [2] | - | 2.9 | A |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -55 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [2] [3] | - | 20 | kV |
| | | ISO 10605; contact discharge; $C = 330 \text{ pF}$, $R = 330 \Omega$ | [2] [3] | - | 20 | kV |
| | | ISO 10605; contact discharge; $C = 150 \text{ pF}$, $R = 330 \Omega$ | [2] [3] | - | 20 | kV |

[1] According to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

[3] Device stressed with ten non-repetitive ESD pulses.

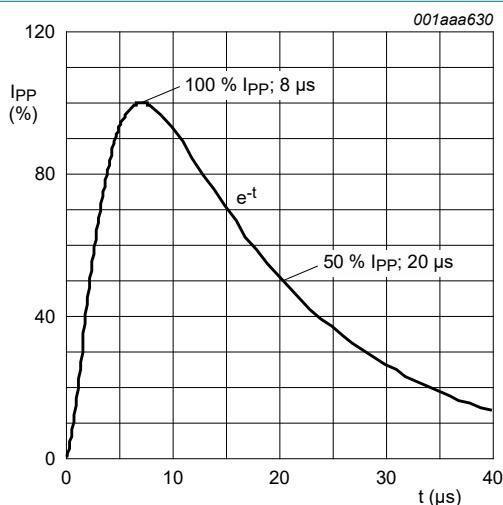


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

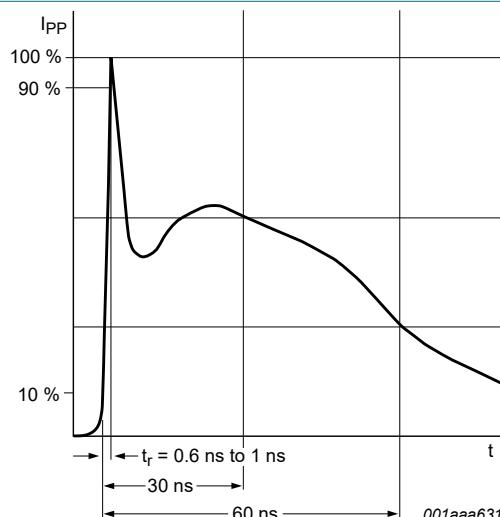


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

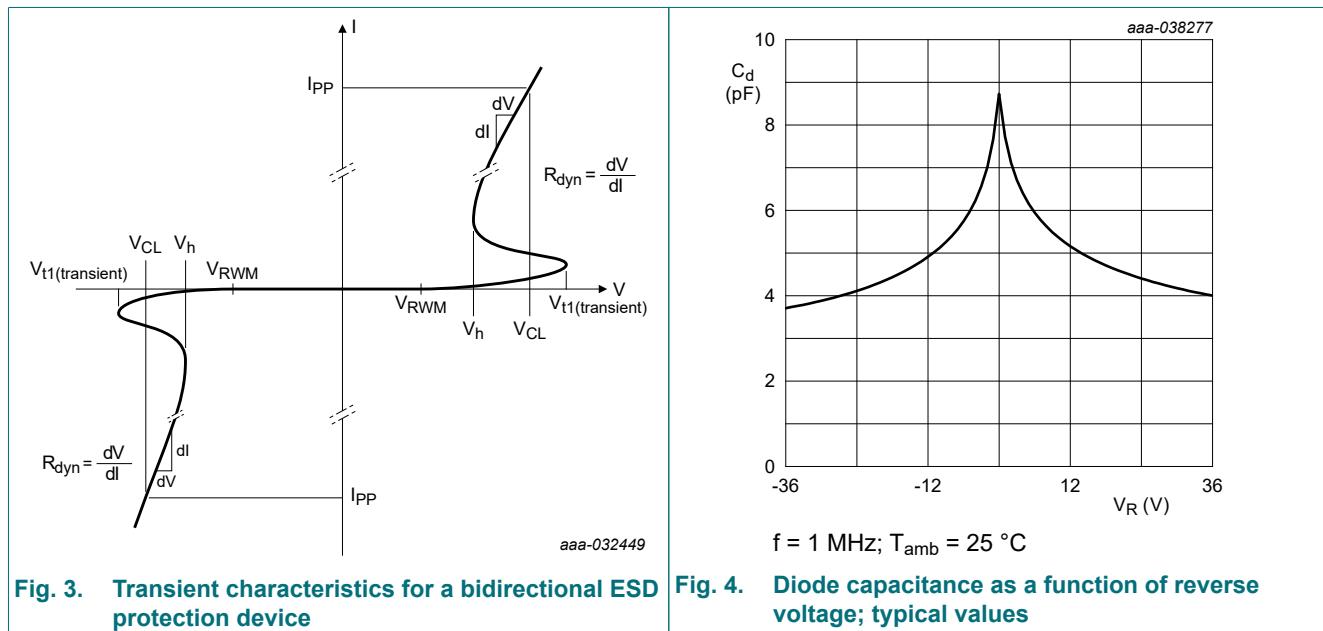
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|----------------------------|--|---------|-----|-----|-----|----------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25^\circ C$ | | - | - | 36 | V |
| V_{BR} | breakdown voltage | $I_R = 10 \text{ mA}; T_{amb} = 25^\circ C$ | [1] | 37 | 41 | 47 | V |
| I_{RM} | reverse leakage current | $V_{RWM} = 36 \text{ V}; T_{amb} = 25^\circ C$ | [1] | - | 1 | 50 | nA |
| C_d | diode capacitance | $f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25^\circ C$ | [1] | - | 8.7 | 10 | pF |
| | diode capacitance matching | $f = 1 \text{ MHz}; V_R = 2.5 \text{ V}; T_{amb} = 25^\circ C$ | [2] | - | 0.5 | - | % |
| V_{CL} | clamping voltage | $I_{PP} = 1 \text{ A}; t_p = 8/20 \mu\text{s}; T_{amb} = 25^\circ C$ | [3] [1] | - | 42 | - | V |
| | | $I_{PP} = 16 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25^\circ C$ | [4] [1] | - | 52 | - | V |
| R_{dyn} | dynamic resistance | $I_R = 10 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25^\circ C$ | [4] [1] | - | 1.1 | - | Ω |

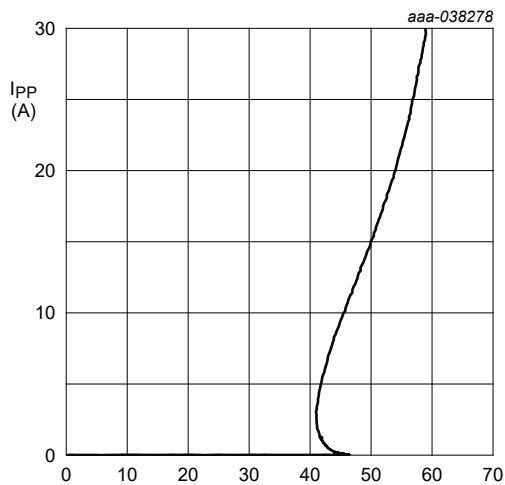
[1] Measured from pin 1 or 2 to pin 3.

[2] ΔC_d is the difference of the capacitance measured between pin 1 and pin 3 and the capacitance measured between pin 2 and pin 3.

[3] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

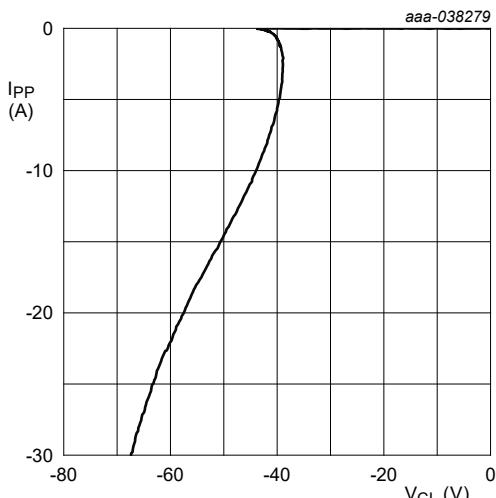
[4] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008





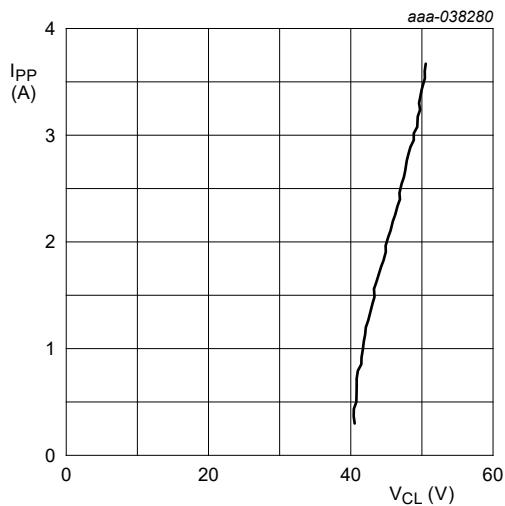
Transmission Line Pulse (TLP);
 $t_p = 100$ ns; $t_r = 1$ ns

Fig. 5. Positive clamping voltage (TLP); typical values



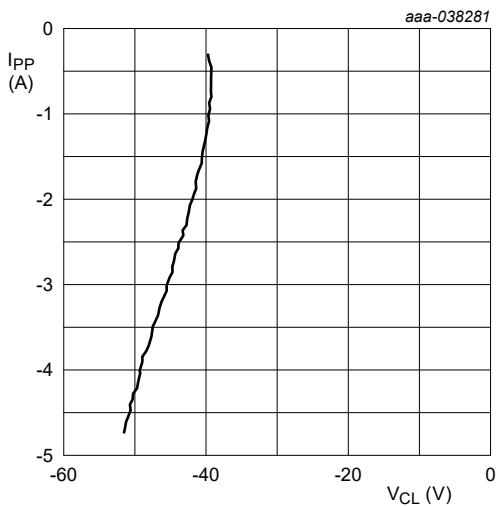
Transmission Line Pulse (TLP);
 $t_p = 100$ ns; $t_r = 1$ ns

Fig. 6. Negative clamping voltage (TLP); typical values



IEC 61000-4-5; $t_p = 8/20$ μ s; positive pulse

Fig. 7. Positive clamping voltage; typical values



IEC 61000-4-5; $t_p = 8/20$ μ s; negative pulse

Fig. 8. Negative clamping voltage; typical values

10. Application information

The device is designed for the protection of two automotive in-vehicle bus lines, e.g. CAN (FD), from the damage caused by ESD and surge pulses.

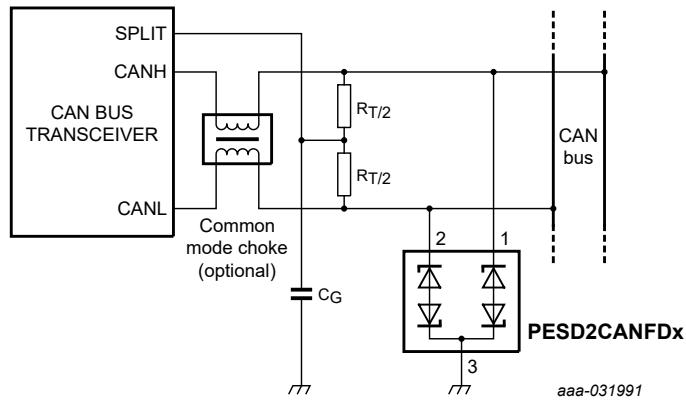


Fig. 9. Typical application: ESD protection of two automotive CAN bus lines

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

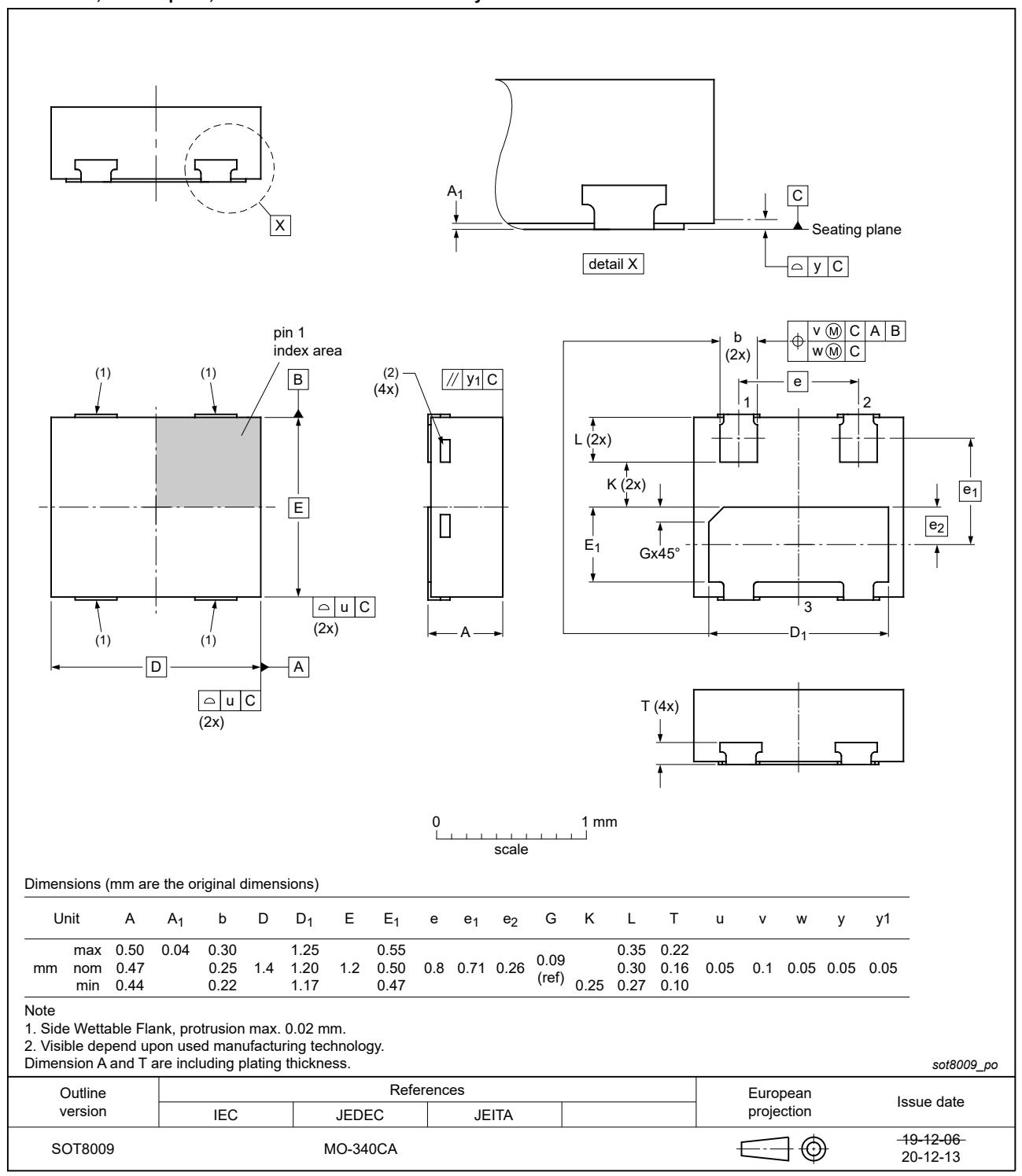
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1412D-3: plastic, leadless ultra small outline package with side-wettable flanks (SWF);
3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body

SOT8009



13. Soldering

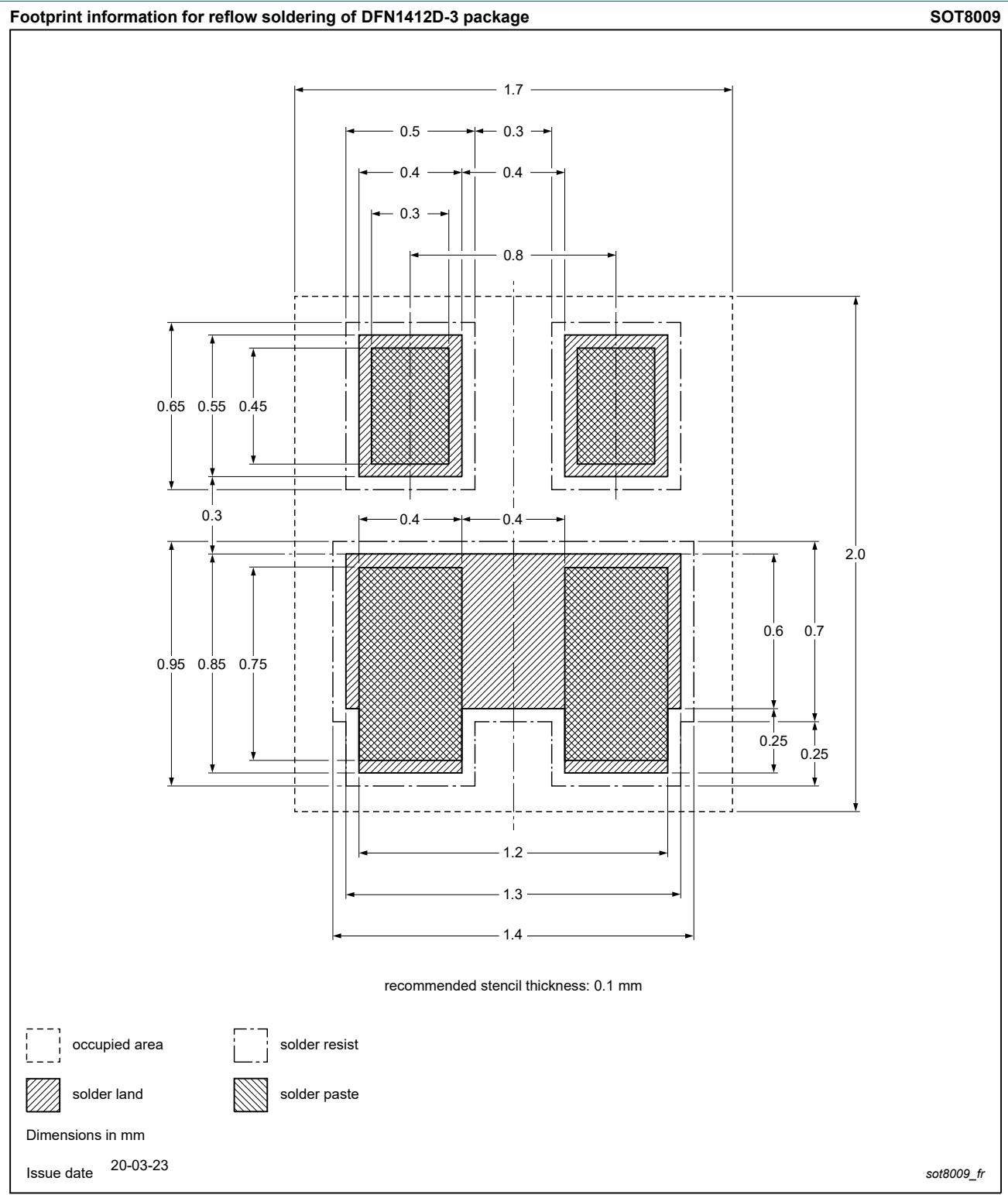


Fig. 11. Reflow soldering footprint for DFN1412D-3 (SOT8009)

14. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|--------------|--------------------|---------------|------------|
| PESD2CANFD36LQC-Q v.1 | 20240105 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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