



# PESD18VF1BALS-Q

Ultra-low capacitance bidirectional ESD protection diode

18 January 2024

Product data sheet

## 1. General description

Ultra-low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006BD-2 (SOD882BD) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect one signal line from the damage caused by ESD and other transients.

## 2. Features and benefits

- Ultra low diode capacitance  $C_d = 0.38$  pF
- High reverse standoff voltage  $V_{RWM} = 18$  V
- Very small voltage dependency of the capacitance
- ESD protection up to  $\pm 15$  kV according to IEC 61000-4-2, level 4
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- NFC and antenna protection
- Protection of high-speed data lines

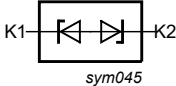
## 4. Quick reference data

Table 1. Quick reference data

| Symbol    | Parameter                | Conditions                                  | Min | Typ  | Max  | Unit |
|-----------|--------------------------|---------------------------------------------|-----|------|------|------|
| $V_{RWM}$ | reverse standoff voltage | $T_{amb} = 25$ °C                           | -   | -    | 18   | V    |
| $C_d$     | diode capacitance        | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | -   | 0.38 | 0.47 | pF   |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description       | Simplified outline                                                                                                                            | Graphic symbol                                                                                       |
|-----|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 1   | K1     | cathode (diode 1) | <br>Transparent<br>top view<br><b>DFN1006BD-2 (SOD882BD)</b> | <br><i>sym045</i> |
| 2   | K2     | cathode (diode 2) |                                                                                                                                               |                                                                                                      |

6. Ordering information

Table 3. Ordering information

| Type number     | Package     |                                                                                                                                |          |
|-----------------|-------------|--------------------------------------------------------------------------------------------------------------------------------|----------|
|                 | Name        | Description                                                                                                                    | Version  |
| PESD18VF1BALS-Q | DFN1006BD-2 | Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body | SOD882BD |

7. Marking

Table 4. Marking codes

| Type number     | Marking code |
|-----------------|--------------|
| PESD18VF1BALS-Q | N#N          |

8. Limiting values

Table 5. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol              | Parameter                       | Conditions                       |     | Min | Max | Unit |
|---------------------|---------------------------------|----------------------------------|-----|-----|-----|------|
| T <sub>j</sub>      | junction temperature            |                                  |     | -   | 150 | °C   |
| T <sub>amb</sub>    | ambient temperature             |                                  |     | -55 | 150 | °C   |
| T <sub>stg</sub>    | storage temperature             |                                  |     | -65 | 150 | °C   |
| ESD maximum ratings |                                 |                                  |     |     |     |      |
| V <sub>ESD</sub>    | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [1] | -   | 15  | kV   |
|                     |                                 | IEC 61000-4-2; air discharge     | [1] | -   | 15  | kV   |

[1] Device stressed with ten non-repetitive ESD pulses.

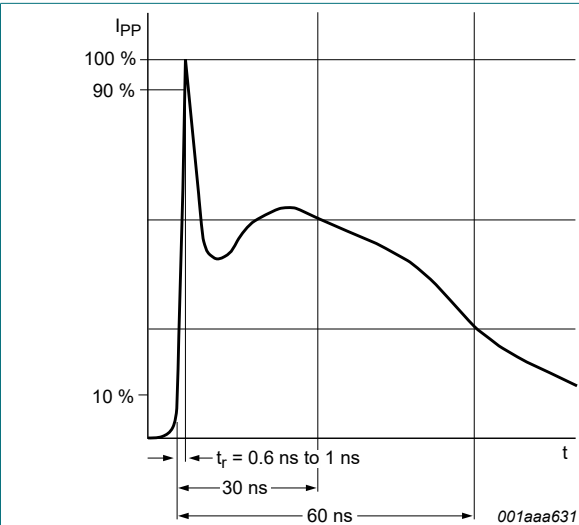


Fig. 1. ESD pulse waveform according to IEC 61000-4-2

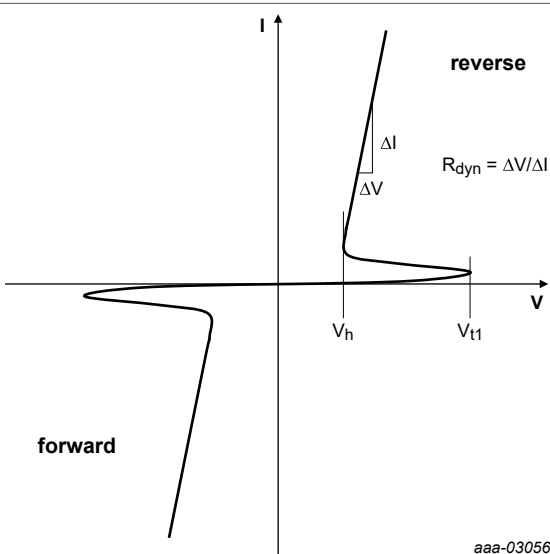


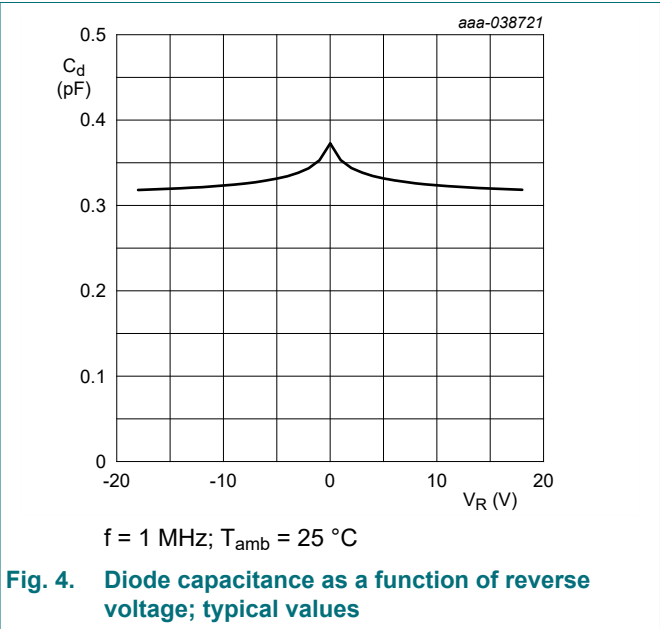
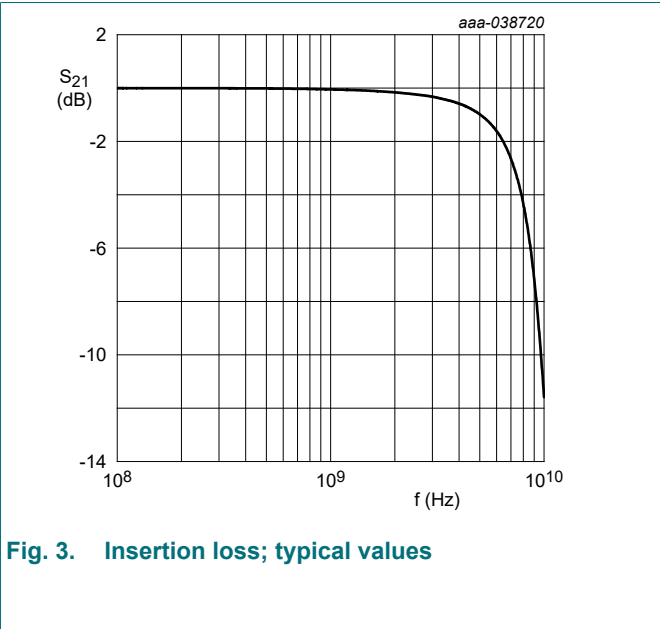
Fig. 2. V-I characteristics for a bidirectional ESD protection diode

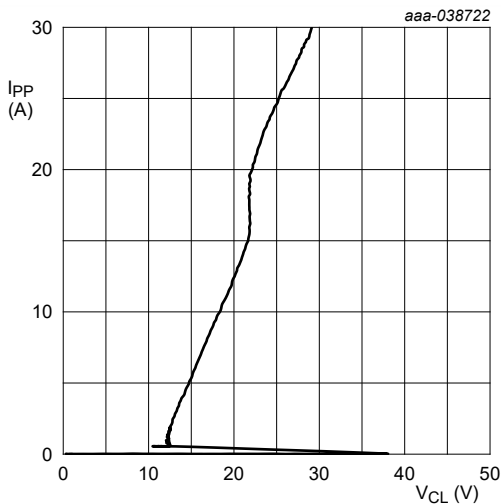
9. Characteristics

Table 6. Characteristics

| Symbol    | Parameter                | Conditions                                                                               |     | Min | Typ  | Max  | Unit     |
|-----------|--------------------------|------------------------------------------------------------------------------------------|-----|-----|------|------|----------|
| $V_{RWM}$ | reverse standoff voltage | $T_{amb} = 25\text{ }^{\circ}\text{C}$                                                   |     | -   | -    | 18   | V        |
| $V_{BR}$  | breakdown voltage        | $I_R = 10\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                            |     | 19  | 24   | -    | V        |
| $I_{RM}$  | reverse leakage current  | $V_R = 18\text{ V}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$                             |     | -   | 1    | 30   | nA       |
| $C_d$     | diode capacitance        | $f = 1\text{ MHz}$ ; $V_R = 0\text{ V}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$         |     | -   | 0.38 | 0.47 | pF       |
| $V_{CL}$  | clamping voltage         | $I_{TLP} = 8\text{ A}$ ; $t_p = 100\text{ ns}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$  | [1] | -   | 16.5 | -    | V        |
|           |                          | $I_{TLP} = 16\text{ A}$ ; $t_p = 100\text{ ns}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | -   | 21   | -    | V        |
| $R_{dyn}$ | dynamic resistance       | $I_R = 10\text{ A}$ ; $t_p = 100\text{ ns}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$     | [1] | -   | 0.7  | -    | $\Omega$ |

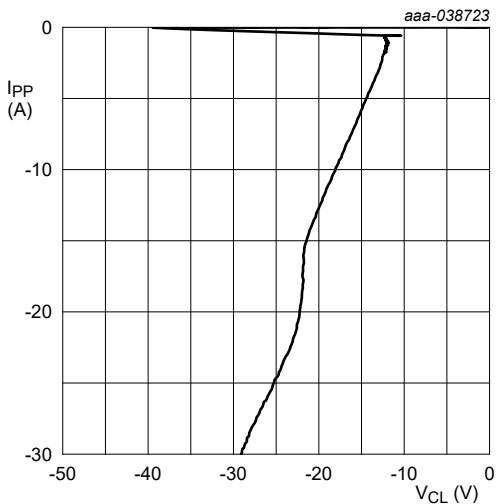
[1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.





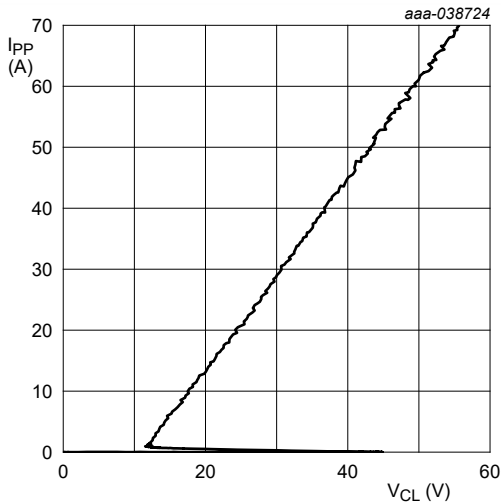
Transmission Line Pulse (TLP);  
 $t_p = 100\text{ ns}$ ;  $t_r = 1\text{ ns}$

Fig. 5. Dynamic resistance with positive clamping; typical values



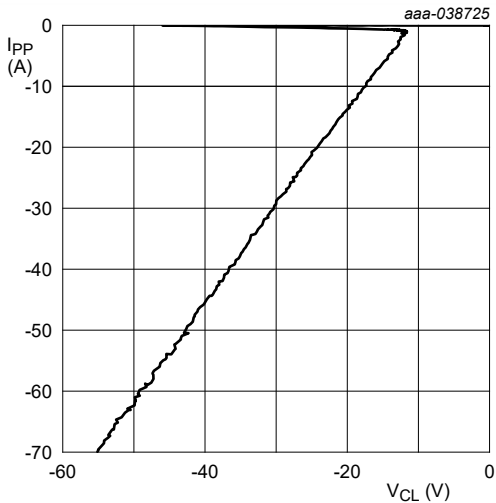
Transmission Line Pulse (TLP);  
 $t_p = 100\text{ ns}$ ;  $t_r = 1\text{ ns}$

Fig. 6. Dynamic resistance with negative clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP);  
 $t_p = 5\text{ ns}$ ;  $t_r = 600\text{ ps}$

Fig. 7. Dynamic resistance with positive clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP);  
 $t_p = 5\text{ ns}$ ;  $t_r = 600\text{ ps}$

Fig. 8. Dynamic resistance with negative clamping; typical values

## 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

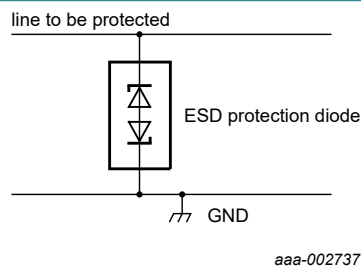


Fig. 9. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

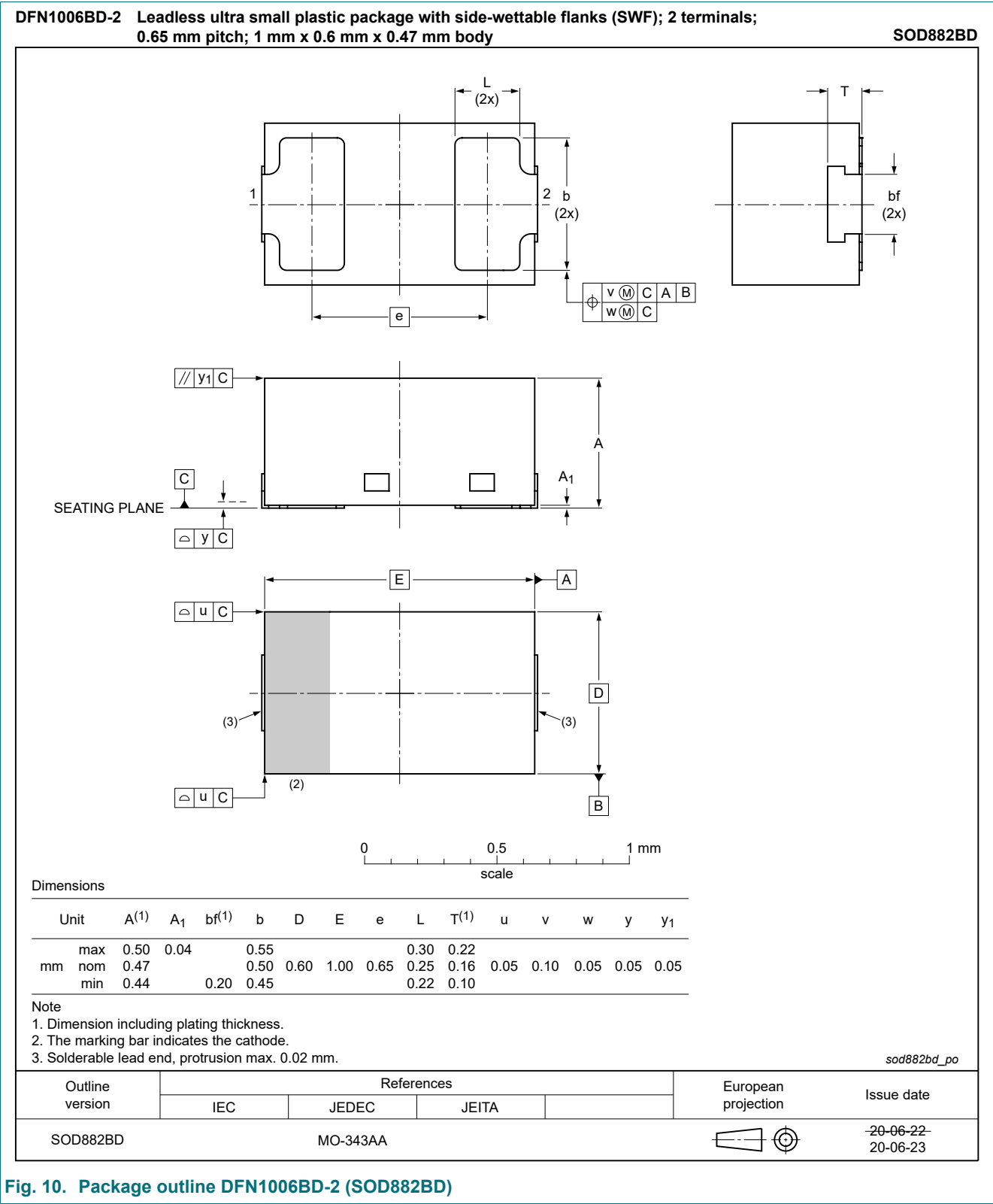
1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

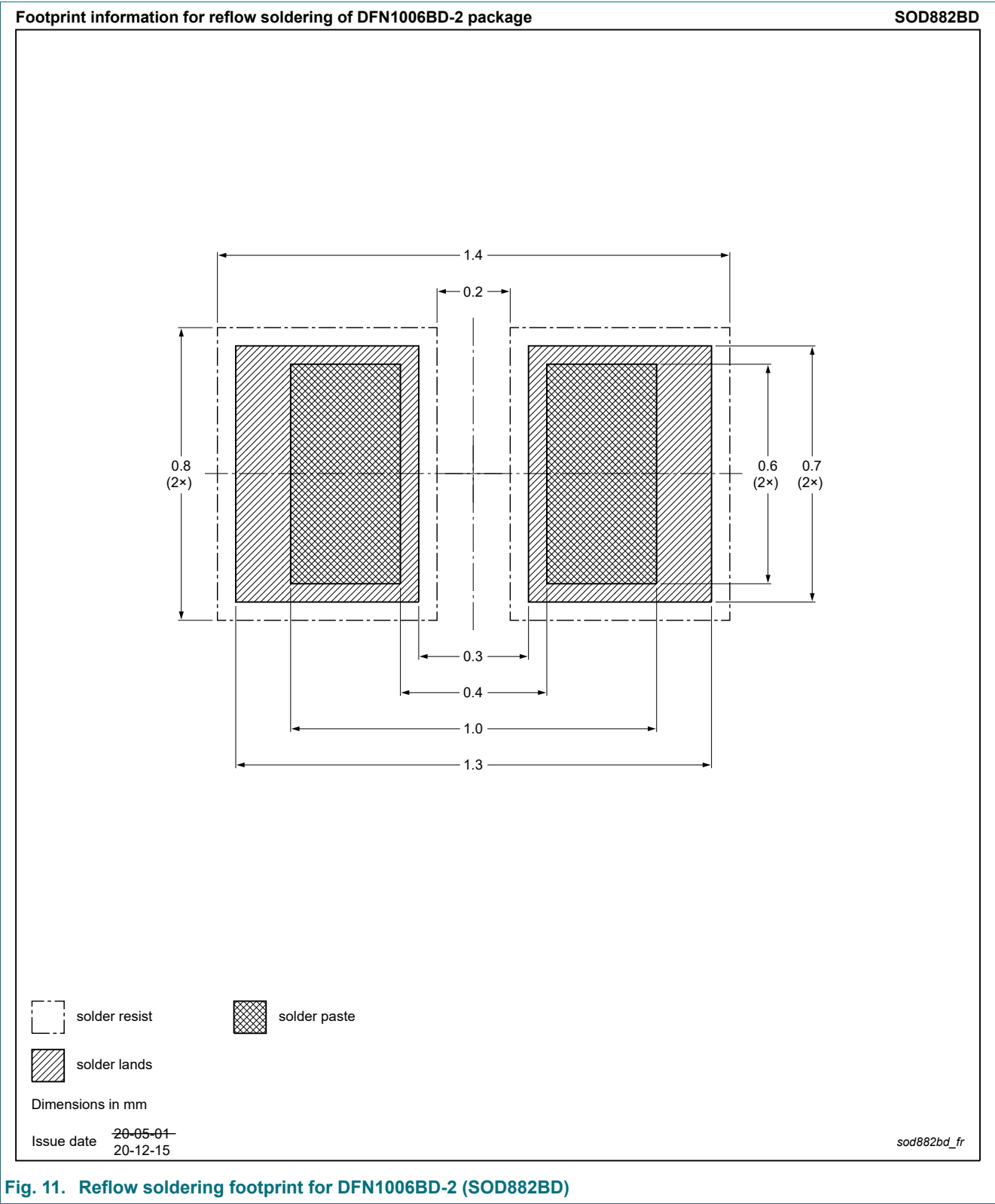
### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering





14. Revision history

Table 7. Revision history

| Data sheet ID          | Release date | Data sheet status  | Change notice | Supersedes |
|------------------------|--------------|--------------------|---------------|------------|
| PESD18VF1BALS-Q<br>v.1 | 20240118     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Characteristics.....4

10. Application information..... 6

11. Test information..... 6

12. Package outline..... 7

13. Soldering..... 8

14. Revision history.....9

15. Legal information.....10

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