

## 1. General description

The NXS0506 is an SD 3.0-compatible bidirectional dual supply level translator with auto-direction control. It is designed to interface between a memory card operating at 1.7 V to 3.6 V signal levels and a host with a nominal supply voltage of 1.1 V to 1.95 V. The device supports SD 3.0: SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has a built-in EMI filter and robust ESD protection (IEC 61000-4-2, level 4).

## 2. Features and benefits

- Supports up to 208 MHz clock rate
- SD 3.0 specification-compatible voltage translation to support: SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.1 V to 1.95 V host side interface voltage support
- Auto-direction sensing
- Low power consumption
- Integrated pull-up resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- 16-bumps WLCSP16 package; pitch 0.35 mm
- 16-terminal XQFN16 package; pitch 0.4 mm
- Latch-up performance exceeds 100 mA per JESD78 Class II.A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
  - IEC61000-4-2, level 4, contact discharge on all memory card-side pins exceeds 8000 V
  - IEC61000-4-2, level 4, air discharge on all memory card-side pins exceeds 15000 V
- Specified from -40 °C to +85 °C

## 3. Applications

- Smartphone
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

## 4. Ordering information

Table 1. Ordering information

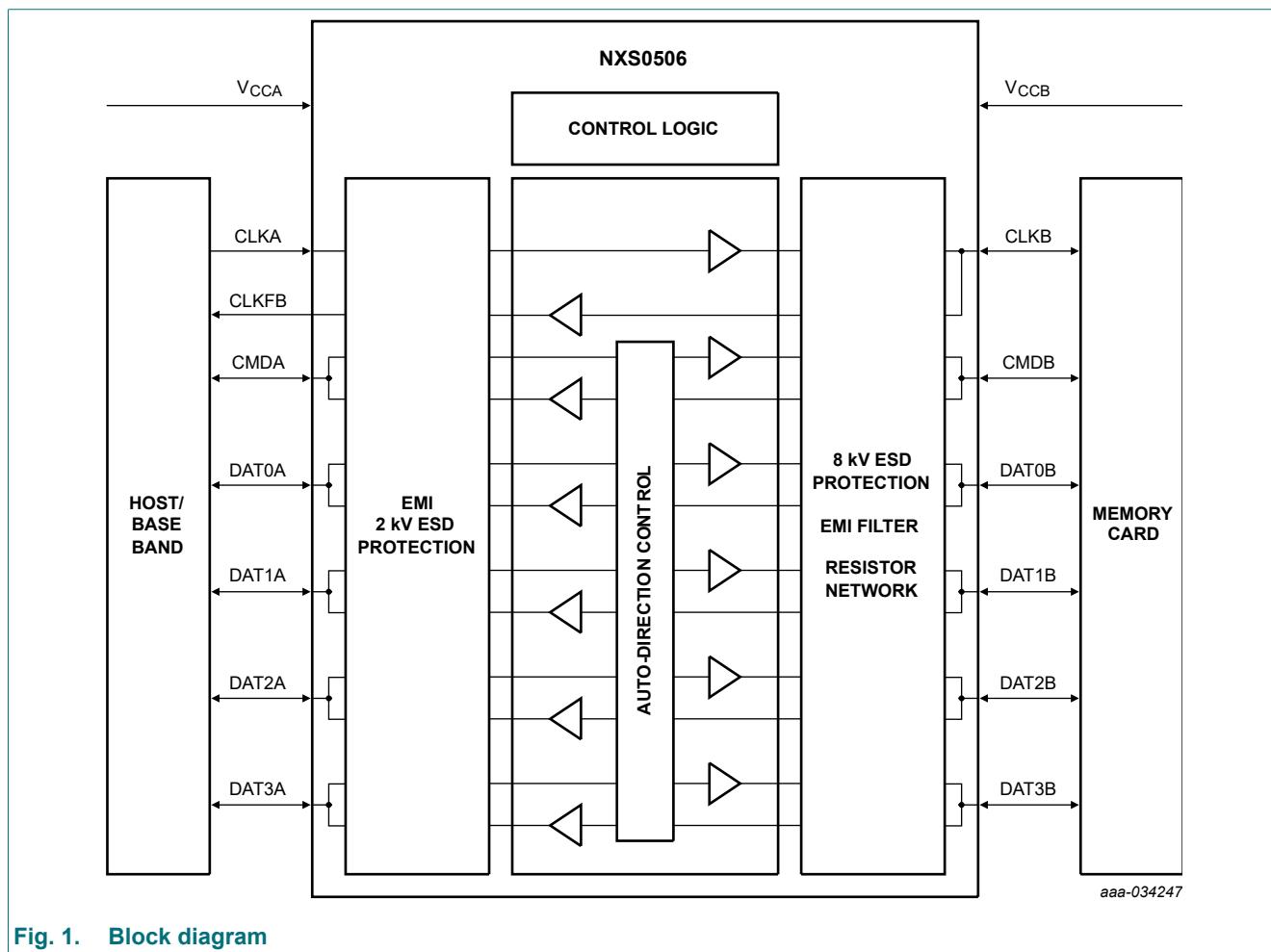
Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">NXS0506UP</a>	-40 °C to +85 °C	WLCSP16	wafer level chip-scale package; 16 bumps; 1.455 × 1.455 × 0.43 mm body	<a href="#">SOT8025-1</a>
<a href="#">NXS0506GU</a>	-40 °C to +85 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	<a href="#">SOT1161-1</a>

## 5. Marking

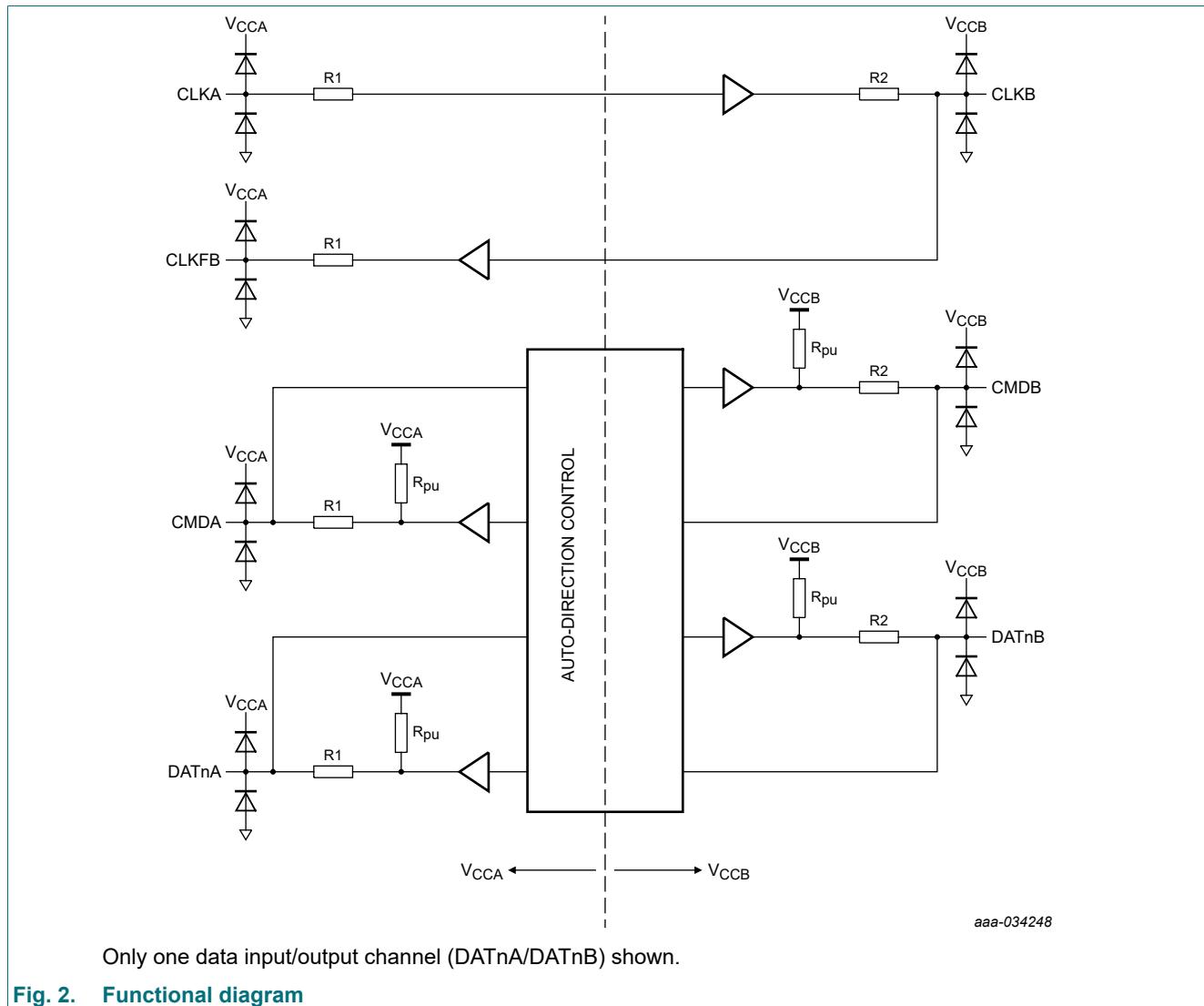
Table 2. Marking codes

Type number	Marking code
NXS0506UP	m5
NXS0506GU	m5

## 6. Block diagram



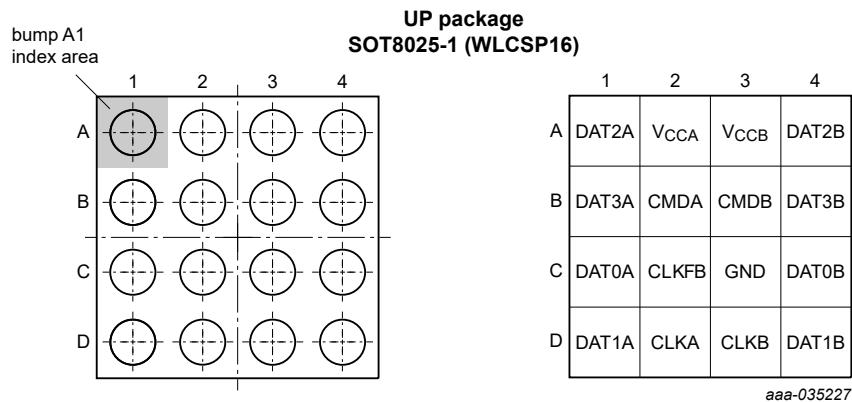
## 7. Functional diagram



**Fig. 2. Functional diagram**

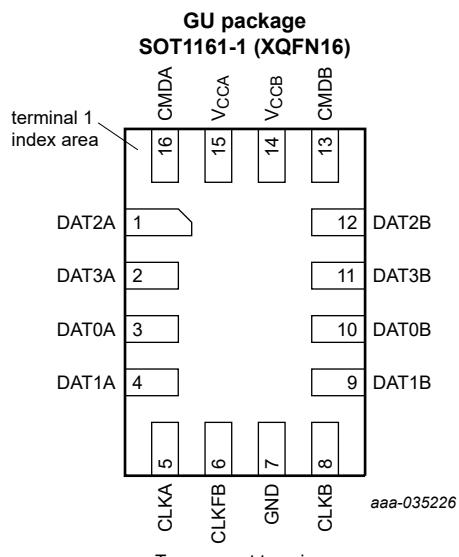
## 8. Pinning information

### 8.1. Pinning



Transparent top view

Bump CLKFB (C2) can be left floating.



## 8.2. Pin description

**Table 3. Pin description**

Symbol[1]	Bump/Pin		Description
	WLCSP16	XQFN16	
DAT2A	A1	1	data 2 input or output on host side
DAT3A	B1	2	data 3 input or output on host side
DAT0A	C1	3	data 0 input or output on host side
DAT1A	D1	4	data 1 input or output on host side
V <sub>CCA</sub>	A2	15	supply voltage A (host side)
CMDA	B2	16	command input or output on host side
CLKFB	C2	6	clock feedback signal on host side, this pin can be left floating
CLKA	D2	5	clock signal input on host side
V <sub>CCB</sub>	A3	14	supply voltage B (memory card side)
CMDB	B3	13	command input or output on memory card side
GND	C3	7	supply ground
CLKB	D3	8	clock signal input on memory card side
DAT2B	A4	12	data 2 input or output on memory card side
DAT3B	B4	11	data 3 input or output on memory card side
DAT0B	C4	10	data 0 input or output on memory card side
DAT1B	D4	9	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.  
See [Section 9.6](#) for options to swap identical channels.

## 9. Functional description

### 9.1. Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Auto direction sensing circuitry determines if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode). The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

**Table 4. Supported modes**

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

## 9.2. Enable and direction control

The device contains an auto-enable feature. If  $V_{CCB}$  rises above 1.5 V, the level translator logic is enabled automatically. As soon as  $V_{CCB}$  drops below 0.65 V, the memory card side drivers and the level translator logic are disabled. All pins on the host side, excluding CLKA are configured as inputs with a 70 k $\Omega$  resistor pulled up to  $V_{CCA}$ .

The device features an auto correction control for all data channels except CLK. For these pins the direction of data flow is sensed by the direction control logic and the output drivers are controlled accordingly. There is no need for the host interface to indicate the direction of data flow.

## 9.3. Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

## 9.4. EMI filter

All input/output driver stages are equipped with EMI filters to reduce interference towards sensitive mobile communication.

## 9.5. ESD protection

The device has robust ESD protections on all memory card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

## 9.6. Pin and channel naming

The channel/pin naming as shown in [Fig. 2](#) and in [Section 8](#) aims at using NXS0506 for SD-card interfaces. The sequence of the channels is chosen to easily connect to SD-card connectors. As the internal design of channels DAT0 (pins DAT0A and DAT0B), DAT1 (pins DAT1A and DAT1B), DAT2 (pins DAT2A and DAT2B), DAT3 (pins DAT3A and DAT3B) and CMD (pins CMDA and CMDB) is identical, these channels can be exchanged. Swapping channels in the above mentioned group can help ease PCB layout issues. E.g. DAT0 can be swapped with DAT1 or DAT3 with CMD without impact on functionality of NXS0506.

## 10. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage	4 ms transient; on pin V <sub>CCA</sub>	-0.5	4.6	V
		4 ms transient; on pin V <sub>CCB</sub>	-0.5	4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.3 V or V <sub>I</sub> > V <sub>CC</sub> + 0.3 V	[1]	-	±20 mA
V <sub>I</sub>	input voltage	4 ms transient at I/O pins	-0.5	4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.3 V or V <sub>O</sub> > V <sub>CCA</sub> + 0.3 V	[1]	-	±20 mA
		V <sub>O</sub> < -0.3 V or V <sub>O</sub> > V <sub>CCB</sub> + 0.3 V	[1]	-	±50 mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	250	mW
T <sub>stg</sub>	storage temperature		-55	+150	°C
I <sub>lu(IO)</sub>	input/output latch-up current	JESD78F: -0.5V <sub>CC</sub> < V <sub>I</sub> < 1.5V <sub>CC</sub> ; T <sub>j</sub> < 125 °C	-100	100	mA

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 11. Recommended operating conditions

**Table 6. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	on pin V <sub>CCA</sub>	[1]	1.1	-	1.95 V
		on pin V <sub>CCB</sub>	[1]	1.7	-	3.6 V
V <sub>I</sub>	input voltage	host side	-0.3	-	V <sub>CCA</sub> + 0.3	V
		memory card side	[2]	-0.3	-	V <sub>CCB</sub> + 0.3
T <sub>amb</sub>	ambient temperature		-40	+25	+85	°C

[1] V<sub>CCB</sub> ≥ V<sub>CCA</sub>

[2] The voltage must not exceed 3.6 V.

**Table 7. Integrated resistors**

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
R <sub>pu</sub>	pull-up resistance		42	70	100	kΩ
R <sub>s</sub>	series resistance	host side; R1	[2]	-	22.5	Ω
		card side; R2	[2]	-	15	Ω

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2] Guaranteed by design and characterization.

## 12. Static characteristics

**Table 8. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V) unless otherwise specified.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
<b>Automatic enable feature: V<sub>CCB</sub></b>						
V <sub>en</sub>	device enable voltage level	V <sub>CCA</sub> ≥ 1.0 V; V <sub>CCB</sub> rising edge	0.9	1.2	1.5	V
V <sub>dis</sub>	device disable voltage level	V <sub>CCA</sub> ≥ 1.0 V; V <sub>CCB</sub> falling edge	0.65	1.0	1.3	V
<b>Host-side input signals: CMDA, DAT0A to DAT3A and CLKA</b>						
V <sub>IH</sub>	HIGH-level input voltage	1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	0.65V <sub>CCA</sub>	-	V <sub>CCA</sub> + 0.3	V
V <sub>IL</sub>	LOW-level input voltage	1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	-0.3	-	0.35V <sub>CCA</sub>	V
I <sub>I</sub>	input leakage current	CLKA; V <sub>CCA</sub> = 1.95 V; V <sub>I</sub> = 0 V to 1.95 V	-	-	1	μA
<b>Host-side output signals: CMDA and DAT0A to DAT3A</b>						
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -2 μA; V <sub>I</sub> = V <sub>IH</sub> (card side); 1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	0.8V <sub>CCA</sub>	-	V <sub>CCA</sub> + 0.3	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub> (card side); 1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	-0.3	-	0.15V <sub>CCA</sub>	V
<b>Host-side output signals: CLKFB</b>						
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -2 mA; V <sub>I</sub> = V <sub>IH</sub> (host side); 1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	0.8V <sub>CCA</sub>	-	V <sub>CCA</sub> + 0.3	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub> (host side); 1.1 V ≤ V <sub>CCA</sub> ≤ 1.95 V	-0.3	-	0.15V <sub>CCA</sub>	V
<b>Card-side input signals: CMDB and DAT0B to DAT3B</b>						
V <sub>IH</sub>	HIGH-level input voltage	1.7 V ≤ V <sub>CCB</sub> ≤ 3.6 V	0.625V <sub>CCB</sub>	-	V <sub>CCB</sub> + 0.3	V
V <sub>IL</sub>	LOW-level input voltage	1.7 V ≤ V <sub>CCB</sub> ≤ 1.95 V	-0.3	-	0.35V <sub>CCB</sub>	V
		2.7 V ≤ V <sub>CCB</sub> ≤ 3.6 V	-0.3	-	0.30V <sub>CCB</sub>	V
<b>Card-side output signal: CMDB, DAT0B to DAT3B and CLKB</b>						
V <sub>OH</sub>	HIGH-level output voltage	CLKB; V <sub>CCB</sub> = 1.7 V; I <sub>O</sub> = -2 mA; V <sub>I</sub> = V <sub>IH</sub> (host side)	0.85V <sub>CCB</sub>	-	2.0	V
		CLKB; V <sub>CCB</sub> = 2.7 V; I <sub>O</sub> = -4 mA; V <sub>I</sub> = V <sub>IH</sub> (host side)	0.85V <sub>CCB</sub>	-	V <sub>CCB</sub> + 0.3	V
		CMDB, DATnB; V <sub>CCB</sub> = 1.7 V; I <sub>O</sub> = -2 μA; V <sub>I</sub> = V <sub>IH</sub> (host side)	0.85V <sub>CCB</sub>	-	2.0	V
V <sub>OL</sub>	Low-level output voltage	I <sub>O</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub> (host side); V <sub>CCB</sub> = 1.7 V	-0.3	-	0.125V <sub>CCB</sub>	V
		I <sub>O</sub> = 4 mA; V <sub>I</sub> = V <sub>IL</sub> (host side); V <sub>CCB</sub> = 2.7 V	-0.3	-	0.125V <sub>CCB</sub>	V

## SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
<b>Current consumption</b>						
I <sub>CC</sub>	supply current	host side; all inputs = HIGH; V <sub>I</sub> = V <sub>CCA</sub> ; V <sub>CCA</sub> = 1.95 V; V <sub>CCB</sub> = 3.6 V	-	-	4	µA
		card side; all inputs = HIGH; V <sub>I</sub> = V <sub>CCA</sub> ; V <sub>CCA</sub> = 1.7 V; V <sub>CCB</sub> = 1.7 V	-	-	7	µA
		card side; all inputs = HIGH; V <sub>I</sub> = V <sub>CCA</sub> ; V <sub>CCA</sub> = 1.95 V; V <sub>CCB</sub> = 3.6 V	-	-	20	µA

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 13. Dynamic characteristics

### 13.1. Level translator

**Table 9. Level translator dynamic characteristics**

At recommended operating conditions; for waveform and test circuit see [Fig. 3](#) and [Fig. 4](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to 85 °C			Unit	
			Min	Typ[1]	Max		
<b>Host-side output transition times</b>							
t <sub>l</sub>	transition time	V <sub>CCA</sub> = 1.2 V to 1.8 V; output transition time between V <sub>X</sub> = 0.35V <sub>CCA</sub> and V <sub>Y</sub> = 0.65V <sub>CCA</sub>	[2]	-	0.3	1.0	ns
<b>Host-side input rise and fall times</b>							
t <sub>r</sub> , t <sub>f</sub>	rise and fall time	V <sub>CCA</sub> = 1.2 V to 1.8 V; input rise and fall time between V <sub>X</sub> = 0.35V <sub>CCA</sub> and V <sub>Y</sub> = 0.65V <sub>CCA</sub>	-	0.4	1.0	ns	
<b>Card-side output transition times</b>							
t <sub>l</sub>	transition time	V <sub>CCB</sub> = 1.8 V; output transition time between V <sub>X</sub> = 0.45 V and V <sub>Y</sub> = 1.4 V	[2]	0.4	0.88	1.32	ns
<b>Card-side input rise and fall times</b>							
t <sub>r</sub>	rise time	V <sub>CCB</sub> = 1.8 V; input rise time between 0.58 V and 1.27 V	0.2	0.5	0.96	ns	
t <sub>f</sub>	fall time	V <sub>CCB</sub> = 1.8 V; input fall time between 0.58 V and 1.27 V	0.2	0.45	0.96	ns	
<b>Host-side to card-side propagation delay; DATnA to DATnB, CMDA to CMDB and CLKA to CLKB</b>							
t <sub>pd</sub>	propagation delay	V <sub>CCA</sub> = 1.2 V; V <sub>CCB</sub> = 1.8 V	[3]	-	3.1	5.4	ns
		V <sub>CCA</sub> = 1.2 V; V <sub>CCB</sub> = 3.3 V	[3]	-	2.2	4.0	ns
		V <sub>CCA</sub> = 1.8 V; V <sub>CCB</sub> = 1.8 V	[3]	-	2.7	4.8	ns
		V <sub>CCA</sub> = 1.8 V; V <sub>CCB</sub> = 3.3 V	[3]	-	1.7	3.1	ns
t <sub>sk(o)</sub>	output skew time	V <sub>CCA</sub> = 1.2 V; V <sub>CCB</sub> = 1.8 V	-	-	200	ps	
		V <sub>CCA</sub> = 1.2 V; V <sub>CCB</sub> = 3.3 V	-	-	200	ps	
		V <sub>CCA</sub> = 1.8 V; V <sub>CCB</sub> = 1.8 V	-	-	200	ps	
		V <sub>CCA</sub> = 1.8 V; V <sub>CCB</sub> = 3.3 V	-	-	200	ps	

## SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection

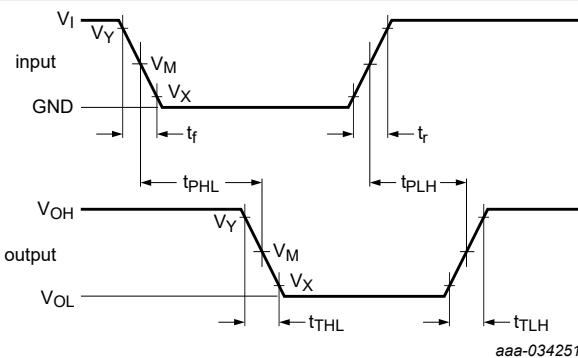
Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}C$ to $85^{\circ}C$			Unit	
			Min	Typ [1]	Max		
<b>Card-side to host-side propagation delay; DATnB to DATnA and CMDB to CMDA</b>							
$t_{pd}$	propagation delay	$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	[3]	-	2.7	4.6	ns
		$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	[3]	-	1.7	3.0	ns
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	[3]	-	2.7	4.6	ns
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	[3]	-	1.6	2.7	ns
$t_{sk(o)}$	output skew time	$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	-	-	200	ps	
		$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	-	-	200	ps	
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	-	-	200	ps	
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	-	-	200	ps	
<b>Host-side to host-side propagation delay; CLKA to CLKFB</b>							
$t_{pd}$	propagation delay	$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	[3]	-	5.8	10	ns
		$V_{CCA} = 1.2\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	[3]	-	3.9	7.0	ns
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 1.8\text{ V}$	[3]	-	5.4	9.4	ns
		$V_{CCA} = 1.8\text{ V}$ ; $V_{CCB} = 3.3\text{ V}$	[3]	-	3.3	5.8	ns
<b>Bus signal equivalent capacitance</b>							
$C_{I/O}$	input/output capacitance	$V_I = 0\text{ V}$ ; $f_i = 1\text{ MHz}$ ; $V_{CCA} = 1.8\text{ V}$ ; host side	[4]	-	5	-	pF
		$V_I = 0\text{ V}$ ; $f_i = 1\text{ MHz}$ ; $V_{CCB} = 1.8\text{ V}$ ; card side	[4]	-	12	-	pF

[1] Typical values are measured at  $T_{amb} = 25^{\circ}C$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[4] EMI filter line capacitance from I/O driver to pin;  $C_{I/O}$  is guaranteed by design.



Measurement points are given in [Table 10](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

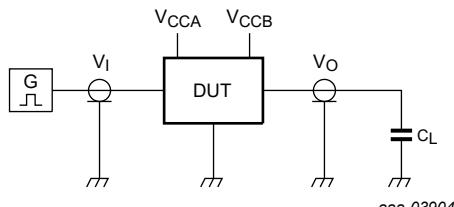
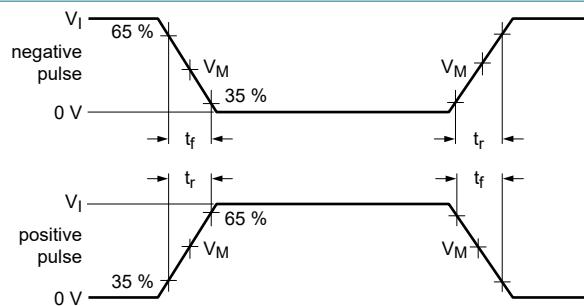
**Fig. 3. The input to output propagation delays, input rise and fall times and output transition times**

**Table 10. Measurement points**

Supply voltage		Input		Output
$V_{CCA}$	$V_{CCB}$	$V_I$ [1]	$V_M$ [1]	$V_M$ [2]
1.1 V to 1.95 V	1.7 V to 3.6 V	$V_{CCI}$	$0.5V_{CCI}$	$0.5V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

**SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection**


aaa-039048

Test data is given in [Table 11](#).

All input pulses are supplied by generators having the following characteristics:

PRR  $\leq$  10 MHz.

$Z_O = 50 \Omega$ ;

input edges ( $t_r$ ,  $t_f$ ) are defined in [Section 13](#);

Definitions test circuit:

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig. 4. Test circuit for measuring switching time**

**Table 11. Test data**

Supply voltage		Input	Load	
$V_{CCA}$	$V_{CCB}$	$V_I$ [1]	$C_L$ (host side)	$C_L$ (card side)
1.1 V to 1.95 V	1.7 V to 3.6 V	$V_{CCI}$	10 pF	15 pF

[1]  $V_{CCI}$  is the supply voltage associated with the input.

## 14. Application information

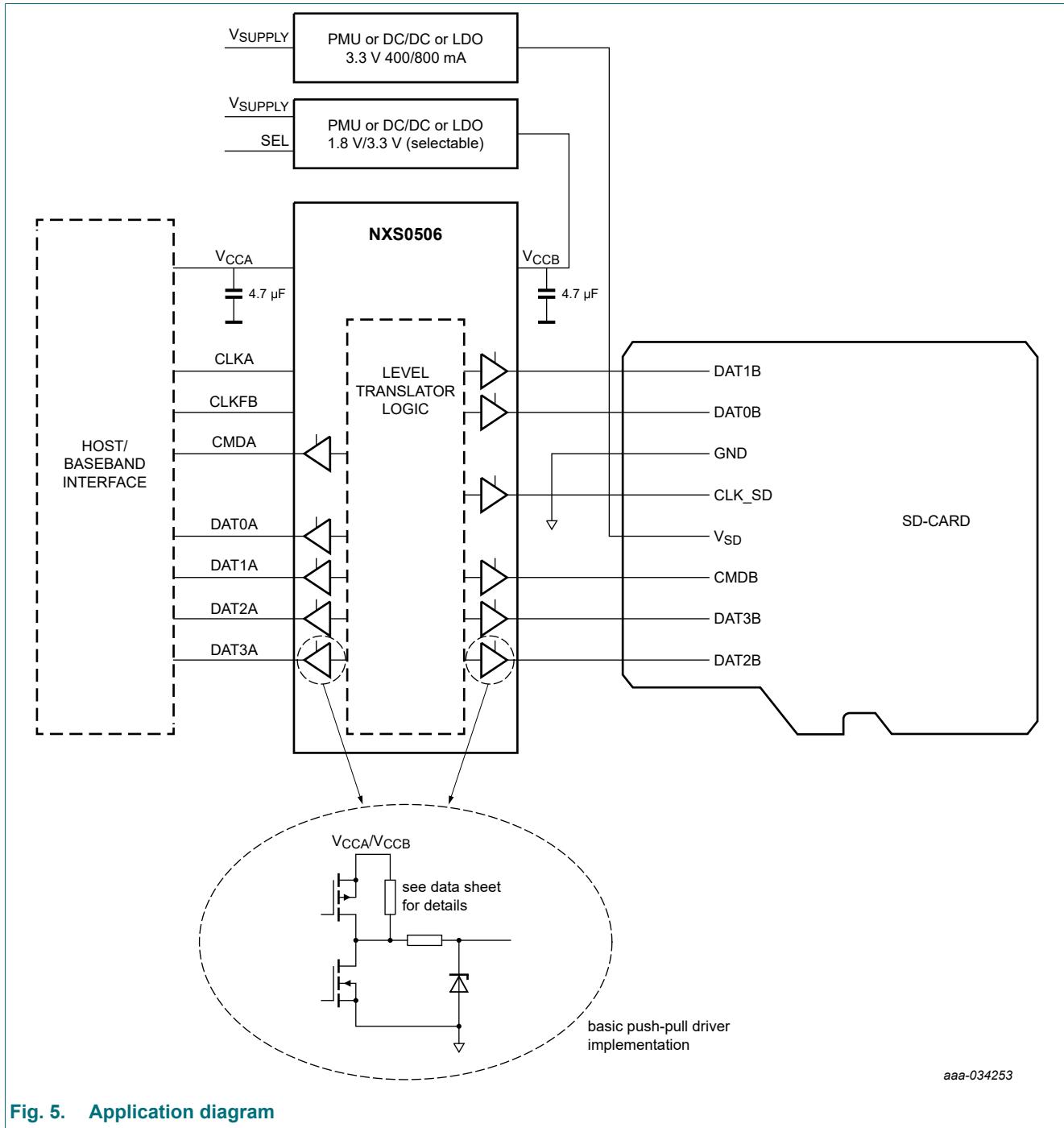


Fig. 5. Application diagram

### 14.1. PCB design guidelines

The translator can operate with frequencies up to 208 MHz so the PCB connections between host and translator and translator and card can start to act as transmission lines, affecting the signal integrity.

For PCB connections below 8 cm ( $t_r = 0.4$  ns) no degradation of the signal integrity is to be expected. For longer connections it's important to take pre-cautions and check the signal integrity during the development phase of the PCB. If the CLKFB is used to synchronize the data that is read from the card, it is important to place the translator as close as possible to the card connector.

## 15. Design and assembly recommendations

This section is only applicable for type number NXS0506UP (SOT8025-1/WLCSP16).

### 15.1. PCB design guidelines

For optimum performance, use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to [Table 12](#) for the recommended PCB design parameters.

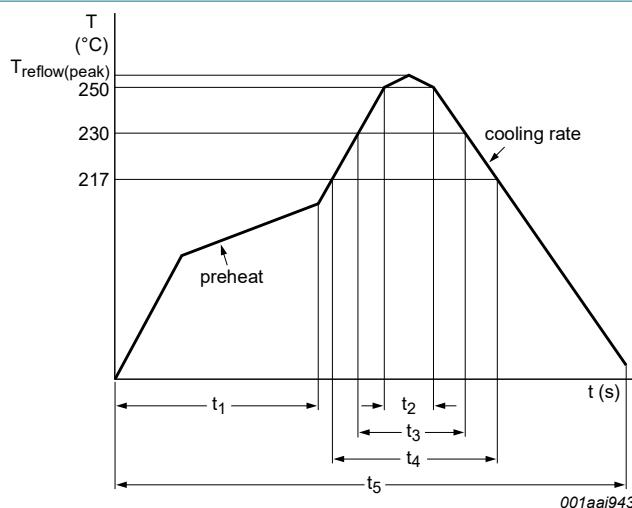
**Table 12. Recommended PCB design parameters**

Parameter	Value or specification
PCB Cu pad shape	circular
PCB Cu pad diameter	200 $\mu\text{m}$
PCB solder resist diameter	270 $\mu\text{m}$
WLCSP pad diameter (UBM)	200 $\mu\text{m}$

### 15.2. PCB assembly guidelines for Pb-free soldering

**Table 13. Assembly recommendations**

Parameter	Value or specification
PCB stencil shape	circular
PCB stencil aperture diameter	200 $\mu\text{m}$
PCB stencil thickness	80 $\mu\text{m}$
Solder paste material	SnAg <sub>4</sub> Cu (Cu 0.5%) (SAC405)
Solder reflow profile	see <a href="#">Fig. 6</a>



The device can withstand at least three reflows with this profile.

**Fig. 6. Pb-free solder reflow profile**

**SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection****Table 14. Reflow soldering process characteristics** $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{reflow(peak)}$	peak reflow temperature		230	-	260	$^{\circ}\text{C}$
$t_1$	time 1	soak time	60	-	180	s
$t_2$	time 2	time during $T \geq 250 \text{ }^{\circ}\text{C}$	-	-	30	s
$t_3$	time 3	time during $T \geq 230 \text{ }^{\circ}\text{C}$	10	-	50	s
$t_4$	time 4	time during $T \geq 217 \text{ }^{\circ}\text{C}$	30	-	150	s
$t_5$	time 5		-	-	540	s
$dT/dt$	rate of temperature change	cooling rate	-	-	-6	$^{\circ}\text{C/s}$
		preheat	2.5	-	4.0	$^{\circ}\text{C/s}$

## 16. Package outline

WLCSP16: wafer level chip-scale package; 16 bumps; 1.455 mm x 1.455 mm x 0.43 mm body

SOT8025-1

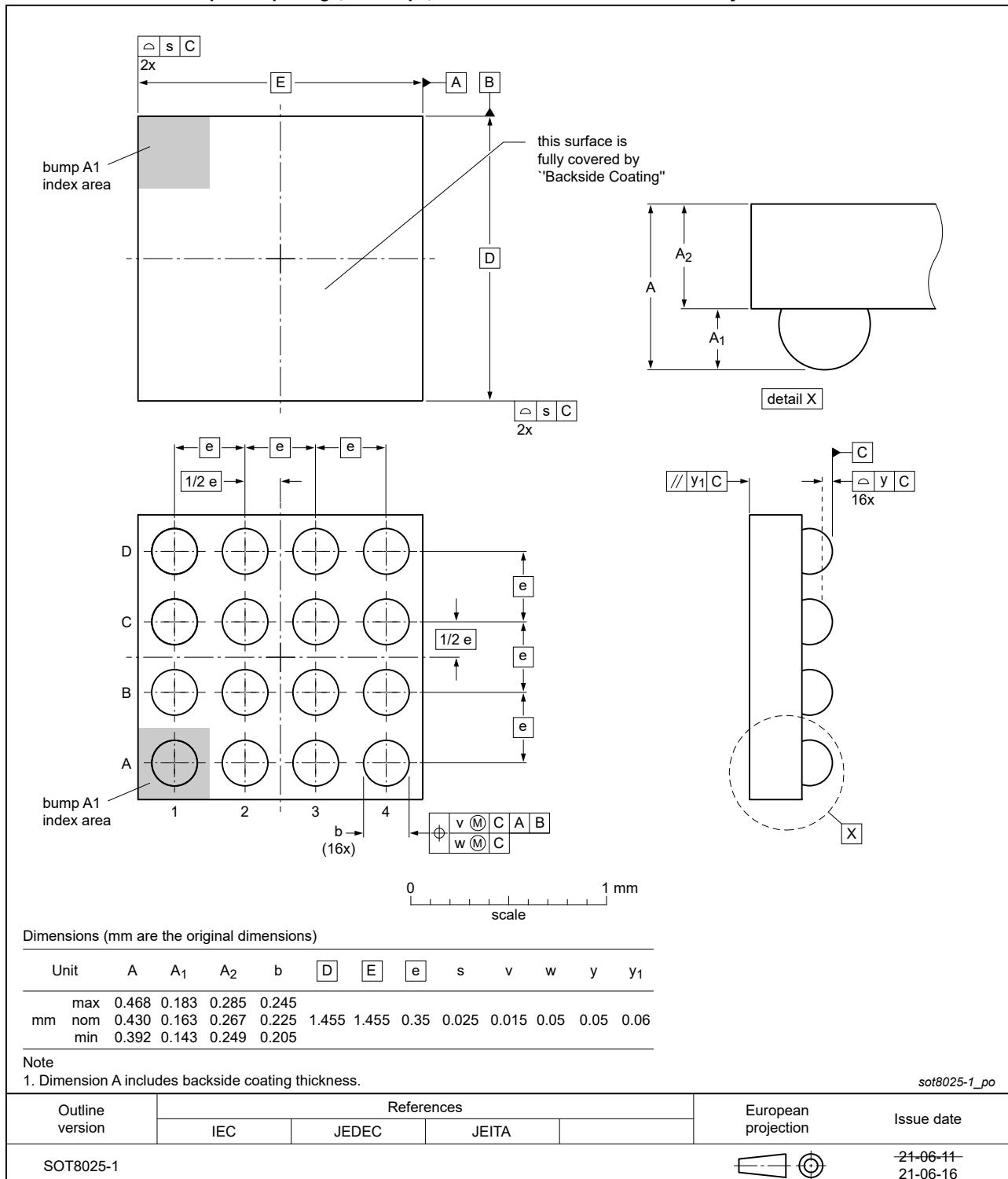


Fig. 7. Package outline SOT8025-1 (WLCSP16)

**SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection**

XQFN16: plastic, extremely thin quad flat package; no leads;  
16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1

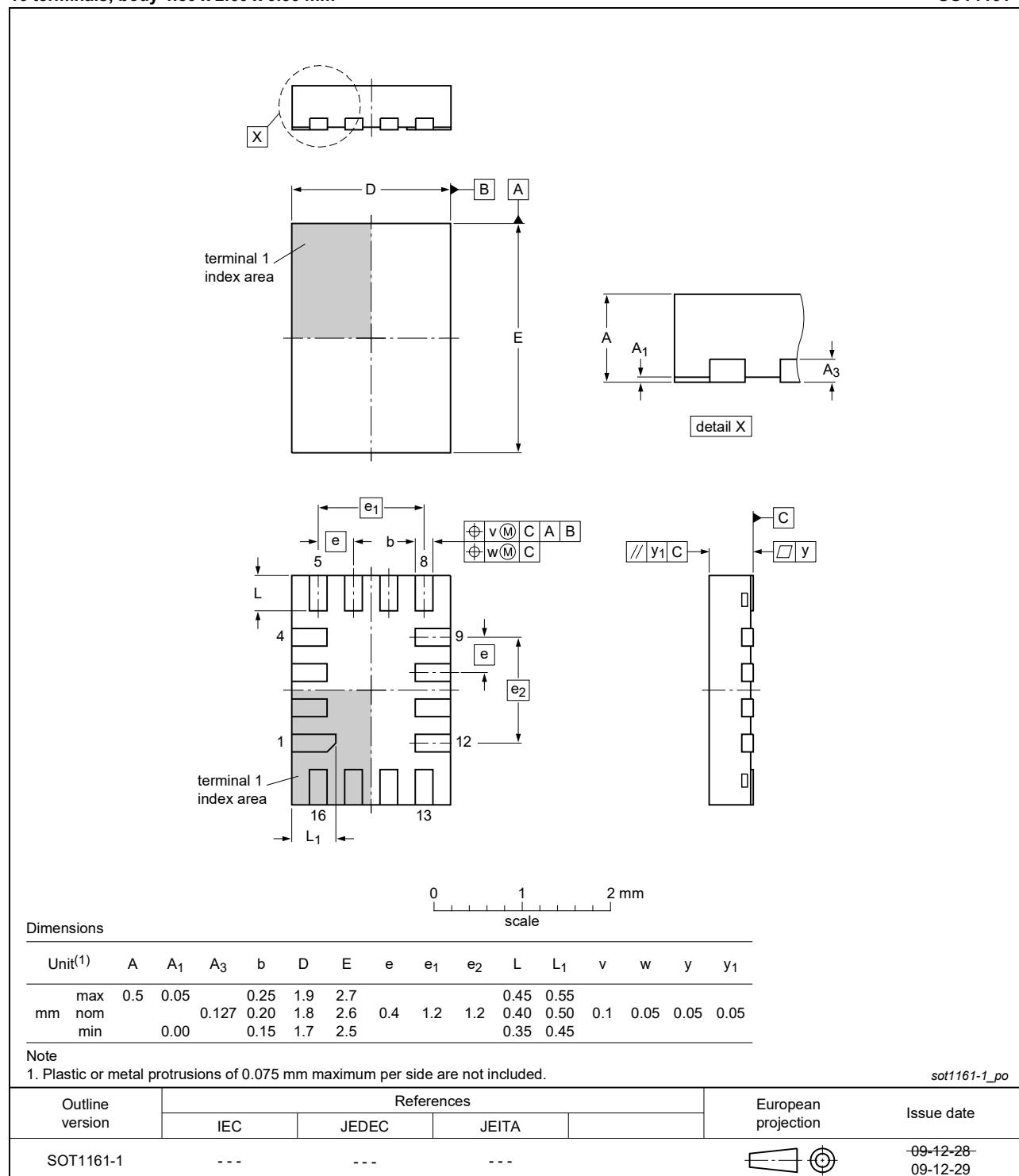


Fig. 8. Package outline SOT1161-1 (XQFN16)

## 17. Abbreviations

**Table 15. Abbreviations**

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
EMI	Electro Magnetic Interface
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FR4	Flame Retard 4
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LDO	Low-Dropout
MMC	MultiMedia Card
NSMD	Non-Solder Mask PCB Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PMU	Project Management Unit
PRR	Pulse Rate Repetition
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
UBM	Under Bump Metallization
WLCSP	Wafer-Level Chip-Scale Package

## 18. Revision history

**Table 16. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NXS0506 v.4.1	20240731	Product data sheet	-	NXS0506 v.4
NXS0506 v.4	20240202	Product data sheet	-	NXS0506 v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Fig. 2</a> updated.</li> <li>• <a href="#">Table 5</a>: input and output clamping current added.</li> </ul>			
NXS0506 v.3	20231030	Product data sheet	-	NXS0506 v.2
Modifications:	<ul style="list-style-type: none"> <li>• Type number NXS0506GU (SOT1161-1/XQFN16) added.</li> <li>• <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 12</a>: input leakage current conditions have changed. (errata)</li> <li>• <a href="#">Table 9</a> updated, with additional output skew time (<math>t_{sk(o)}</math>) parameters.</li> <li>• <a href="#">Fig. 5</a>: application diagram updated.</li> <li>• <a href="#">Section 15</a> updated.</li> </ul>			
NXS0506 v.2	20220308	Product data sheet	-	NXS0506 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Fig. 1</a> and <a href="#">Fig. 2</a> have changed (errata).</li> </ul>			
NXS0506 v.1	20220131	Product data sheet	-	-

## 19. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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