



GAN041-650WSB

650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package

12 January 2021

Product data sheet

1. General description

The GAN041-650WSB is a 650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Ultra-low reverse recovery charge
- Simple gate drive (0 V to +10 V or 12 V)
- Robust gate oxide (± 20 V capability)
- High gate threshold voltage (+4 V) for very good gate bounce immunity
- Very low source-drain voltage in reverse conduction mode
- Transient over-voltage capability

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

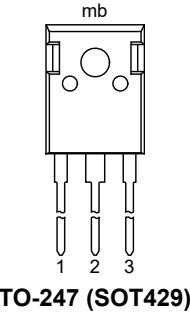
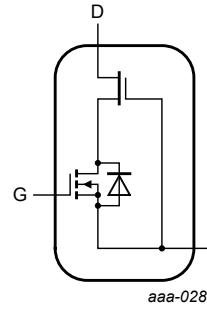
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$-55^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$		-	-	650	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25^{\circ}\text{C}$; Fig. 2		-	-	47.2	A
P_{tot}	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$; Fig. 1		-	-	187	W
T_j	junction temperature			-55	-	175	$^{\circ}\text{C}$
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 32$ A; $T_j = 25^{\circ}\text{C}$; Fig. 11		-	35	41	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 32$ A; $V_{DS} = 400$ V; $V_{GS} = 10$ V;		-	6.6	-	nC
$Q_{G(tot)}$	total gate charge	$T_j = 25^{\circ}\text{C}$; Fig. 13 ; Fig. 14		-	22	-	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 32$ A; $dI_S/dt = -1000$ A/μs; $V_{GS} = 0$ V; $V_{DS} = 400$ V; Fig. 20		-	150	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		
mb	S	mounting base; connected to source	 TO-247 (SOT429)	 aaa-028116

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN041-650WSB	TO-247	plastic, single-ended through-hole package; 3 leads; 5.45 mm pitch; 20.45 mm x 15.6 mm x 4.95 mm body	SOT429

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN041-650WSB	GAN041 650WSB

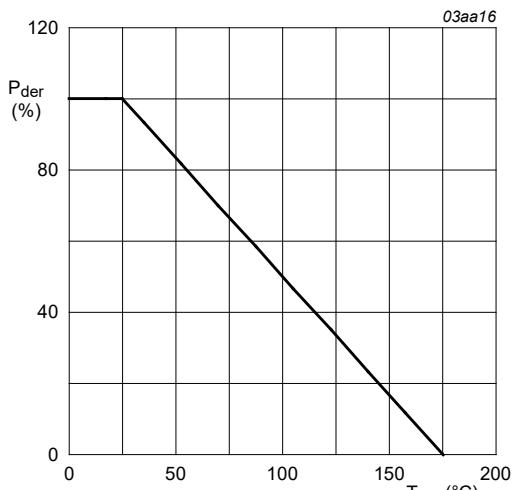
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

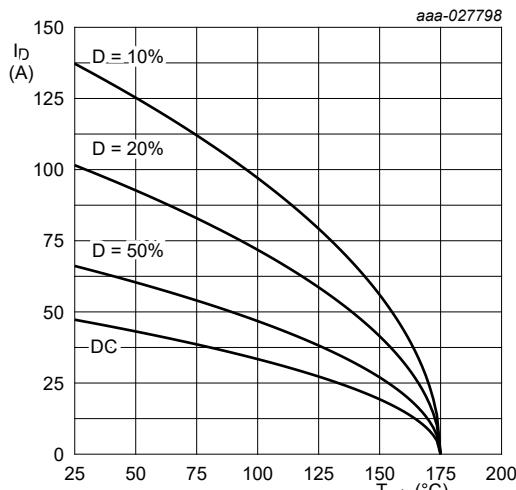
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$-55^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$	-	650	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1 \mu\text{s}$; $\delta_{\text{factor}} = 0.01$	-	725	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$; Fig. 1	-	187	W
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 25^{\circ}\text{C}$; Fig. 2	-	47.2	A
		$V_{GS} = 10 \text{ V}$; $T_{mb} = 100^{\circ}\text{C}$; Fig. 2	-	33.4	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$; Fig. 3	-	240	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{\text{sld(M)}}$	peak soldering temperature		-	260	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 0\text{ V}$		-	47.2	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$		-	240	A



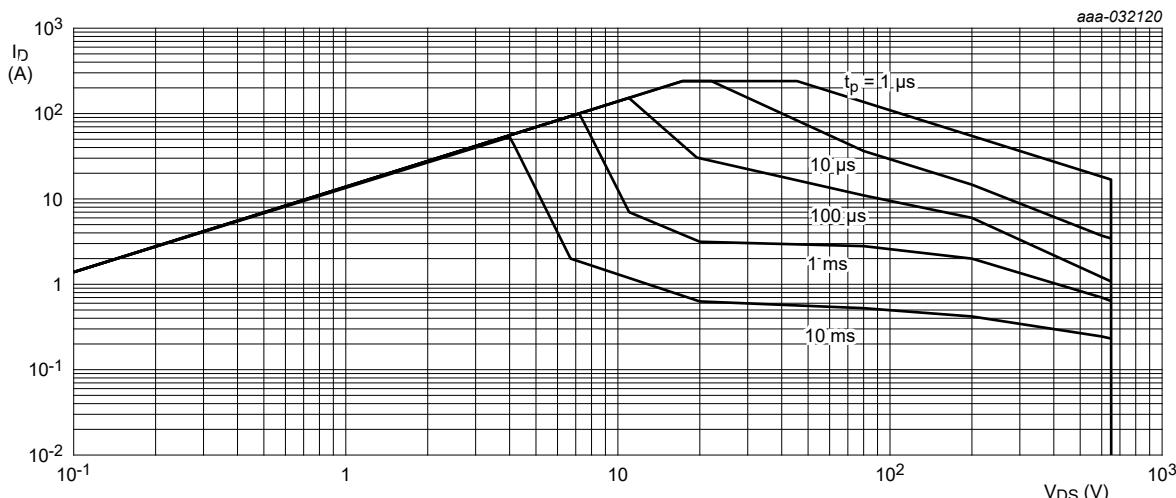
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$; Pulse width $\leq 10\text{ }\mu\text{s}$

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	0.8	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	40	K/W

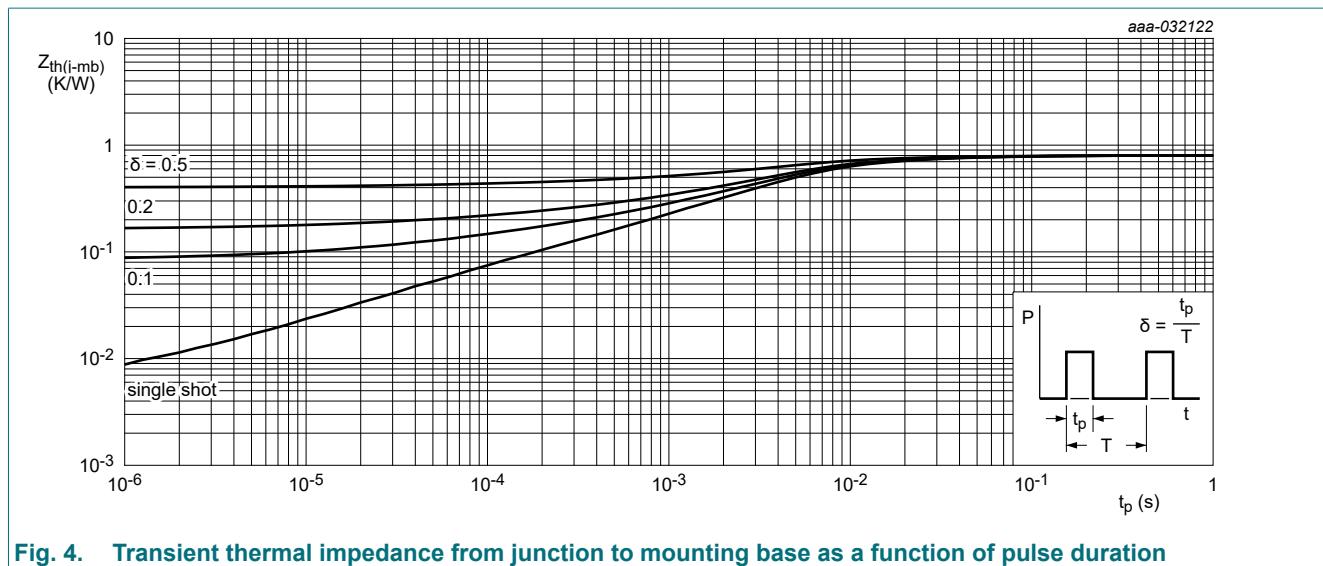


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C		3.4	3.9	4.5	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 10		2.2	-	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 10		-	-	5.2	V
I _{DSS}	drain leakage current	V _{DS} = 650 V; V _{GS} = 0 V; T _j = 25 °C		-	2.5	25	μA
		V _{DS} = 650 V; V _{GS} = 0 V; T _j = 175 °C		-	20	-	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	10	400	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	10	400	nA
R _{DSON}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 32 A; T _j = 25 °C; Fig. 11		-	35	41	mΩ
		V _{GS} = 10 V; I _D = 32 A; T _j = 175 °C; Fig. 12		-	84	98	mΩ
R _G	gate resistance	f = 1 MHz		0.8	1.9	4.8	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 32 A; V _{DS} = 400 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13; Fig. 14		-	22	-	nC
Q _{GS}	gate-source charge			-	8.4	-	nC
Q _{GD}	gate-drain charge			-	6.6	-	nC
C _{iss}	input capacitance	V _{DS} = 400 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	1500	-	pF
C _{oss}	output capacitance			-	147	-	pF
C _{rss}	reverse transfer capacitance			-	5	-	pF
C _{o(er)}	effective output capacitance, energy related	0 V ≤ V _{DS} ≤ 400 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	220	-	pF
C _{o(tr)}	effective output capacitance, time related	0 V ≤ V _{DS} ≤ 400 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C		-	380	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400$ V; $R_L = 12.5$ Ω; $V_{GS} = 12$ V; $R_{G(ext)} = 12$ Ω; $I_S = 32$ A; Fig. 17 ; Fig. 18	-	14	-	-	ns
t_r	rise time		-	14	-	-	ns
$t_{d(off)}$	turn-off delay time		-	36	-	-	ns
t_f	fall time		-	17	-	-	ns
Q_{oss}	output charge	$V_{GS} = 0$ V; $V_{DS} = 400$ V	-	150	-	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 32$ A; $V_{GS} = 0$ V; $T_j = 25$ °C; Fig. 19	-	1.8	-	-	V
		$I_S = 16$ A; $V_{GS} = 0$ V; $T_j = 25$ °C; Fig. 19	-	1.3	-	-	V
t_{rr}	reverse recovery time	$I_S = 32$ A; $dI_S/dt = -1000$ A/μs; $V_{GS} = 0$ V; $V_{DS} = 400$ V; Fig. 20	-	59	-	-	ns
Q_r	recovered charge		-	150	-	-	nC

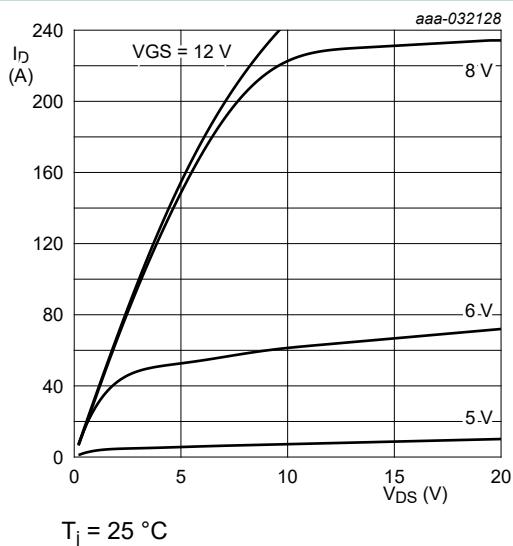


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

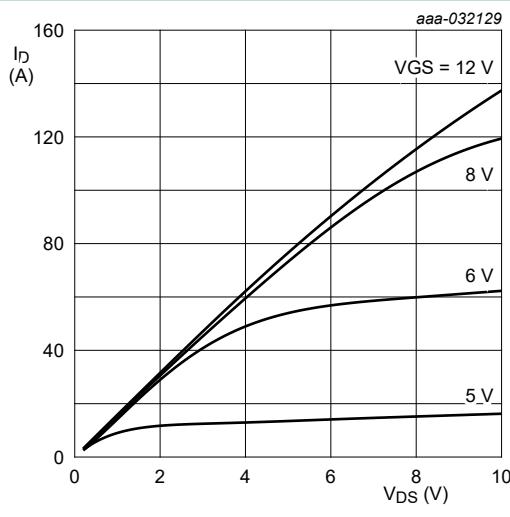


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

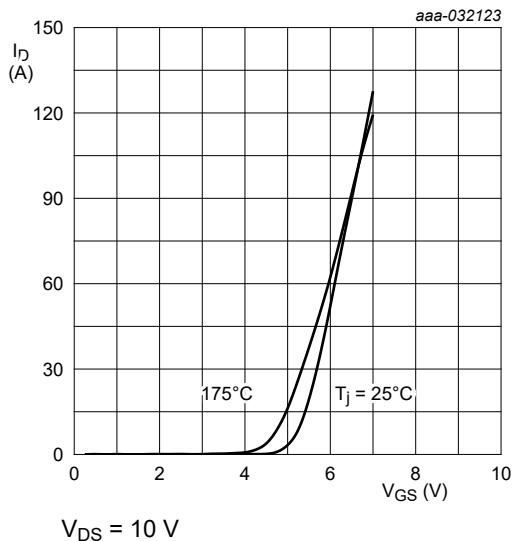


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

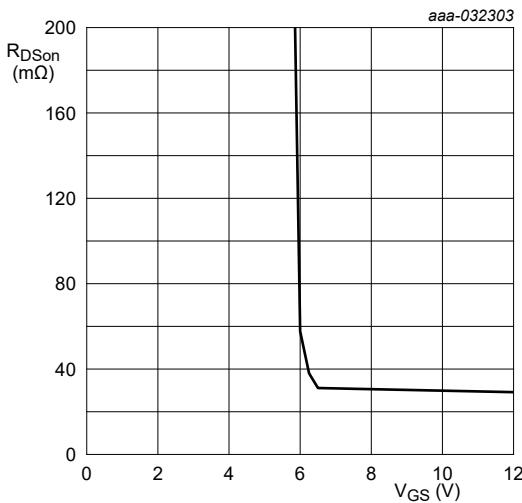


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

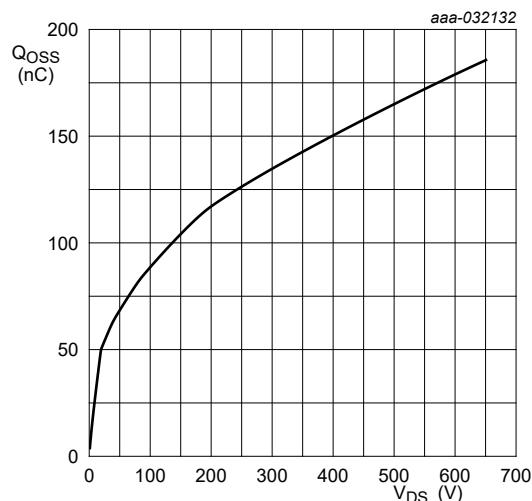


Fig. 9. Typical QOSS

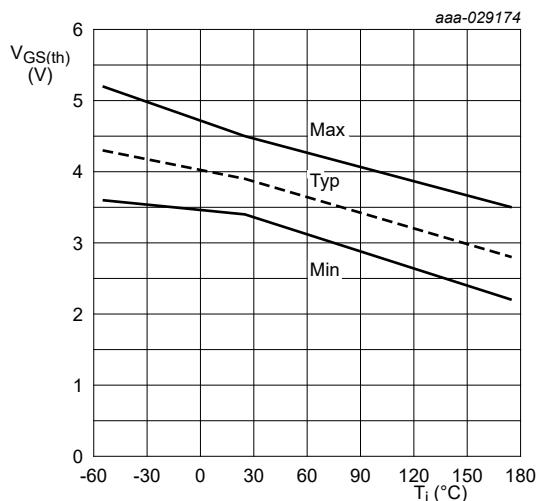
 $I_D = 1 \text{ mA} ; V_{DS} = V_{GS}$

Fig. 10. Gate-source threshold voltage as a function of junction temperature

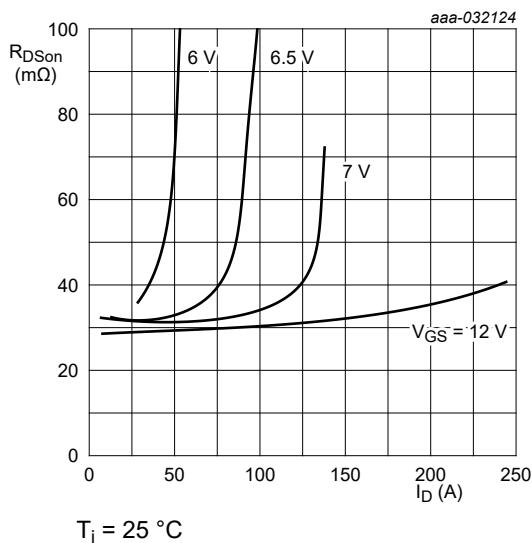
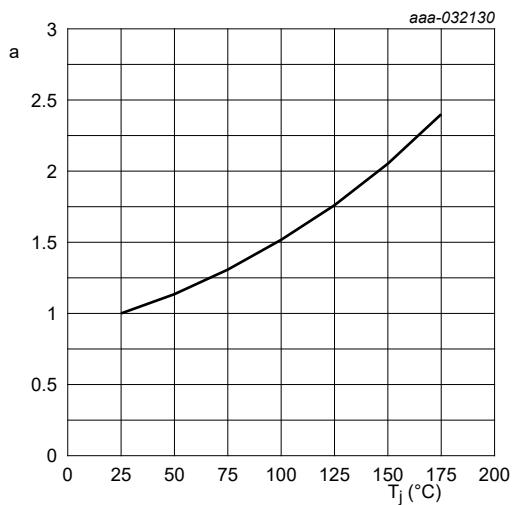
 $T_j = 25 \text{ °C}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

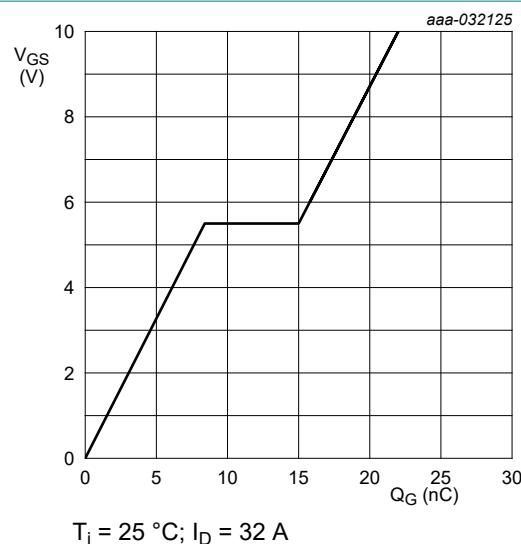


Fig. 13. Gate-source voltage as a function of gate charge; typical values

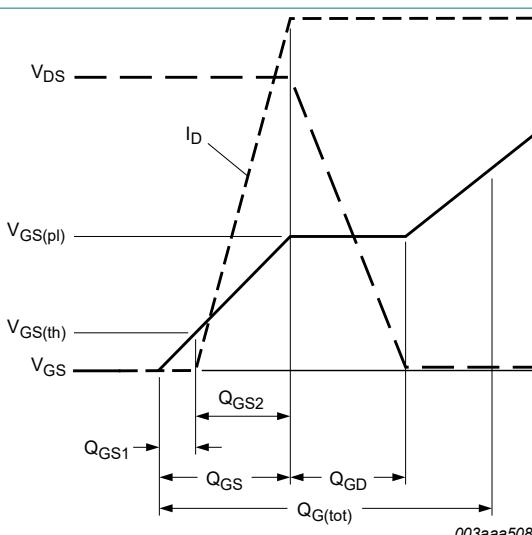


Fig. 14. Gate charge waveform definitions

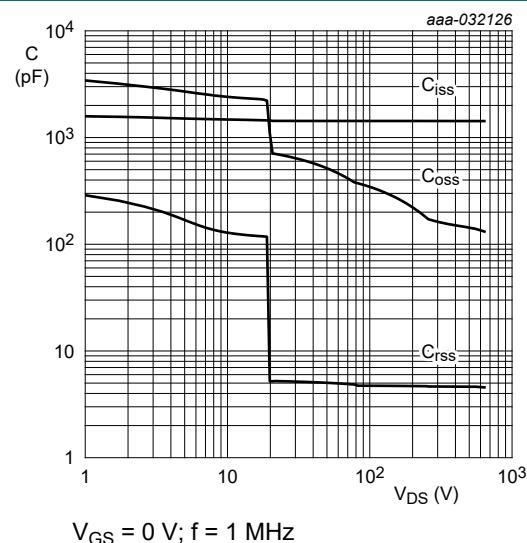


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

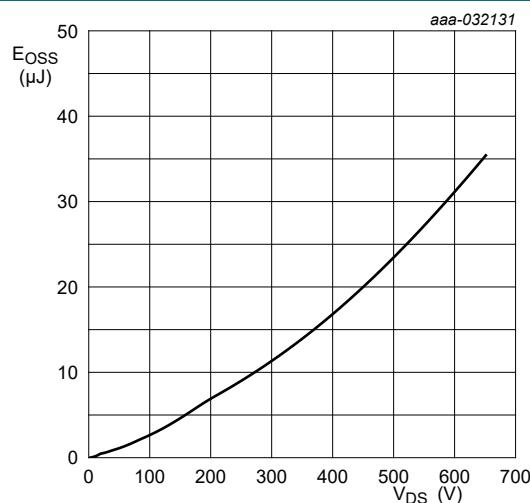


Fig. 16. Typical COSS Stored Energy

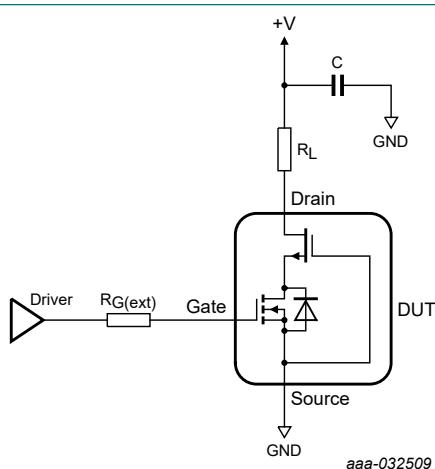


Fig. 17. Switching time test circuit

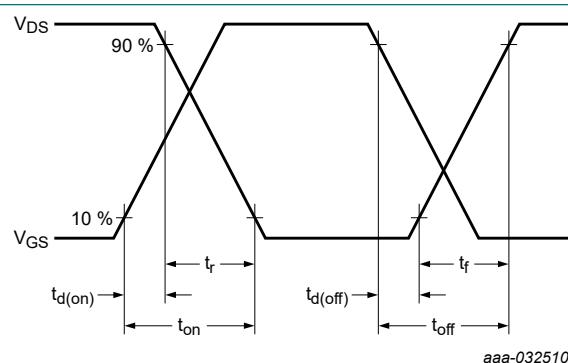
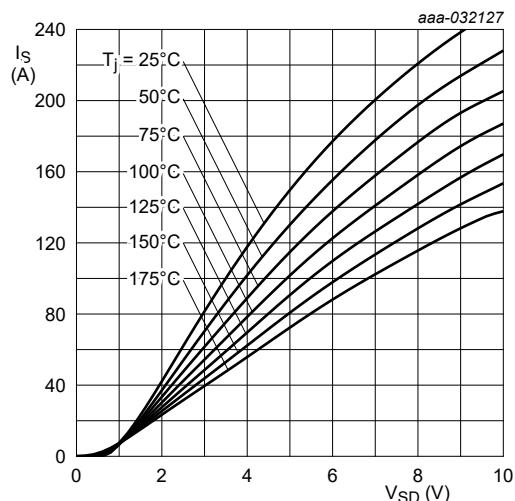


Fig. 18. Switching time waveform



$V_{GS} = 0 \text{ V}$

Fig. 19. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

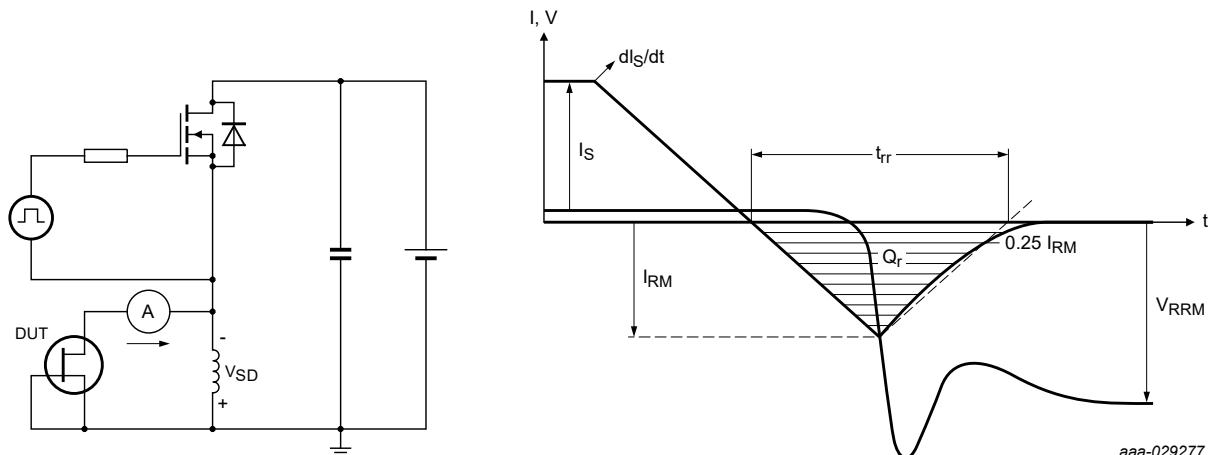


Fig. 20. Diode reverse recovery test circuit and waveform

11. Application information

A Ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin, (see figure below). Keeping the gate-source loop as compact as possible minimizes the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be 200 Ω — 270 Ω @ 100 MHz, (recommended p/n BLM18AG221SN1D).

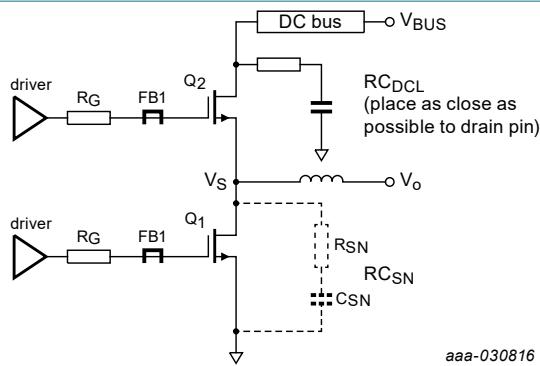
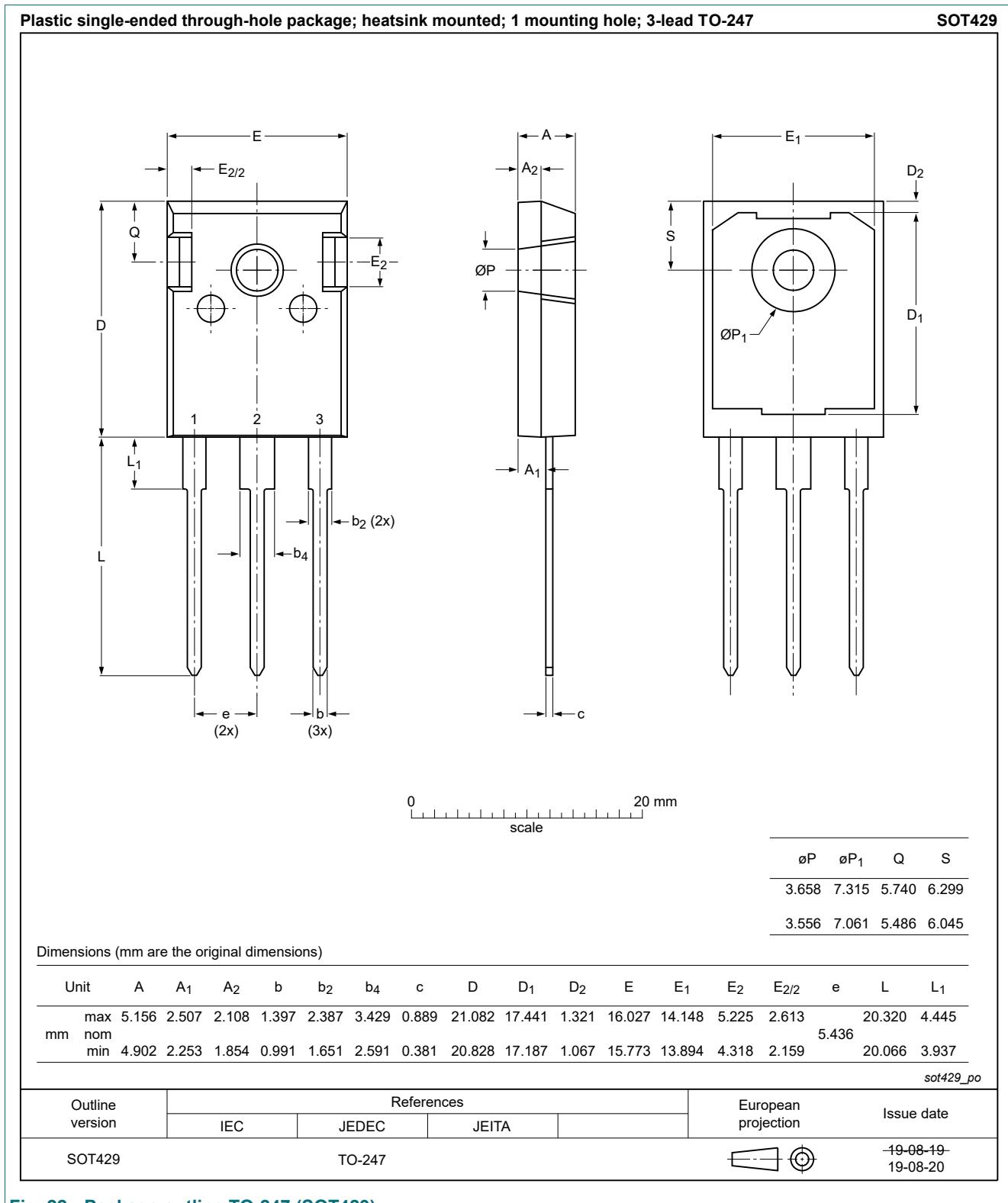


Fig. 21. Ferrite bead and RC snubber

A DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω, most easily achieved with parallel combination 10 nF and 8 Ω. This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

12. Package outline



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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