



BUK7J2R4-80M

N-channel 80 V, 2.4 mOhm, Standard level MOSFET in LFPAK56E

3 July 2024

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 14 low ohmic split-gate technology, for ultra-low R_{DSon} capability, housed in a LFPAK56E package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 14 split-gate technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Fast and efficient switching with optimal damping and low spiking
- LFPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints
- LFPAK copper clip technology:
 - Improved reliability, with reduced R_{th} , R_{DSon} and package inductance
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting and solenoid control
- Ultra high-performance power switching

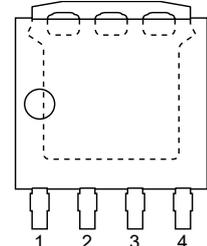
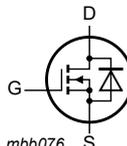
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	231	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	294	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	1.3	1.9	2.4	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	42.5	85	127	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7J2R4-80M	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7J2R4-80M	72M480J

8. Limiting values

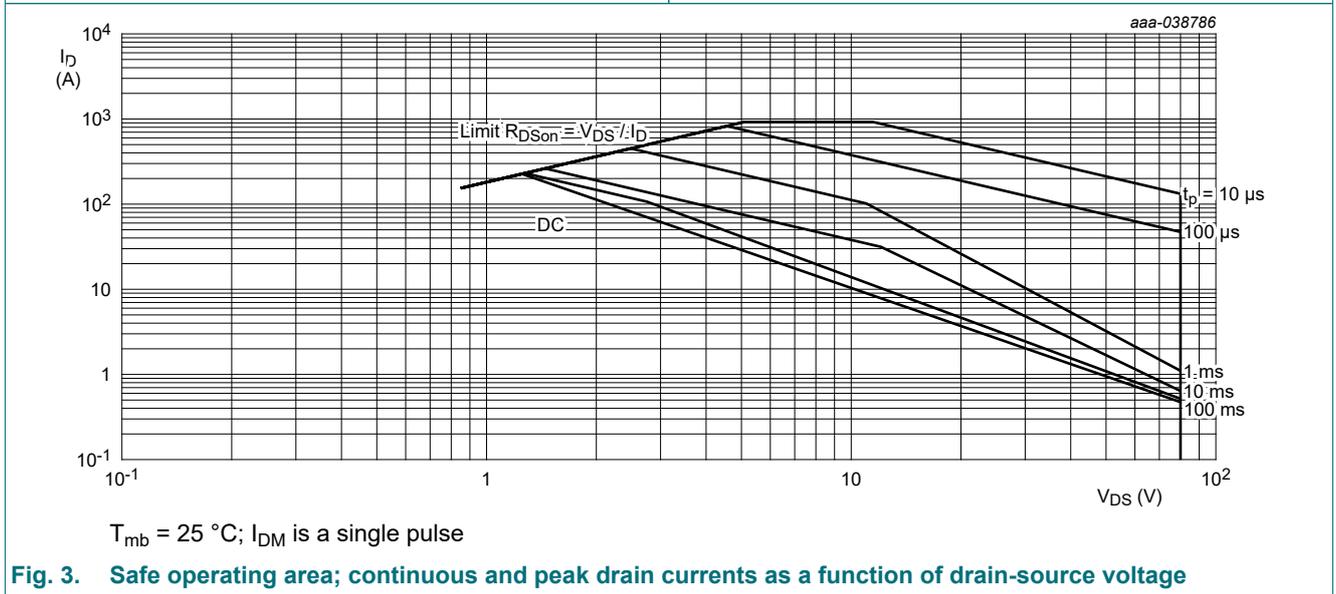
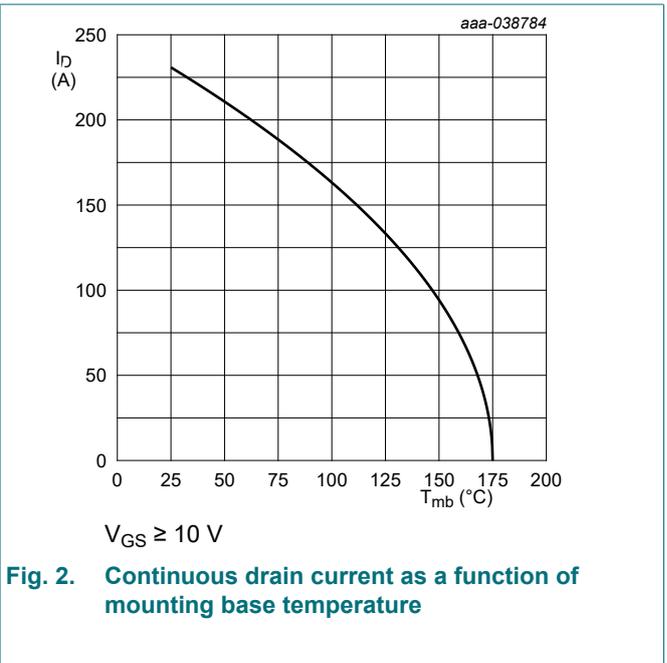
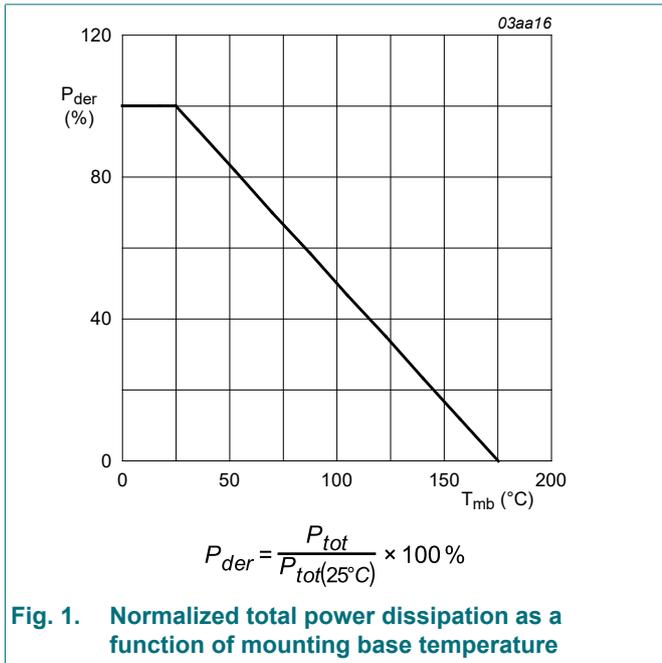
Table 5. Limiting values

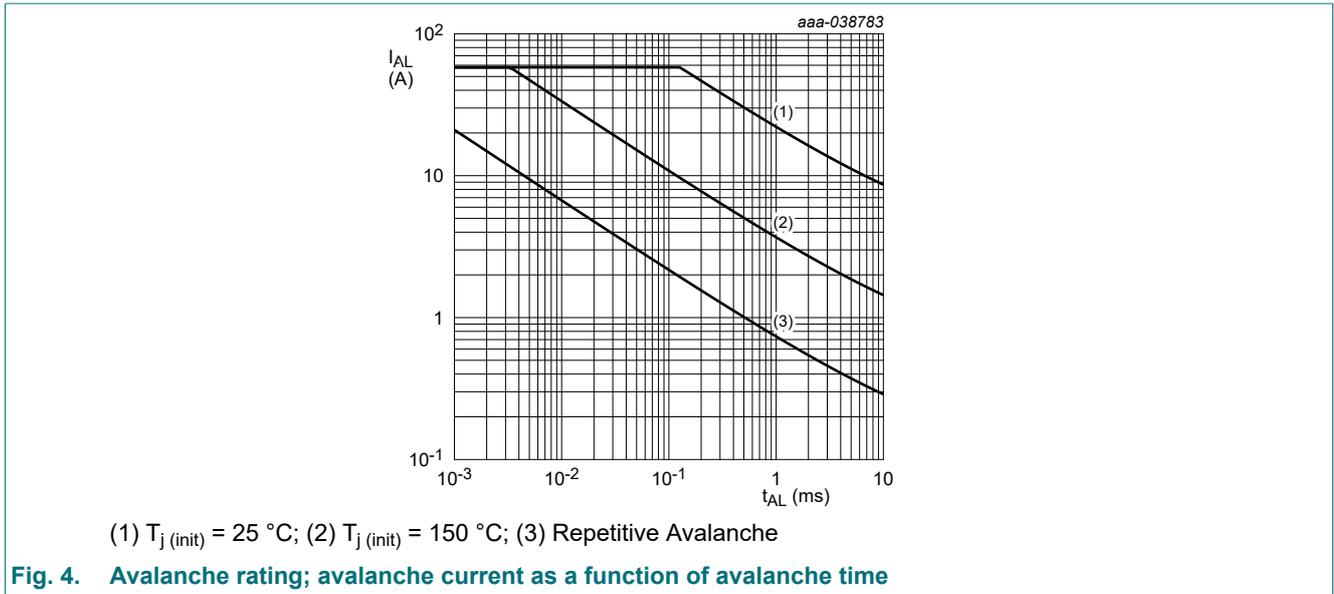
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	294	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	231	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	163	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	923	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
I_{AS}	non-repetitive avalanche current	$V_{sup} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[1]	58	A
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	231	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	923	A

Symbol	Parameter	Conditions	Min	Max	Unit
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 58 \text{ A}$; $V_{sup} \leq 80 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 4	[1] [2] [3]	-	383 mJ

- [1] Protected by 100% test.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



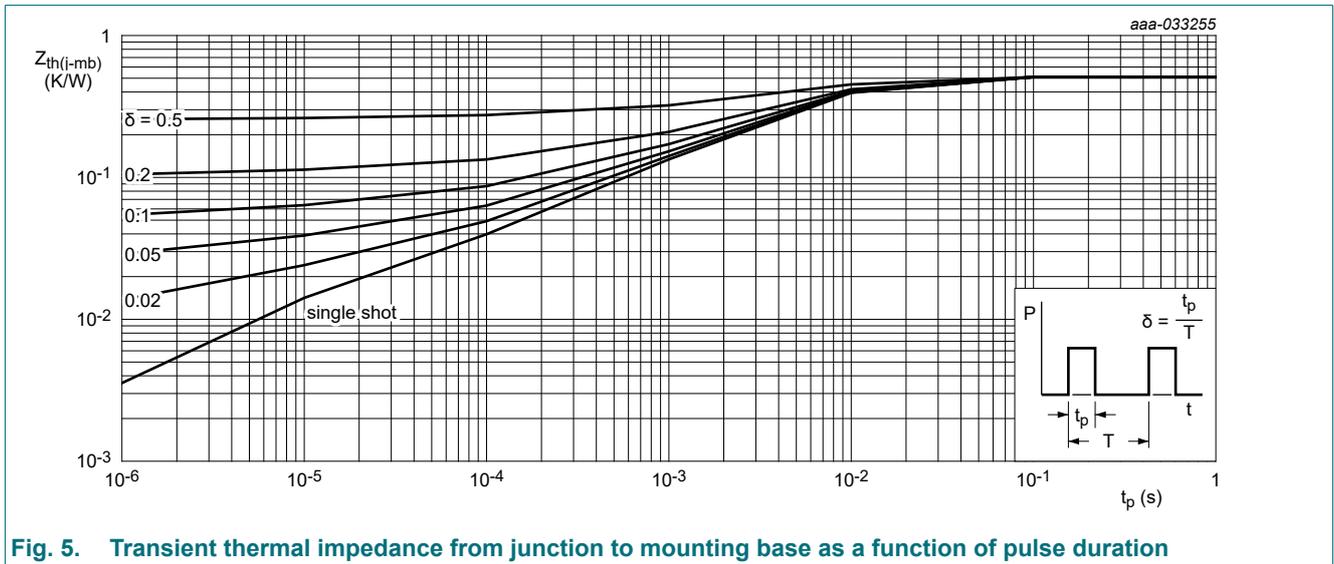


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

$T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	80	87	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -40\text{ °C}$	-	85	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ °C}$	72	84	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25\text{ °C}$; Fig. 9	2	3	4	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 175\text{ °C}$; Fig. 10	1	1.9	-	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55\text{ °C}$; Fig. 10	-	3.3	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 80\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	-	0.01	1	μA
		$V_{DS} = 80\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 125\text{ °C}$	-	3	100	μA
		$V_{DS} = 80\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ °C}$	-	76	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ °C}$	-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ °C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	1.3	1.9	2.4	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 105\text{ °C}$; Fig. 12	2	3.1	3.8	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 125\text{ °C}$; Fig. 12	2.2	3.4	4.3	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175\text{ °C}$; Fig. 12	2.8	4.4	5.5	m Ω
R_G	gate resistance	$f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	0.4	0.8	1.6	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	42.5	85	127	nC
Q_{GS}	gate-source charge		8.8	22	35	nC
Q_{GD}	gate-drain charge		5.8	16.5	38	nC
C_{iss}	input capacitance	$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; Fig. 15	3510	5850	8191	pF
C_{oss}	output capacitance		554	1385	2493	pF
C_{rss}	reverse transfer capacitance		4	44	102	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 40\text{ V}$; $R_L = 1.6\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$	-	19	-
t_r	rise time	-		18	-	ns
$t_{d(off)}$	turn-off delay time	-		53	-	ns
t_f	fall time	-		29	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16	-	0.79	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	38	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$; Fig. 17	-	33	-	nC

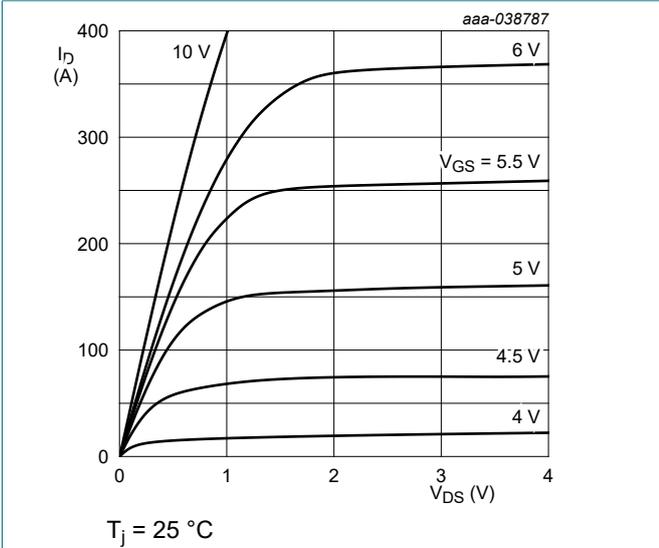


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

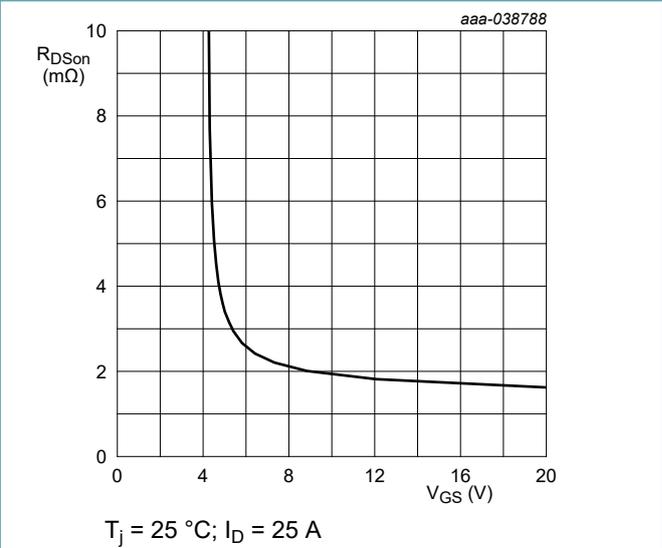


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

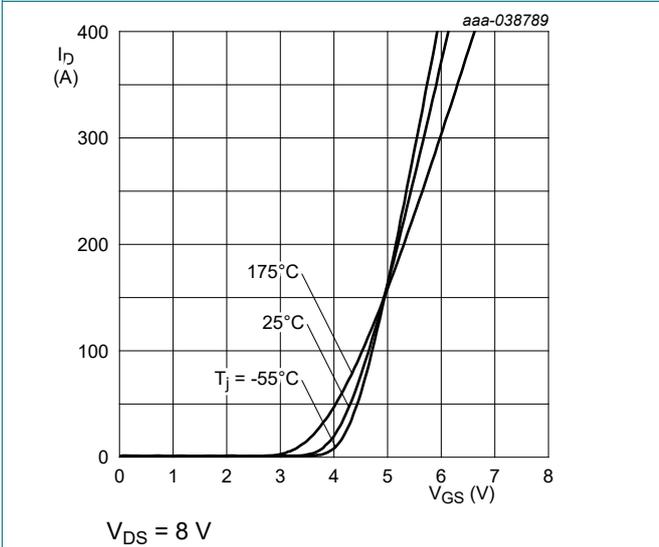


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

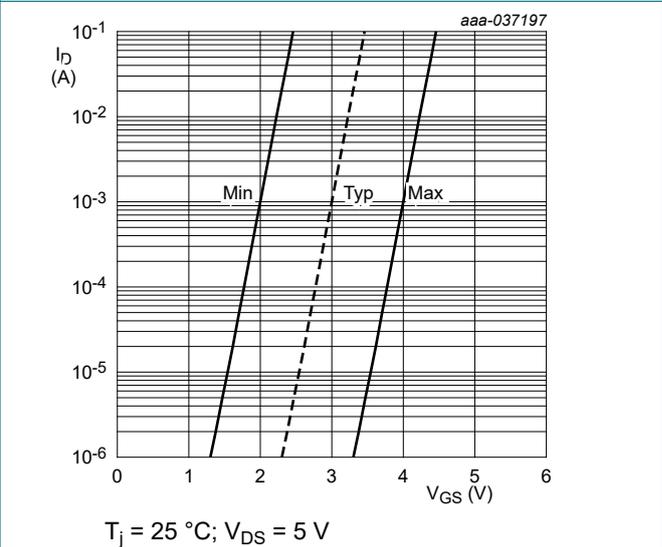


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

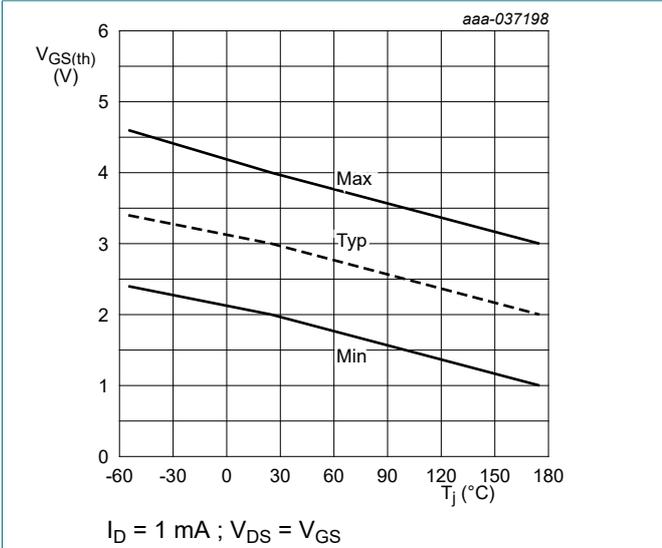


Fig. 10. Gate-source threshold voltage as a function of junction temperature

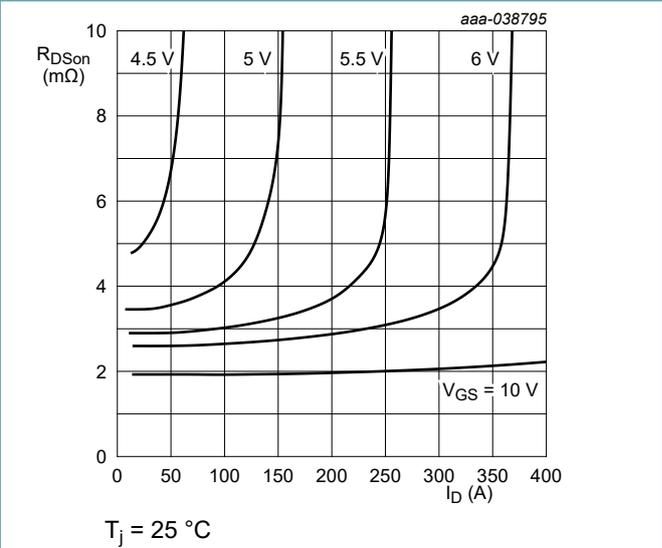


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

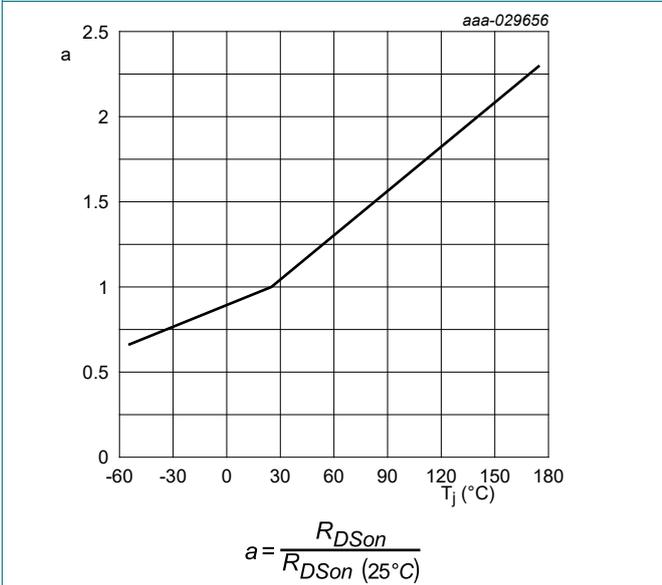


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

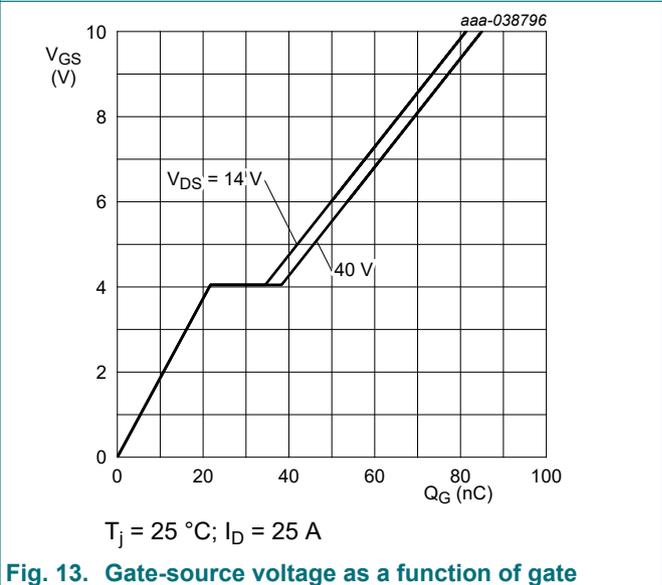


Fig. 13. Gate-source voltage as a function of gate charge; typical values

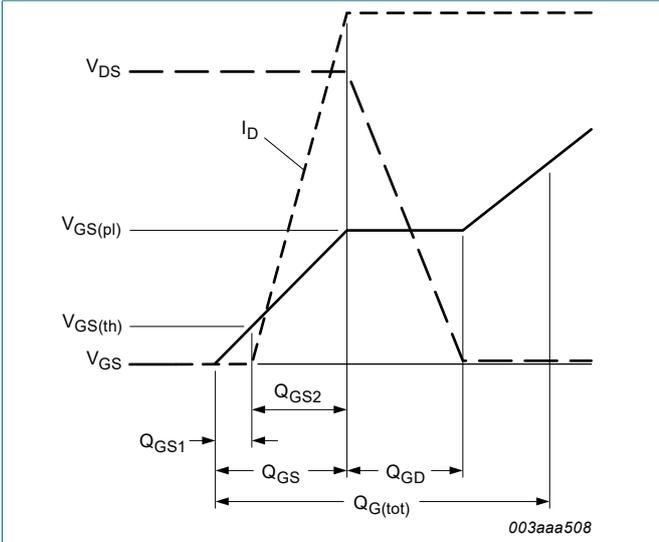


Fig. 14. Gate charge waveform definitions

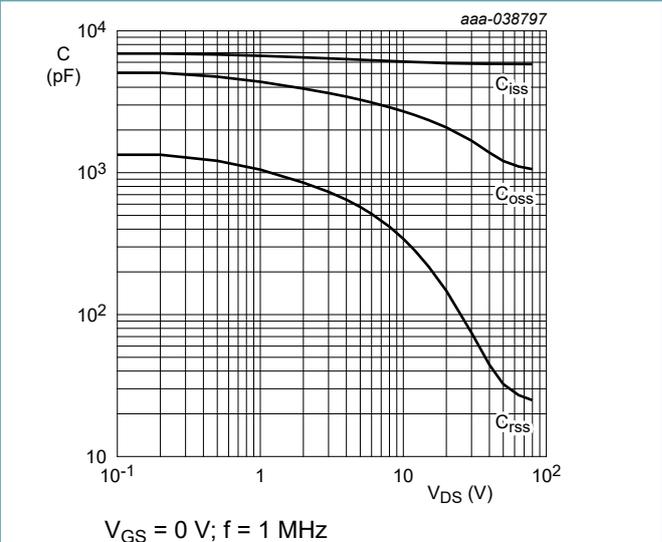


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

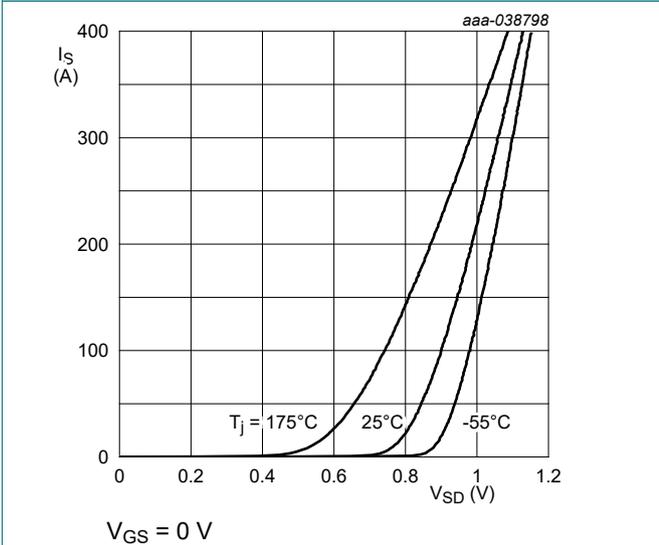


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

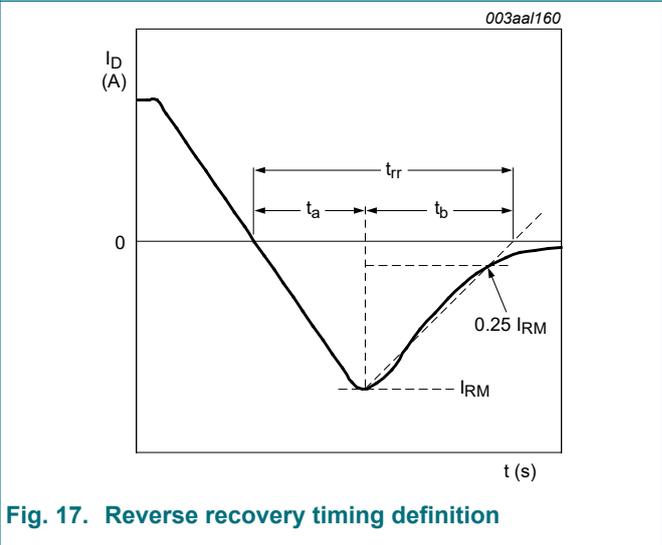


Fig. 17. Reverse recovery timing definition

11. Package outline

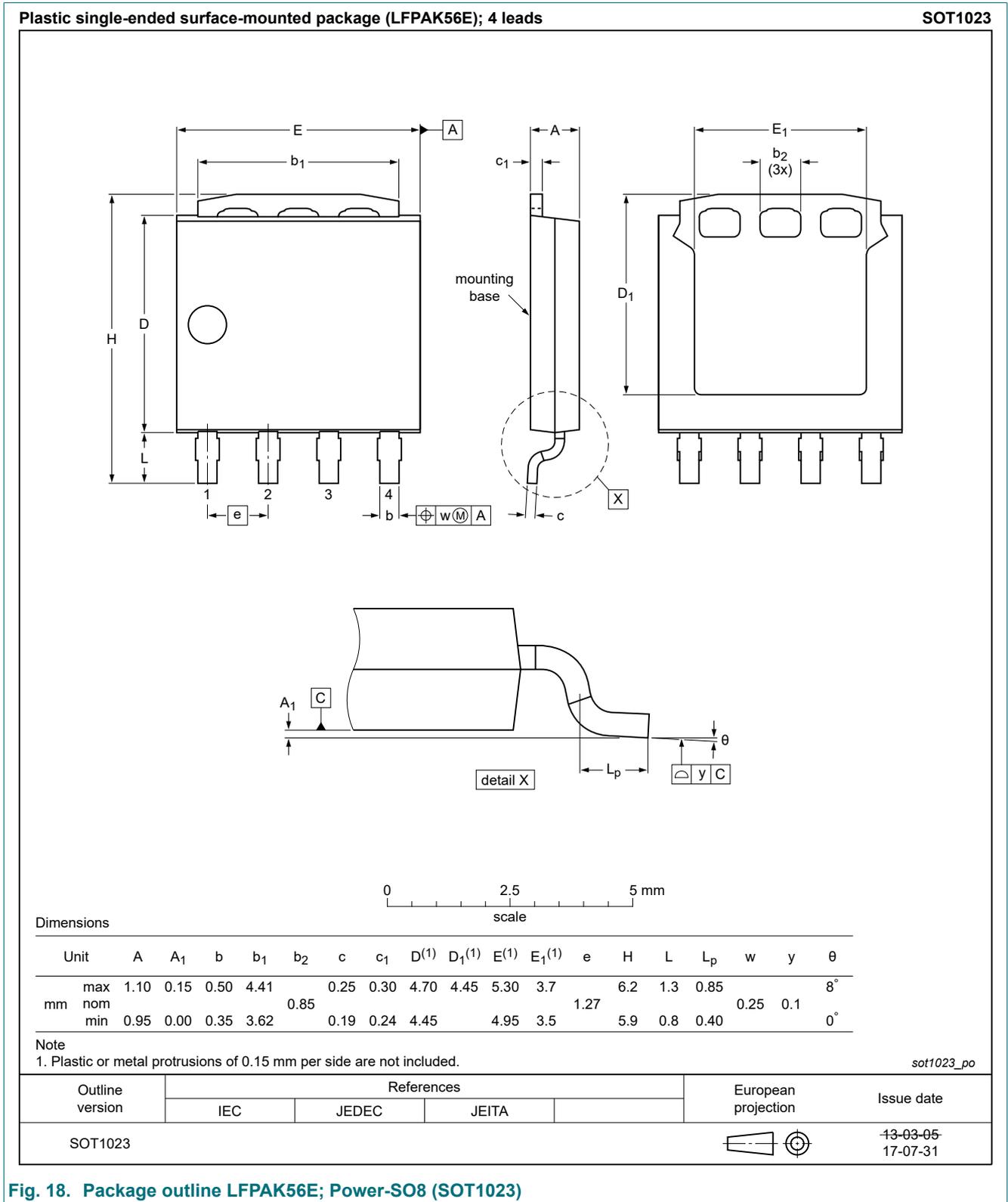


Fig. 18. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

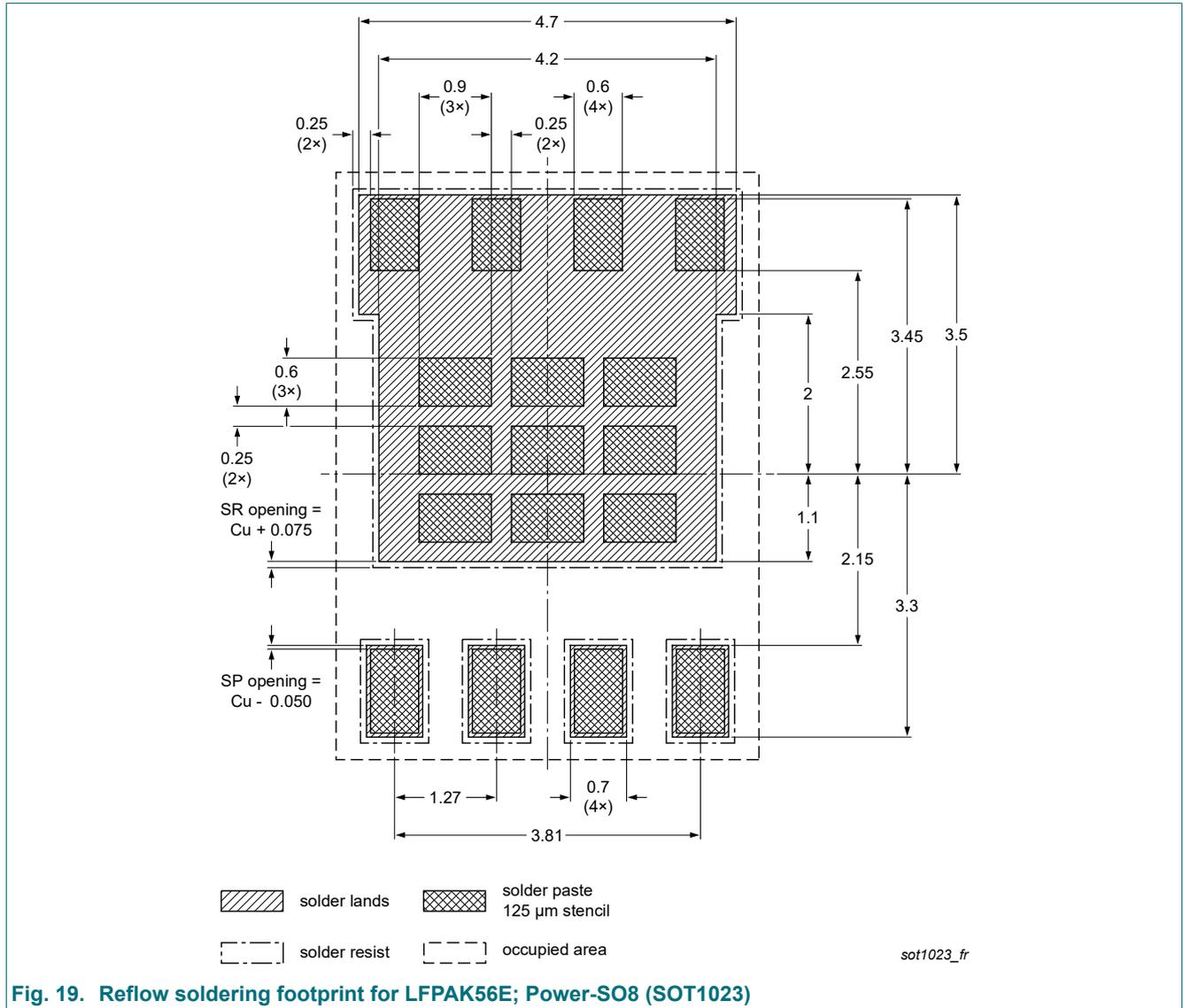


Fig. 19. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
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