Bridgetek Pte Ltd

MN820 BT820 Mini Module Datasheet

1 Introduction

The MN820 is a development module featuring Bridgetek's 5th generation embedded video engine (EVE) BT820. Combined with the VM820C development baseboard, it demonstrates the BT820's features, allowing developers to evaluate the IC's performance and functionality.

The MN820 mini module integrates a 1Gbit DDR3L memory and the BT820 chip, along with a DC-DC buck converter that powers the onboard memory independently, enabling operation with a single power source.

Developers can seamlessly integrate the BT820 into their products by using the MN820 and connecting it via a 100-pin board-to-board connector. This approach reduces development time and eliminates the complexity of designing high-speed DDR3 sub-system, allowing for a low cost PCB implementation.

When paired with the VM820C baseboard, which includes power and audio circuits, a USB-QSPI bridging IC, and IO connectors, developers can easily communicate with external devices and fully utilize BT820's capabilities.

1.1 Features

- 5th generation EVE controller BT820
- On-board 1Gbit DDR3L SDRAM
- Integrated DC-DC step-down converter for DDR3L interface
- Easy to use 100-pin high-speed board-to-board connector
- Single 3.3V power supply

2 Ordering Information

Part No.	Description
MN820	BT820 Mini Module, with on-board 1Gbit DDR3L SDRAM

Table 1 - Ordering Information

Table of Contents

3 Hardware Description

3.1 MN820 System on Module

The MN820 is a four-layer PCB featuring double-sided component placement and a thickness of 1.6 mm. The dimensions of the PCBA are 49 mm x 29 mm x 3.74 mm.

Figure 1 - MN820 Module PCBA - Front View

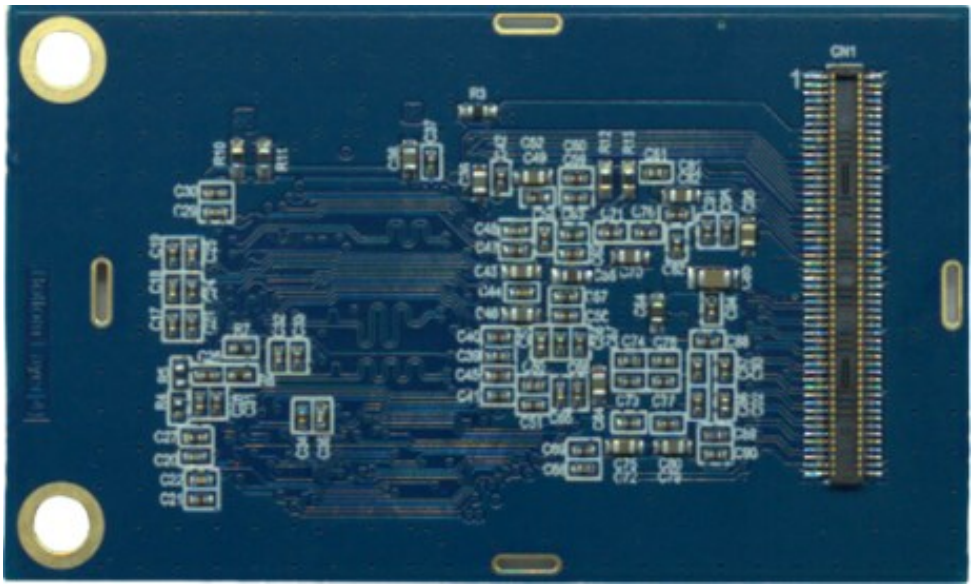

Figure 2 - MN820 Module PCBA - Back View

Key Features:

- Bridgetek's BT820 EVE chip for graphics, touch and audio controller
- 1Gbit DDR3L Memory IC with 667 MHz parallel interface
- Integrated DC-DC step-down converter
- 100-position high-speed board-to-board connector (plug) for connection to host controller board

3.2 Physical Descriptions

3.2.1 PCB Layout

The MN820 was designed with 100-ohm impedance trace control for both LVDS transmission and reception traces as well as 85-ohm impedance trace control for DDR3L differential clock and strobe signals.

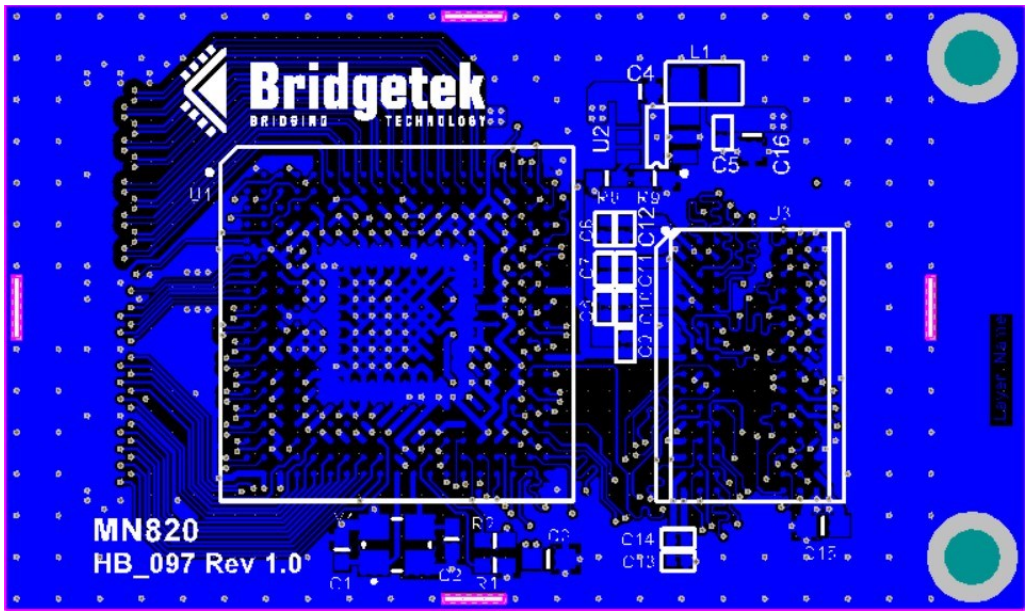

Figure 3 - Top Layer (Signal)

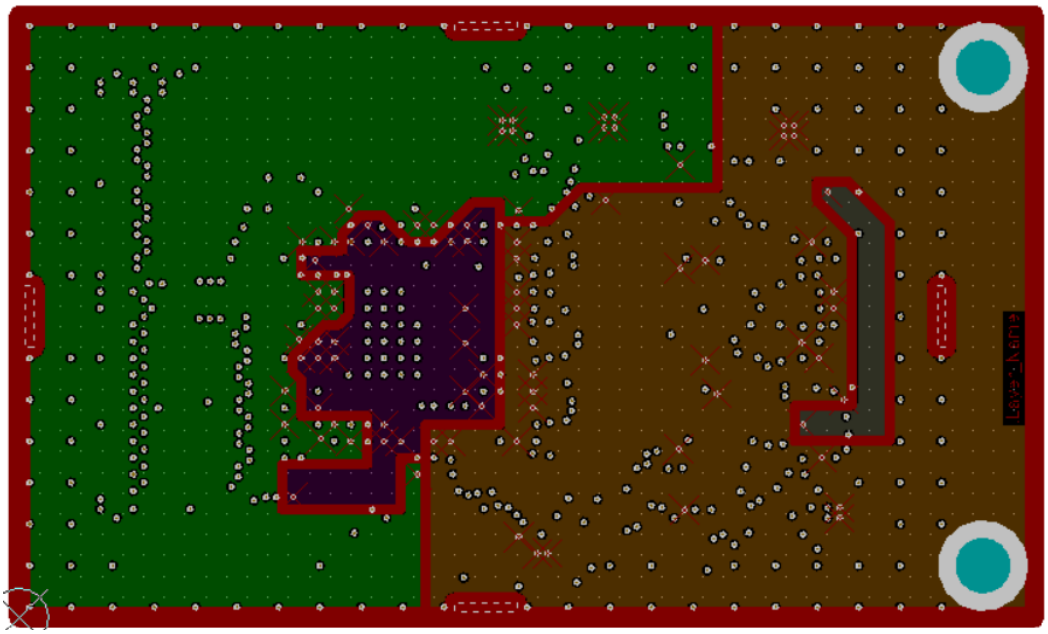

Figure 4 - Second Layer (Power)

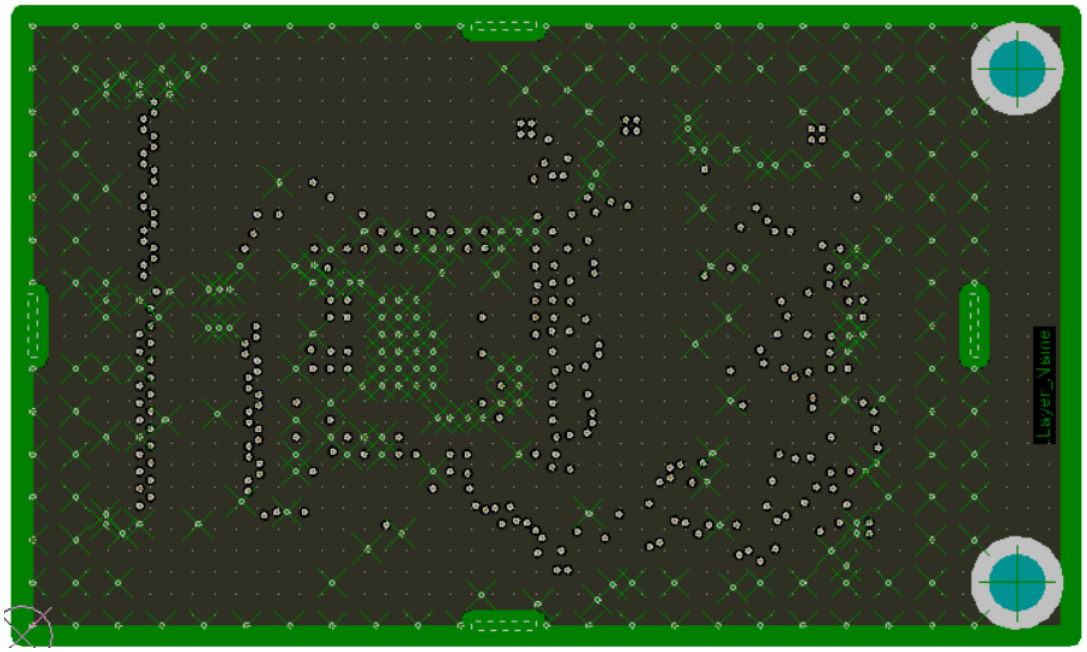

Figure 5 - Third Layer (Ground)

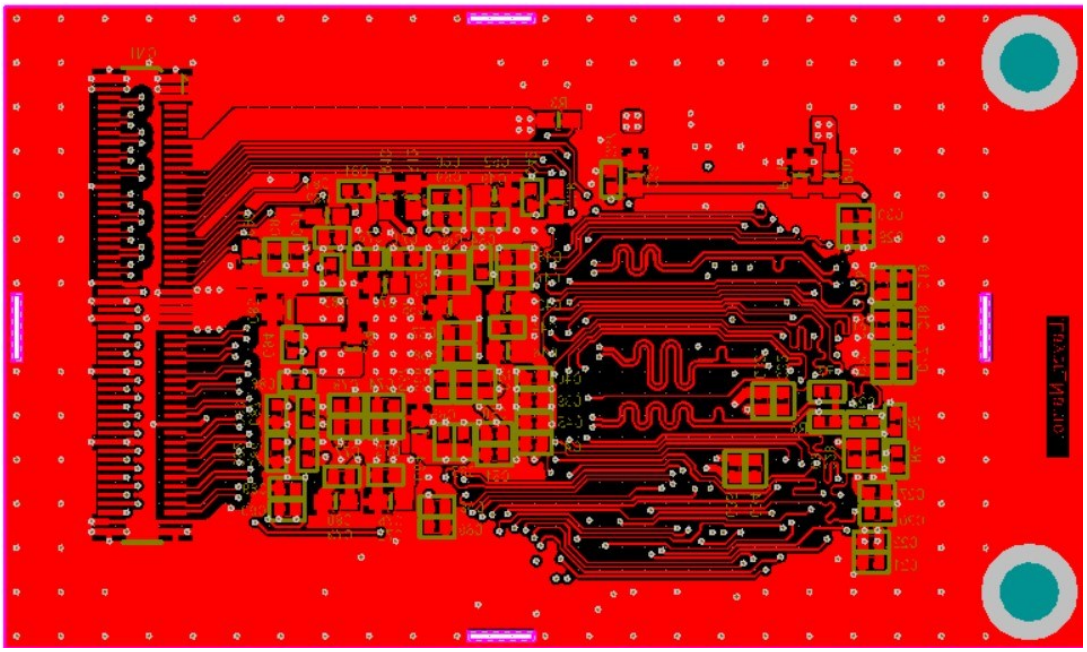

Figure 6 - Bottom Layer (Signal)

3.2.2 Decoupling Capacitor Placements

Using the BT820 EVE IC requires double-sided component placement due to its BGA package design. Most of the power pins are concentrated at the center of the IC, so decoupling capacitors for the BT820 were positioned directly beneath it, on the bottom side of the PCB. For the DDR3 memory, the power and ground pins are located along the edges of the IC. This allows designers the flexibility to place decoupling capacitors either on the same side or the bottom side of the PCB. In the VM820, decoupling capacitors for the memory are placed on both the top and bottom sides, with priority given to capacitors for Vref signals. Capacitors of 0402 size were chosen to minimize parasitic inductance and improve performance.

3.2.3 Controlled Impedance Signals

The VM820 mini module includes two sets of controlled impedance signal traces:

i. 85Ω ±10% for DDR3L data strobe and clock signals
ii. 100Ω ±10% for BT820 LVDS transmit and receive signals

Figure 7 to Figure 9 shows both sets of these controlled impedance signal traces.

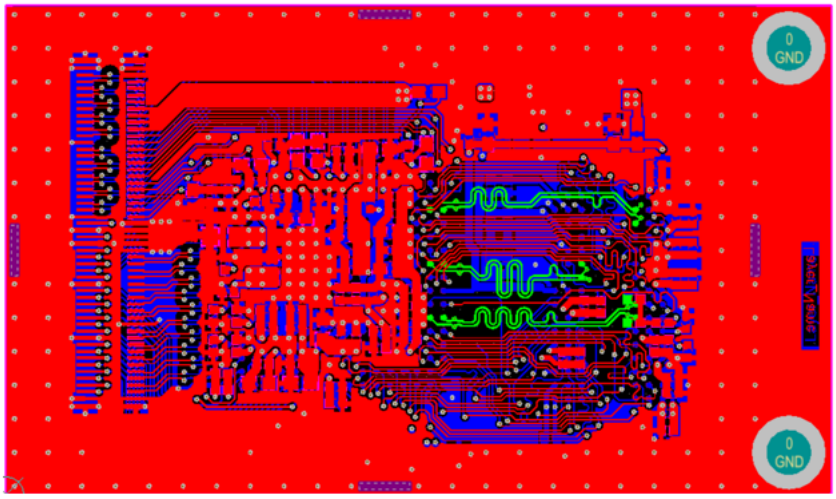

Figure 7 - 85Ω controlled impedance for memory strobe and clock signals

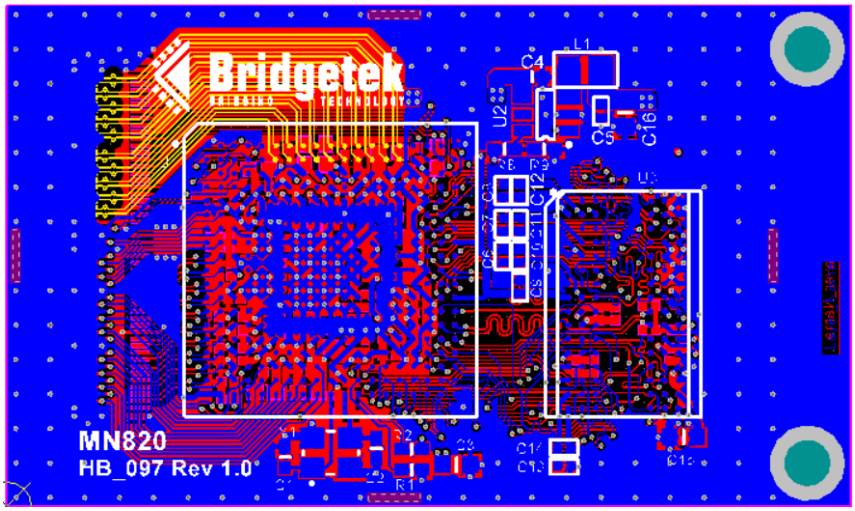

Figure 8 - 100Ω controlled impedance for LVDS receive signals

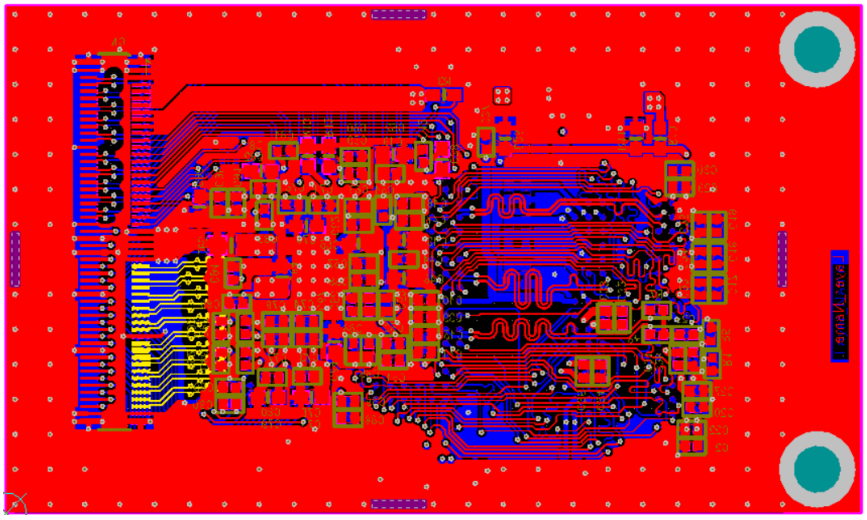

Figure 9 - 100Ω controlled impedance for LVDS transmit signals

3.2.4 DDR3L Routing

The design of DDR3L (Double Data Rate 3 Low Voltage) memory requires careful attention to PCB layout to ensure proper functionality and signal integrity. However, due to size constraints and the use of a single DDR3 memory IC in the MN820, only a subset of the complete DDR3L design guidelines was implemented:

1. **Differential Impedance:** Data strobe and clock differential traces, as illustrated in
2.
3.

Figure 7 - 85Ω controlled impedance for memory strobe and clock signals

4. , were routed with an impedance of 85Ω ±10%.
5. **Length Matching:** The mismatch between P and N traces of these differential pairs was kept within ±5 mils.
6. **Power and Ground Planes:** Solid power and ground planes were maintained beneath all DDR traces to provide stable reference layers.
7. **Byte Lane Trace Lengths:** The trace length deviation within a single data byte lane was limited to ±20 mils.

8. **Address/Command/Control Signals:** The trace length deviation between address, command, and control signals relative to the CK/CKB signals was limited to a maximum of ±25 mils.

9. **Via Limitation:** All signal traces were routed with a maximum of two vias to minimize signal degradation.

3.2.5 MN820 Connector

CN1 – SoM Baseboard Interconnector

This dual row 100-position 0.4mm pitch board-to-board connector serves as the interface between the MN820 System on Module (SoM) and VM820C baseboard. This USB4 Gen.2 connector, model "DF40C-100DP-0.4V (51)" from Hirose, supports data transmission speeds of up to 20 Gbps.

Pin No.	Name	Type	Description
1	GND	P	Ground
2	GND	P	Ground
3	GND	P	Ground
4	LVDS_RX0_D0_N	I	LVDS RX odd channel data bit 0
5	NC	NA	No Connection
6	LVDS_RX0_D0_P	I	LVDS RX odd channel data bit 0
7	NC	NA	No Connection
8	LVDS_RX0_D1_N	I	LVDS RX odd channel data bit 1
9	NC	NA	No Connection
10	LVDS_RX0_D1_P	I	LVDS RX odd channel data bit 1
11	NC	NA	No Connection
12	LVDS_RX0_D2_N	I	LVDS RX odd channel data bit 2
13	VCC3V3	P	3.3V output power supply
14	LVDS_RX0_D2_P	I	LVDS RX odd channel data bit 2
15	VCC3V3	P	3.3V output power supply
16	LVDS_RX0_CLK_N	I	LVDS RX odd channel clock differential N
17	VCC3V3	P	3.3V output power supply
18	LVDS_RX0_CLK_P	I	LVDS RX odd channel clock differential P
19	VCC3V3	P	3.3V output power supply
20	LVDS_RX0_D3_N	I	LVDS RX odd channel data bit 3
21	SD_CD	I	SD Card: Card Detect
22	LVDS_RX0_D3_P	I	LVDS RX odd channel data bit 3
23	SD_D0	I/O	SD Card: Data bus line 0
24	GND	P	Ground
25	SD_D1	I/O	SD Card: Data bus line 1
26	LVDS_RX1_D0_N	I	LVDS RX even channel data bit 0
27	SD_D2	I/O	SD Card: Data bus line 2
28	LVDS_RX1_D0_P	I	LVDS RX even channel data bit 0
29	SD_D3	I/O	SD Card: Data bus line 3
30	LVDS_RX1_D1_N	I	LVDS RX even channel data bit 1
31	SD_CLK	O	SD Card: Serial clock output
32	LVDS_RX1_D1_P	I	LVDS RX even channel data bit 1
33	SD_CMD	I/O	SD Card: Command signal
34	LVDS_RX1_D2_N	I	LVDS RX even channel data bit 2
35	SPIM_MOSI	I/O	SPI flash MOSI line
36	LVDS_RX1_D2_P	I	LVDS RX even channel data bit 2
37	SPIM_MISO	I/O	SPI flash MISO line

38	LVDS_RX1_CLK_N	I	LVDS RX even channel clock differential N
39	SPIM_IO3	I/O	SPI flash IO3 line
40	LVDS_RX1_CLK_P	I	LVDS RX even channel clock differential P
41	SPIM_IO2	I/O	SPI flash IO2 line
42	LVDS_RX1_D3_N	I	LVDS RX even channel data bit 3
43	SPIM_SS_N	O	SPI flash chips select output line
44	LVDS_RX1_D3_P	I	LVDS RX even channel data bit 3
45	SPIM_SCLK	O	SPI flash clock output line
46	GND	P	Ground
47	GND	P	Ground
48	AUDIO_R	O	Audio Sigma-delta right output
49	GND	P	Ground
50	GND	P	Ground
51	GND	P	Ground
52	AUDIO_L	O	Audio Sigma-delta left output
53	GND	P	Ground
54	GND	P	Ground
55	GND	P	Ground
56	I2S_LRCLK	I	I2S left/right clock indicator
57	LVDS_TX0_D0_N	O	LVDS TX odd channel data bit 0
58	I2S_BCLK	I	I2S bit clock
59	LVDS_TX0_D0_P	O	LVDS TX odd channel data bit 0
60	I2S_SDA	O	I2S serial data output
61	LVDS_TX0_D1_N	O	LVDS TX odd channel data bit 1
62	DISP	O	LCD Display general purpose control
63	LVDS_TX0_D1_P	O	LVDS TX odd channel data bit 1
64	BKLIT_PWM	O	LED backlight brightness PWM control
65	LVDS_TX0_D2_N	O	LVDS TX odd channel data bit 2
66	GND	P	Ground
67	LVDS_TX0_D2_P	O	LVDS TX odd channel data bit 2
68	GPIO3	I/O	General purpose IO 3
69	LVDS_TX0_CLK_N	O	LVDS TX odd channel clock differential N
70	GPIO2	I/O	General purpose IO 2
71	LVDS_TX0_CLK_P	O	LVDS TX odd channel clock differential P
72	GPIO4	I/O	General purpose IO 4
73	LVDS_TX0_D3_N	O	LVDS TX odd channel data bit 3
74	GPIO6	I/O	General purpose IO 6
75	LVDS_TX0_D3_P	O	LVDS TX odd channel data bit 3
76	GPIO5	I/O	General purpose IO 5
77	GND	P	Ground
78	GPIO7	I/O	General purpose IO 7
79	LVDS_TX1_D0_N	O	LVDS TX even channel data bit 0
80	GPIO8	I/O	General purpose IO 8
81	LVDS_TX1_D0_P	O	LVDS TX even channel data bit 0
82	GND	P	Ground
83	LVDS_TX1_D1_N	O	LVDS TX even channel data bit 1

84	SPIS_MISO	I/O	SPI data line 1
85	LVDS_TX1_D1_P	O	LVDS TX even channel data bit 1
86	SPIS_SCLK	I	SPI clock input
87	LVDS_TX1_D2_N	O	LVDS TX even channel data bit 2
88	SPIS_SS_N	I	SPI slave select input
89	LVDS_TX1_D2_P	O	LVDS TX even channel data bit 2
90	SPIS_MOSI	I/O	SPI data line 0
91	LVDS_TX1_CLK_N	O	LVDS TX even channel clock differential N
92	SPIS_IO3	I/O	SPI data line 3
93	LVDS_TX1_CLK_P	O	LVDS TX even channel clock differential P
94	SPIS_IO2	I/O	SPI data line 2
95	LVDS_TX1_D3_N	O	LVDS TX even channel data bit 3
96	INT_N	OD/O	Interrupt to host, active low
97	LVDS_TX1_D3_P	O	LVDS TX even channel data bit 3
98	RESET_N	I	Global reset pin.
99	GND	P	Ground
100	GND	P	Ground

Table 2 - CN1 Pinout

For a more detailed description of the SoM IO pins, please refer to the BT820 Datasheet.

4 Board Schematic

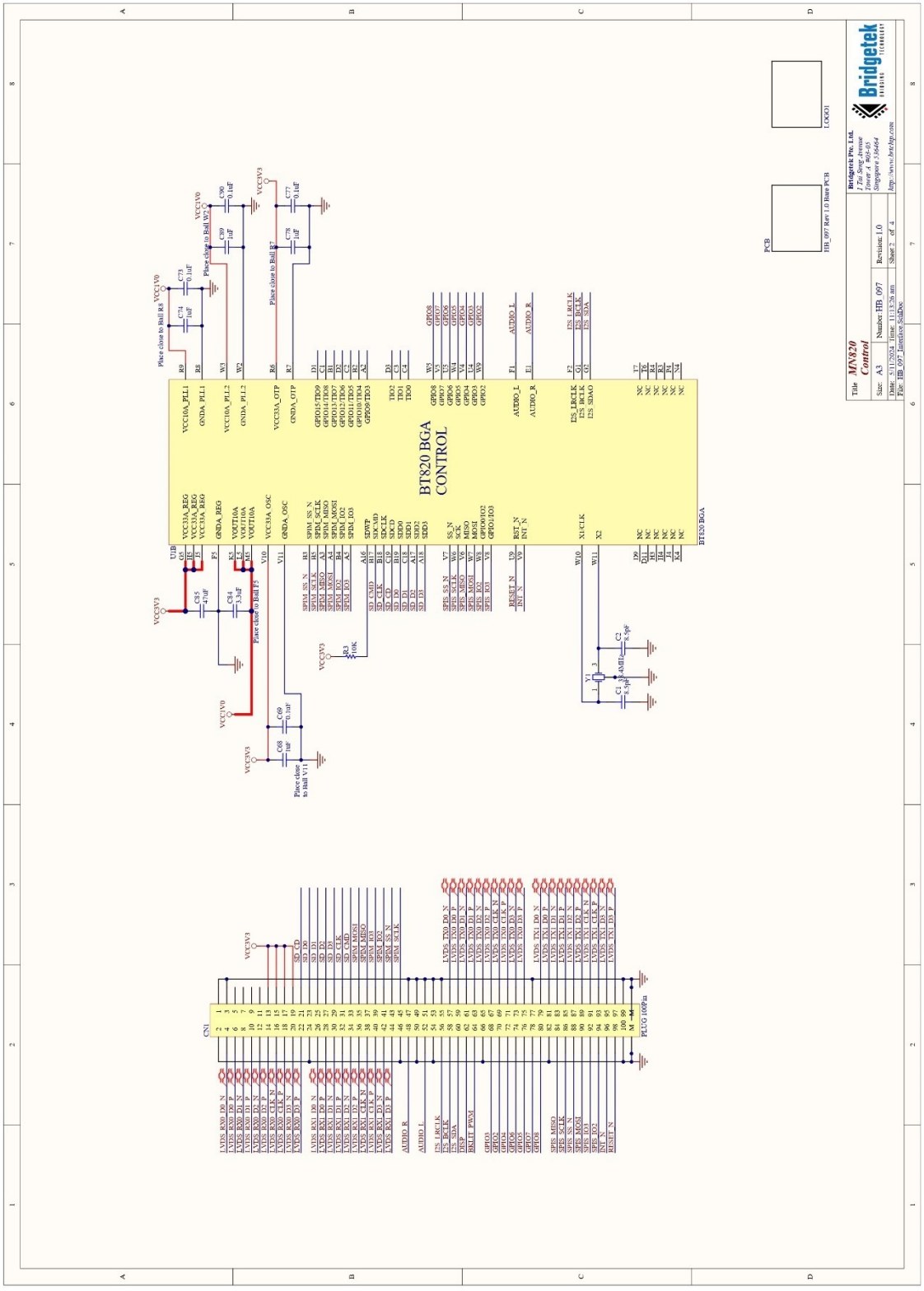

Figure 10 - Interface Connector & Control

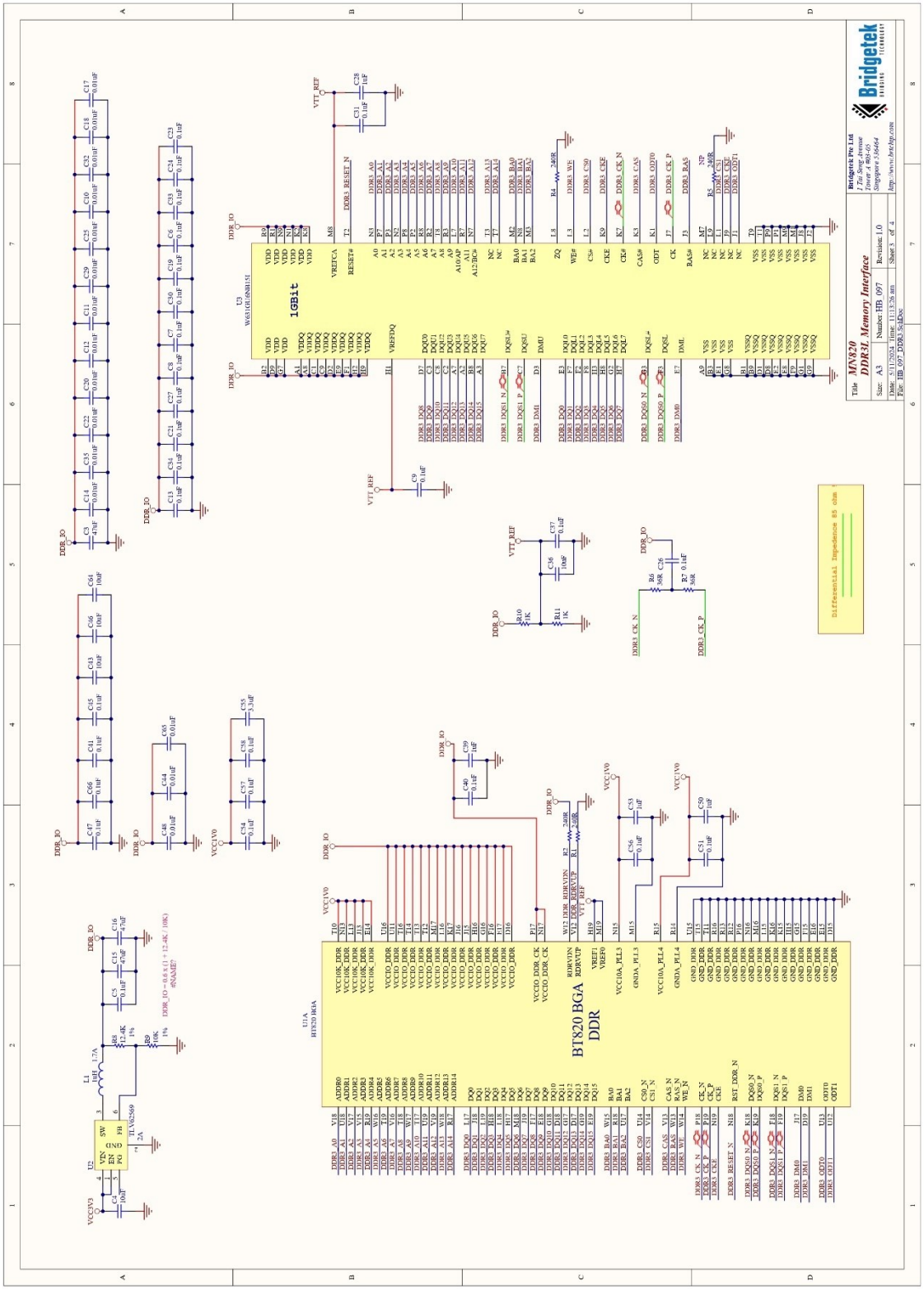

Figure 11 - DDR3L Memory

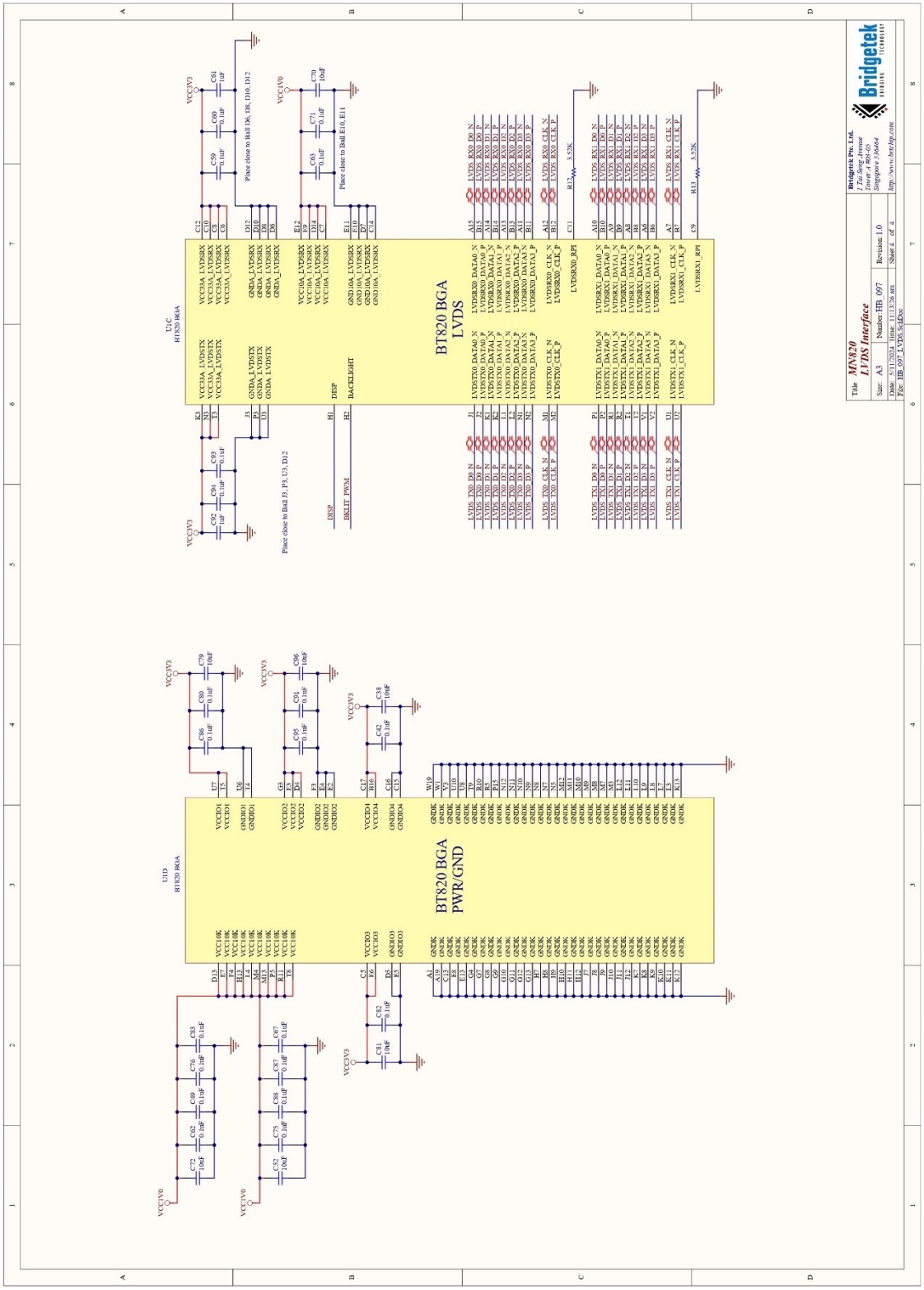

Figure 12 - LVDS Interface

5 Interface to MN820

5.1 Power

The MN820 SoM is a standalone module capable of generating its core and memory power from a single power source. It accepts an input voltage in the range of 3.0 to 3.6 volts and internally generates 1.1V for core operation and 1.35V for the onboard DDR3L memory.

5.2 Memory

The module integrates a 667MHz 1 Gbit DDR3L memory capable of running at speed rate of 133MT/s with data width of 16bits.

5.3 Interface Connector

The MN820 SoM connects to external components via a high-speed board-to-board connector. The selected connector, Hirose "DF40C-100DP-0.4V (51)", supports data transfer rates of up to 20 Gbps.

When paired with the VM820C baseboard, the module uses a Hirose "DF40C-100DS-0.4V (51)" connector, resulting in a stacking height of 1.5 mm. For applications requiring a higher stacking height, developers can opt for the "DF40HC (3.0)-100DS-0.4V" receptacle, which provides a stacking height of 3.0 mm.

5.4 EMI

The SoM features a designated footprint to accommodate an EMI shield measuring 44mm in length and 28mm in width. The minimum height of the shield should exceed 1.5mm to avoid contact with taller capacitors.

6 MN820 Hardware Setup

To facilitate the integration of the MN820 into their designs and products, developers can pair the SoM with Bridgetek's VM820C module—a baseboard specifically designed to complement the MN820. Using the VM820C, developers can explore the operation of the BT820 EVE IC, evaluate its performance, and assess its features through the baseboard's host interface options, audio and power circuits, and various I/O connectors.

This section provides a concise guide for setting up the MN820 with the VM820C for development purposes. Figure 13 - MN820 Setup
below illustrates the setup for BT820 development modules, configured to drive an LVDS display panel with active speakers and support of various host interface options.

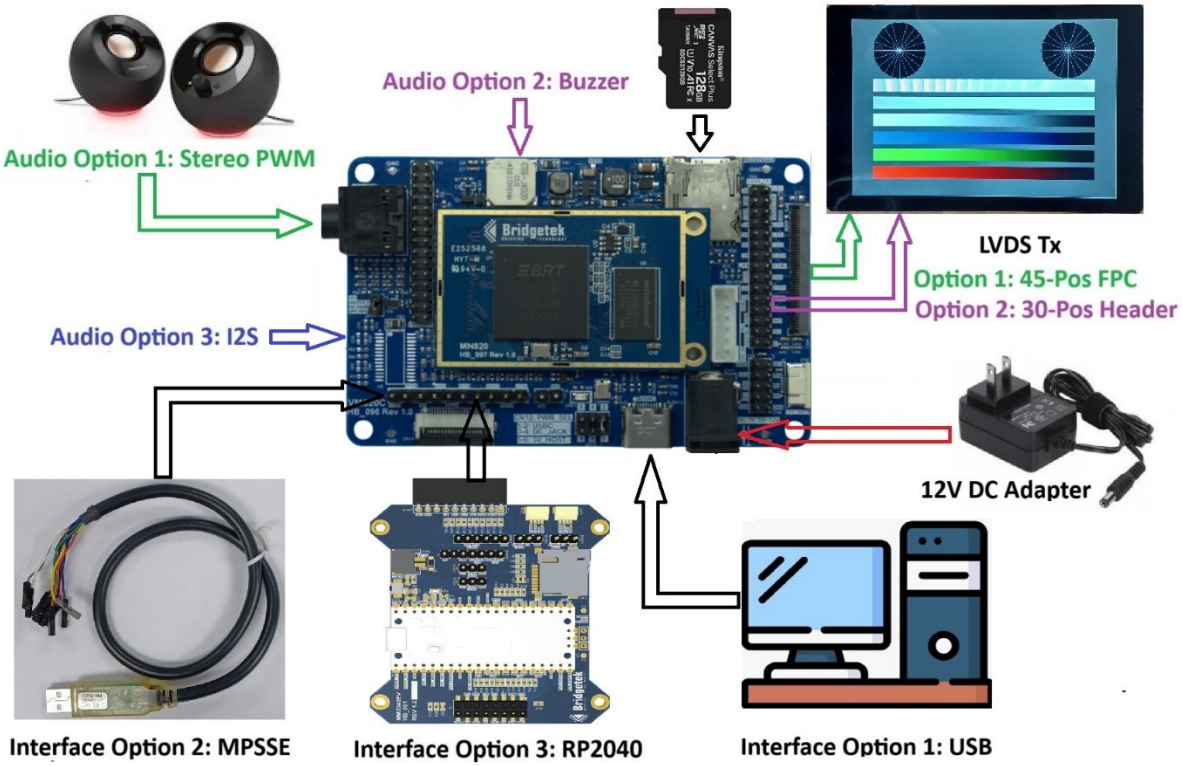

Figure 13 - MN820 Setup

When paired with the VM820C, the MN820 enables communication with external systems via the VM820C's USB and SPI/QSPI interface connectors.

With the VM820C's onboard Tx and Rx connectors, developers can connect LVDS LCD panels to the I/O connectors for data reception and display functionality.

The VM820C also features integrated audio systems, allowing developers to connect active speakers for BT820 PWM stereo audio. Additionally, it supports a buzzer circuit for testing BT820 built-in sound synthesizer, as well as an I2S digital audio interface with an onboard footprint catered for Texas Instruments PCM5121 DAC circuit.

For a detailed description of operating the MN820 and VM820C as a development kit, please refer to the VM820C datasheet.

7 Specifications

7.1 Electrical Specifications

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
VCC3V3	Output voltage range	3.0	3.3	3.6	V
Icc_3V3*Note	Operating current, VCC=3V3	-	245	-	mA
Voh	Output Voltage High	2.4	-	-	V
Vol	Output Voltage Low	-	-	0.4	V
Vih	Input High Voltage	2.0	-	-	V
Vil	Input Low Voltage	-	-	0.8	V
T	Operating temperature	-20	-	+70	℃

Table 3 - Operating Voltage and Current

Note: Operating current is measured while displaying a test card.

8 Mechanical Dimensions

8.1 MN820 PCB Dimensions

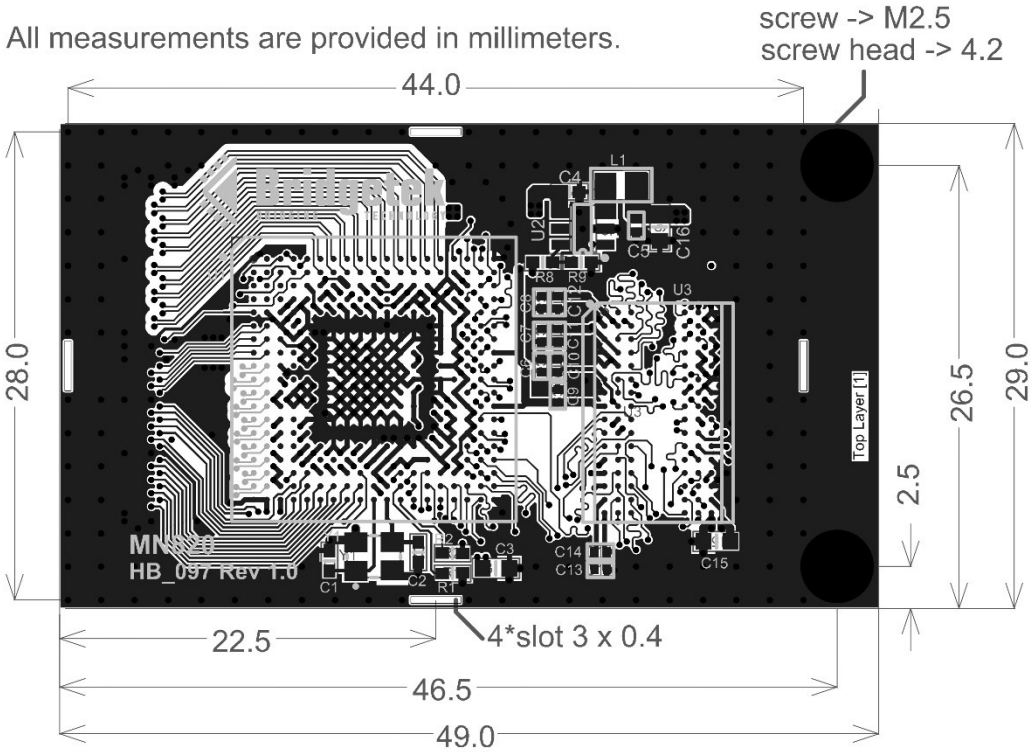

Figure 14 - MN820 PCBA Dimensions (Top View)

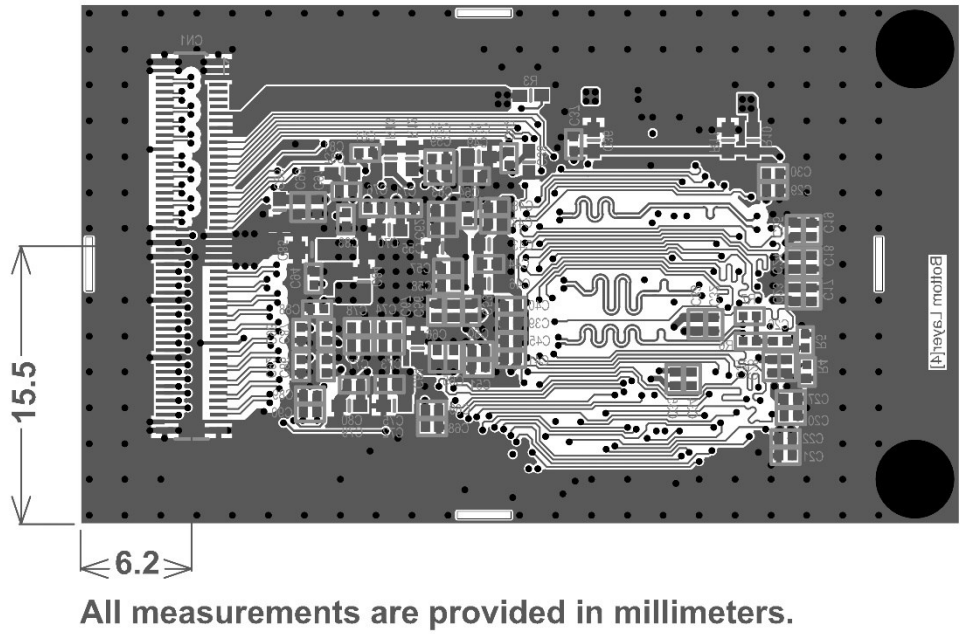

Figure 15 - MN820 PCBA Dimensions (Bottom View)

9 Contact Information

Refer to https://brtchip.com/contact-us/ for contact information.

Distributor and Sales Representatives

Please visit the Distribution Network – IC & Module (brtchip.com) page for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

BT820 Datasheet

Acronyms and Abbreviations

Terms	Description
DAC	Digital Analog Converter
DDR3L	Low Voltage Double Data Rate 3
EVE	Embedded Video Engine
IC	Integrated Circuit
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling
MPSSE	Multi-Purpose Synchronous Serial Engine
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembled
Rx	Receive
SoM	System On Module
Tx	Transmit
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

List of Tables

List of Figures

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Bridgetek:

MN820