Diotec Semiconductor

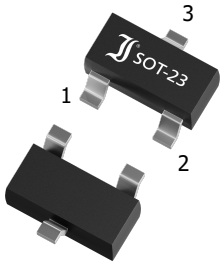
MMFTP2319

P-Channel Enhancement Mode FET
P-Kanal FET – Anreicherungstyp

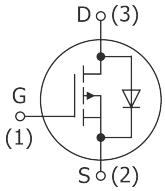
I_D = - 4.2 A
$R_{DS(on)}$ < 80 mΩ
T_{jmax} = 150°C
V_{DS} = - 40 V
P_{tot} = 750 mW

Version 2022-10-19

SOT-23
TO-236



SPICE Model & **STEP** File [1])



Marking Code
UJ

HS Code 85412100

Typical Applications
Signal processing
Battery management
Drivers
Logic level converter
Commercial / Industrial grade
Suffix -Q: AEC-Q101 compliant [1])
Suffix -AQ: in AEC-Q101 qualification [1])

Typische Anwendungen
Signalverarbeitung
Batteriemanagement
Treiberstufen
Logikpegelwandler
Standardausführung
Suffix -Q: AEC-Q101 konform [1])
Suffix -AQ: in AEC-Q101 Qualifikation [1])

Features
Fast switching times
Compliant to RoHS (w/o exemp.)
REACH, Conflict Minerals [1])

Besonderheiten
Schnelle Schaltzeiten
Konform zu RoHS (ohne Ausn.)
REACH, Konfliktmineralien [1])

Mechanical Data [1])

Taped and reeled	3000 / 7"	Gegurtet auf Rolle
Weight approx.	0.01 g	Gewicht ca.
Case material	UL 94V-0	Gehäusematerial
Solder & assembly conditions	260°C/10s	Löt- und Einbaubedingungen
	MSL = 1	

Mechanische Daten [1])

Maximum ratings [1]) **Grenzwerte [2])**

			MMFTP2319
Drain-Source-voltage Drain-Source-Spannung		$-V_{DS}$	40 V
Gate-Source-voltage Gate-Source-Spannung	D open	V_{GSO}	± 20 V
Power dissipation Verlustleistung		P_{tot}	750 mW [2])
Drain current Drainstrom	DC	$-I_D$	4.2 A
Peak Drain current Drain-Spitzenstrom		$-I_{DM}$	30 A
Junction temperature – Sperrschichttemperatur Storage temperature – Lagerungstemperatur		T_j T_S	-55...+150°C -55...+150°C

1 Please note the detailed information on our website or at the beginning of the data book
Bitte beachten Sie die detaillierten Hinweise auf unserer Internetseite bzw. am Anfang des Datenbuches
1 T_A = 25°C, unless otherwise specified – T_A = 25°C, wenn nicht anders angegeben
2 Mounted on P.C. board with 6.45 cm² copper pad at each terminal
Montage auf Leiterplatte mit 6,45 cm² Kupferbelag (Lötpad) an jedem Anschluss

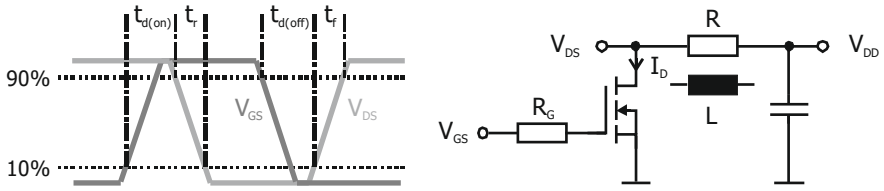
Characteristics (static) **Kennwerte (statisch)**

		T_j = 25°C	Min.	Typ.	Max.
Drain-Source breakdown voltage – Drain-Source-Durchbruchspannung - I_D = 250 µA		- $V_{(BR)DSS}$	40 V	–	–
Drain-Source leakage current – Drain-Source-Leckstrom - V_{DS} = 40 V		- I_{DSS}	–	–	1 µA
Gate-Source leakage current – Gate-Source-Leckstrom V_{GS} = ± 20 V		I_{GSS}	–	–	± 100 nA
Gate-Source threshold voltage – Gate-Source Schwellspannung V_{GS} = V_{GS}, - I_D = 1 mA		- $V_{GS(th)}$	1 V	–	3 V
Drain-Source on-state resistance – Drain-Source Einschaltwiderstand - V_{GS} = 10 V, - I_D = 3.1 A - V_{GS} = 4.5 V, - I_D = 2.6 A		$R_{DS(on)}$	–	–	80 mΩ 120 mΩ

Characteristics (dynamic) **Kennwerte (dynamisch)**

Forward Transfer Admittance – Übertragungssteilheit - V_{DS} = 10 V, - I_D = 4.2 A		g_{fs}	–	7.6 S	–
Input Capacitance – Eingangskapazität - V_{DS} = 20 V, f = 1 MHz		C_{iss}	–	1179 pF	–
Output Capacitance – Ausgangskapazität - V_{DS} = 20 V, f = 1 MHz		C_{oss}	–	82 pF	–
Reverse Transfer Capacitance – Rückwirkungskapazität - V_{DS} = 20 V, f = 1 MHz		C_{rss}	–	40 pF	–
Turn-On Time – Anstiegszeit -V_{GS} = 10 V, -V_{DD} = 20 V, -I_D = 4.2 A, R_G = 6 Ω	(Fig. 1)	$t_{d(on)}$ t_r	–	15 ns 28 ns	–
Turn-Off Time – Abfallzeit -V_{GS} = 0 V, -V_{DD} = 20 V, -I_D = 4.2 A, R_G = 6 Ω	(Fig. 1)	$t_{d(off)}$ t_f	–	19 ns 4 ns	–
Total Gate Charge – Gesamte Gate-Ladung -V_{GS} = 10 V, -V_{DD} = 20 V, -I_D = 4.2 A		Q_g	–	20 nC	–
Gate-Source Charge – Gate-Source-Ladung -V_{GS} = 10 V, -V_{DD} = 20 V, -I_D = 4.2 A		Q_{gs}	–	4 nC	–
Gate-Drain Charge – Gate-Drain-Ladung -V_{GS} = 10 V, -V_{DD} = 20 V, -I_D = 4.2 A		Q_{gd}	–	2.6 nC	–
Intrinsic Gate resistance – Innerer Gatewiderstand f = 1 Mhz D open		R_{Gi}	–	4.6 Ω	–

Fig. 1
Test circuit for switching times (R) and avalanche energy (L)
("rise" and "fall" refer to I_D)
Testaufbau für Schaltzeiten (R) und Avalanche-Energie (L)
("rise" und "fall" beziehen sich auf I_D)



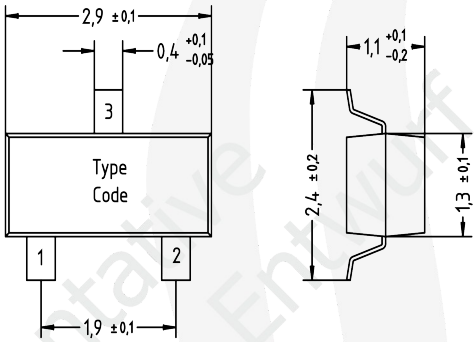
Characteristics (diode) **Kennwerte (Diode)**

		T_j = 25°C	Min.	Typ.	Max.
Forward voltage – Durchlass-Spannung					
V_{GS} = 0 V	$-I_S$ = 1.3 A	$-V_{SD}$	–	–	1.2 V
Reverse recovery time – Sperrverzugszeit					
I_S = 4.2 A,	di/dt = -100 A/µs	t_{rr}	–	13.3 ns	–
Reverse recovery charge – Sperrverzugsladung					
I_S = 4.2 A,	di/dt = -100 A/µs	Q_{rr}	–	8.5 nC	–

Characteristics (thermal) **Kennwerte (thermisch)**

Thermal resistance junction to ambient Wärmewiderstand Sperrschicht – Umgebung	t = 5 s Steady State	R_{thA}	< 100 K/W < 166 K/W [1])

Dimensions – Maße [mm]



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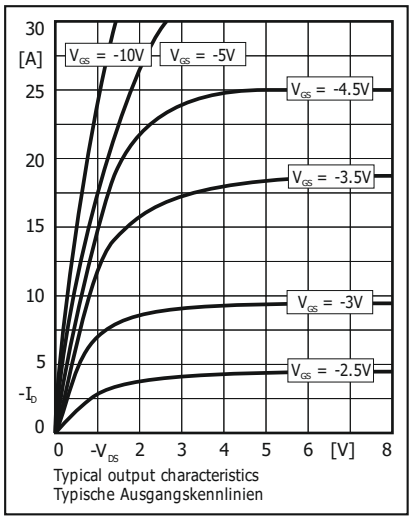
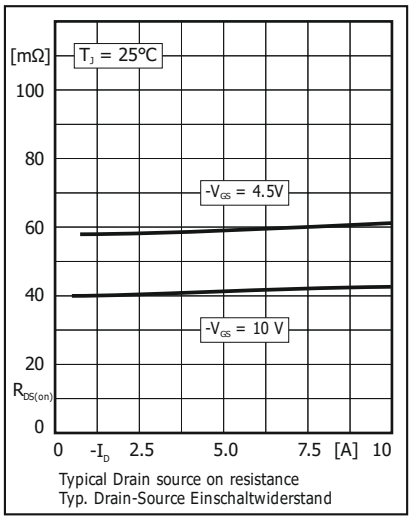
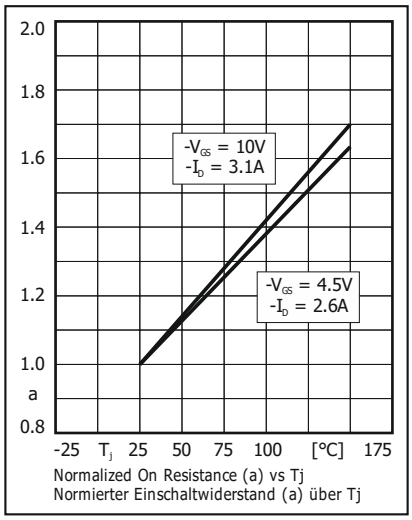


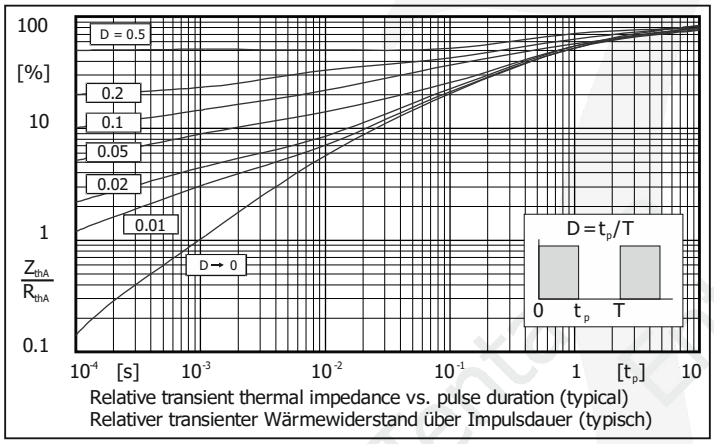
Typical output characteristics
Typische Ausgangskennlinien



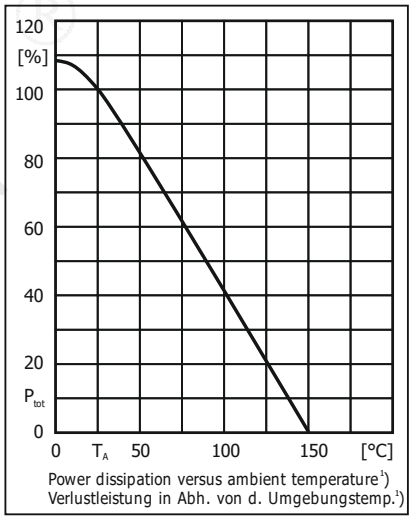
Typical Drain source on resistance
Typ. Drain-Source Einschaltwiderstand



Normalized On Resistance (a) vs Tj
Normierter Einschaltwiderstand (a) über Tj



Relative transient thermal impedance vs. pulse duration (typical)
Relativer transienter Wärmewiderstand über Impulsdauer (typisch)



Power dissipation versus ambient temperature[1])
Verlustleistung in Abh. von d. Umgebungstemp.[1])

Disclaimer: See data book page or website
Haftungssauschluss: SieheDatenbuch Seite 2 oder Internet