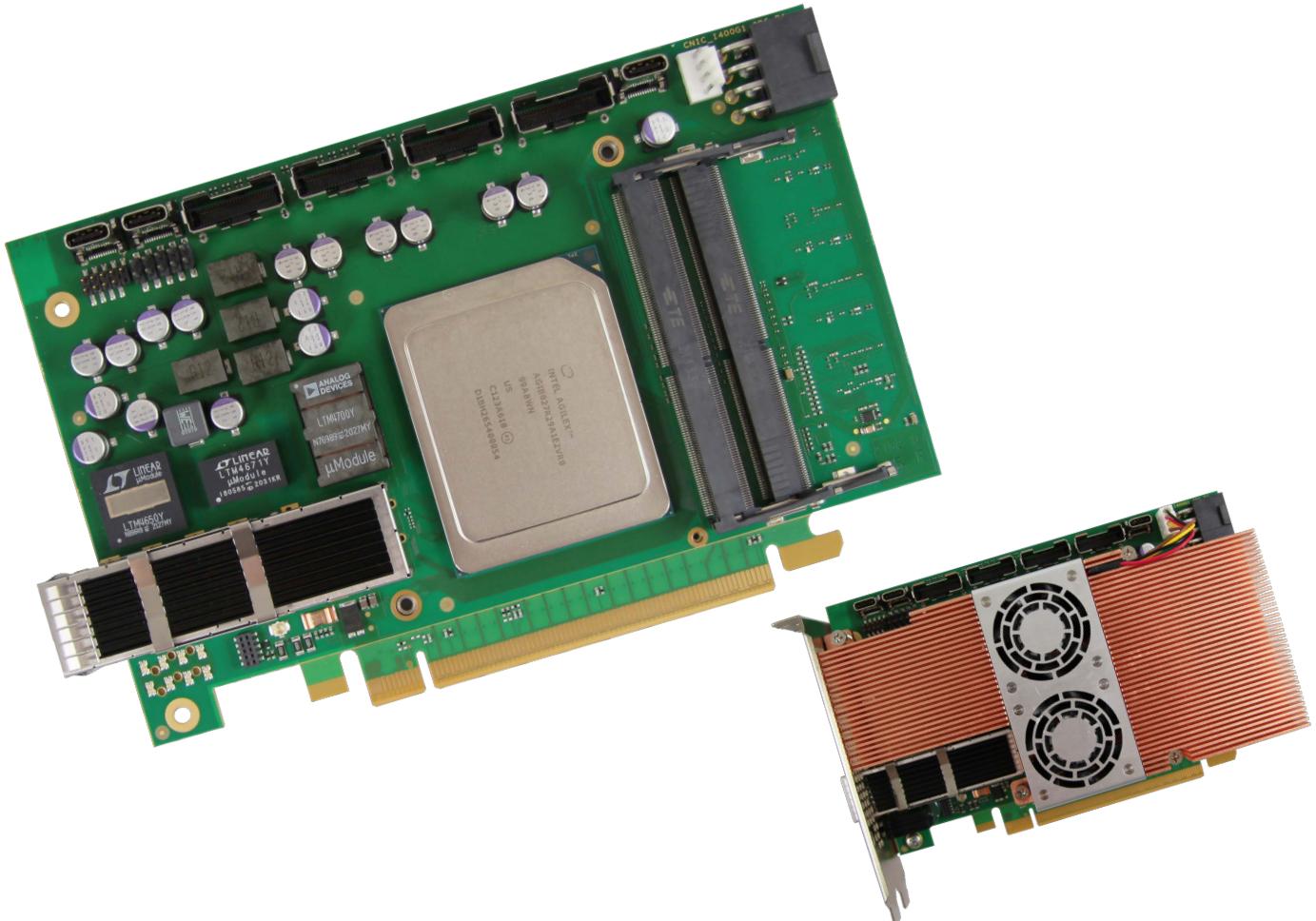


# XpressSX AGI-FH400G

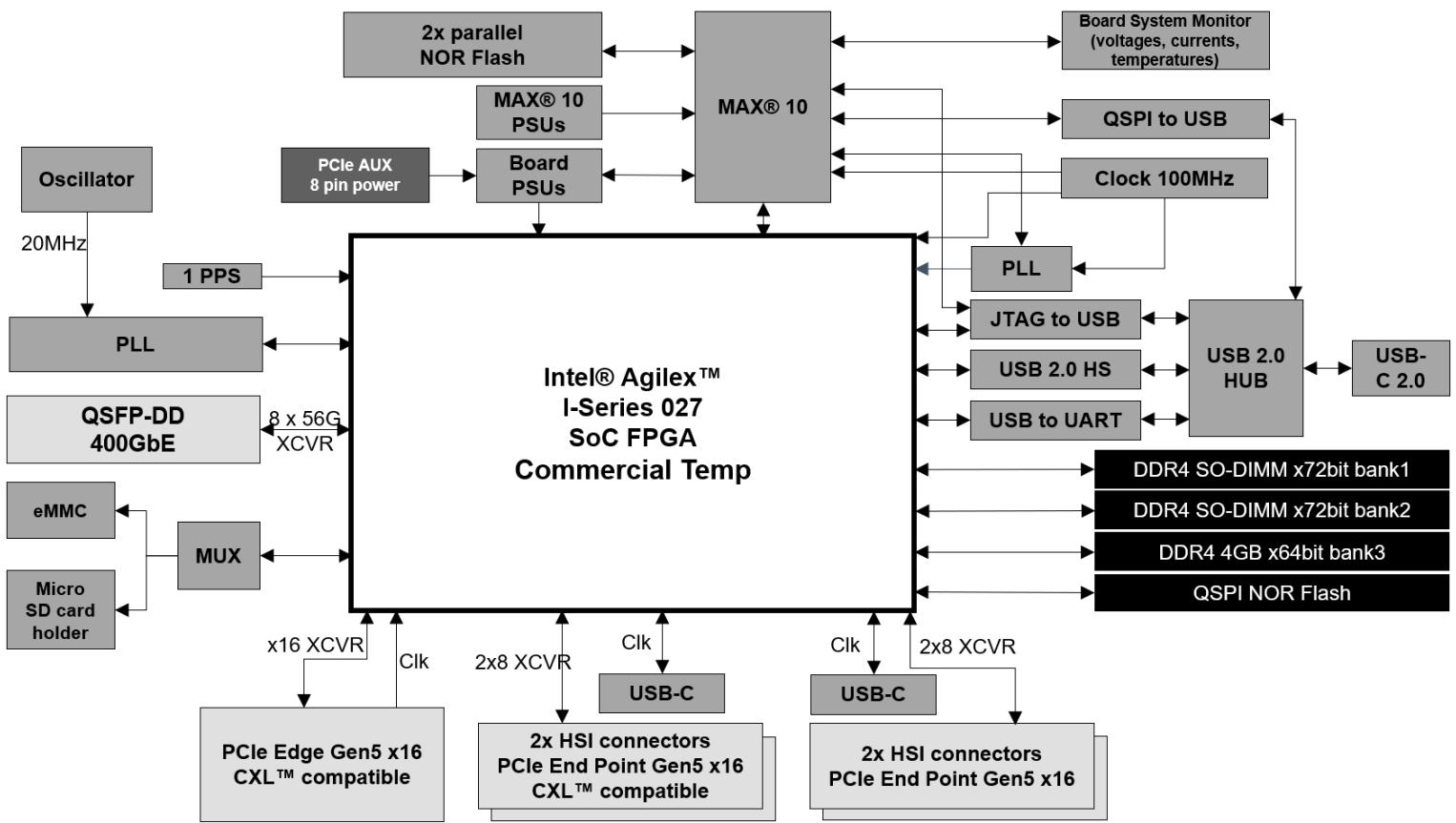
Full height, half length PCIe Gen5 Network Processing board



- Intel® Agilex™ I-Series SoC
- Quad Core ARM® Cortex® A53
  - 2700 KLE
- PCIe Edge Gen5 x16, CXL™

- 400GbE (8 x 56)
- 3x DDR4
- 4x HSI connectors (PCIe Gen5 x16 EP)

- Security
- SmartNIC
- Networking Acceleration



## Full Specifications

FPGA Configuration	<ul style="list-style-type: none"> <li>Intel® Agilex™ I-Series : AGIB027R29A1E2V including SoC: Quad Core ARM® Cortex® A53</li> </ul> <p>SoC support for the Production Silicon version 400GT only</p> <ul style="list-style-type: none"> <li>Flash configuration</li> <li>USB 2.0 Hub for JTAG, UART, BMC, USB2</li> </ul>	Board Dimensions	<ul style="list-style-type: none"> <li>Full height half length: 167.7mm x 111.15mm</li> </ul>
Memory	<ul style="list-style-type: none"> <li>1x on-board DDR4 (mutual SoC / FPGA), x64 bit bus, 4GBytes up to 2666 MT/s</li> <li>2x DDR4 SO-DIMM sockets, each capable up to 32GBytes SO-DIMM, with ECC</li> <li>eMMC or SD Card holder (if used) for SoC</li> </ul>	Communication Interfaces	<ul style="list-style-type: none"> <li>PCIe Edge Gen5 x16</li> <li>CXL™ standard compatible*: <ul style="list-style-type: none"> <li>Open standard interconnection for high-speed CPU-to-device and CPU-to-memory</li> <li>Built on the PCIe physical and electrical interface</li> </ul> </li> <li>8x QSFP56-DD (8x 56G: 400G total)</li> <li>2x HSI connectors (ARF6-16-L-RA): Total of 16 transceivers for PCIe Gen5 EP, CXL™ standard compatible</li> <li>2x HSI connectors (ARF6-16-L-RA): Total of 16 transceivers for PCIe Gen5 EP</li> <li>2x USB-C connectors for HSI Clocks &amp; control signals</li> </ul>
Power	<ul style="list-style-type: none"> <li>200W max, delivered with 2-slot active heatsink</li> <li>Powered by the PCIe slot and an 8 pin PCIe Aux ATX external connector (additional power)</li> </ul>	Other Resources	<ul style="list-style-type: none"> <li>Board Management Controller (MAX®10 device)</li> <li>Programmable PLL</li> </ul>
Operating Range	<ul style="list-style-type: none"> <li>0°C to 35°C</li> </ul>	Standards and Compliance	<ul style="list-style-type: none"> <li>RoHS/REACH compliant</li> <li>UL certified</li> <li>ISO9001 certified</li> </ul>
Storage Range	<ul style="list-style-type: none"> <li>0°C to 70°C</li> </ul>		

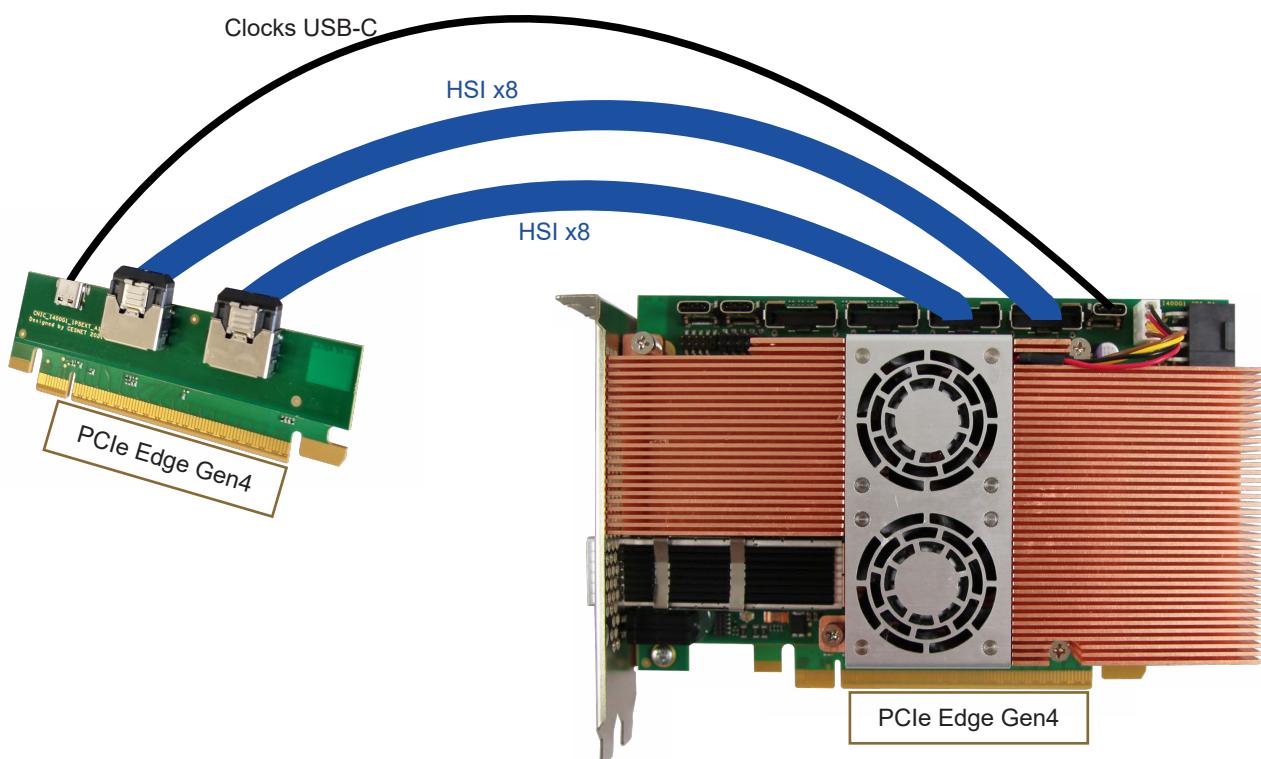
\*Use of CXL™ features might require separate CXL™ IP license purchase. Please contact Intel® for details.

## Additional PCIe Gen4 x16 daughter

The XpressSX AGI-FH400G board needs to be inserted in a PCIe Gen5 compatible server in order to deliver the full PCIe Gen5 x16 performances.

In case the user is only using a PCIe Gen4 compatible server, the XpressSX AGI-FH400G is delivered with this PCIe Gen4 x16 daughter card. This way, the system will achieve 2x Gen4 x16 performances similar to PCIe Gen5 x16, using two R-Tile PCIe Hard IPs inside the FPGA.

The daughter card also supports x8x8 bifurcation mode.



## Deliverables

- Full height half length 2-slot PCIe board with active heatsink and PCIe bracket
- 2x DDR4 SO-DIMM 32GByte each
- Board Support Package: Manuals, 2D drawing, HDL reference designs (Contact REFLEX CES for PCIe Gen5 CXL™ interface validation)
- DWF/STEP models (upon request)
- Online support at [support.reflexces.com](http://support.reflexces.com)
- NDK package (including DPDK NIC application) provided separately by BrnoLogic
- 2x HSI cables (ARC6-16-10.0-LU-LD-2-1) and 1x USB-C to USB-C cables (0.72ft), 3.1 Gen2 to connect the PCIe Gen4 x16 daughter card
- PCIe Gen4 x16 daughter card

## Ordering information

XpressSXAGI-FH400GT-ES	= Intel® Agilex™ SoC I-Series ES Silicon (AGIB027R29A1E2VR3), 3 banks DDR4 - No SoC support
XpressSXAGI-FH400GT	= Intel® Agilex™ SoC I-Series Production Silicon (AGIB027R29A1E2V), 3 banks DDR4

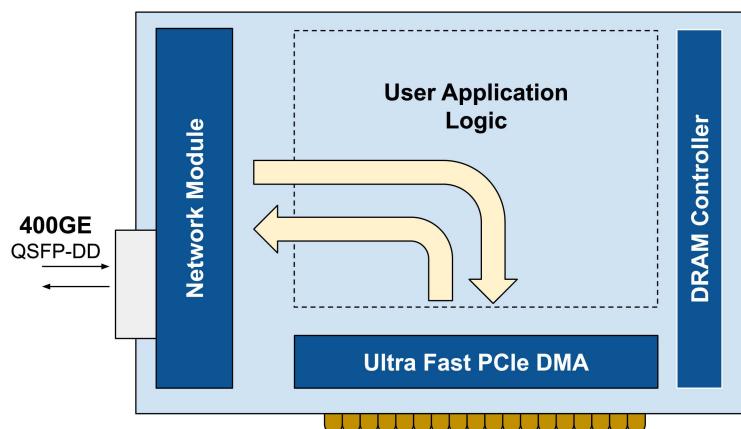
Contact sales for availability and pricing

# Development Framework for High-speed Packet Processing

## Start your design from standard NIC

- Provided as a free demo application
- Network module based on F-Tile 400G Ethernet  
Hard IP
- Ultra fast DMA with 400 Gbps throughput based on PCIe Gen5 x16 interface (R-Tile)
- Easy to use memory interface for single read/write data from/to card
- Preconfigured DDR4 controller for memory access from the user logic
- Precise timestamps with 2.5 ns resolution for 400G Ethernet

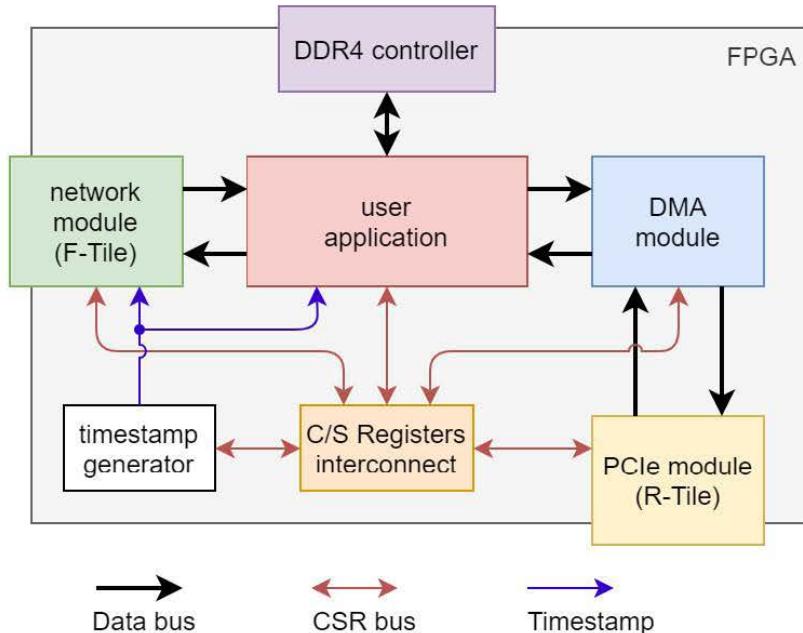
Standard NIC with high-speed packet capture  
1x400GE, 2x200GE, 4x100GE, 8x50GE, 2x40GE, 8x25GE, 8x10GE



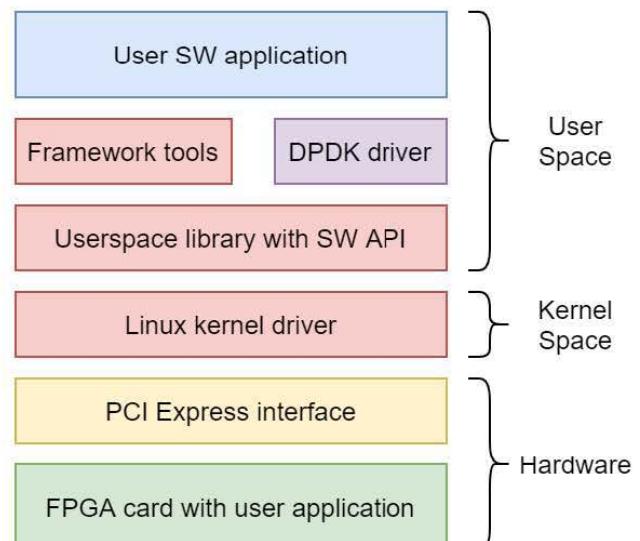
## Easy to use NDK Development Framework

- Set of open-source IP cores for data manipulation
- Automatic scripts for complete design synthesis
- Single make command to create complete FPGA bitstream
- Bitstream identification through DeviceTree ROM
- Easy to use software stack in a single RPM package
- Linux kernel driver, DPDK support, user space library, tools for the configuration of components
- Easy creation of custom application by user-friendly API for component access and DMA transfers
- Fully parameterizable and modular hardware and software architecture

## FPGA design architecture



## Software stack



Part number: NDK-PROF-SUPPORT

BRNO LOGIC

sales@brnologic.cz  
www.brnologic.cz

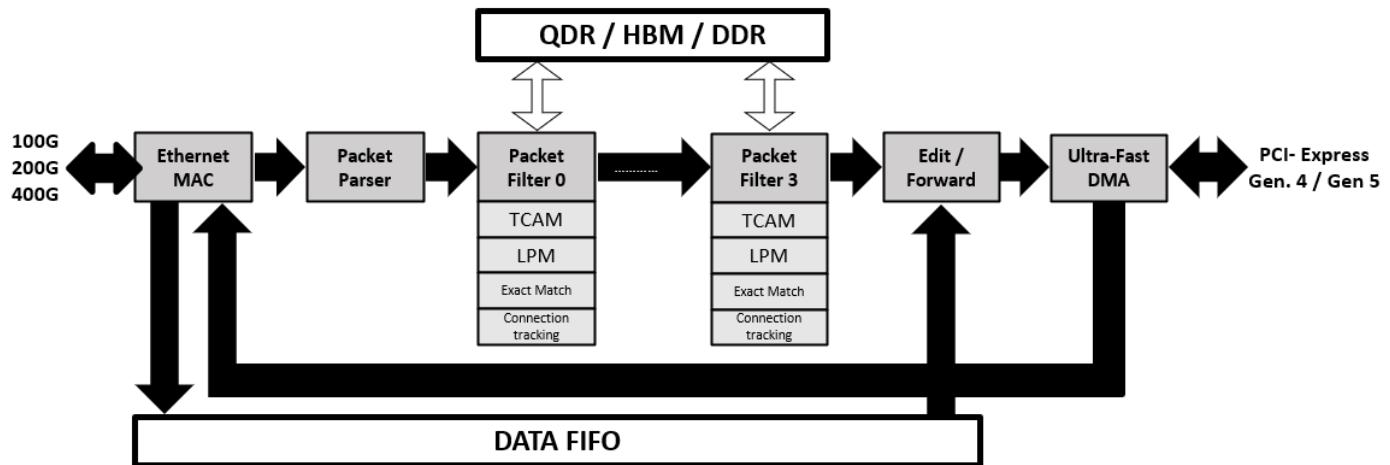
cesnet

Open source IP core library  
www.liberouter.org/ndk

## Target Network Applications

Hardware acceleration of precise network monitoring, IDS/IP systems, next generation firewalls, test equipment, Anti DDoS and other time-critical networking applications.

Only one card for 10, 40, 100, 200 and 400 GE link speeds.



### Security devices

- Hardware filters and pattern matching to accelerate IDS/IPS systems
- Precise packet filtering and packet capture for lawful interception
- Anti DDoS with hardware IP or flow filtering controlled by software

### Network monitoring probes

- High-speed packet capture with up to 512 receive queues, DPDK support
- Extraction of features for encrypted traffic analysis
- Variety of packet classification engines with wire-speed performance:
  - TCAM with up to 512 general rules, each defined with individual wildcard mask
  - Longest Prefix Match in deep pipeline with capacity for up to 100k prefixes
  - Exact Match hash table with support for up to a million unique keys
  - DDR/QDR/HBM based connection tables with tens of millions flow records

### Design services

The card is prepared for custom hardware acceleration in FPGA

We provide FPGA design based on high-speed 400 Gb IP cores for:

- packet headers parsing (Ethernet, ICMP, IPv4, IPv6, MPLS, etc.),
- packet filtering and classification,
- flow cache and connection tracking tables,
- fast pattern matching and
- many other IP cores for fast packet processing in deep pipelines.

### Contact information

BRNO  L O G I C

[sales@brnologic.cz](mailto:sales@brnologic.cz)  
[www.brnologic.cz](http://www.brnologic.cz)

**cesnet**  


Open source IP library  
[www.liberouter.org/ndk](http://www.liberouter.org/ndk)

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