

DIO6155

High-Efficiency, 2 A Output Synchronous Step-Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (25 mΩ)
- 2.5 V to 5.5 V input voltage range
- Adjustable output voltage: 0.6 V to 5 V
- More than 2 A output current capability
- Low quiescent current: 10 μ A
- 2 MHz switching frequency minimizes the external components
- Operation mode: FPWM or auto mode
- High efficiency at light load
- 100% duty cycle for the lowest dropout
- Output discharge function
- Protection:
 - Short-circuit protection
 - Thermal shutdown protection
 - Over-current protection
- Package: 1.5 mm x 1.5 mm DFN-6

Applications

- IP network cameras
- Portable electronics
- Solid state drive
- Industrial PCs
- Multifunction printers

Descriptions

The DIO6155 is a high-efficiency, high-frequency synchronous step-down DC-DC regulator IC capable of delivering more than 2 A output currents.

The DIO6155 features a selection function that switches the device between the force pulse width modulation (FPWM) and auto mode. When the SEL pin is driven HIGH, the DIO6155 enters (FPWM) mode. The device enters the auto mode if the SEL pin is LOW.

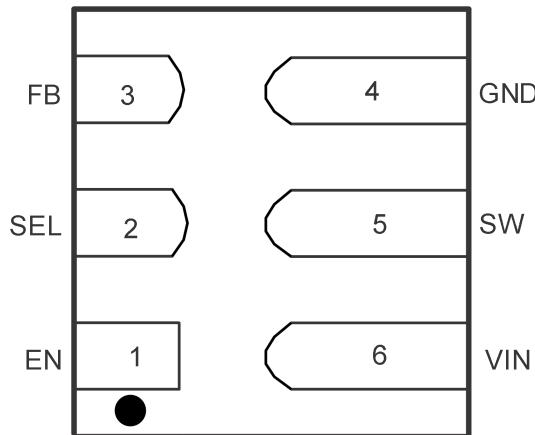
If the DIO6155 is selected to work under FPWM mode, the device works with ultra-low output ripple. Under auto mode, the DIO6155 works in PWM (Pulse Width Modulation) mode under medium to heavy load. In such conditions, the DIO6155 functions with a 2 MHz switching frequency to minimize the size of the inductor and output capacitor. If the load drops to meet the light load condition, the DIO6155 automatically enters PSM (Power Save Mode) for high efficiency.

The DIO6155 has a fast transient response feature. The device operates over a wide input range from 2.5 V to 5.5 V with very low $R_{DS(ON)}$ to minimize the conduction loss. The DIO6155 is capable of delivering output down to 0.6 V with a feedback voltage of ± 6 mV accuracy over -20°C to 85°C junction temperature.

Ordering Information

| Part Number | Top Marking | MSL | RoHS | T_A | Package | |
|-------------|-------------|-----|-------|-------------|--------------|-------------------|
| DIO6155CL6 | 5EYW | 1 | Green | -40 to 85°C | DFN1.5*1.5-6 | Tape & Reel, 3000 |

Pin Assignment



DFN 1.5*1.5-6

Figure 1. Bottom view

Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|----------|--|
| 1 | EN | Enable control. Pull high to turn on. Do not leave it floating, Maximum available pull-down resistor: 1 MΩ. |
| 2 | SEL | Select pin. Use the pin to select between FPWM and auto mode. But can not be left floating, Maximum allowable pull-down resistor: 1 MΩ. SEL = 0 selects auto mode. SEL = 1 selects FPWM. |
| 3 | FB | Output feedback pin. Connect this pin to the center point of the output resistor divider. |
| 4 | GND | Ground pin. |
| 5 | SW | Inductor pin. Connect this pin to the switching node of inductor. |
| 6 | VIN | Input voltage pin. |

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-------|-----------|------|
| | VIN, FB, EN, SEL input pin voltage ⁽¹⁾ | -0.3 | 6 | V |
| | SW (DC) output pin voltage ⁽¹⁾ | -0.3 | VIN + 0.3 | V |
| T _J | Operating junction temperature | -40 | 150 | °C |
| T _{STG} | Storage temperature | -65 | 150 | °C |
| ESD | Human-body model (HBM) | ±5000 | | |
| | Charge-device model (CDM) | ±2000 | | |

Note:

(1) All voltage values are with respect to the network ground terminal.

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. Does not Recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------|---|-----|-------|-----|------|
| V _{IN} | Input voltage range | 2.5 | | 5.5 | V |
| V _{OUT} | Output voltage range | 0.6 | | 5.0 | V |
| I _{OUT} | Output current range | 0 | | 2.0 | A |
| T _J | Operating junction temperature | -40 | | 125 | °C |
| R _{θJA} | Junction-to-ambient thermal resistance | | 107.8 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 24.2 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 20.5 | | °C/W |

DC Electrical Characteristics

$T_J = -40^\circ\text{C}$ to 125°C , and $V_{IN} = 2.5\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$, unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|------|----------|------|------------------|
| Supply | | | | | | |
| I_Q | Quiescent current | $EN = \text{High}$, no load, device not switching | | 10 | 18 | μA |
| $I_Q^{(1)}$ | Quiescent current | $EN = \text{High}$, no load, FPWM devices, $V_{IN} = 2.5\text{ V}$ to 5 V | | 9 | 18 | mA |
| I_{SD} | Shutdown current | $EN = \text{Low}$, $T_J = -40^\circ\text{C}$ to 85°C | | 0.15 | 0.5 | μA |
| V_{UVLO} | Undervoltage lockout threshold | V_{IN} rising | 2.22 | 2.35 | 2.48 | V |
| | Undervoltage lockout hysteresis | V_{IN} falling | | 150 | | mV |
| T_{JSD} | Thermal shutdown threshold | T_J rising | | 150 | | $^\circ\text{C}$ |
| | Thermal shutdown hysteresis | T_J falling | | 20 | | $^\circ\text{C}$ |
| Logic interface EN, SEL | | | | | | |
| V_{IH} | High-level threshold voltage | $V_{IN} = 2.5\text{ V}$ to 5.5 V | 0.9 | | | V |
| V_{IL} | Low-level threshold voltage | $V_{IN} = 2.5\text{ V}$ to 5.5 V | | | 0.4 | V |
| Soft-start | | | | | | |
| t_{ss} | Soft-start time | Time from EN high to 95% of V_{OUT} nominal | | 1.8 | | ms |
| Output | | | | | | |
| $V_{FB}^{(1)}$ | Feedback regulation voltage | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C | 591 | 600 | 609 | mV |
| | | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $T_J = -20^\circ\text{C}$ to 85°C | 594 | 600 | 606 | mV |
| $I_{FB,LKG}$ | Feedback input leakage current for adjustable output voltage | $V_{FB} = 0.6\text{ V}$ | | 0.01 | | μA |
| R_{DIS} | Output discharge resistance | $V_{SW} = 0.4\text{ V}$; $EN = \text{LOW}$ | | 4 | | Ω |
| | Load regulation | $I_{OUT} = 0.5\text{ A}$ to 2 A , $V_{OUT} = 1.8\text{ V}$ | | 0.1 | | $%/A$ |
| | Output voltage total accuracy ⁽¹⁾ | $2.5\text{ V} \leq V_{IN} \leq 5.0\text{ V}$, $10\text{ mA} \leq I_{OUT} \leq 300\text{ mA}$, $T_J = -40^\circ\text{C}$ to 85°C , PFM Mode | -3 | | 3 | $\%$ |
| | Output load transient response ⁽¹⁾ | $10\text{ mA} \leq I_{OUT} \leq 300\text{ mA}$, $0.25\text{ A}/\mu\text{s}$ | | ± 25 | | mV |
| | Output line transient response ⁽¹⁾ | $3.5\text{ V} \leq V_{IN} \leq 4.0\text{ V}$, $500\text{ mV}/10\text{ }\mu\text{s}$, $I_{OUT} = 300\text{ mA}$ | | ± 25 | | mV |
| Power switch | | | | | | |
| $R_{DS(on)}$ | High-side FET on-resistance | | | 26 | | $\text{m}\Omega$ |
| | Low-side FET on-resistance | | | 25 | | $\text{m}\Omega$ |
| $I_{LIM}^{(1)}$ | High-side FET switch current limit, DC | | 2.7 | 3.1 | 4.1 | A |
| | Low-side FET current limit, DC | | | | 3.5 | A |
| f_{sw} | PWM switching frequency | $I_{OUT} = 1\text{ A}$, $V_{OUT} = 1.8\text{ V}$ | | 2 | | MHz |

Note:

(1) Guaranteed by design simulation.

(2) Specifications subject to change without notice.

Typical Performance Characteristic

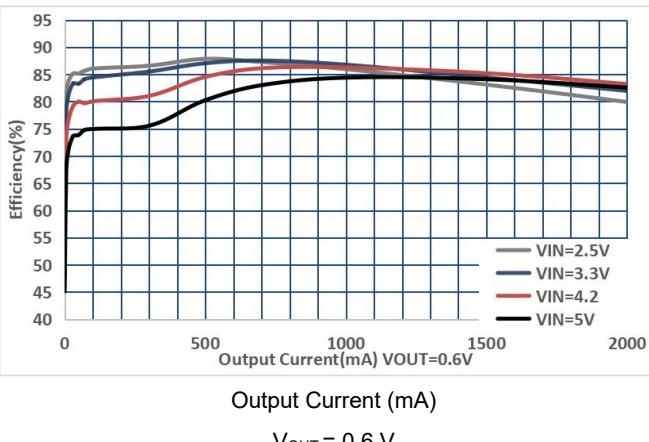


Figure 2. Efficiency vs. I_{OUT}

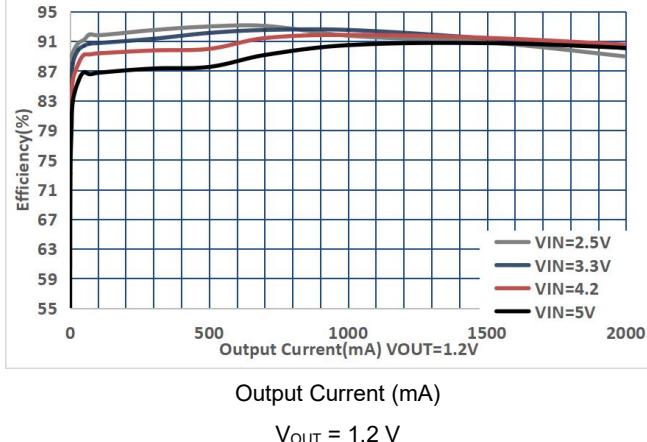


Figure 3. Efficiency vs. I_{OUT}

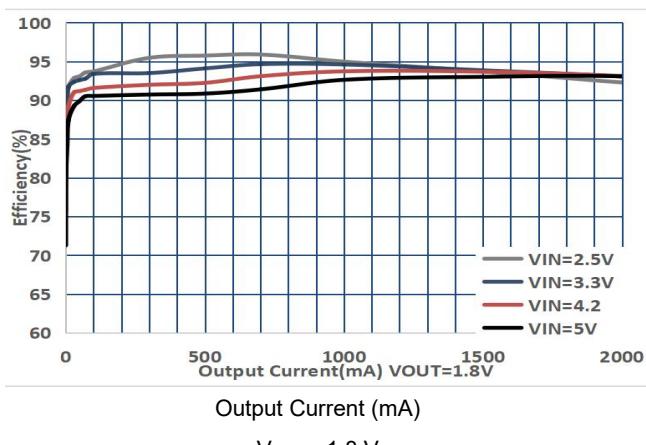


Figure 4. Efficiency vs. I_{OUT}

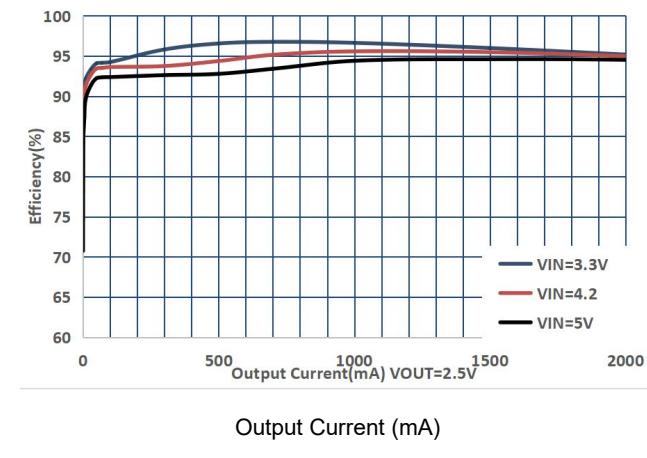


Figure 5. Efficiency vs. I_{OUT}

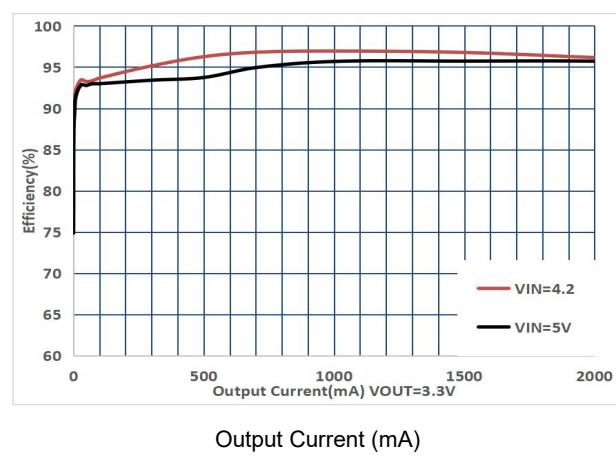


Figure 6. Efficiency vs. I_{OUT}

Typical Performance Characteristic (Continue)

$V_{IN} = 3.3 \text{ V}$, $L = 0.47 \mu\text{H}$, $C_{IN} = 10 \mu\text{F}$, $C_{OUT} = 2 \times 10 \mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

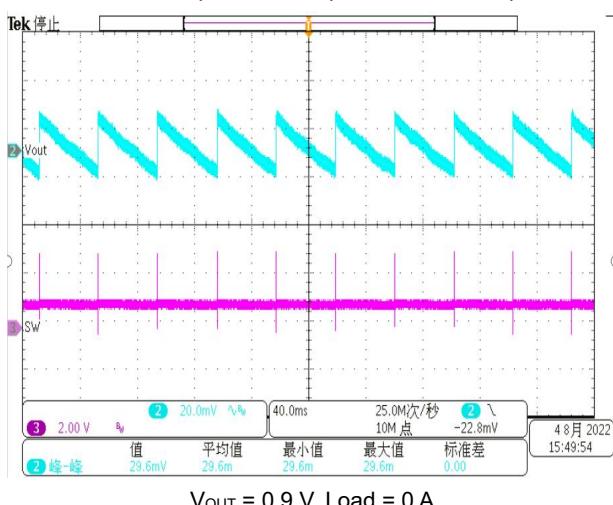


Figure 7. Auto mode operation

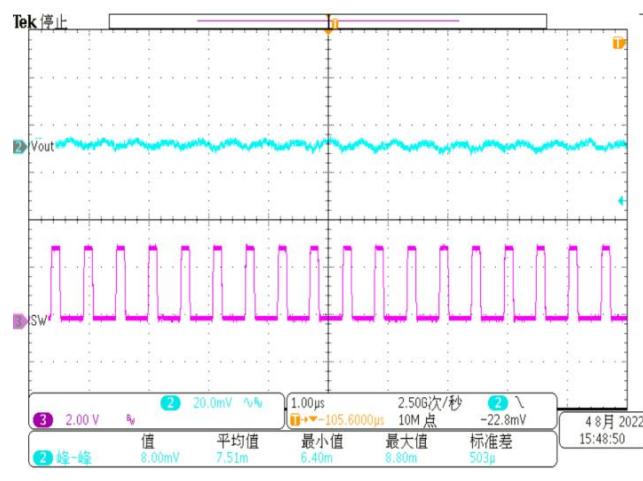


Figure 8. FPWM operation

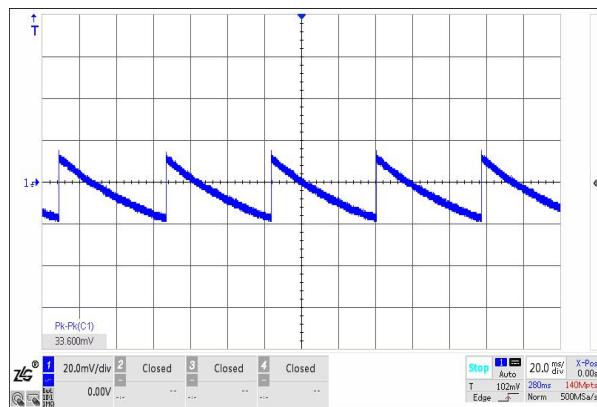


Figure 9. Auto mode operation

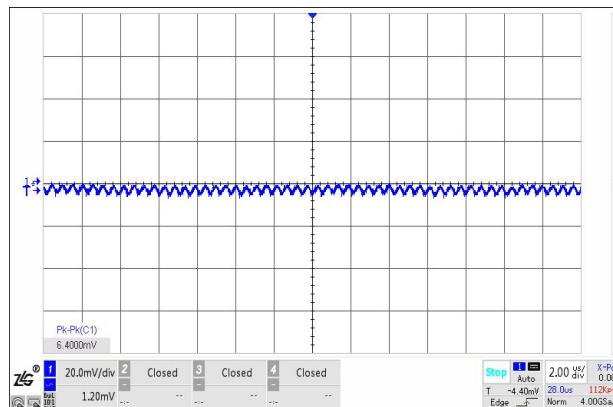


Figure 10. FPWM operation

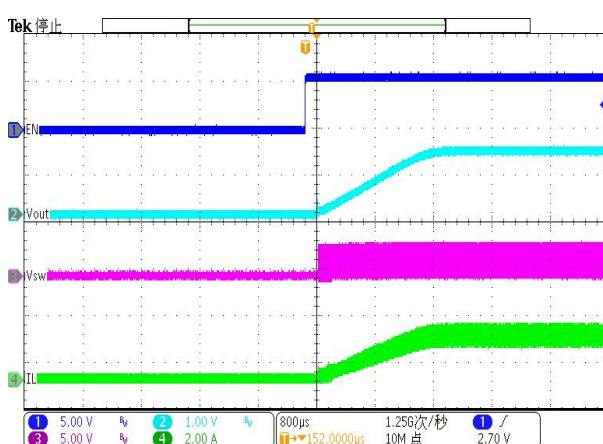


Figure 11. Enable start-up

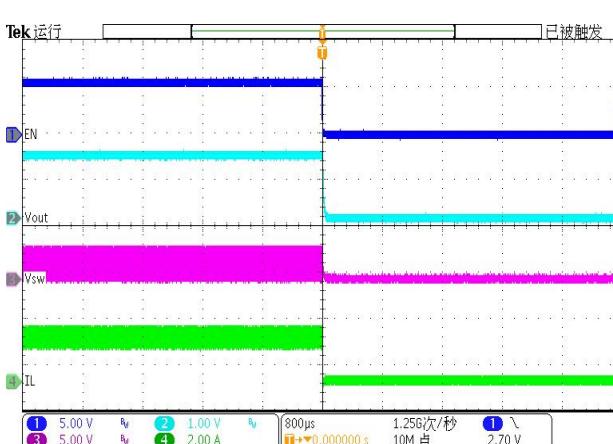
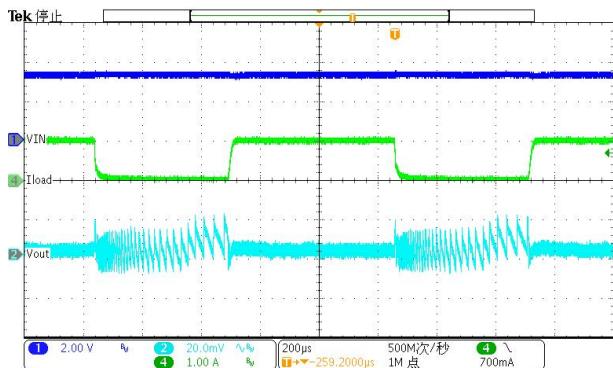
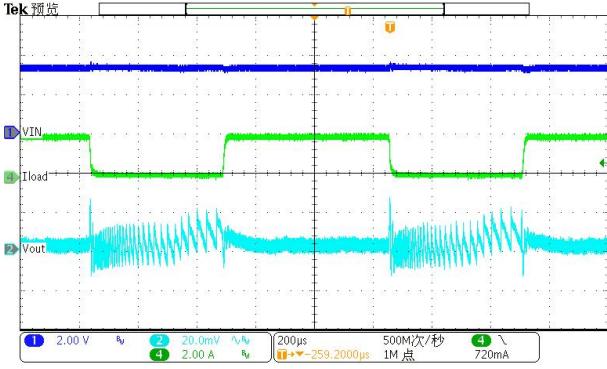


Figure 12. Enable shut-down



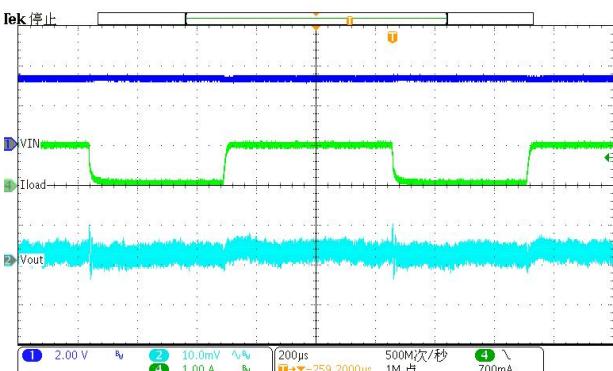
Auto mode ($I_{load} = 0.005$ A to 1.0 A)

Figure 13. Load transient



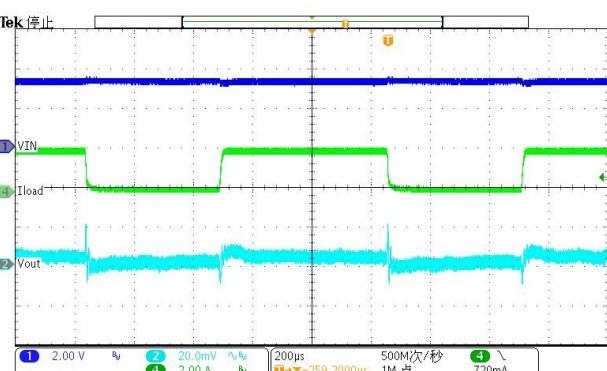
Auto mode ($I_{load} = 0.005$ A to 2.0 A)

Figure 14. Load transient



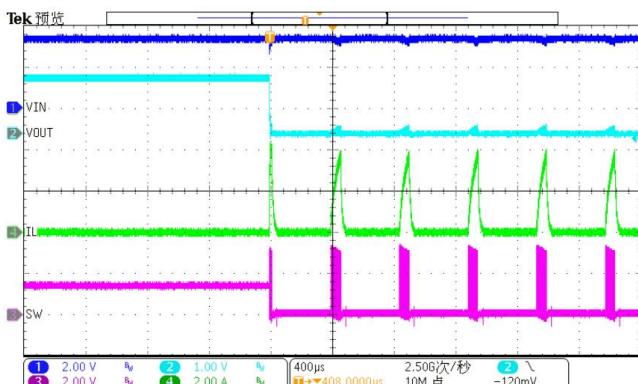
FPWM mode ($I_{load} = 0.005$ A to 1.0 A)

Figure 15. Load transient



FPWM mode ($I_{load} = 0.005$ A to 2.0 A)

Figure 16. Load transient



Auto mode

Figure 17. Short-circuit protection

Block Diagram

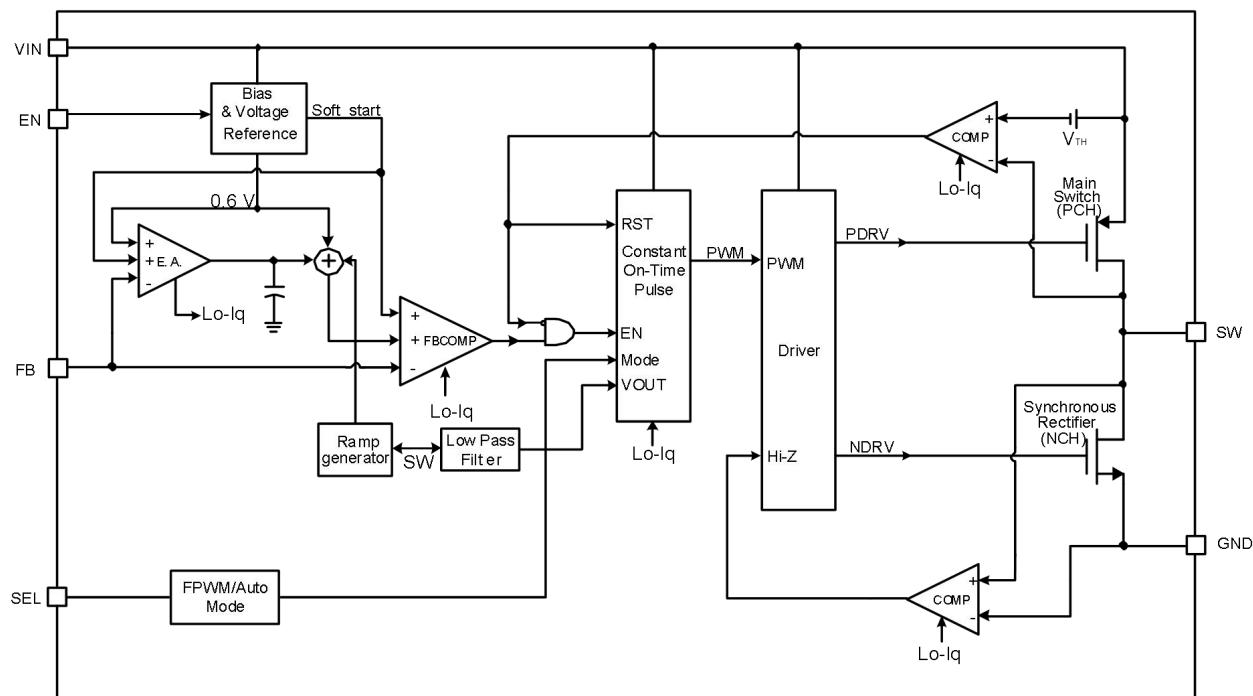


Figure 18. Block diagram

High-Efficiency, 2 A Output Synchronous Step-Down Converter

Detailed Description

Overview

The DIO6155 is a synchronous buck regulator IC with an adaptive constant on-time (COT) control, and top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size and thus achieve the minimum solution footprint.

The DIO6155 has a selection function, which can select between forced pulse width modulation (FPWM) and auto mode. When the SEL pin is pulled to HIGH, the DIO6155 enters the forced pulse width modulation (FPWM). If the SEL pin is driven LOW, it enters the auto mode.

During FPWM mode, the converter maintains a continuous conduction mode operation and keeps the output voltage ripple very low across the whole load range. During auto mode, the DIO6155 enters PWM (Pulse Width Modulation) mode for medium to heavy load conditions or enters PSM (Power Save Mode) for a light load. Under PWM mode, the converter operates with a typical 2 MHz switching frequency to minimize the size of the inductor and capacitor. As the load current decreases, the converter enters PSM (Power Save Mode), reducing the switching frequency to keep high efficiency over the entire load current range.

Pulse Width Modulation (PWM) Operation

The device will operate in continuous conduction mode (CCM) when the output current is high. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode. The PWM operation is based on an adaptive constant on-time (COT) control with stabilized switching frequency. In a steady state condition, the on-time is calculated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500\text{ns} \quad (1)$$

Power Save Mode (PSM) Operation

Under light load conditions, the DIO6155 enters power save mode (PSM) to maintain high efficiency. Meanwhile, the device works continuously in discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates now with a fixed on-time and the switching frequency further decreases proportionally to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \left(\frac{V_{IN} - V_{OUT}}{L} \right)} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized by using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM and can only maintain output regulation in PWM mode.

Soft-Start

The DIO6155 employs a soft-start (SS) mechanism to ensure smooth output ramping during power-up. When EN goes high, an internal soft-start circuitry controls the output voltage during start-up. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage, V_{FB} . This feature avoids excessive inrush current and ensures a controlled output voltage ramp.

Switch Current Limit and Short-Circuit Protection

The protection function prevents the device from drawing excessive current in case of externally-caused over-current or short-circuit conditions. If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles, the device turns off the high-side MOSFET for about 200 μ s and then restarts again with a soft-start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

In FPWM devices, a negative current limit (I_{LIMN}) is enabled to prevent excessive current flowing backward to the input. When the inductor current reaches I_{LIMN} , the low-side MOSFET turns off and the high-side MOSFET turns on and is kept on until t_{ON} time expires.

Undervoltage Lockout

The DIO6155 being powered up, if the input voltage is larger than typical 2.35 V, the DIO6155 starts switching. If the input voltage is lower than UVLO threshold with a 150 mV hysteresis, the DIO6155 will be shut down.

Thermal Shutdown

The device goes into thermal shutdown as soon as the junction temperature exceeds typical 150°C with a 20°C hysteresis.

Device Functional Modes

1. Enable, Disable and Output Discharge

Pulling the EN pin LOW (< 0.4 V) will shut down the device. If the EN pin is driven HIGH (> 0.9 V), the device will be turned on again. Always do not leave EN floating. Shutdown mode is forced if EN is pulled low with a shutdown current of typical 150 nA. During shutdown mode, the device is turned off and the output voltage is actively discharged through the SW pin by a current sink.

2. SEL

The DIO6155 has the selection function. Either forced pulse width modulation (FPWM) mode or Auto mode can be selected. When the SEL pin is pulled HIGH, the DIO6155 enters the forced pulse width modulation (FPWM). When the SEL pin is driven LOW, the DIO6155 enters auto mode. (see Table 1).

Table 1. SEL pin logic

| Operation Mode | SEL Pin |
|----------------|---------|
| FPWM | H |
| Auto mode | L |

Typical Applications

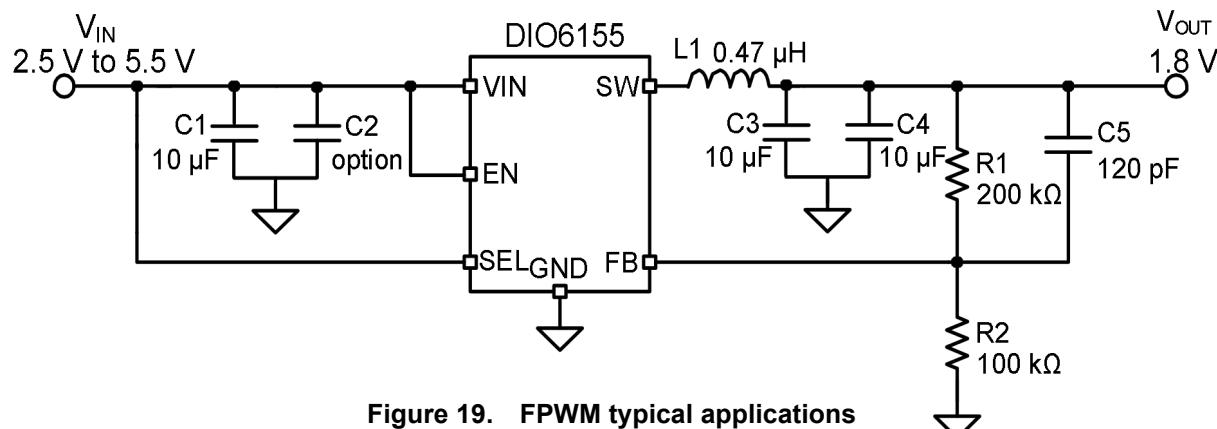


Figure 19. FPWM typical applications

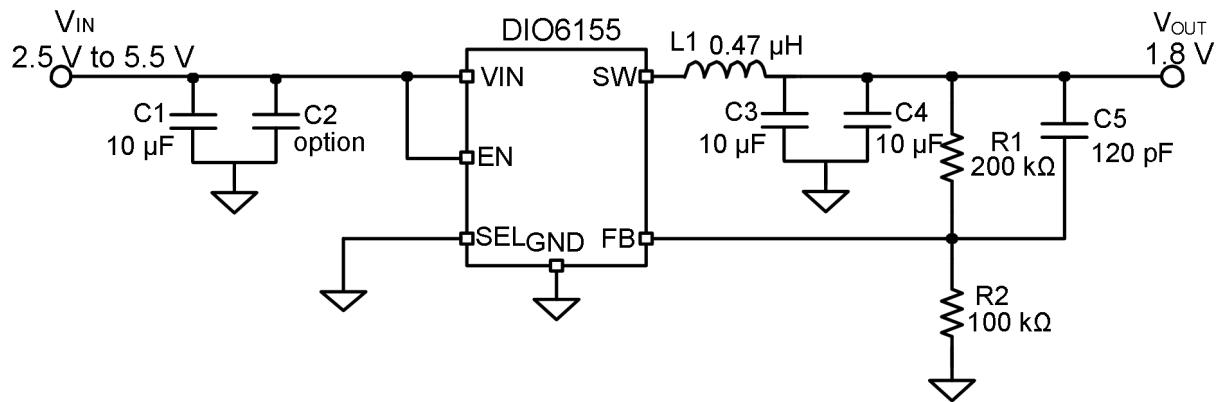


Figure 20. Auto mode typical applications

Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design parameters

| Design Parameter | Example Value |
|------------------------|----------------|
| Input voltage | 2.5 V to 5.5 V |
| Output voltage | 1.8 V |
| Output ripple voltage | < 20 mV |
| Maximum output current | 2 A |

Table 3 lists the components used for the example.

Table 3. List of Components

| Reference | Description | Manufacturer |
|-----------|---|--------------|
| C1 | 10 μ F, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D | Murata |
| C2 | Optional | - |
| C3 | 10 μ F, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D | Murata |
| C4 | 10 μ F, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D | Murata |
| C5 | 120 pF, ceramic capacitor, 50 V, size 0402 | Std |
| L1 | 0.47 μ H, power inductor, XFL4015-471MEB | Coilcraft |
| R1 | Depending on the output voltage, 1%, size 0402 | Std |
| R2 | 100 k Ω , chip resistor, 1/16 W, 1%, size 0402 | Std |

Detailed Design Procedure

Setting the Output Voltage

Set the desired output voltage by using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set by an external resistor divider according to Equation (4):

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (3)$$

R2 must not be higher than 100 k Ω to achieve high efficiency at light load while providing acceptable noise sensitivity. Equation (5) shows how to compute the value of the feedforward capacitor for a given R2 value. For the recommended 100 k Ω value for R2, a 120 pF feedforward capacitor is used.

$$C5 = \frac{12\mu}{R2} \quad (4)$$

Output Filter Design

The inductor and the output capacitor together provide a low-pass filter function. To simplify this process, Table 4 recommends the inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab tests. Further combinations should be checked for each individual application.

Table 4. Matrix of Output Capacitor and Inductor Combinations

| Nominal L1 (μ H) ⁽²⁾ | Nominal C _{OUT} (μ F) ⁽³⁾ | | | |
|--------------------------------------|--|------------------|----|-----|
| | 10 | 2 x 10 or 22 | 47 | 100 |
| 0.33 | | | | |
| 0.47 | + | + ⁽¹⁾ | + | |
| 1.0 | | | | |

(1) This LC combination is the standard value and recommended for most applications.

(2) Inductor tolerance and current de-rating are anticipated. The effective inductance can vary by 20% and -30%.

(3) Capacitance tolerance and bias voltage de-rating are anticipated. The effective capacitance can vary by 20% and -35%.

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. Lowering the inductor values helps to reduce the size and cost, thus improving the transient response of the circuit. Meanwhile, it increases the inductor ripple current and output voltage ripple. Also lowering the inductor value reduces the efficiency due to the higher peak currents. To calculate the maximum inductor current under static load conditions, Equation (6) is given.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L_1 \times f_{SW}} \quad (5)$$

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (6)$$

Where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L_1 = Inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Table 5 lists recommended inductors.

Table 5. List of Recommended Inductors

| Inductance (μ H) | Current Rating (A) | Dimensions (L x W x H mm) | Max DC Resistance (m Ω) | Manufacturer Part Number |
|--------------------------|-----------------------|------------------------------|------------------------------------|-----------------------------|
| 0.47 | 4.8 | 2.0 x 1.6 x 1.0 | 32 | HTEN20161T-R47MDR, Cyntec |
| | 4.6 | 2.0 x 1.2 x 1.0 | 25 | HTEH20121T-R47MSR, Cyntec |
| | 4.8 | 2.0 x 1.6 x 1.0 | 32 | DFE201610E - R47M, MuRata |
| | 4.8 | 2.0 x 1.6 x 1.0 | 32 | DFE201210S - R47M, MuRata |
| | 5.1 | 2.0 x 1.6 x 1.0 | 34 | TFM201610ALM-R47MTAA, TDK |
| | 5.2 | 2.0 x 1.6 x 1.0 | 25 | TFM201610ALC-R47MTAA, TDK |
| | 6.6 | 4.0 x 4.0 x 1.6 | 8.36 | XFL4015-471ME, Coilcraft |
| | 8.0 | 3.5 x 3.2 x 2.0 | 10.85 | XEL3520-471ME, Coilcraft |
| | 6.8 | 4.5 x 4 x 1.8 | 11.2 | WE-LHMI-744373240047, Würth |

Capacitor Selection

The IC is optimized for ceramic output capacitors. The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for the best filtering and must be placed between VIN and GND as close as possible.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple. DIOO recommends using X7R or X5R dielectrics.

Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

Layout Guidelines

The layout design of the DIO6155 regulator is relatively simple. For the best efficiency and minimum noise issues, place the following components close to the IC: C_{IN} , L_1 , R_1 , and R_2 .

1. Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
2. C_{IN} must be close to IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.
3. The PCB copper area associated with the SW pin must be minimized to avoid the potential noise issue.
4. The components R_1 and R_2 , and the trace connected to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise issue.

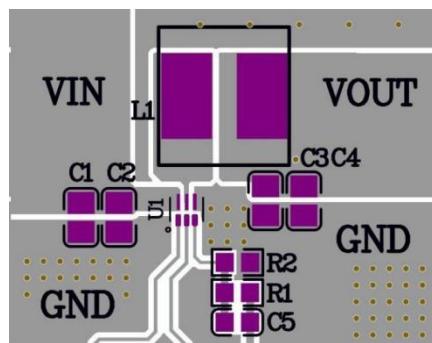


Figure 21. PCB Layout Guide

Board Layout

This section provides the DIO6155 EVM board layout and illustrations from Figure 22 through Figure 24.

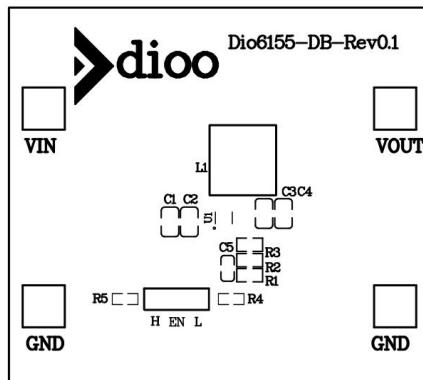


Figure 22. Top Assembly

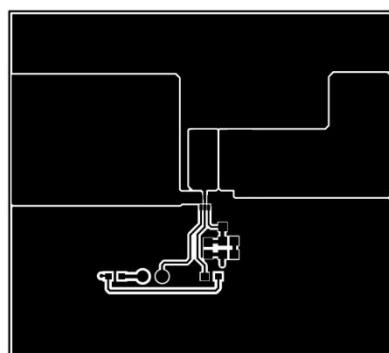


Figure 23. Top Layer

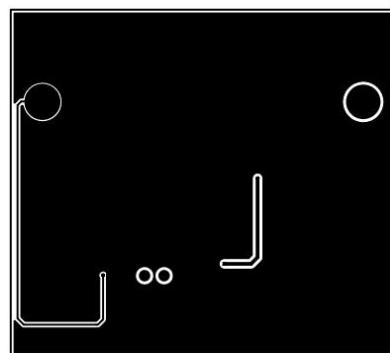
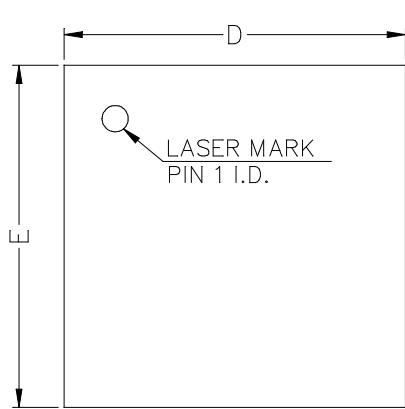
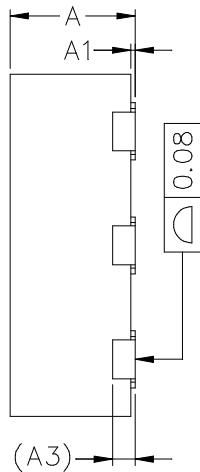
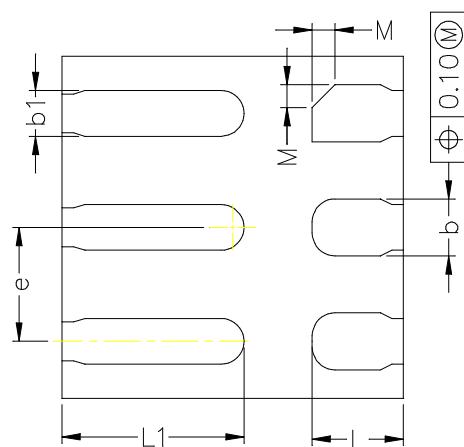
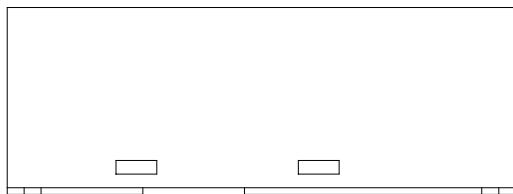
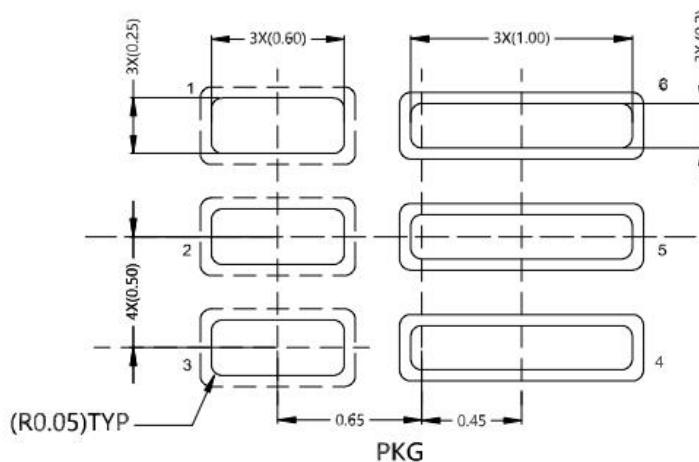
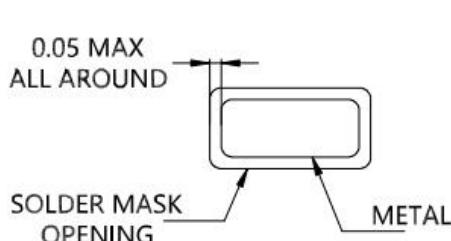
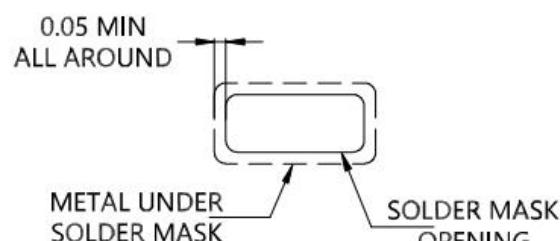
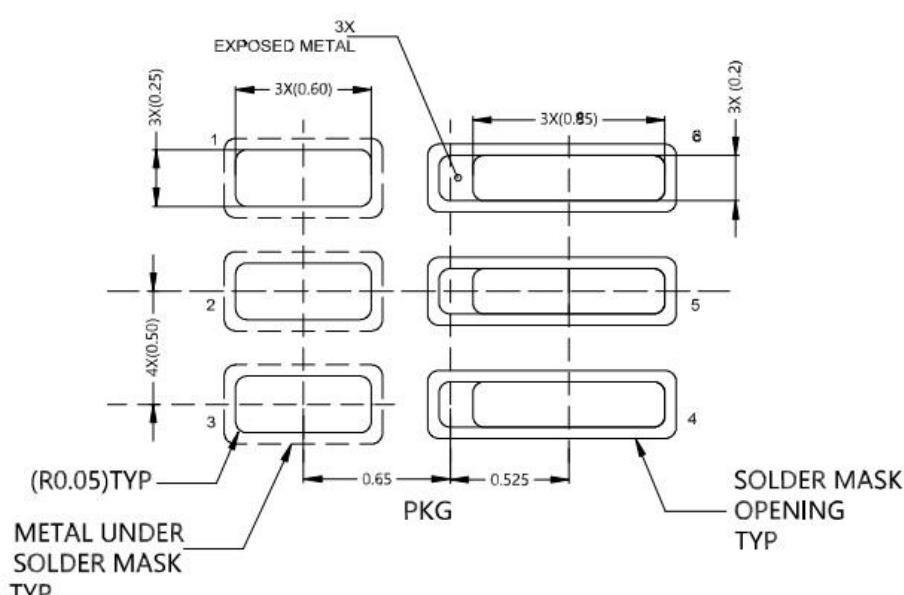


Figure 24. Bottom Layer

Physical Dimensions:DFN1.5*1.5-6


TOP VIEW

SIDE VIEW

BOTTOM VIEW

SIDE VIEW

| Common Dimensions (Units of measure = Millimeter) | | | |
|--|----------|------|------|
| Symbol | Min | Nom | Max |
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.10 REF | | |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.15 | 0.20 | 0.25 |
| D | 1.40 | 1.50 | 1.60 |
| E | 1.40 | 1.50 | 1.60 |
| e | 0.40 | 0.50 | 0.60 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.70 | 0.80 | 0.90 |
| M | 0.10 REF | | |

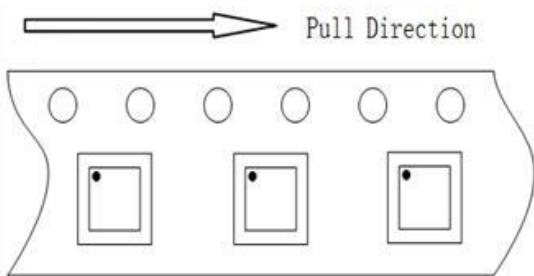

LAND PATTERN EXAMPLE

**PADS 4-6
NON SOLDER MASK
DEFINED**

**PADS 1-3
SOLDER MASK
DEFINED**
SOLDER MASK DETAILS

SOLDER PASTE EXAMPLE

DIO6155 Package Description

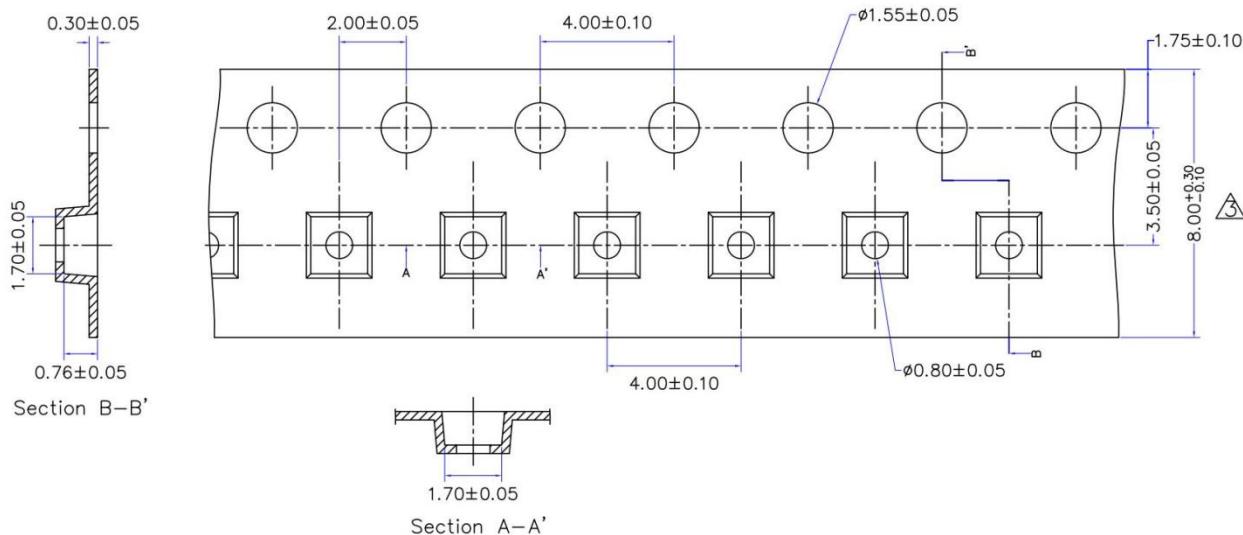
DIO6155CL6 DFN-6 MSL1

Package: Tape & Reel + Moisture Barrier Bag + Vacuum

1. Tape & Reel orientation



2. Tape dimensions



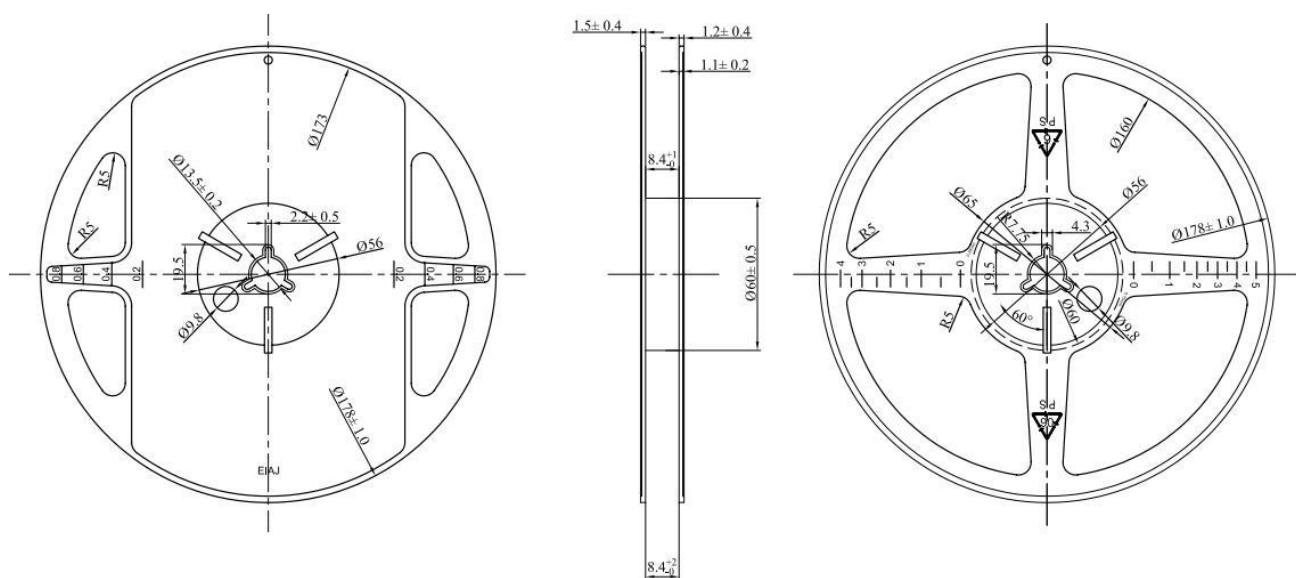
3. Cover tape attachment method

Hot attachment

4. Reel / Cover antistatic specifications

| Item | Materials | Surface Resistance (Ω) | Friction Voltage |
|------|-----------|---------------------------------|------------------|
| 1 | Cover | $1*10^4\sim1*10^{10}$ | <100 V |
| 2 | Reel | $1*10^5\sim1*10^9$ | <100 V |

5. Reel drawing (7 inches)



6. Packing specification

| PKG | Pcs / reel | Reel / box | Pcs / box | Box / carton | Pcs / carton |
|-------|------------|------------|-----------|--------------|--------------|
| DFN-6 | 3000 | 4 | 12000 | 12 | 144000 |

Revision History

- **Revision 0.1 initial preliminary datasheet for Google review**
- **Changes from Revision 0.1 to Revision 0.2**
 - 1、 Updated spec according to simulation matrix.
 - 2、 Updated POD.
- **Changes from Revision 0.2 to Revision 0.3**
 - 1、 Added V_{FB} range under $T_J = -20^{\circ}\text{C}$ to 85°C .
 - 2、 Added ESD rating.
 - 3、 Added the maximum values of I_Q , I_{LIM} .
 - 4、 Added the maximum target current for I_{LIM} of Low-side FET negative current limit, DC.
 - 5、 Added layout guidelines.
- **Changes from Revision 0.3 to Revision 0.4**
 - 1、 Added pin description: "Maximum available pulldown resistor: 1 $\text{M}\Omega$ " at EN & SEL pin.
 - 2、 Updated block diagram.
 - 3、 Updated Equation (4) to be $R1=R2\times\left(\frac{V_{OUT}}{V_{FB}}-1\right)=R2\times\left(\frac{V_{OUT}}{0.6\text{V}}-1\right)$
 - 4、 Added the layout guideline Gerber diagram.
 - 5、 Added the "LAND PATTERN EXAMPLE" & "SOLDER MASK DETAILS" & "SOLDER PASTE EXAMPLE".
- **Changes from Revision 0.4 to Revision 1.0**
 - 1、 Updated I_{DIS} to 100 mA.
 - 2、 Updated f_{SW} to 2 MHz.
 - 3、 Updated equation (1).
 - 4、 Updated $C1$ to 10 μF .
 - 5、 Added "SEL = 0 Auto mode, SEL = 1 FPWM" in the description of SEL pin.
 - 6、 Added application curves.
- **Changes from Revision 1.0 to Revision 1.1**
 - 1、 Added " $V_{IN} = 2.5\text{ V}$ to 5 V " to the conditions of quiescent current (I_Q) in DC Electrical Characteristics table.
 - 2、 Updated V_{OUT} to $0.6\text{ V} \sim 5.0\text{ V}$.
- **Changes from Revision 1.1 to Revision 1.2**
 - 1、 Updated the SEL pin application information in Pin Descriptions table, "Maximum allowable pulldown resistor: 1 $\text{M}\Omega$."
- **Changes from Revision 1.2 to Revision 1.3**
 - 1、 Updated $R_{\theta JA}$ to 107.8°C/W .
 - 2、 Updated $R_{\theta JC(\text{top})}$ to 24.2°C/W .
 - 3、 Updated $R_{\theta JB}$ to 20.5°C/W .
 - 4、 Updated the Typical Performance Characteristic table
- **Changes from Revision 1.3 to Revision 1.4**
 - 1、 Added "MSL=1"
 - 2、 Added "Charge-device model (CDM) = $\pm 2000\text{ V}$ "
 - 3、 Added " $R_{DIS} = 4\ \Omega$ "
 - 4、 Delete " $I_{DIS} = 100\text{ mA}$ "
 - 5、 Added package description



DIO6155

High-Efficiency, 2 A Output Synchronous Step-Down Converter

➤ Changes from Revision 1.4 to Revision 1.5

1. Added "the Output voltage total accuracy = $\pm 3\%$ " in DC Electrical Characteristics table.
2. Added "the Output load transient response = $\pm 25 \text{ mV}$ " in DC Electrical Characteristics table.
3. Added "the Output line transient response = $\pm 25 \text{ mV}$ " in DC Electrical Characteristics table.
4. Updated the high-level threshold voltage from 1.0 V to 0.9 V.



CONTACT US

Dioo is a professional design and sales corporation for high-quality performance analog semiconductors. The company focuses on industry markets, such as cell phones, handheld products, laptops, medical equipment, and so on. Dioo's product families include analog signal processing and amplifying, LED drivers, and charger ICs. Go to <http://www.dioo.com> for a complete list of Dioo product families.

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