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R1801K Series

Buck DC/DC Converter for Energy Harvester with Adjustable Maximum Power Point Control, Adjustable Output Voltage and PG Function

No. EA-422-201210

OVERVIEW

R1801K is a power-storing buck DC/DC converter for a photovoltaic and vibration energy harvester. The Power Good (PG) function can output PG signal according to the output voltage facilitating to build a system. A low operating quiescent current allows a harvester to be used under a low-illumination environment, and it is suitable for an equipment with low power supplied from a harvester.

KEY BENEFITS

● Providing a low power supply (I_Q 200 nA) and a high efficiency (approximately 80%@10 μA).
● Monitoring the output voltage to output Power Good (PG) signal.
● Adjustable the output voltage and maximum power point control voltage in 100 mV step by the setting pins.

KEY SPECIFICATIONS

● Input Voltage Range: 2.3 V to 5.5 V
● Output Voltage Range: 2.3 V to 4.5 V
● Maximum Power Point Control Voltage Range :2.7 V to 5.3 V
● Output Voltage Accuracy: ± 3.0%
● Operating Quiescent Current:
   Typ. 200 nA (Ta =25°C, at no load)
   under condition of V_{IN} = 4 V, V_{OUT} = 3.0 V
● Starting Power: 1 μW (V_{IN} = 4 V, V_{OUT} = 3.0 V)
● Reverse Current Protection (V_{IN} ≥ 2.0 V)
● Adjustable Maximum Power Point Control, Adjustable Output Voltage
● Power Good Function

TYPICAL CHARACTERISTICS

Efficiency vs. Output Current V_{OUT} = 3.0 V

APPLICATION

● Energy harvesting module of a photovoltaic and vibration energy harvester

PACKAGE

DFN(PLP)2730-12

3.0 mm x 2.7 mm x 0.6 mm

SELECTION GUIDE

Product Name	Package	Quantity per Reel
R1801KxxxA-TR	DFN(PLP)2730-12	5,000 pcs

xxx: Select the ideal combination of the set output voltage (V_{SET}) and the set maximum power point control voltage (V_{MPSET}) from the code number starting from 001.
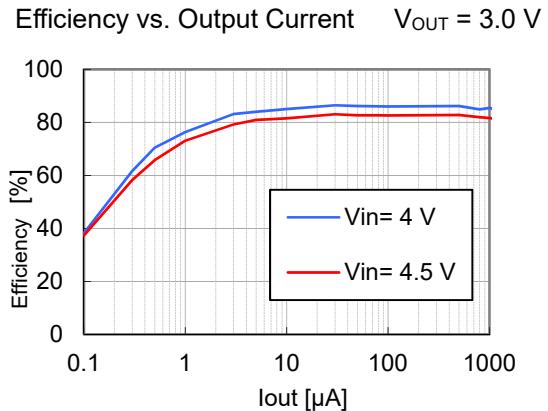
TYPICAL APPLICATION

L = 22 μH, C_{IN} = 10 μF, C_{OUT} = 47 μF

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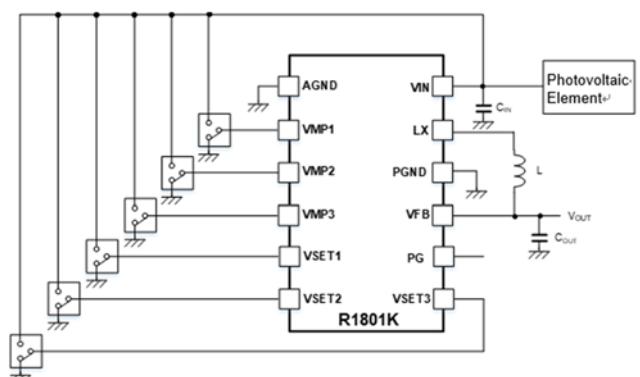
SELECTION GUIDE

The set output voltage and the set maximum power point control voltage are user-selectable options.

Selection Guide

| Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1801KxxxA-TR	DFN(PLP)2730-12	5,000 pcs	Yes	Yes

xxx: Select the ideal combination of the set output voltage (V_{SET}) and the set maximum power point control voltage (V_{MPSET}) from the code number starting from 001.

Refer to CODE LIST for lineup.

When use the PG function, put the V_{SET} voltage 2.5 V or higher.

It is recommended to set as $V_{MPSET} \geq V_{SET} + 0.5$ V.

BLOCK DIAGRAM

R1801K Block Diagram

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PIN DESCRIPTION

Top View

Bottom View
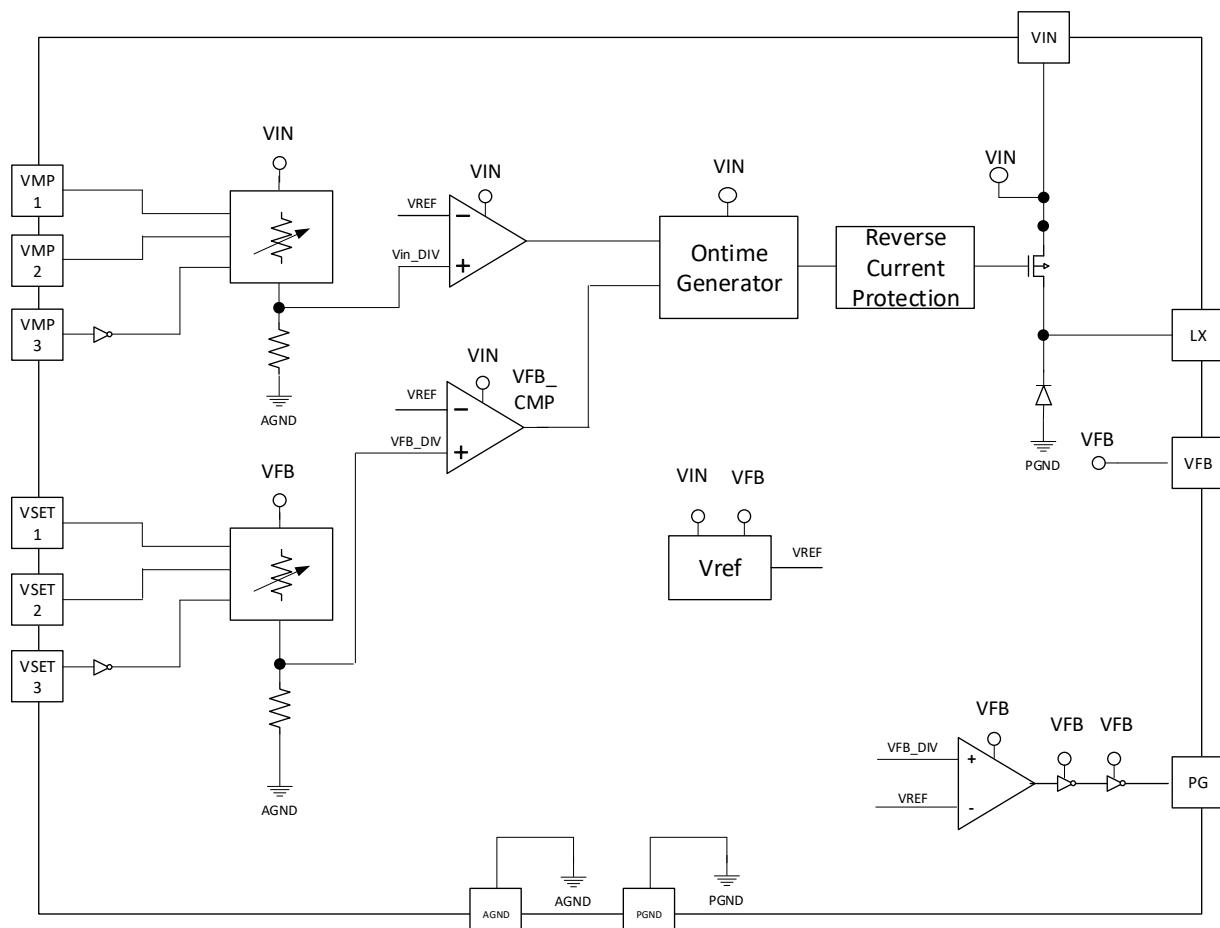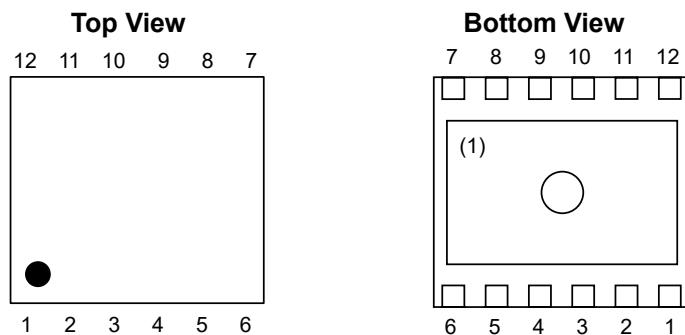
DFN (PLP) 2730-12 Pin Configuration

[1] The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level).
It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN(PLP)2730-12 Pin Description

Pin No.	Symbol	Description
1	AGND	Analog Ground Pin
2	VMP1	Maximum Power Point Control Voltage Adjustment Pin 1
3	VMP2	Maximum Power Point Control Voltage Adjustment Pin 2
4	VMP3	Maximum Power Point Control Voltage Adjustment Pin 3
5	VSET1	Output Voltage Adjustment Pin 1
6	VSET2	Output Voltage Adjustment Pin 2
7	VSET3	Output Voltage Adjustment Pin 3
8	PG	Power Good Pin
9	VFB	Output Voltage Pin
10	PGND	Power Ground Pin
11	LX	DC/DC Switching Pin
12	VIN	Pin for Connecting Photovoltaic Element

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ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Voltage	−0.3 to 6.5	V
V_{LX}	LX Pin Voltage	−0.3 to V_{IN} + 0.3	V
V_{VFB}	VFB Pin Voltage	−0.3 to 6.5	V
V_{VMP1}	VMP1 Pin Voltage	−0.3 to 6.5	V
V_{VMP2}	VMP2 Pin Voltage	−0.3 to 6.5	V
V_{VMP3}	VMP3 Pin Voltage	−0.3 to 6.5	V
V_{VSET1}	VSET1 Pin Voltage	−0.3 to 6.5	V
V_{VSET2}	VSET2 Pin Voltage	−0.3 to 6.5	V
V_{VSET3}	VSET3 Pin Voltage	−0.3 to 6.5	V
V_{PG}	Power Good Pin	−0.3 to 6.5	V
P_D	Power Dissipation	Refer to Appendix "POWER DISSIPATION"	
Tj	Junction Temperature Range	−40 to 85	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	2.3 to 5.5	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

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ELECTRICAL CHARACTERISTICS

The specifications surrounded by ☐ are guaranteed by design engineering at $-40°C \leq Ta \leq 85°C$.

R1801K   Electrical Characteristics   (Ta = 25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	$V_{IN} \geq V_{SET}$ + 0.5 V, $V_{VSET1\sim3}$ = "L", at no load	V_{SET} x0.97		V_{SET} x1.03	V
		$V_{IN} \geq V_{SET}$ + 0.5 V, $V_{VSET1\sim3} \neq$ "L", at no load	V_{SET} x0.96		V_{SET} x1.04	
I_Q	Operating Quiescent Current	V_{IN} = 5.0 V, V_{VFB} = 3.0 V, device not switching VFB pin current is converted by V_{IN} current		200	420	nA
$V_{MP}{}^*$	Accuracy of Maximum Power Point Control Voltage	V_{VFB} = 0 V	$V_{MP}{}^*$ -200		$V_{MP}{}^*$ +200	mV
V_{PGH}	PG"H" Detection Voltage	V_{IN} = 5.5 V, V_{FB} rising	V_{OUT} x0.845	Vout × 0.9	V_{OUT} x0.955	V
V_{PGL}	PG"L" Detection Voltage	V_{IN} = 5.5 V, V_{FB} falling	1.8	1.9	2.19	V
$I_{VMP1\ to\ 3}$	VMP1 to 3 Pin "H"/"L"Leakage Current	V_{IN} = 5.5V, $V_{VMP1\ to\ 3}$ = 5.5 V / 0 V			0.1	uA
$I_{VSET1\ to\ 3}$	VSET1 to 3 Pin "H"/"L" Leakage Current	V_{IN} = 5.5 V, $V_{VSET1\ to\ 3}$ = 5.5 V / 0 V			0.1	uA
I_{LEAK}	Output Driver "H"/"L" Leakage Current	V_{IN} = 5.5 V, V_{LX} = 5.5 V / 0 V			0.1	uA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).
Test circuit is operated with "Open Loop Control" (GND = 0 V), unless otherwise specified.
* The Accuracy of Maximum Power Point Control Voltage also includes an externally set voltage.

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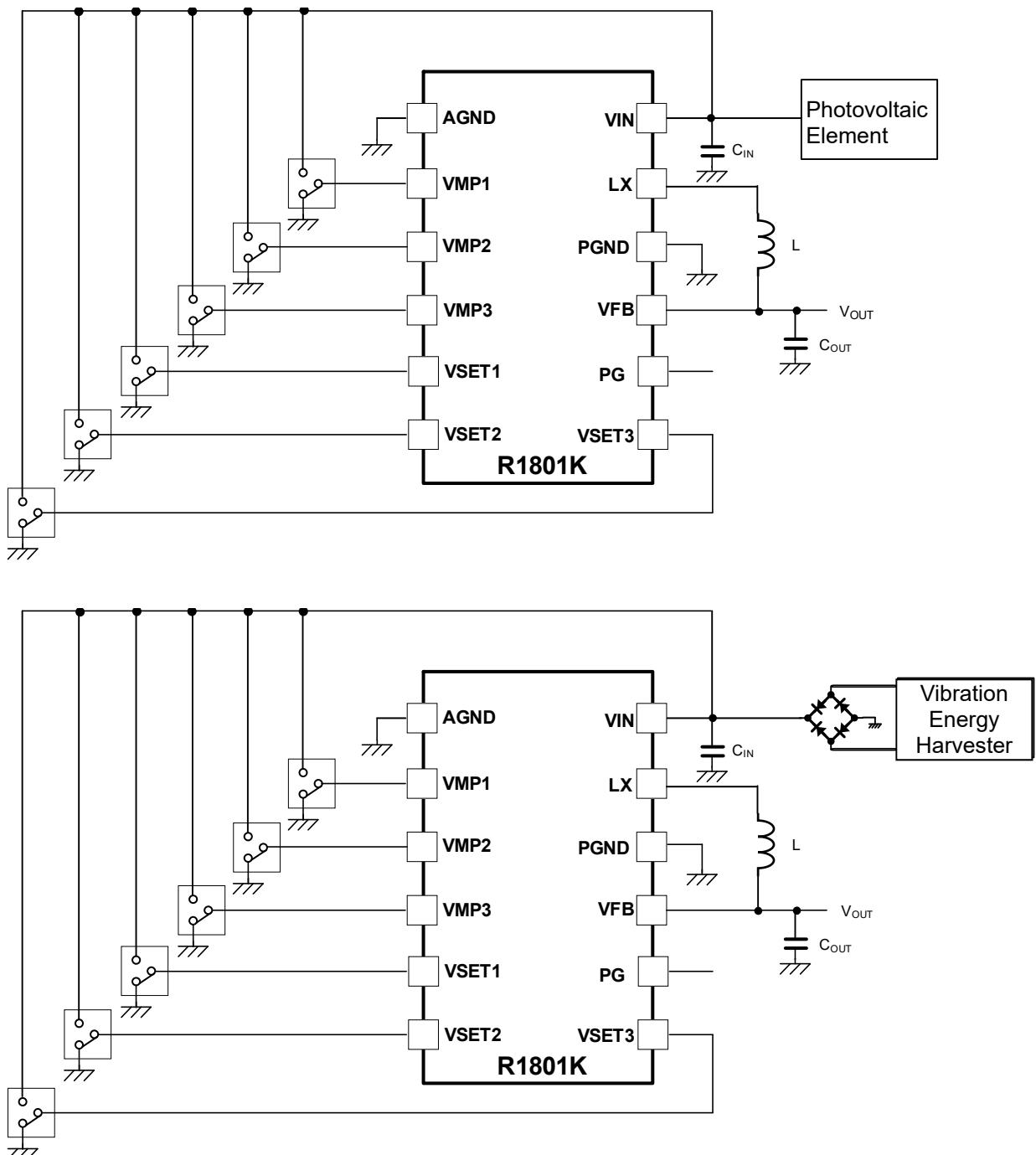
TYPICAL APPLICATION CIRCUIT

R1801K Typical Application Circuit

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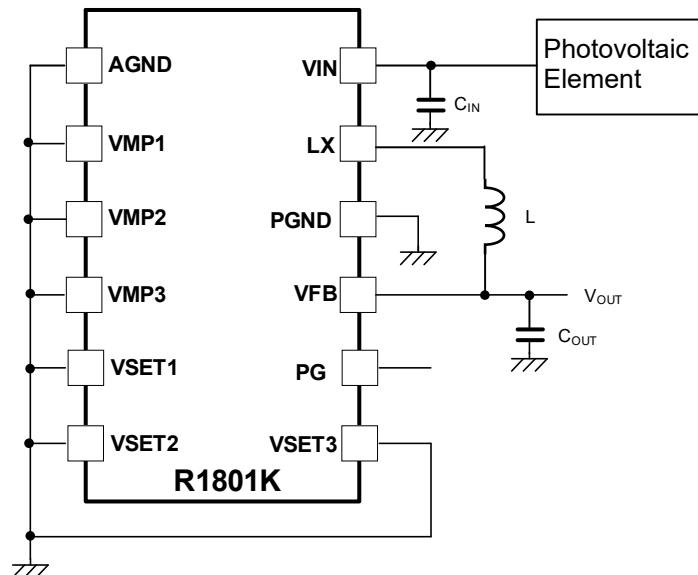
R1801K Typical application circuit when external function is noused

Recommended External Components

Symbol	Descriptions
C_{IN}	Ceramic Capacitor 10 µF or higher
C_{OUT}	Ceramic Capacitor 47 µF or higher, or Ceramic Capacitor 10 µF or higher and Large-capacity Electrical Storage Device
L	Inductor 22 µH

Recommended Large-capacity Electrical Storage Devices

Manufacturer	Product	Part #	Capacity	Type	Notes
TDK	CeraCharge™	BCT1812M101AG	100 µAh	All-solid-state Li-ion	CeraCharge™ is a trademark of TDK
Nichicon	SLB series	SLB03070LR35	350 µAh	Li-ion	
NGK	EnerCera®	ET1210C-R ET2016C-R ET271704P-H	5 mAh 25 mAh 5 mAh	Li-ion	EnerCera® is a trademark of NGK
Murata	CT series	CT04120	3 mAh	Li-ion	

(Note)

When capacitance value of ceramic capacitor is small, output ripple becomes large, then the output ripple may excess the voltage rating of storage battery or subsequent devices.

While considering ESR of storage battery, adjust values of set voltage and ceramic capacitor as not exceeding the voltage rating.

Adjust ceramic capacitor and output ripple values referencing the formula below.

output ripple voltage[V] = 0.45[uC] ÷ C[uF](ceramic capacitor effective capacitance value)

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TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit.
A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

● Use a ceramic capacitor with a lower equivalent series resistance (ESR). A capacitor of 10 µF or higher for C_{IN} between VIN and GND pins is recommended. A ceramic capacitor of 47 µF or higher, or a ceramic capacitor of 10 µF or higher and a large-capacity storage device is recommended for C_{OUT}. Stable operation is guaranteed if the capacitor is above the recommended capacitance value without bias in the operating temperature range. Care must be taken with insulation resistance. Capacitors with low insulation resistance increase leakage current and are not recommended for systems. (Refer to *Measurement Components for Typical Characteristics* in the datasheet)

● It is recommended that the inductor has a rated current (400mA or more), equivalent series resistance, and DC superimposition characteristics that are equal to or higher than spec used when measuring the typical characteristic in the datasheet. If the equivalent series resistance is large or the DC superimposition characteristics are poor, the efficiency will inefficient, additionally note that if the rating is too low, the inductor may be damaged.

● When an intermediate voltage other than VIN or GND is input to the VMP1 to 3 and VSET1 to 3 pins, the supply current may increase due to the cross-conduction current of the IC internal logic circuit. When the VMP1 to 3 and VSET1 to 3 pins are open, the maximum power point control voltage and VSET voltage may vary. When using the IC, connect the VMP1 to 3 and VSET1 to 3 pins to "VIN" or "GND".

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THEORY OF OPERATION

BUCK CONVERTER OPERATION

The basic buck DC / DC converter operation is illustrated in the following figures.

The buck DC / DC converter charges energy in the inductor when the high-side transistor turns ON, and discharges the energy from the inductor when the high-side transistor turns OFF and controls with less energy loss, so that a lower output voltage (V_{OUT}) than the input voltage (V_{IN}) is obtained.
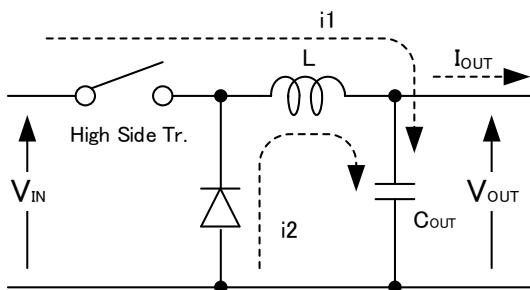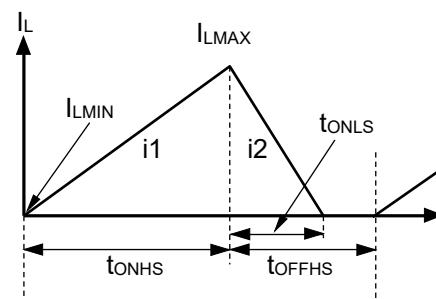
Basic Circuit   **Current through Inductor**

Step1. The high-side transistor turns on, I_L = i1 flows, the inductor is charged with energy, and C_{OUT} is charged to supply the output current (I_{OUT}). At this moment, I_L = i1 increases from $I_L = I_{LMIN}$ = 0 in proportion to the ON time of the high-side transistor (t_{ONHS}), and reaches the maximum value of the current flowing through the inductor (I_{LMAX}).

Step2. When the high-side transistor turns OFF, the inductor flows current I_L = i2 from the diode to maintain $I_L = I_{LMAX}$.

Step3. I_L = i2 decreases gradually, after the ON time of the low-side transistor (t_{ONLS}), becomes $I_L = I_{LMIN}$ = 0.

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ADJUSTABLE MAXIMUM POWER POINT CONTROL / OUTPUT VOLTAGE
When the pin voltage of VMP1 to 3 and VSET1 to 3 is "H", the maximum power voltage and VSET voltage are adjustable externally. 1 corresponds to -100 mV, 2 corresponds to -200 mV and 3 corresponds to +300 mV, and Typ. ± 300 mV is adjustable. However, setting all bits to "H" is a prohibited.
Due to the circuit configuration, the "H" / "L" level threshold voltage of each pin depends on the input voltage.
When setting to "H" voltage, pull up both of VMP / VSET to the input voltage.
When setting to "L" voltage, short it to GND.
All adjustment pins should not be OPEN, use them as "H" / "L" levels.

Regulated Voltage Logic Table of Maximum Power Point Control Voltage

Regulated Voltage	VMP1	VMP2	VMP3
- 300 mV	H	H	L
- 200 mV	L	H	L
- 100 mV	H	L	L
0 mV	L	L	L
100 mV	L	H	H
200 mV	H	L	H
300 mV	L	L	H
Prohibited	H	H	H

Regulated Voltage Logic Table of Output Voltage

Regulated Voltage	VSET1	VSET2	VSET3
- 300 mV	H	H	L
- 200 mV	L	H	L
- 100 mV	H	L	L
0 mV	L	L	L
100 mV	L	H	H
200 mV	H	L	H
300 mV	L	L	H
Prohibited	H	H	H

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MAXIMUM POWER POINT CONTROL
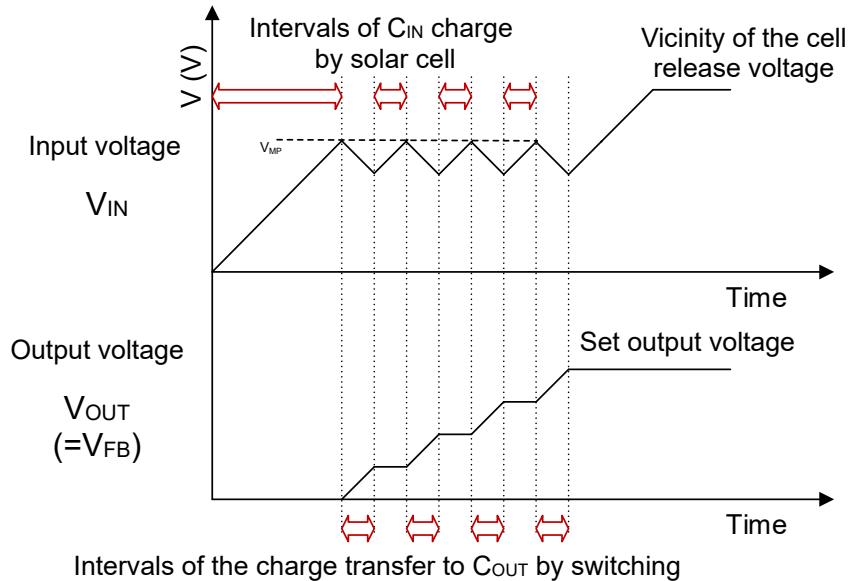
R1801K transfers power to C_{OUT} at maximum power voltage (V_{MP}), which is the operating point of the maximum amount of power generation of a solar cell. After R1801K receives power from the solar cell, the input voltage increases and when it reaches the V_{MP}, a switching starts and the R1801K transfers power to C_{OUT}.

When a power transfer amount exceeds the supplied power from the solar cell, the input voltage decreases by the switching. When the V_{IN} drops below the V_{MP} voltage, the next switching is stopped, the C_{IN} is charged by the solar cell, and the V_{IN} rises. When V_{IN} reaches the V_{MP} voltage, it transfers power to Cout again.

When the input voltage reaches the V_{MP} again, the R1801K transfers power to C_{OUT}. By repeating this operation enables transferring power to C_{OUT} while maintaining the operating point of the maximum amount of power generation of the solar cell.

OPERATION IN STABLE STATE
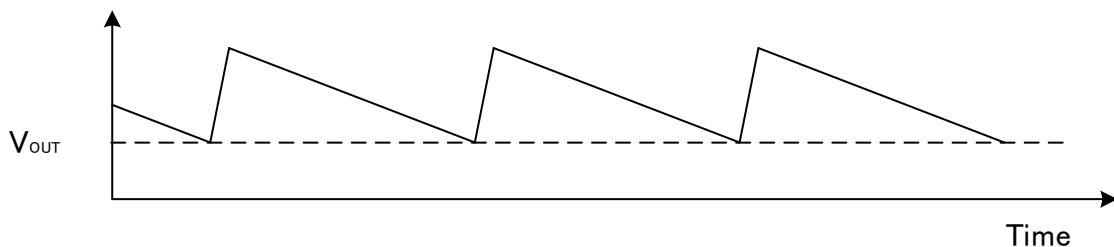
Output Voltage Waveforms Near the Set Voltage

This section explains the R1801K's operation when the output voltage rises to the set voltage When the output voltage exceeds the set voltage, the R1801K stops switching even if the V_{IN} voltage exceeds the V_{MP} voltage. After that, switching resumes when the output voltage decreases below the V_{OUT} voltage due to the load etc. R1801K repeats the above operation to keep the output voltage at the set voltage.

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POWER GOOD (PG) FUNCTION

When switching starts and the V_{OUT} voltage exceeds the PG"H" voltage (V_{OUT} × 90%), after 4 ms (Typ.), the "H" signal is output from the PG pin. The output status can be determined by the PG pin voltage, enabling sequence control.

Once the PG pin voltage has risen, the "L" signal is not output until the V_{OUT} voltage decreases below 1.9 V (Typ.) or lower.

During the period of PG ="H", the same voltage as the V_{OUT} voltage is output.

In addition, since the PG function operates using the FB pin's voltage as the power supply, it works regardless whether V_{IN} is supplied or not.

For example, in a system that operates intermittently several times a day, if a large-capacity storage device is connected to the C_{OUT}, if the V_{OUT} voltage is 1.9 V, the PG will continue to hold the H voltage even if the V_{IN} disappears.

However, in order to secure the minimum operating voltage of the PG function, set the V_{SET} voltage to 2.5 V or higher when using the PG function.

Sequence of PG function
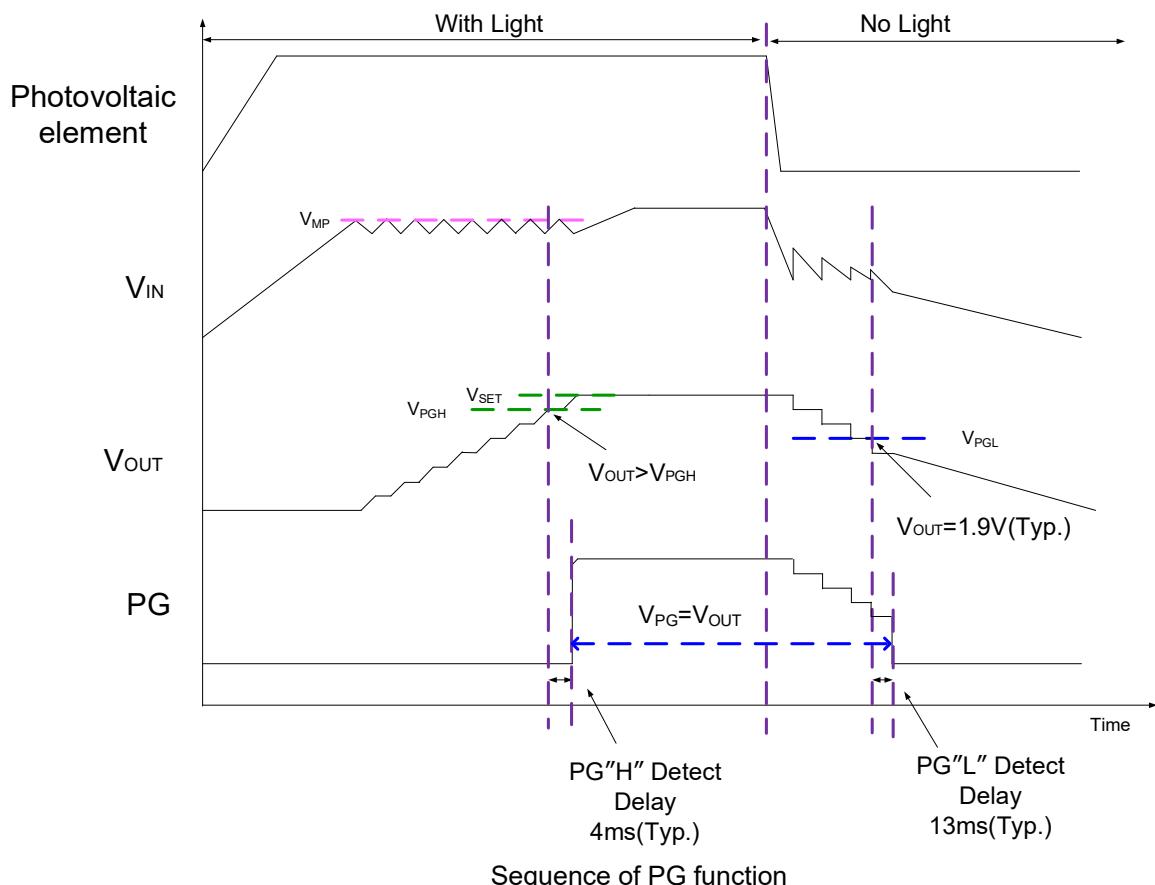
REVERSE CURRENT PROTECTION
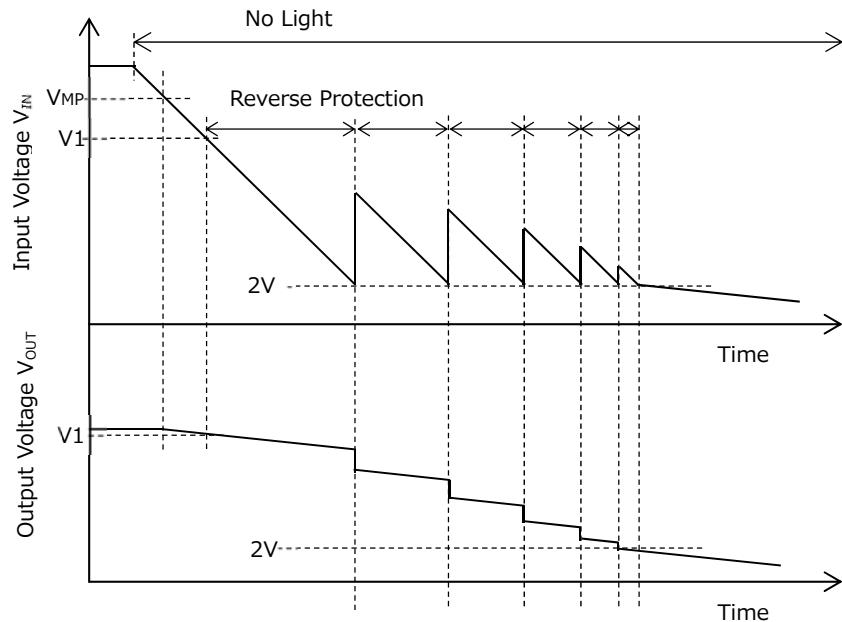
The R1801K has a reverse current protection to prevent the electric charge stored in the C_{OUT} or the large-capacity power storage device connected to the VFB pin from flowing back to the IC even if the light irradiation when the solar cell is cut off. This keeps the charge stored in the C_{OUT} and large-capacity power storage devices for a long time.

When the light is cut off, the charge stored in the C_{IN} is consumed as the supply current to the IC, and the input voltage V_{IN} slowly drops. When the input voltage becomes lower than the output voltage V_{OUT}, the reverse current protection works, so even if $V_{IN} \leq V_{OUT}$, the charge stored in the C_{OUT} or the large-capacity power storage device does not flow back to the IC side.

An input voltage of 2 V or higher is required for the reverse current protection to operate. When the input voltage drops below 2 V, the reverse current protection is canceled and the charge on the output side flows back to the input side through the IC.

If $V_{IN} \geq 2V$, the reverse current protection will work again. Normally, the backflow of charge from the output to the input is completed in a short time, and the input voltage rises to near the output voltage. By repeating this, the input voltage and output voltage will decrease.

Due to variations in the reverse current protection detection threshold, here is a possibility to be detected as the reverse status even when $V_{IN} = V_{OUT}$. It is recommended to set as $V_{MPSET} \geq V_{SET} + 0.5$ V.

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APPLICATION INFORMATION

CODE LIST

Product Name	V_{SET} （$V_{SET1\sim3}$="L"） [V]	V_{MP} （$V_{MP1\sim3}$="L"） [V]
R1801K001A	2.8	3.7
R1801K002A	2.8	4.1
R1801K003A	3.5	4.1
R1801K004A	2.8	4.5
R1801K005A	3.5	4.5
R1801K006A	2.6	3.1
R1801K007A	2.8	4.9
R1801K008A	3.5	4.9

* Please contact us for other than code listed above.

PCB LAYOUT
R1801K
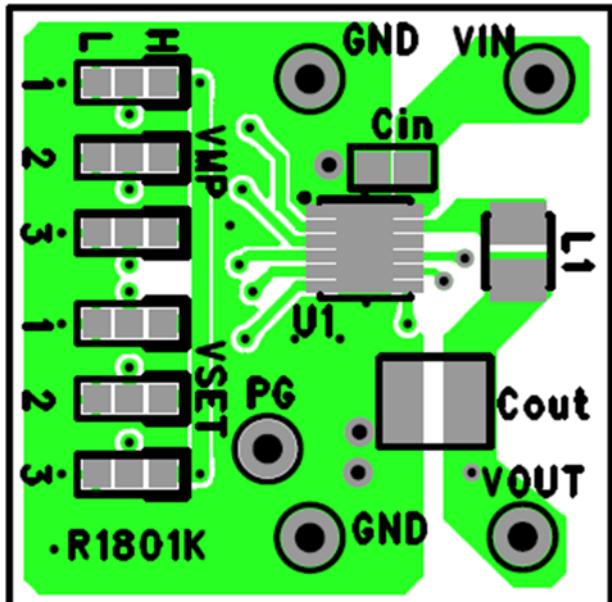
Top Layer

Bottom Layer

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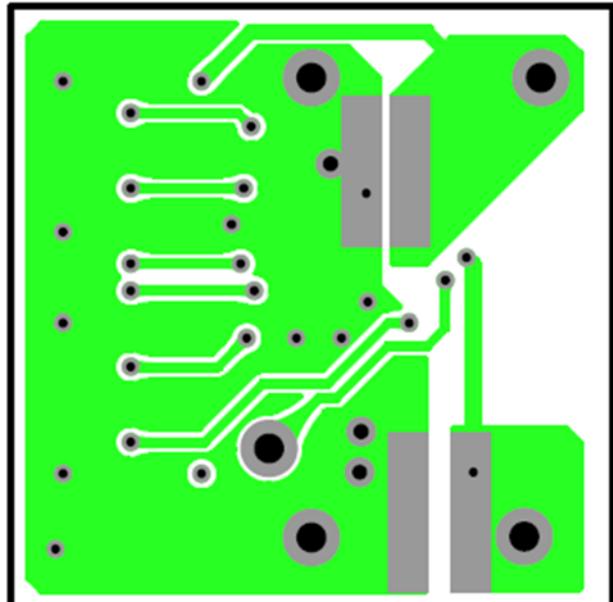
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Efficiency vs. Output Current

V_{SET} = 2.8 V

2) Quiescent Current vs. Temperature

V_{IN} = 5.0 V, V_{FB} = 3.0 V

3) Output Voltage vs. Output Current

V_{SET} = 2.8 V
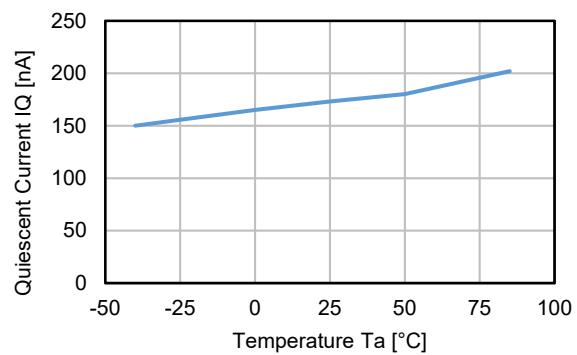
4) Minimum Starting Power

V_{SET} = 3.3 V, I_{IN} = 222 nA

5) Start with Power Generation Element

Using R1801K003A**,**
Power Generation Element= AM-1801
V_{MP} = 4.0 V, V_{SET} = 3.3 V

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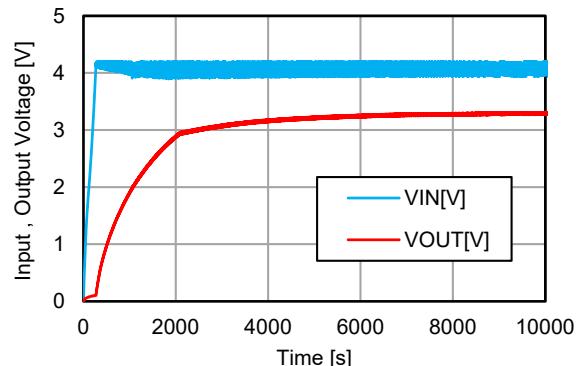
Test Circuit and Components for Measurement
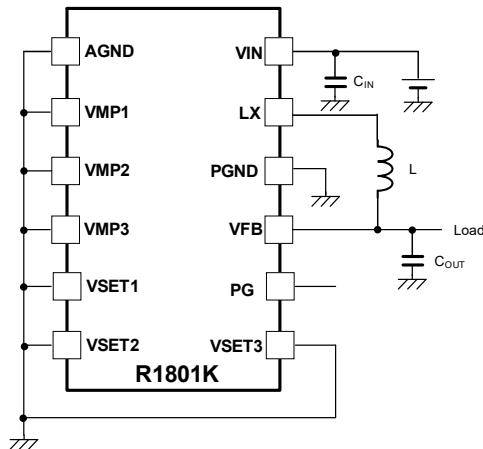
Test Circuit for Typical Characteristics 1) to 4)

Measurement Components for Typical Characteristics

Symbol	Specification	Manufacturer	Parts number
C_{IN}	10µF	TDK	C1608X5R1E106M
C_{OUT}	47µF	TDK	C3216X6S1A476M160AC
L	22µH	TDK	VLS201612CX-220M
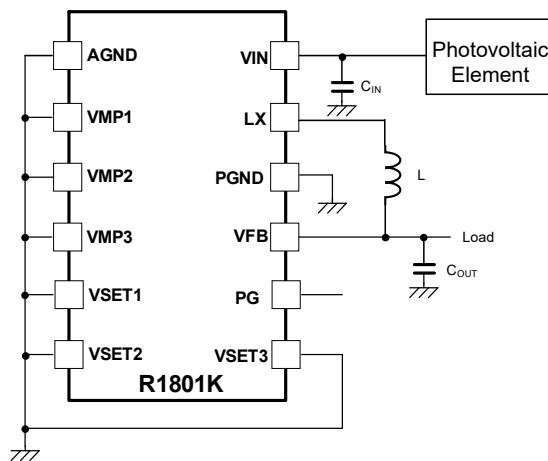
Test Circuit for Typical Characteristics 5)

(When connecting to photovoltaic element, large-capacity capacitor)

Measurement Components for Typical Characteristics

Symbol	Specification	Manufacturer	Parts number
Photovoltaic Element	Open Circuit Voltage 5.0V (at White Fluorescent Lighting 200lx)	Panasonic	AM-1801
C_{IN}	10μF	TDK	C1608X5R1E106M
C_{OUT} *1	1mF	Rubycon	10ZLH1000MEFC8X16
L	22μH	TDK	VLS201612CX-220M

*1 Used as an alternative of a large-capacity electrical storage device.

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POWER DISSIPATION

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions.
The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 23 pcs

Measurement Result

(Ta = 25°C, Tjmax = 85°C)

Item	Measurement Result
Power Dissipation	1850 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter
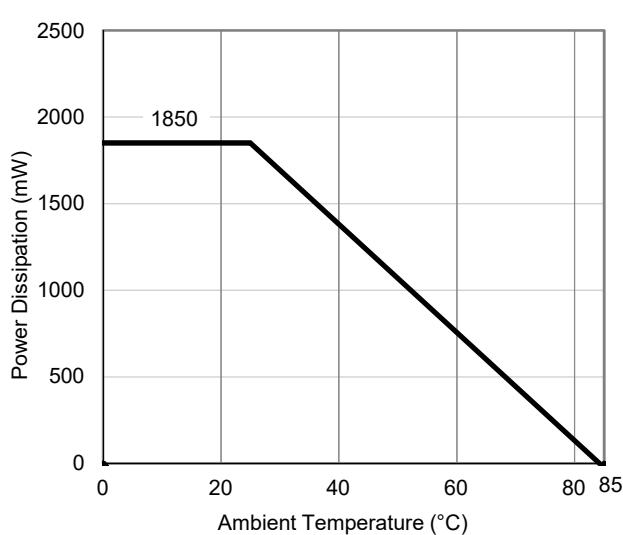
Power Dissipation vs. Ambient Temperature
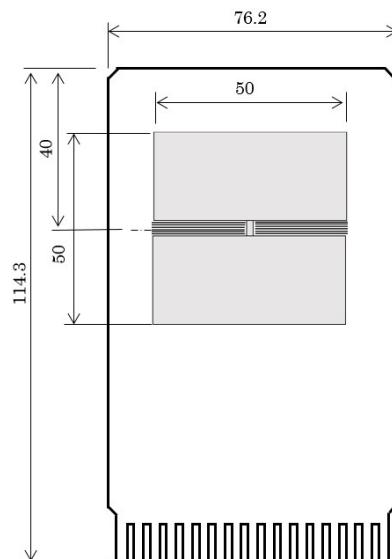
Measurement Board Pattern

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DFN(PLP)2730-12 Package Dimensions (Unit: mm)

RICOH RICOH ELECTRONIC DEVICES CO., LTD.

Official website
https://www.n-redc.co.jp/en/
Contact us
https://www.n-redc.co.jp/en/buy/

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