ISL80020, ISL80020A, ISL80015, ISL80015A

Compact Synchronous Buck Converters

FN6692
Rev 3.00
June 5, 2015

The ISL80020, ISL80020A, ISL80015 and ISL80015A are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver up to 2A of continuous output current from a 2.7V to 5.5V input supply. They use peak current mode control architecture to allow very low duty cycle operation. They operate at either 1MHz or 2MHz switching frequency, thereby providing superior transient response and allowing for the use of small inductors. They have excellent stability.

The ISL80020, ISL80020A, ISL80015 and ISL80015A integrate very low $r_{DS(ON)}$ MOSFETs in order to maximize efficiency. In addition, since the high-side MOSFET is a PMOS, the need for a Boot capacitor is eliminated, thereby reducing external component count. They can operate at 100% duty cycle (at 1MHz).

The device is configured in PWM (pulse width modulation) for fast transient response, which helps reduce the output noise and RF interference.

These devices are offered in a space saving 8 pin 2mmx2mm TDFN lead free package with exposed pad for improved thermal performance. The complete converter occupies less than $64mm^2$ area.

Related Literature

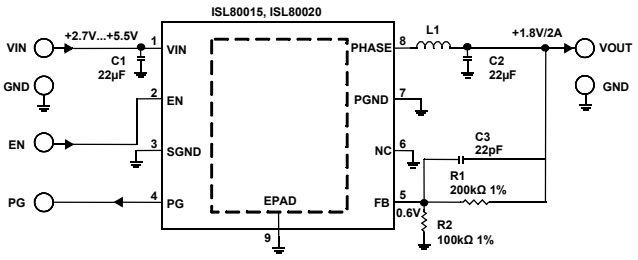
UG026, “ISL800xxxDEMO1Z Demonstration Boards User Guide”

Features

- V_{IN} range 2.7V to 5.5V
- I_{OUT} maximum is 1.5A or 2A (see Table 1 on page 2)
- Switching frequency is 1MHz or 2MHz (see Table 1 on page 2)
- Overcurrent and short circuit protection
- Over-temperature/thermal protection
- Negative current protection
- Power-good and enable
- 100% duty cycle (1MHZ)
- Internal soft-start and soft-stop
- V_{IN} undervoltage lockout and V_{OUT} overvoltage protection
- Up to 95% peak efficiency

Applications

- General purpose POL
- Industrial, instrumentation, and medical equipment
- Telecom and networking equipment
- Game console



$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 1)}$$

FIGURE 1. TYPICAL APPLICATION CIRCUIT CONFIGURATION

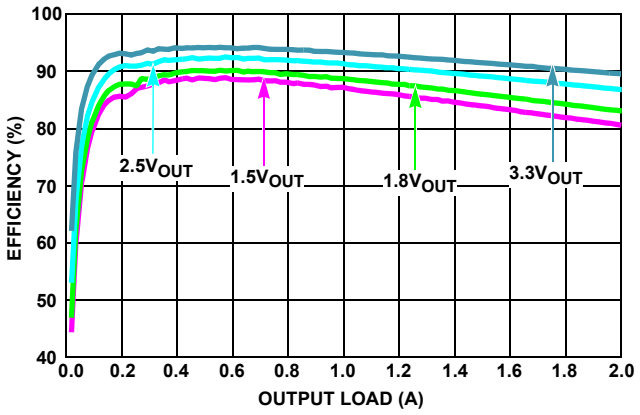


FIGURE 2. EFFICIENCY vs LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

TABLE 1. SUMMARY OF KEY DIFFERENCES

PART#	I_{OUT} (MAX) (A)	f_{SW} (MHz)	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	PACKAGE SIZE
ISL80015	1.5	1	2.7 to 5.5	0.6 to 5.5	8 pin 2mmx2mm TDFN
ISL80015A	1.5	2			
ISL80020	2	1			
ISL80020A	2	2			

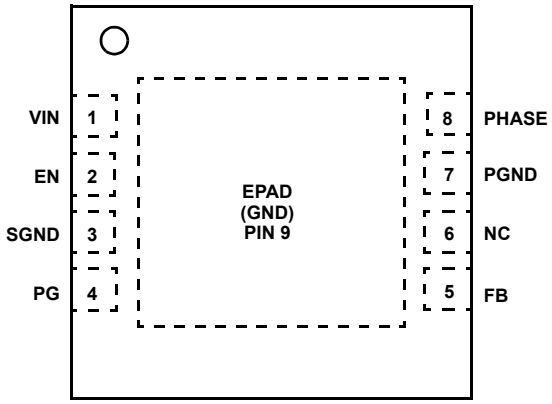
NOTE: In this datasheet, the parts listed in the table are collectively called “device”.

TABLE 2. COMPONENT VALUE SELECTION TABLE

V_{OUT} (V)	C1 (µF)	C2 (µF)	C3 (pF)	L1 (µH)	R1 (kΩ)	R2 (kΩ)
0.8	22	22	22	1.0~2.2	33	100
1.2	22	22	22	1.0~2.2	100	100
1.5	22	22	22	1.0~2.2	150	100
1.8	22	22	22	1.0~3.3	200	100
2.5	22	22	22	1.5~3.3	316	100
3.3	22	22	22	1.5~4.7	450	100

Pin Configuration

ISL80020, ISL80020A, ISL80015, ISL80015A
(8 LD 2x2 TDFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	PIN DESCRIPTION
1	VIN	The input supply for the power stage of the PWM regulator and the source for the internal linear regulator that provides bias for the IC. Place a minimum of 10µF ceramic capacitance from VIN to GND and as close as possible to the IC for decoupling.
2	EN	Device enable input. When the voltage on this pin rises above 1.4V, the device is enabled. The device is disabled when the pin is pulled to ground. When the device is disabled, a 100Ω resistor discharges the output through the PHASE pin. See Figure 3, "FUNCTIONAL BLOCK DIAGRAM" on page 4 for details.
3	SGND	Connect pin 3 to EPAD
4	PG	Power-good output is pulled to ground during the soft-start interval and also when the output voltage is below regulation limits. There is an internal 5MΩ internal pull-up resistor on this pin.
5	FB	Feedback pin for the regulator. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the power-good PWM regulator's power-good and undervoltage protection circuits use FB to monitor the output voltage.
6	NC	Connect NC pin to EPAD
7	PGND	Power and analog ground connections. Connect directly to the board GROUND plane.
8	PHASE	Power stage switching node for output voltage regulation. Connect to the output inductor. This pin is discharged by an 100Ω resistor when the device is disabled. See Figure 3, "FUNCTIONAL BLOCK DIAGRAM" on page 4 for details.
9	E PAD	The exposed pad must be connected to the PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the PGND plane for optimal thermal performance.

Functional Block Diagram

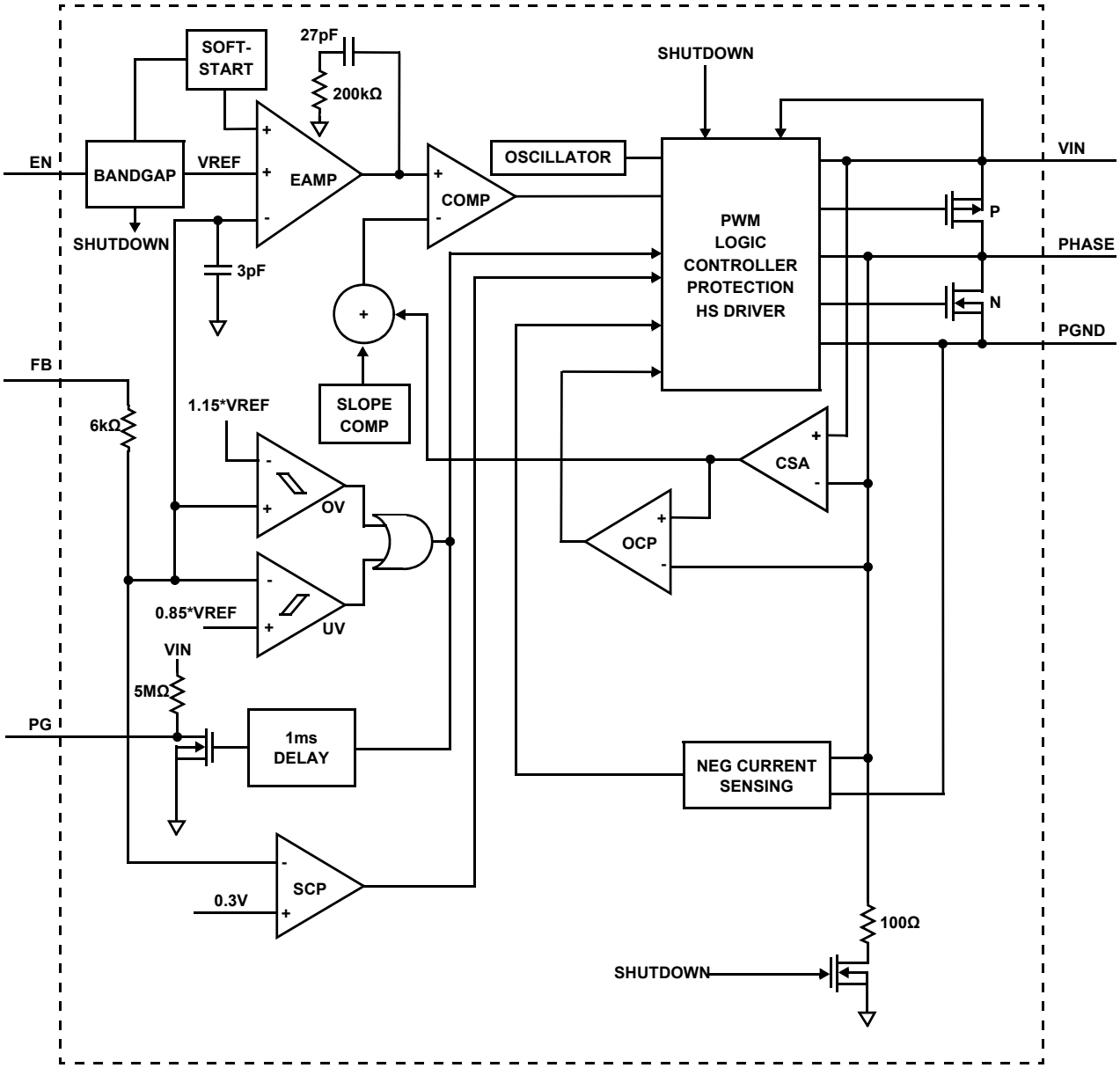


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TAPE AND REEL QUANTITY	PART MARKING	TECHNICAL SPECIFICATIONS	TEMP. RANGE (°C)	PACKAGE Tape and Reel (RoHS Compliant)	PKG. DWG. #
ISL80020IRZ-T	1000	020	2A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80020IRZ-T7A	250	020	2A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80020AIRZ-T	1000	20A	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80020AIRZ-T7A	250	20A	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80015IRZ-T	1000	015	1.5A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80015IRZ-T7A	250	015	1.5A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80015AIRZ-T	1000	A15	1.5A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80015AIRZ-T7A	250	A15	1.5A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80020FRZ-T	1000	20F	2A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80020FRZ-T7A	250	20F	2A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80020AFRZ-T	1000	0AF	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80020AFRZ-T7A	250	0AF	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80015FRZ-T	1000	15F	1.5A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80015FRZ-T7A	250	15F	1.5A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80015AFRZ-T	1000	5AF	1.5A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80015AFRZ-T7A	250	5AF	1.5A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL80020, ISL80020A, ISL80015, ISL80015A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VIN . . . . . -0.3V to 6V (DC) or 7V (20ms)
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6V (DC) or 7V (20ms)
EN, PG . . . . . -0.3V to VIN + 0.3V
FB . . . . . -0.3V to 2.7V
Junction Temperature Range at 0A . . . . . +150°C
ESD Rating
Human Body Model (Tested per JESD22-JS-001). 4kV
Machine Model (Tested per JESD22-A115C) 300V
Charged Device Model (Tested per JESD22-C101D) 2kV
Latch-up (Tested per JESD78D, Class 2, Level A) . . . ± 100mA at +125°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x2 TDFN Package	71	7

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +125°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 2A
Temperature . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.4		V
Quiescent Supply Current	I_{VIN}	f_{SW} = 1MHz, no load at the output		7	**15**	mA
		f_{SW} = 2MHz, no load at the output		10	**22**	mA
Shutdown Supply Current	I_{SD}	V_{IN} = 5.5V, EN = low		1.2	**10**	µA
OUTPUT REGULATION						
Feedback Voltage	V_{FB}		**0.594**	0.600	**0.606**	V
		T_A= -40°C to +125°C	0.589		0.606	V
VFB Bias Current	I_{VFB}	V_{FB} = 2.7V, T_A = -40°C to +125°C	-350	50	350	nA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (nominal 3.6V) T_A= -40°C to +125°C	-0.32	-0.05	0.28	%/V
Load Regulation		See (Note 7)		< -0.2		%/A
Soft-start Ramp Time Cycle (Note 7)				1		ms
PROTECTIONS						
Positive Peak Current Limit	IPLIMIT	2A application (V_{IN} = 3.6V)	**2.8**	3.18	**3.6**	A
		1.5A application (V_{IN} = 3.6V)	**2.1**	2.5	**2.9**	A
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis (Note 7)		Temperature falling		25		°C
COMPENSATION						
Error Amplifier Transconductance (Note 7)				40		µA/V
Transresistance	RT		**0.24**	0.3	**0.40**	Ω
PHASE						
P-channel MOSFET ON-resistance		V_{IN} = 5V, I_O = 200mA		117		mΩ
N-channel MOSFET ON-resistance		V_{IN} = 5V, I_O = 200mA		86		mΩ

Electrical Specifications T_A = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	ISL80020, ISL80015	**800**	1000	**1200**	kHz
		ISL80020A, ISL80015A	**1640**	2000	**2360**	kHz
PG						
Output Low Voltage		1mA sinking current			**0.3**	V
Delay Time (Rising Edge)			**0.5**	1	**2.5**	ms
PGOOD Delay Time (Falling Edge)				5		µs
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.1**	µA
OVP PG Rising Threshold			**110**	115	**125**	%
OVP PG Hysteresis				2		%
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				5		%
EN LOGIC						
Logic Input Low					**0.4**	V
Logic Input High			**1.4**			V
Logic Input Leakage Current	I_{EN}	Pulled up to 5.5V		0.1	**1**	µA

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Not tested in production. Characterized using evaluation board. Refer to Figures 8 through 11 load regulation diagrams. +105°C T_A represents near worst case operating point.

Typical Performance Curves

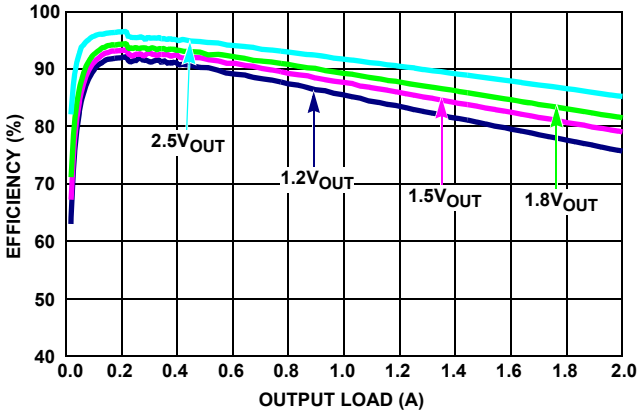


FIGURE 4. EFFICIENCY vs LOAD, f_{SW} = 1MHz, V_{IN} = 3.3V, T_A = +25°C

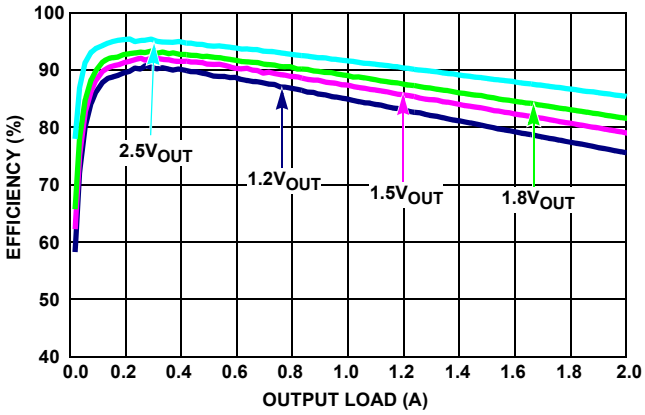


FIGURE 5. EFFICIENCY vs LOAD, f_{SW} = 2MHz, V_{IN} = 3.3V, T_A = +25°C

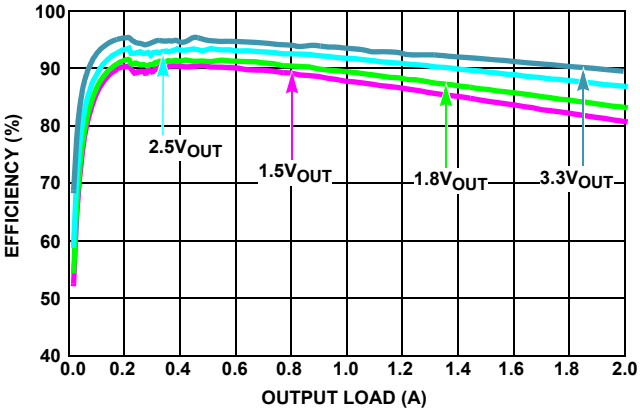


FIGURE 6. EFFICIENCY vs LOAD, f_{SW} = 1MHz, V_{IN} = 5V, T_A = +25°C

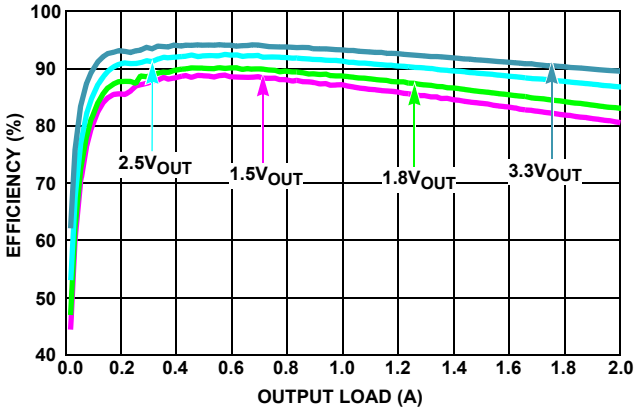


FIGURE 7. EFFICIENCY vs LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

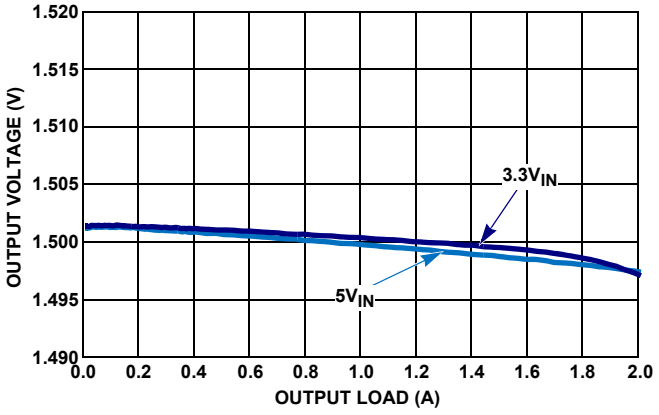


FIGURE 8. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 1.5V, T_A = +25°C

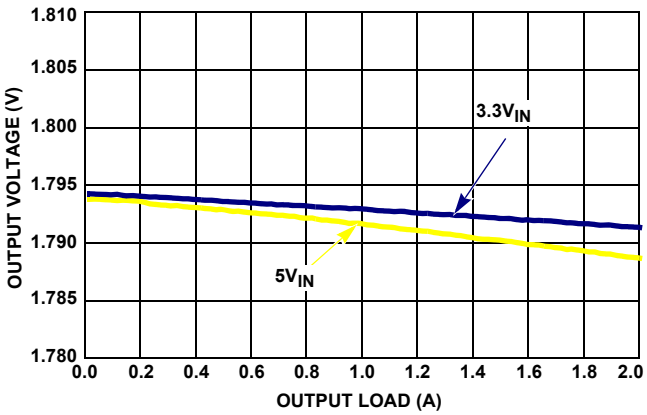


FIGURE 9. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 1.8V, T_A = +25°C

Typical Performance Curves (Continued)

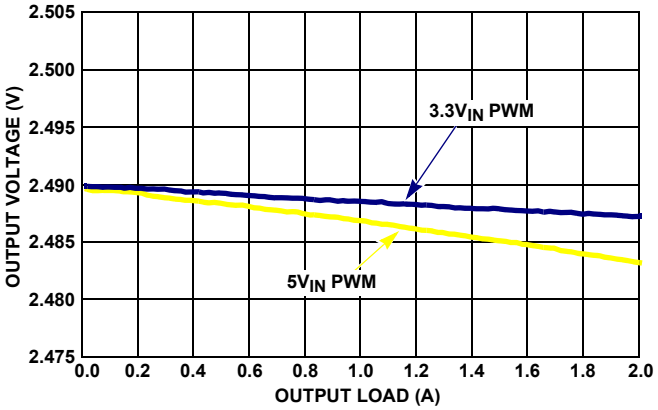


FIGURE 10. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 2.5V, T_A = +25°C

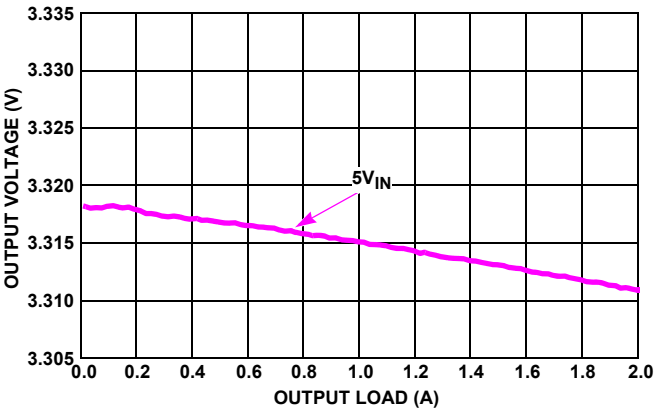


FIGURE 11. V_{OUT} REGULATION vs LOAD, f_{SW} = 2MHz, V_{OUT} = 3.3V, T_A = +25°C

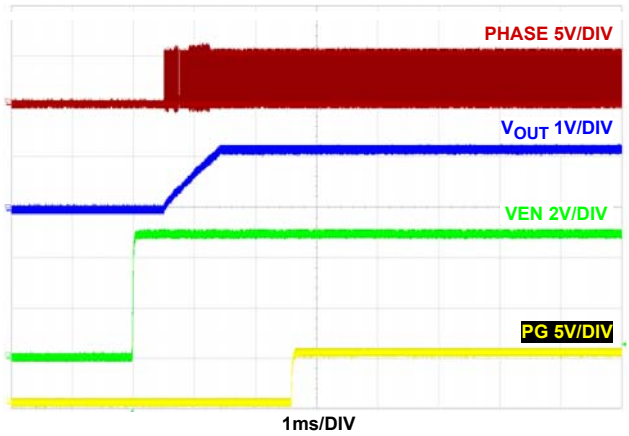


FIGURE 12. START-UP AT NO LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

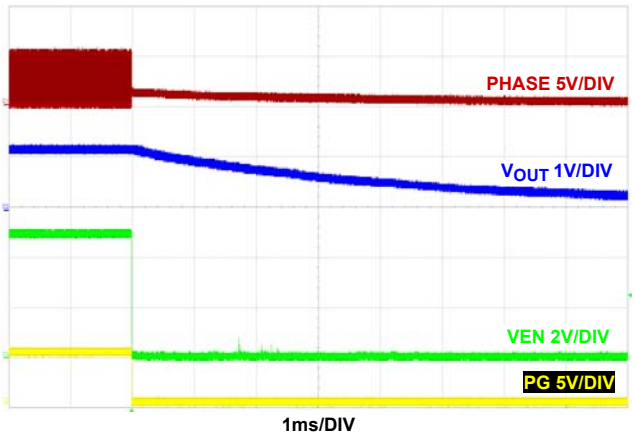


FIGURE 13. SHUTDOWN AT NO LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

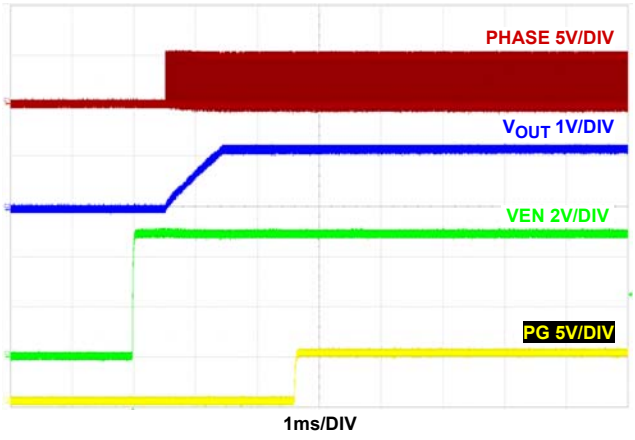


FIGURE 14. START-UP AT 2A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

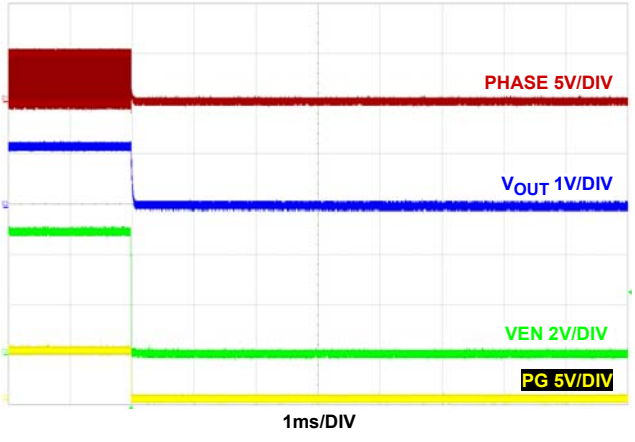


FIGURE 15. SHUTDOWN AT 2A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

Typical Performance Curves (Continued)

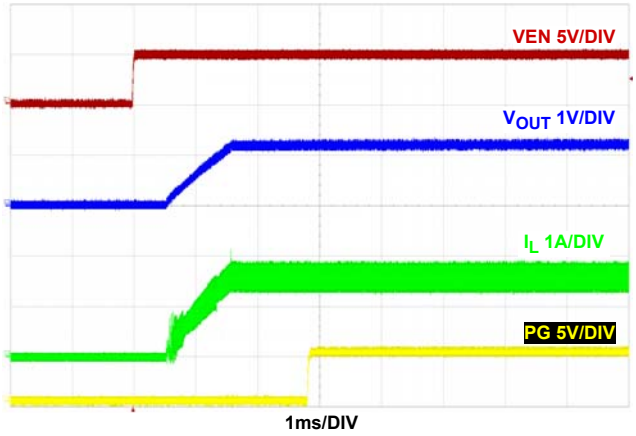


FIGURE 16. START-UP AT 1.5A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

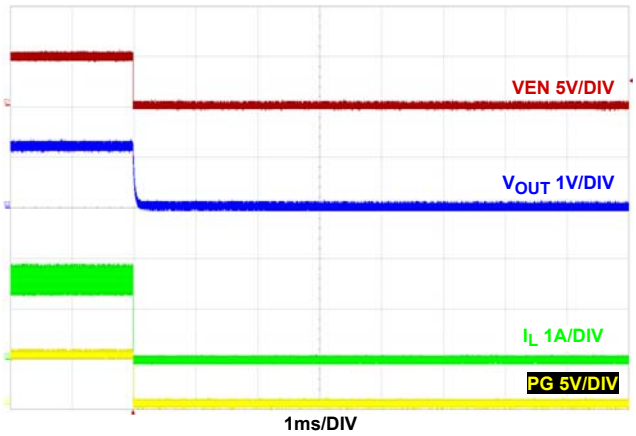


FIGURE 17. SHUTDOWN AT 1.5A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

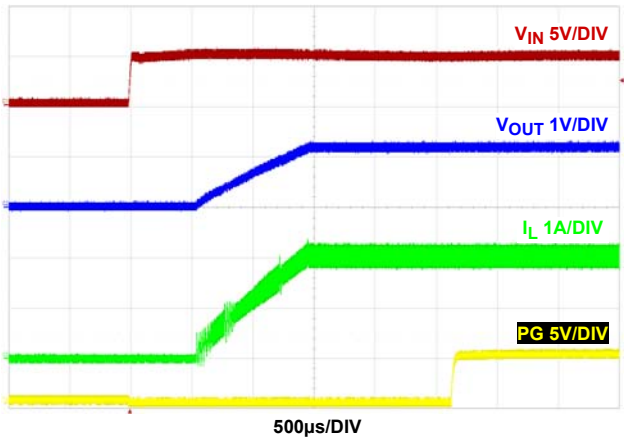


FIGURE 18. START-UP V_{IN} AT 2A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

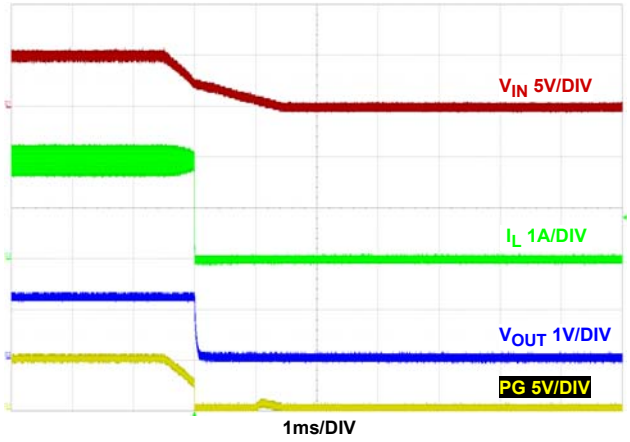


FIGURE 19. SHUTDOWN V_{IN} AT 2A LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

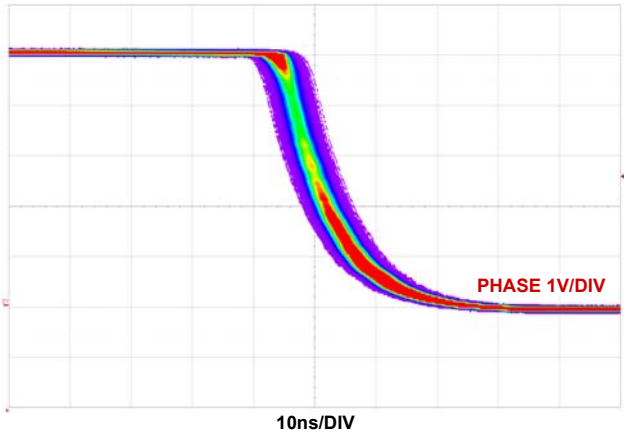


FIGURE 20. JITTER AT NO LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

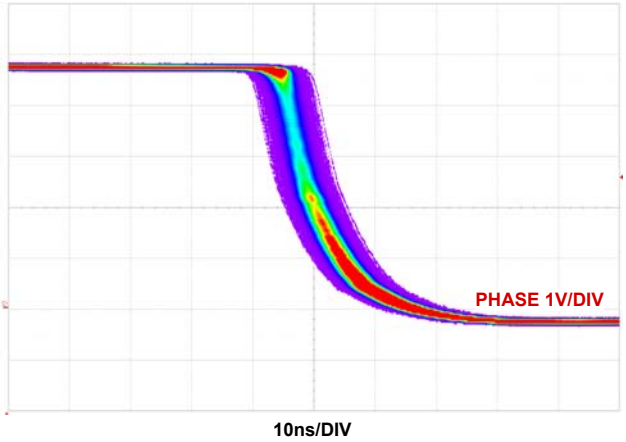


FIGURE 21. JITTER AT FULL LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

Typical Performance Curves (Continued)

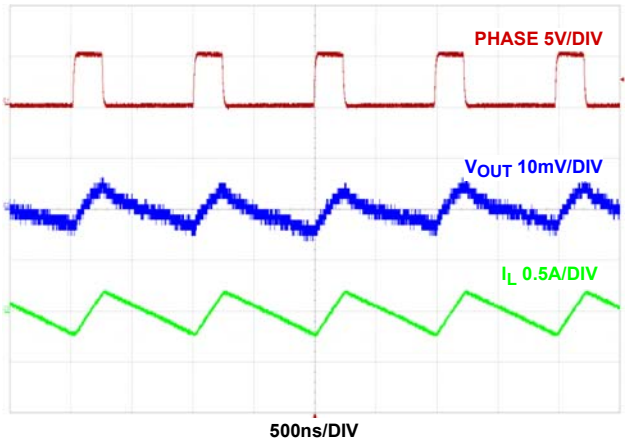


FIGURE 22. STEADY STATE AT NO LOAD, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

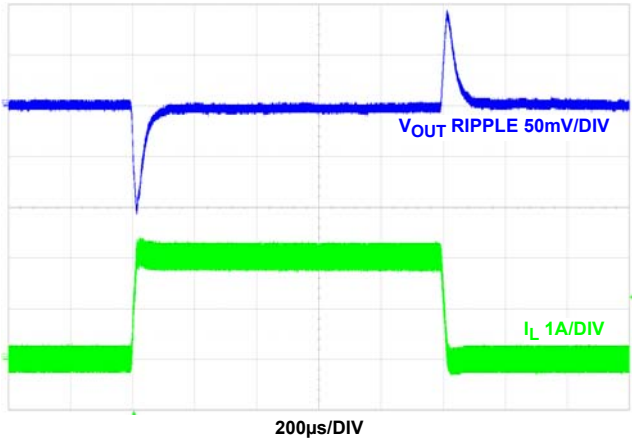


FIGURE 23. LOAD TRANSIENT, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

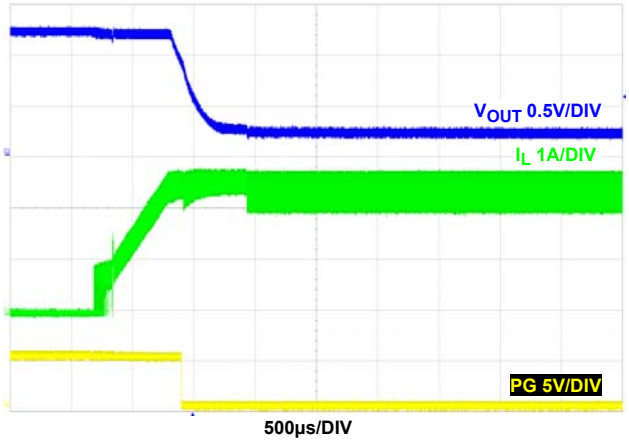


FIGURE 24. OVERCURRENT PROTECTION, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +25°C

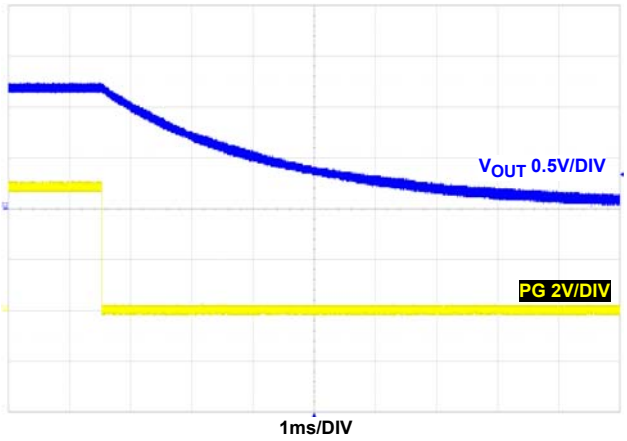


FIGURE 25. OVER-TEMPERATURE PROTECTION, f_{SW} = 2MHz, V_{IN} = 5V, T_A = +163°C

Theory of Operation

The device is a step-down switching regulator optimized for battery powered applications. It operates at a high switching frequency (1MHz or 2MHz), which enables the use of smaller inductors resulting in small form factor, while also providing excellent efficiency. The quiescent current is typically only 1.2µA when the regulator is shut down.

PWM Control Scheme

The device employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. See "Functional Block Diagram" on page 4. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 900mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 300mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-Channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 26 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

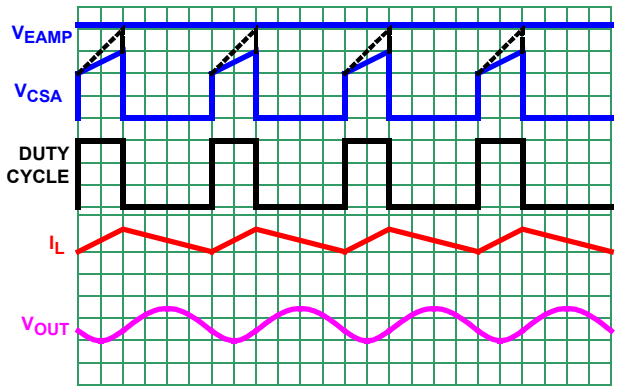


FIGURE 26. PWM OPERATION WAVEFORMS

The reference voltage is 0.6V, which is used by Feedback to adjust the output of the error amplifier, VEAMP. The error amplifier is a trans conductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in the "Functional Block Diagram" on page 4. The current sensing circuit has a gain of 300mV/A, from the P-FET current to the CSA output. When the CSA output reaches a threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. If the overcurrent condition goes away, the output will resume back into regulation point.

Short-Circuit Protection

The short-circuit protection (SCP) comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.3V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in the "Functional Block Diagram" on page 4. When the valley point of the inductor current reaches -1.5A for 2 consecutive cycles, both P-FET and N-FET shut off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation.

PG

PG is an output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as-long-as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 15% above the nominal regulation voltage, the device pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ pull-up resistor to fit most applications. An external resistor can be added from PG to VIN for more pull-up strength.

UVLO

When the input voltage is below the undervoltage lock-out (UVLO) threshold, the regulator is disabled.

Enable, Disable and Soft Start-up

After the VIN pin exceeds its rising POR trip point (nominal 2.5V), the device begins operation. If the EN pin is held low externally, nothing happens until this pin is released. Once the EN is released and above the logic threshold, the internal default soft-start time is 1ms.

Discharge Mode (Soft-stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Thermal Shutdown

The device has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shutdown. As the temperature drops to +125°C, the device resume operation by stepping through the soft-start.

Power Derating Characteristics

To prevent the device from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 2:

$$T_{RISE} = (PD)(\theta_{JA}) \quad \text{(EQ. 2)}$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 3:

$$T_J = (T_A + T_{RISE}) \quad \text{(EQ. 3)}$$

Where T_A is the ambient temperature. For the DFN package, the θ_{JA} is +71°C/W.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

The device delivers full current at ambient temperatures up to +85°C if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level, depending on the input voltage/output voltage combination and the switching frequency. The device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 27 illustrates the approximate output current derating curve versus ambient temperature for the ISL80020EVAL1Z kit.

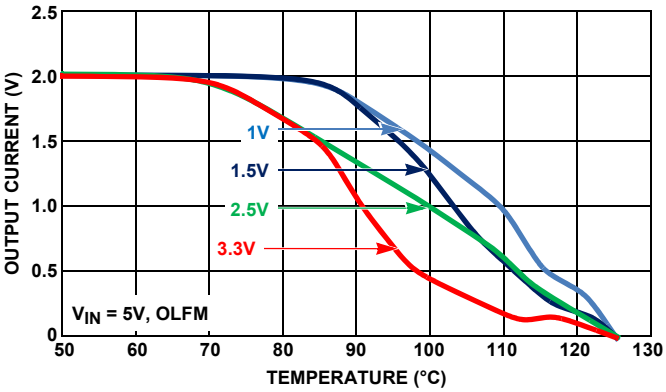


FIGURE 27. DERATING CURVE vs TEMPERATURE

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, the ISL80020A and ISL80015A typically requires a 1.2µH, while the ISL80020 and ISL80015 typically requires a 2.2µH output inductor. Higher or lower inductor values can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor ripple current and output voltage ripple, the output inductor value can be increased. It is recommended to set the inductor ripple current to be approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 4:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_{SW}} \quad \text{(EQ. 4)}$$

The inductor's saturation current rating needs to be at least larger than the peak current.

The device uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier.

The output voltage programming resistor, R_1, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 5.

$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 5)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated and R_1 is shorted. There is a leakage current from VIN to PHASE. It is recommended to preload the output with 10µA minimum. For better performance, add 22pF in parallel with R_1.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good

choice in many applications due to their reliability and extremely low ESR.

Equations 6 and 7 allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR) =

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 6)}$$

Where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 7)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. Equation 8 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * ((V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 8)}$$

Where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load. For an overshoot of 5%, the equation becomes Equation 9:

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (1.05^2 - 1)} \quad \text{(EQ. 9)}$$

Layout Considerations

The PCB layout is a very important converter design step to make sure the designed converter works well. The power loop is composed of the output inductor L's, the output capacitor C_{OUT}, the PHASE's pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as closely as possible to the VIN pin and the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 4 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 5, 2015	FN6692.3	Added Related Literature on page 1. -Thermal information table on page 6: Updated: -Junction Temperature Range: -55°C to +125°C to Maximum Junction Temperature (Plastic Package): +150°C Added: -Ambient Temperature Range: -40°C to +125°C -Operating Junction Temperature Range: -40°C to +125°C -Recommended Operating Conditions on page 6 Updated from “Junction Temperature Range: -40°C to +125°C” to “Temperature: -40°C to +125°C -Electrical Specifications on page 6: In heading: -Changed temperature range, from -40°C to +85°C to: -40°C to +125°C. -Changed from: “TJ = -40°C to +125°C to: “TA = -40°C to +125°C. Under Output Regulation section for test condition updated: -Feedback Voltage from: “TJ = -40°C to +125°C” to “TA = -40°C to +125°C”. -VFB Bias Current from “VFB = 2.7V, TJ = -40°C to +125°C” to “VFB = 2.7V, TA = -40°C to +125°C”. -Line Regulation from “TJ = -40°C to +125°C” to “TA = -40°C to +125°C”. - POD L8.2x2C updated from rev 0 to rev 1. Changes since rev 0: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
April 1, 2015	FN6692.2	Under “Theory of Operation” on page 12, changed typical value from “5µA” to “1.2µA”. Under “Enable, Disable and Soft Start-up” on page 12, changed typical value from “2.7V” to “2.5V”.
February 17, 2015	FN6692.1	Changed MIN value of VFB Bias Current in Electrical Spec Table from -120 to -350.
February 5, 2015	FN6692.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

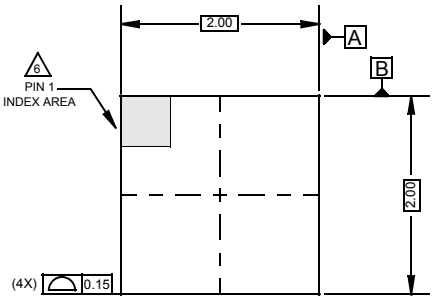
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

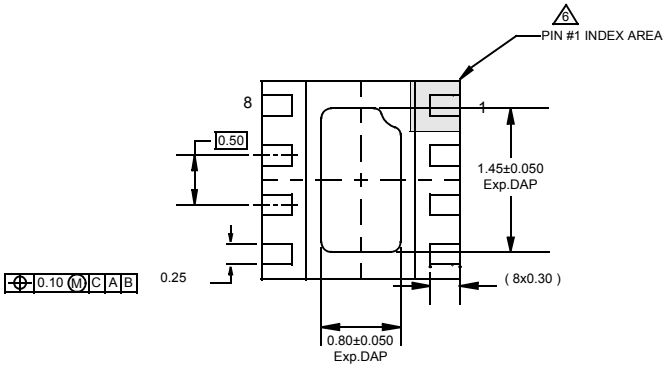
L8.2x2C

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN) WITH E-PAD

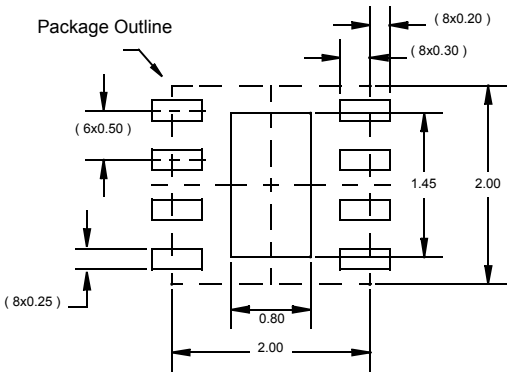
Rev 1, 5/15



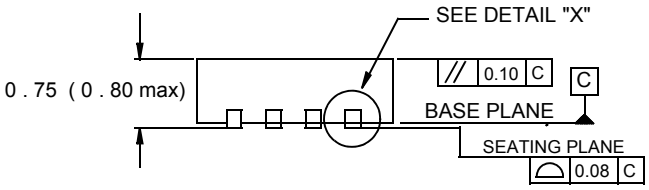
TOP VIEW



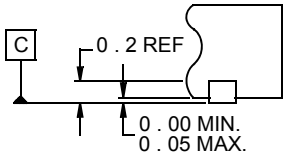
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

ISL80020AFRZ-T7A ISL80020AIRZ-T ISL80020AFRZ-T ISL80020AIRZ-T7A ISL80015IRZ-T7A ISL80015IRZ-T ISL80015FRZ-T7A ISL80015FRZ-T ISL80015AIRZ-T ISL80015AIRZ-T7A ISL80015AFRZ-T7A ISL80015AFRZ-T ISL80020IRZ-T7A ISL80020FRZ-T ISL80020IRZ-T ISL80020FRZ-T7A