RTKA271082DE0000BU

The RTKA271082DE0000BU evaluates the performance of the RAA271082 Automotive PMIC with three synchronous buck regulators and one low dropout linear regulator. The evaluation board is intended for use in point-of-load automotive applications, including camera systems, with 4.5V to 42V input supply range.

In addition to four output voltages, the evaluation board also contains an I²C interface, a RSTB status indicator, and a general purpose I/O (GPIO) signal.

The RAA271082 is offered in a 4mm×4mm 24-lead Step Cut QFN (SCQFN) package with an exposed pad. The RAA271082 is qualified to AEC-Q100, Grade1.

Features

- V_{IN} operating range from 4.0 to 42V
- Start range 4.5 to 42V
- Three synchronous bucks with internal compensation and one LDO
- Fixed Frequency 2.2MHz
- Over-temperature, overcurrent, overvoltage and negative overcurrent protection

Specifications

- V_{IN} range: 4V to 42V
- V_{OUT1} range 2.8V to 5.05V, up to 1A
- V_{OUT2} range 0.85V to 3.3V, up to 1A
- V_{OUT3} range 0.85V to 3.3V, up to 1A
- LDO4 range 2.87V to 3.4V, up to 300mA
- I²C interface
- RSTB and GPIO signals

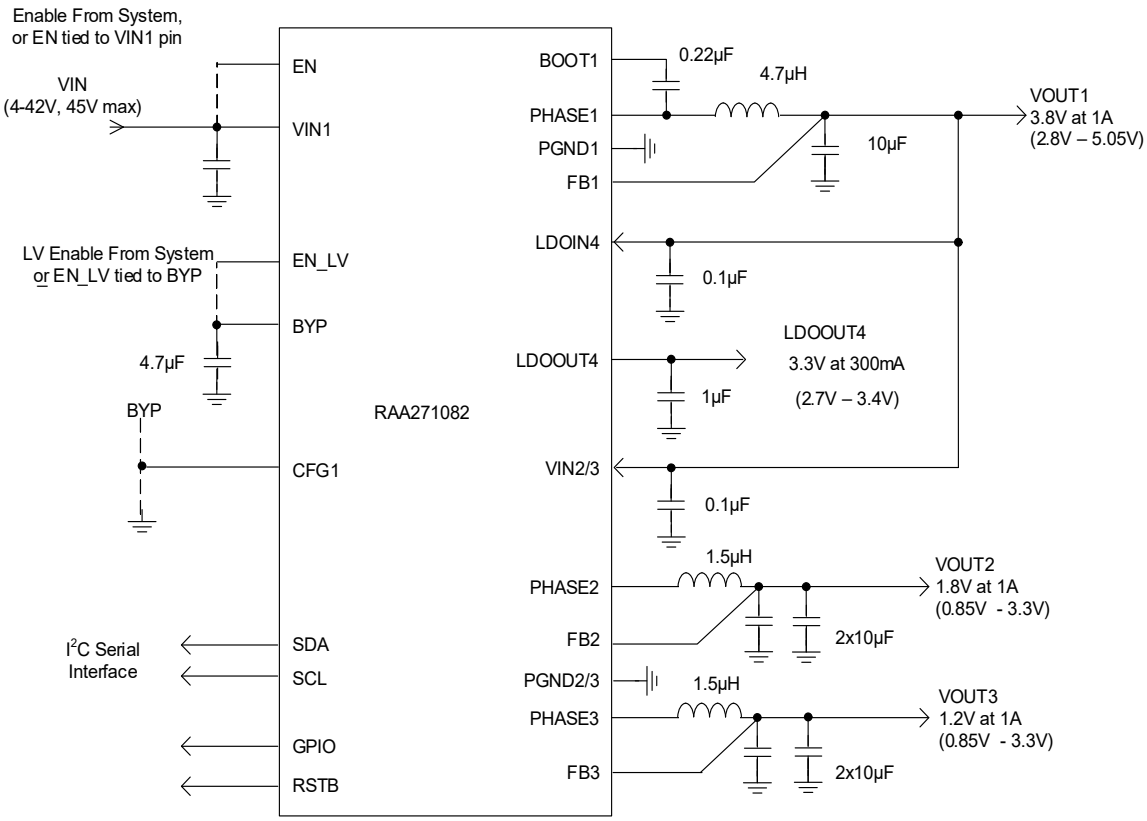

Figure 1. Block Diagram

Contents

1. Functional Description . . . 3
1.1 Manual Output Control using EN and EN_LV . . . 4
1.2 GUI (Graphical User Interface) Control of EN and EN_LV . . . 4
1.3 Testing the Outputs . . . 4
1.3.1 Input and Output Connections and Test Points . . . 5
2. GUI Operation . . . 5
2.1 Changing Programming Options . . . 7
2.2 Fault Status Tab . . . 8
2.2.1 Displaying Detected Faults . . . 9
2.3 Fault Response Mask Tab . . . 10
2.4 Fault to GPIO Control Tab . . . 11
2.5 GPIO Pin Tab . . . 12
2.6 RSTB Pin / WWDT Tab . . . 13
2.6.1 RSTB Operation and Options . . . 13
2.6.2 WWDT Operation and Options . . . 13
2.7 Misc Tab . . . 16
2.7.1 Misc1 Options – Register 0x7B . . . 17
2.7.2 Misc2 Options – Register 0x7C . . . 17
2.7.3 Misc3 Options – Register 0x7D . . . 18
2.8 Reg Map Tab . . . 18
2.9 REA Dongle tab . . . 19
2.10 Log Tab . . . 19
3. Board Design . . . 21
3.1 Layout Guidelines . . . 22
3.2 Schematic Diagram . . . 24
3.3 Bill of Materials . . . 25
3.4 Board Layout . . . 26
4. Typical Performance Graphs . . . 28
5. Ordering Information . . . 30
6. Revision History . . . 30

1. Functional Description

The evaluation board with connections, headers, and test points is shown in Figure 2.

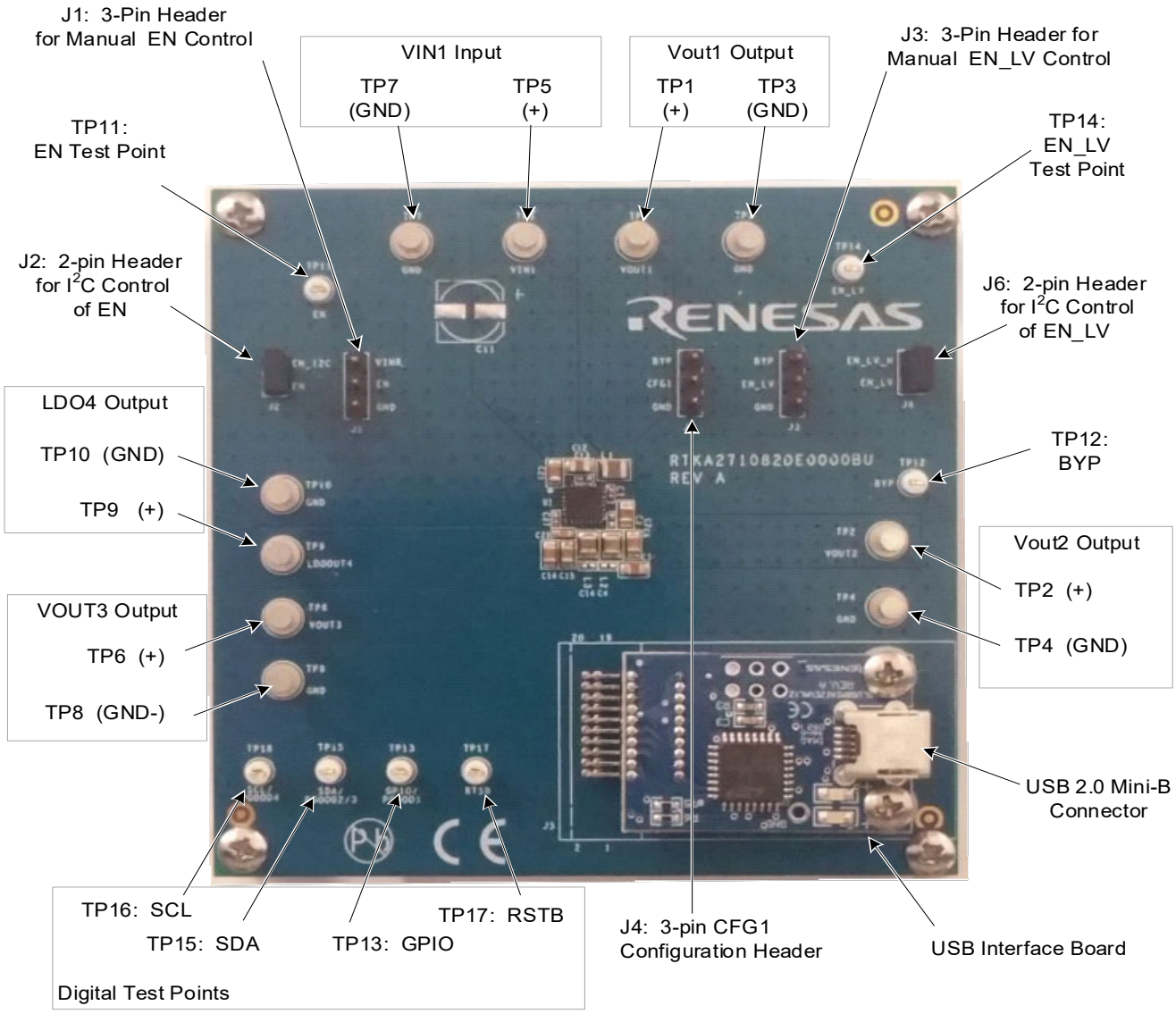

Figure 2. RAA271082 Evaluation Board: Connections, Headers, and Test Points

The EN and EN_LV pins can be manually controlled by installing jumpers J1 (top left) and J3 (top right) as shown in Figure 2. This allows manual control of the Buck1 and Buck2/Buck3/LDO4 regulators.

For EN control, a 2-pin jumper should be installed on either J1 or J2, but not both. Installing both could damage the USB interface board.

For EN_LV control, a 2-pin jumper should be installed on either J3 or J6, but not both. Installing both could damage the USB interface board or the RAA271082 IC.

1.1 Manual Output Control using EN and EN_LV

For manual control of EN, install a jumper on J1 and ensure that J2 jumper is not installed.. The upper position of J1 connects EN to the VIN1 supply and enables the IC. The lower position connects EN to GND and disables the IC. EN can be controlled directly by removing the jumpers from J1 and J2 completely and connecting a DC source to TP11, the EN test point.

The following are the states of the EN:

- EN = GND. The IC is off and in its lowest power state.
- EN = 1.5V. The IC is in Standby Mode. It will communicate through I^2C but all outputs are off. This state cannot be entered using jumpers; removing the jumper and driving EN to 1.5V will enable Standby mode.
- EN > 1.8V. The IC is on and Buck1 (high voltage regulator) is enabled. The low voltage regulators are then enabled/disabled using the EN_LV input.

For manual control of EN_LV, install a jumper on J3 and ensure that J6 jumper is not installed. EN_LV controls outputs Buck2, Buck3, LDO4. The J3 upper position connects EN_LV to the BYP supply and enables the outputs. The J3 lower position connects EN_LV to GND and disables the outputs. EN_LV can also be driven directly by removing the jumper from J3 and J6 and connecting a DC source to TP14, the EN_LV test point.
Note: EN_LV is a low-voltage input limited to 5.5V maximum.

The following are states of the EN_LV:

- EN_LV = GND. The low voltage (Buck2, Buck3, LDO4) outputs are off.
- EN > 1.5V. The low voltage outputs are enabled.

When using manual control of EN and EN_LV, the GUI cannot be used to select options such as output voltage setting, UV and OV thresholds. The GUI is still able to do operations that do not involve option selections, such as:

- Read and clear fault status bits (registers 0x80 – 0x83)
- Enable and disable the IC response to various faults (registers 0x85 – 0x87)
- Enable and disable GPIO and RSTB response to various faults (registers 0x8A – 0x8D)
- Configure and use the Windowed Watchdog Timer (WWDT) (registers 0xA0 – 0xA3)
- Configure the GPIO and RSTB pin functions (registers 0xA4, 0xA5)

1.2 GUI (Graphical User Interface) Control of EN and EN_LV

GUI control of EN and EN_LV is enabled by removing the 2-pin jumpers from J1 and J3, and installing the jumpers on J2 and J6. With GUI control of EN and EN_LV enabled, the GUI provides control of EN and EN_LV and provides added capabilities:

Change option settings for

- Output voltage
- UV and OV thresholds,
- Power-up sequencing, startup delay, shutdown delay

See the I^2C Programming Options section in the *RAA271082 Datasheet* for the full list of available options.

1.3 Testing the Outputs

When the EN and EN_LV inputs have been configured, the outputs can be loaded to perform tests such as load regulation, startup and shutdown, and load transients.

1.3.1 Input and Output Connections and Test Points

The input and output connections are shown in Figure 1 and Table 1

Table 1.

	(+) Test Point	GND Test Point	Default Value (V)
VIN1 (input)	TP5	TP7	12 (4V to 42V, 4.5V to start)
Vout1	TP1	TP3	3.8
Vout2	TP2	TP4	1.8
Vout3	TP6	TP8	1.2
LDO4	TP9	TP10	3.3

The following are more test points (see Figure 1):

- GPIO and RSTB test points located at the bottom edge of the board, TP13 and TP17.
- EN test point at the upper left corner of the board, TP11.
- EN_LV test point at the upper right corner of the board, TP14.
- BYP regulator test point at the right side of the board roughly half way down, TP12.

2. GUI Operation

Before starting the GUI software:

- The USB interface cable must be connected between the host computer and the EVB.
- The VIN1 supply to the EVB must be 4.5V minimum.

For GUI control of EN and EN_LV

- Do not install the jumpers on J1 (top left) and J3 (top right) of the EVB
  - The GUI operates with J1 and J3 installed, but the GUI cannot change options.
- Jumpers must be installed on J2 (top left) and J6 (top right)
  - This allows all the GUI capabilities to operate.

Figure 3 shows the list of the GUI files to be downloaded.

Double-click the RAA271082_GUI_V1.00.exe file to start the GUI software.

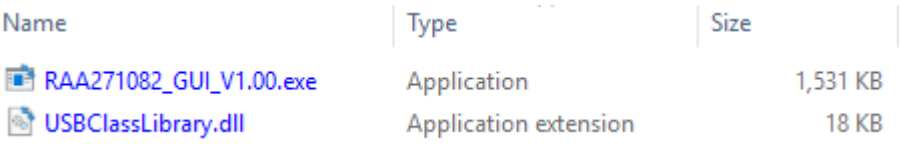

Figure 3. GUI Files

When powered up, the GUI should initially appear as shown in Figure 4.

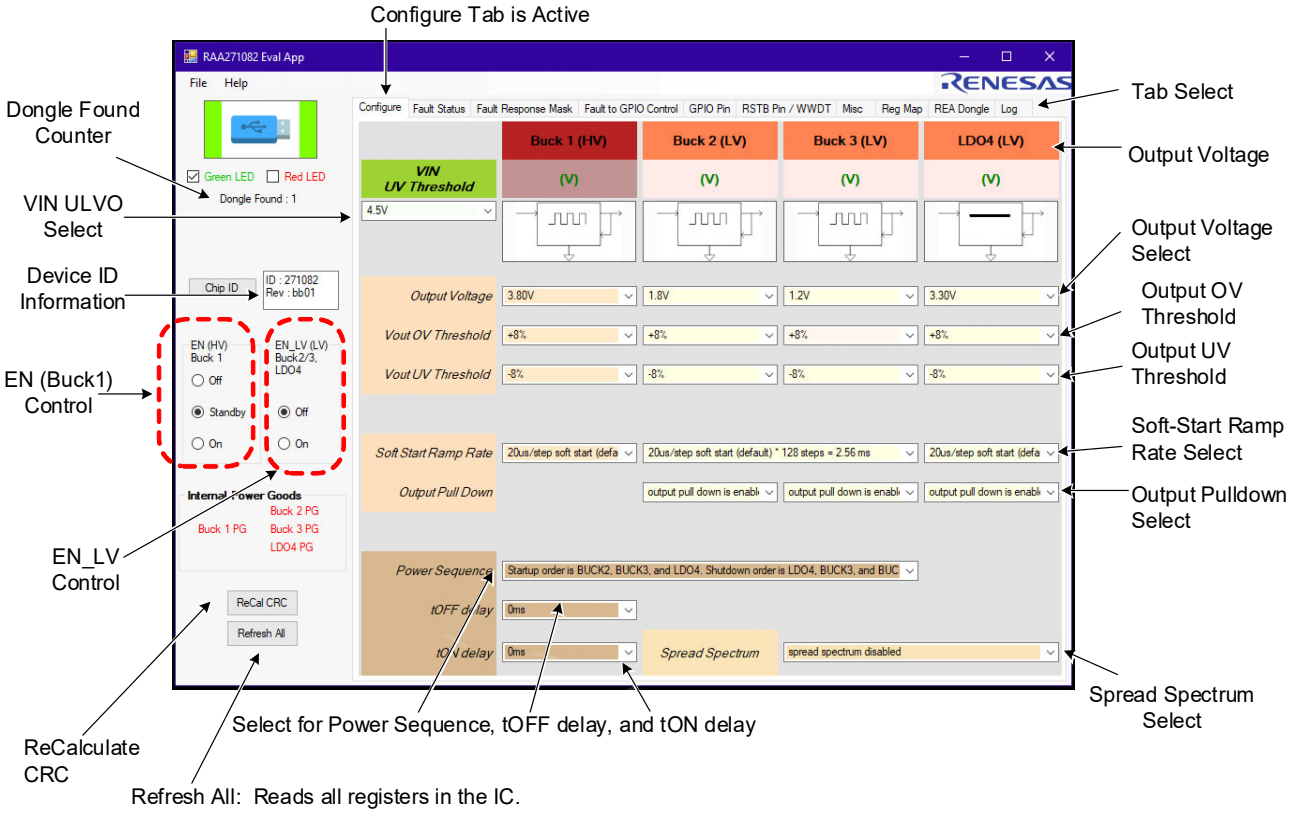

Figure 4. Configure Tab with Labels

The GUI functions are grouped into rows or columns as explained.

The tab shown in Figure 4 is the Configure tab. This tab and the other tabs such as Fault Status, Fault Response Mask are discussed later.

On the right side of the picture, the red arrows point to various functions grouped into rows. **Note:** These rows are shown for the Configure tab; other tabs show different options. The rows are explained as follows:

- **Tab select row:** This row contains buttons for the different tabs in the GUI. Each tab controls a set of functions.

When the tab is selected, the GUI displays the drop-downs and options associated with that tab.

- **Output Voltage:** This row shows the four outputs listed, Buck1, Buck2, Buck3, LDO4.
- **Output Voltage select:** This row contains the drop-downs selecting the output voltages.
- **Output OV Threshold:** This row contains drop-downs for selecting the OV thresholds. Each output can select an independent OV threshold.
- **Output UV Threshold:** This row contains drop-downs for selecting the UV thresholds. Each output can select an independent UV threshold.
- **Soft-Start Ramp Rate selection:** This row contains drop-downs for selecting Soft-Start Ramp Rate.
  - Buck1, Buck2, and LDO4 have independent ramp rate selections.
  - The Buck3 ramp rate is the same as for Buck2.
- **Spread Spectrum:** This contains drop-downs for selecting spread spectrum options.

The following are the areas on the GUI going down the left side:

- **Dongle Found counter:** This indicates how many Dongles (USB interface boards) the GUI recognizes. If the count is zero (0), the GUI is not connected to the USB interface board.

- **VIN UVLO drop-down:** Selects the V_{IN} UVLO threshold.
- **Device ID information:** Reads the device ID and silicon revision.
- **EN control:** Controls the Buck1 output and Standby operation.
- **EN_LV control:** Controls the LV outputs (Buck2, Buck3, LDO4).
- **ReCal button:** Reads all pertinent registers and perrforms a CRC calculation.
- **Refresh All button:** Reads all pertinent registers and updates the current tab displayed. This button can be used at any time on any tab.

Other tabs are updated automatically after a **Refresh All** when they are selected.

- **Power Sequence:** Contains drop-downs for selecting the startup and shutdown order.
- **tOFF delay**: Contains drop-downs for selecting the delay between outputs shutting down.
- **tON delay:** Contains drop-downs for selecting the delay between outputs starting up.

When powered up, the GUI should initially appear as in Figure 4.

The EN and EN_LV controls are at the left side of the display. The EN control has the IC in the Standby position, and the EN_LV control has the LV outputs (Buck2/Buck3/LDO4) in the Off state.

To turn Buck1 on, click the **On** button in the **EN (HV)** control. Vout1 should power up with the factory-set voltage.

To turn the LV outputs on, click the **On** button in the **EN_LV** control. Buck2, Buck3, and LDO4 should power up with their factory-set voltages.

2.1 Changing Programming Options

Complete the following steps to make changes in the options on this tab such as Output Voltage and V_{OUT} OV Threshold:

1. Use the **EN control** to place the IC in Standby. All the options on the **Configure** tab can be changed only when the device is in Standby mode (the **EN_LV control** can be placed in either the Off or On state).
2. Select the desired options by using the specific drop-down menus.
   a. **Note:** There are options not shown on this **Configure** tab, which can only be selected while the device is in Standby mode. These other options are located on the **Misc** tab. Changes on that tab can be made by moving to that tab and selecting the required options.
3. Use the **Refresh All** button to verify the selections.
4. When satisfied that the selections are correct, click the **ReCal CRC** button.
   a. The GUI automatically reads the new CRC calculation result from registers 0xB6, 0xB7
   b. The GUI copies these values into registers 0x7E, 0x7F.
5. Click the Refresh All button.
6. Set EN control to EN.

The device should now power up with the selections chosen. **Note:** When **EN control** is On, the Buck1 output is powered up and you cannot make any changes to the selections on the **Configure** tab. If you try to change a selection, the drop-down may change but a **Refresh All** shows that the device settings have not changed.

Note: If selections are made with the device in Standby and ReCal CRC is not performed, if EN is set to **On,** the outputs start up but quickly shut down because of a CRC Recheck error. If this occurs, place the device in **Standby**, click **ReCal CRC**, click **Refresh All**, and then place EN to the **On** setting. The outputs should come up with the selected options.

The limitation of making selections only during Standby operation does not apply to any of the bits related to: fault status, fault response, fault reporting to GPIO or RSTB, set-up of the Windowed Watchdog Timer, or set-up of the GPIO and RSTB pins. These parameters are shown on the other tabs in the GUI.

Note: While options can be selected, the accuracy of the selected options may be slightly outside the datasheet specifications. Datasheet accuracy limits are assured only for the factory-programmed settings. As an example, if Vout1 is selected to the default value of 3.8V, the output value is finely adjusted at the factory for Vout1 set to 3.8V. If Vout1 is later changed to a different voltage setting, the new Vout1 voltage may be slightly less accurate than the default setting. However, the change in accuracy is minor and should not significantly affect system or board level testing. After the required options have been chosen, the device then can be ordered and factory-adjusted with those specific options, to provide the tightest accuracy available.

If any option is set to a value other than the factory-programmed value, this creates a CRC Recheck fault, see Displaying Detected Faults. This CRC Recheck error is ignored if the steps **ReCal CRC** and **Refresh All** are followed before setting EN to **On**. The CRC Recheck still occurs and is detected and shown as a fault but the fault is ignored, and the device operates as intended.

2.2 Fault Status Tab

The Fault Status tab is selected by clicking the **Fault Status** button in the Tab row. The Fault Status tab is shown on the next page. **Note:** The left side of the GUI, with EN and EN_LV control, and the **ReCal** and **Refresh All** buttons, did not change. This is true for all tabs.

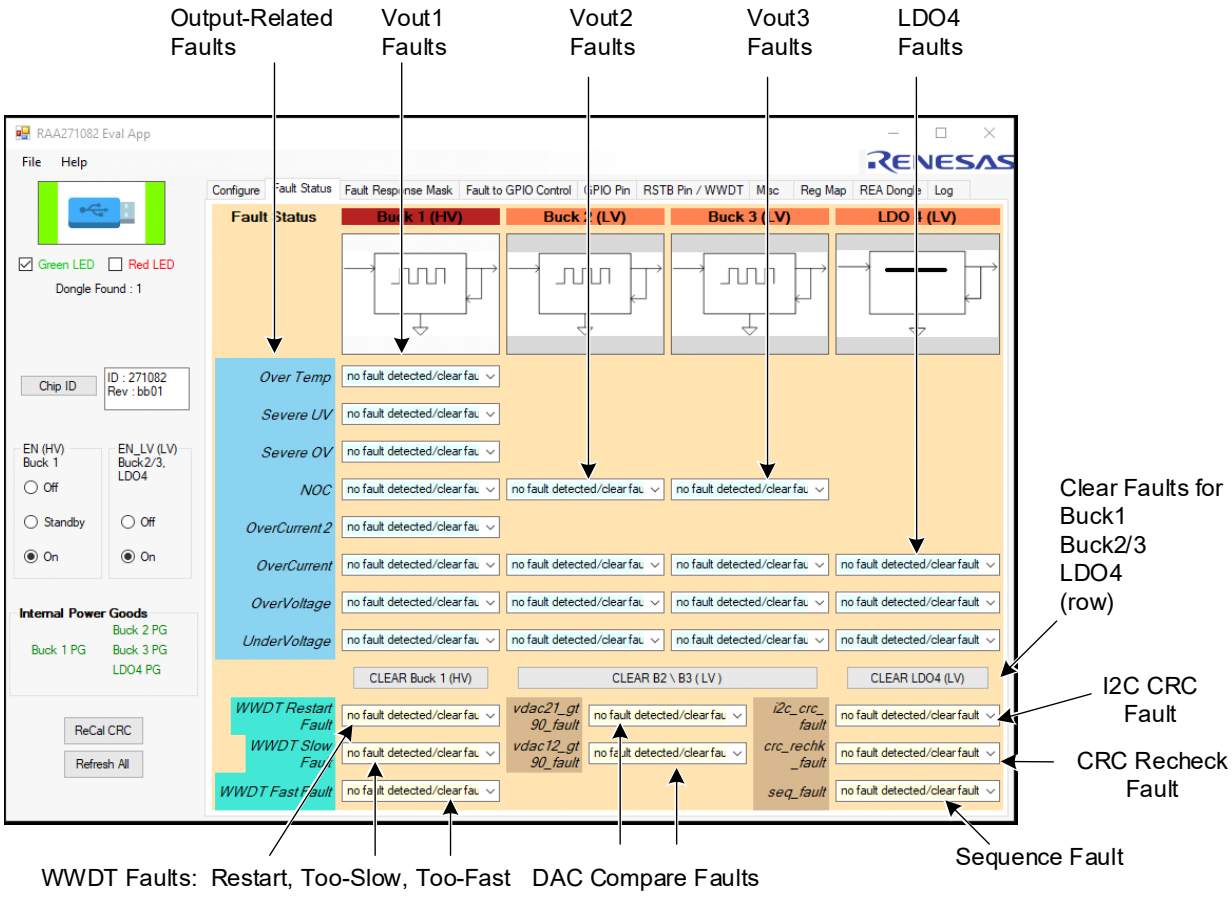

Figure 5. Fault Status Tab with Labels

The Fault Status tab is arranged as follows: The output-related faults are arranged in columns. The first column at left, Output-related faults (in blue background) lists fault types related to an output voltage: such as OV, UV, OC. It also shows the Over-Temp or Over-temperature fault.

The remaining columns moving to the right show the faults which can be detected for Buck1, Buck2, Buck3, and LDO4. LDO4, for instance, has drop-downs shown in the Overcurrent, Overvoltage, and Undervoltage faults. It

does not show drop-downs for NOC (Negative Overcurrent) fault or for Severe UV fault; these faults cannot be detected.

At the bottom of the Fault Status tab are fault indicators for the Watchdog Timer (WWDT), DAC Compare faults, Sequence faults, I2C CRC faults, and CRC Recheck faults.

2.2.1 Displaying Detected Faults

To see what faults are detected, click the **Refresh All** button. Faults detected should highlight as yellow text with red background, as shown in Figure . Here the faults detected are Overcurrent and Undervoltage on Buck1.

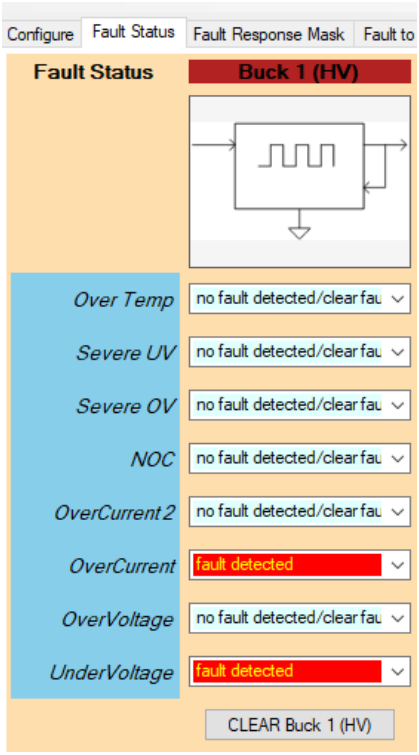

Figure 6. Vout1 Faults

Note: If a fault is detected, the fault status bit for that fault is set to logic 1 and stays at logic 1 until the bit is cleared.

To clear a fault, go to the **fault detected** drop-down and select **no fault detected/clear fault**. The drop-down should read **no fault detected/clear fault** and the text should now appear as black text with light blue background.

It is possible to clear all faults for Buck1 by clicking on the **CLEAR Buck 1 (HV)** button at the bottom of the Buck1 fault list.

Faults for Buck2, Buck3, and LDO4 are displayed and handled in the same manner as faults for Buck1. There are also **CLEAR B2/B3 (LV)** and **CLEAR LDO4 (LV)** buttons. These can be used to clear faults for Buck2/Buck3 and LDO4 respectively, or each fault can be cleared individually by selecting the drop-down.

After clearing faults, click **Refresh All**. If the fault condition is removed, the drop-down reads no fault detected/clear fault. If the fault condition persists or reoccurs, the drop-down shows the fault detected.

As shown in Figure 7, at the bottom of the Fault Status tab are drop-downs for the Windowed Watchdog Timer (WWDT), DAC compares, I2C CRC, CRC Recheck, and Sequence faults. These drop-downs operate the same as fault drop-downs for Buck1. A fault condition is displayed as **fault detected** in yellow text with red background.

In the example, the CRC Recheck fault is detected. In this case, there is no button to clear all these faults at once; each fault must be cleared individually using the drop-downs.

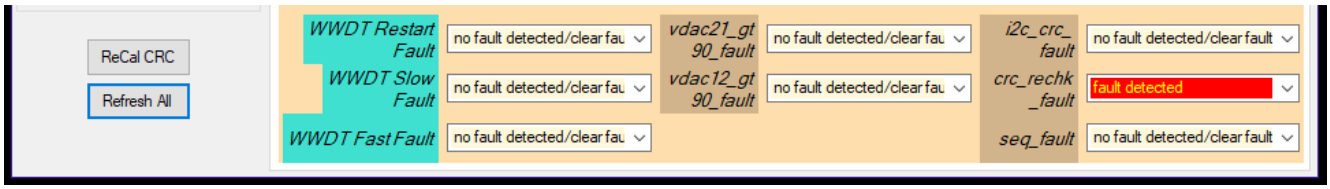

Figure 7. Fault Status Tab – WWDT and Other Faults

In Figure 7, the CRC Recheck fault (far right) shows a fault detected. Any change to the factory programmed options causes a CRC Recheck fault. If the device options are changed, the device detects the change within 5ms and sets the CRC Recheck fault bit high. If changes are done correctly using ReCal CRC and Refresh All, the fault is still detected but it is ignored, which allows users to test various configurations. The fault cannot be cleared because the device does CRC Recheck every 5ms. Even if the fault is cleared, the fault is re-detected within 5ms.

2.3 Fault Response Mask Tab

The Fault Response Mask tab shown in Figure 8 is selected by clicking the **Fault Response Mask** button in the Tab row. This tab controls the response of the device (shut down or ignore) for various faults. The fault response selections for Buck1, Buck2, Buck3, and LDO4 are laid out similarly to the Fault Status tab, with fault response grouped into columns by output and into rows by fault type.

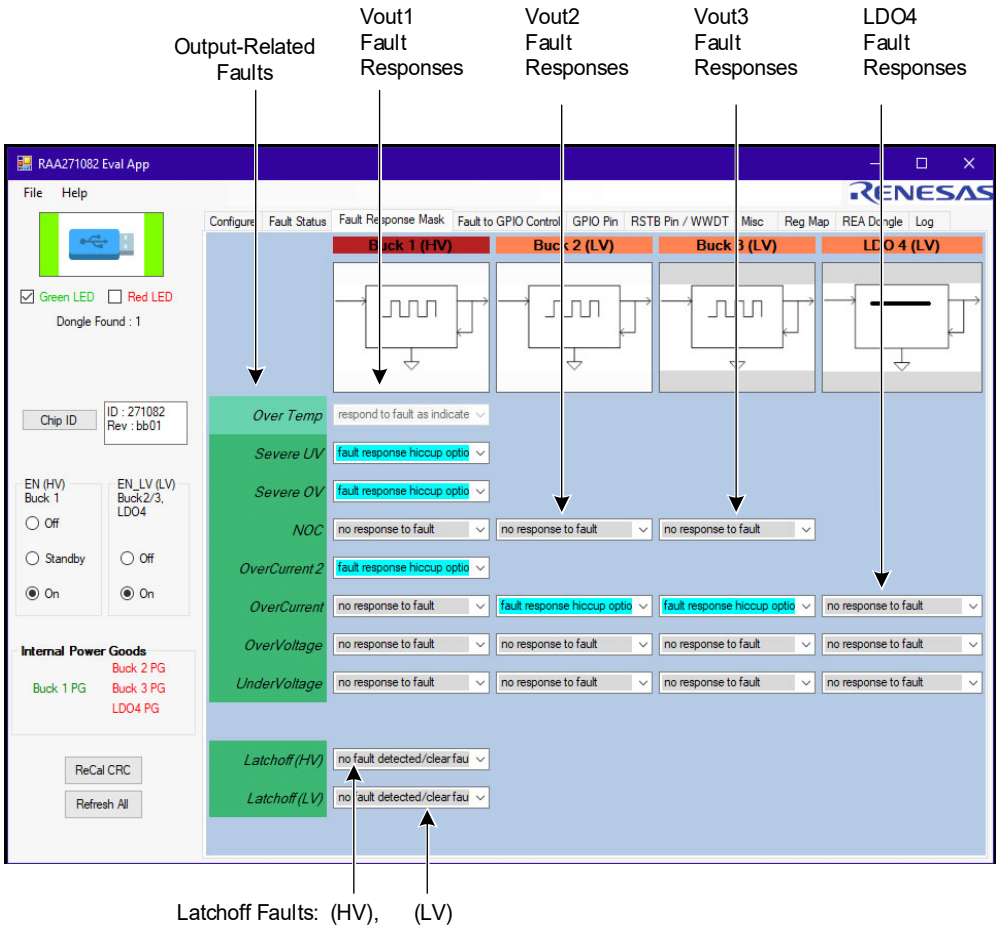

Figure 8. Fault Response Mask Tab with Labels

Each of the output-related fault responses can be enabled or disabled by selecting the drop-down. Selecting **no response to fault** causes the device to not respond (not shut down any outputs) if the fault is detected.

Selecting **fault response hiccup options** causes the device to respond to a fault (shut down an output) in accordance with the hiccup option selected. (Hiccup options are selected on the Misc tab.) These fault response selections can be changed whenever EN is not in the Off state. However, the hiccup options on the Misc tab do require the EN pin to be in Standby to be selected, along with a ReCal CRC/Refresh All cycle.

At the bottom of the Fault Response Mask tab (Figure 8) are the **Latchoff (HV)** and **Latchoff (LV)** drop-downs. Unlike the other drop-downs on this tab, these act also as fault indicators. If a Latchoff event occurs on the HV (Buck1) regulator, the (HV) drop-down reads **latchoff detected** in yellow text with red background. This indicates that the HV Buck1 output is in a latched-off state, which prevents Buck1 from restarting. This state can be cleared by selecting **no fault detected/clear fault** from the drop-down, which allows Buck1 to restart from a latch-off condition.

The **Latchoff (LV)** drop-down does the same function for the LV outputs. If a fault on a LV output (Buck2, Buck3, LDO4) results in a latchoff state, this drop-down indicates a **latchoff detected fault**, which prevents the LV outputs from restarting. This state can be cleared by selecting **no fault detected/clear fault** from the drop-down, which allows the LV outputs to restart from a latch-off condition.

Clicking on **Refresh All** updates the Fault Response settings for the device.

2.4 Fault to GPIO Control Tab

The Fault to GPIO Control shown in Figure 9 is selected by clicking the **Fault to GPIO Control** button in the Tab row. This tab controls which faults are directed to the GPIO pin. The faults for Buck1, Buck2, Buck3, and LDO4 are arranged similarly to the Fault Status tab, with fault response grouped in columns by output and in rows by fault type.

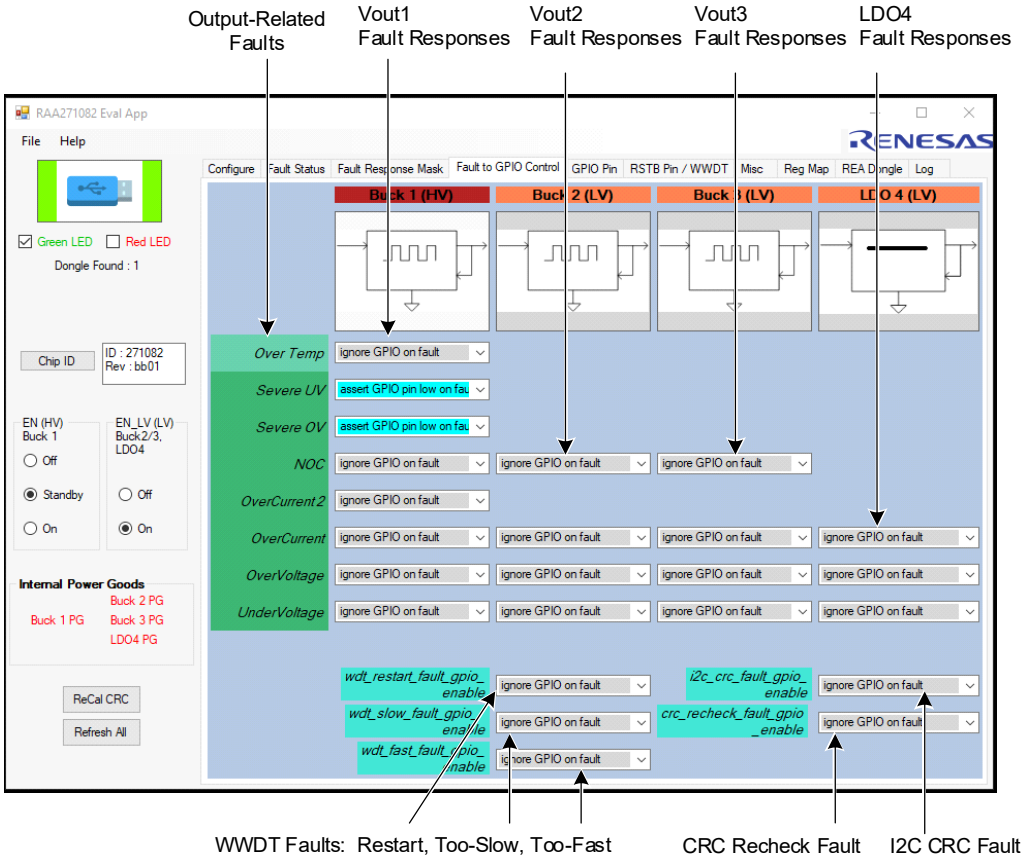

Figure 9. Fault to GPIO Tab with Labels

All drop-downs on this tab are configured to display **ignore GPIO on fault** or **assert GPIO pin low on fault**. Use the drop-downs to select which, if any, faults cause the GPIO pin to assert low when the fault is detected. These selections can be made whenever EN is at Standby or On and have no effect on the ReCal CRC operation.

Note: If the GPIO pin is used as a fault indicator (**assert GPIO pin low on fault**), the GPIO pin also needs to be configured as a fault indicator. This is selected on the GPIO Pin tab. See the GPIO Pin Tab for how to configure GPIO as a fault indicator.

At the bottom of the Fault to GPIO tab are drop-downs for the Watchdog timer faults, the I2C CRC fault, and the CRC recheck fault.

2.5 GPIO Pin Tab

The GPIO Pin tab shown in Figure 10 is selected by clicking the **GPIO Pin** button in the tab row. This tab controls the use of the GPIO pin. **Note:** All functions on this tab are controlled by the GPIO_CTRL register, register 0xA4.

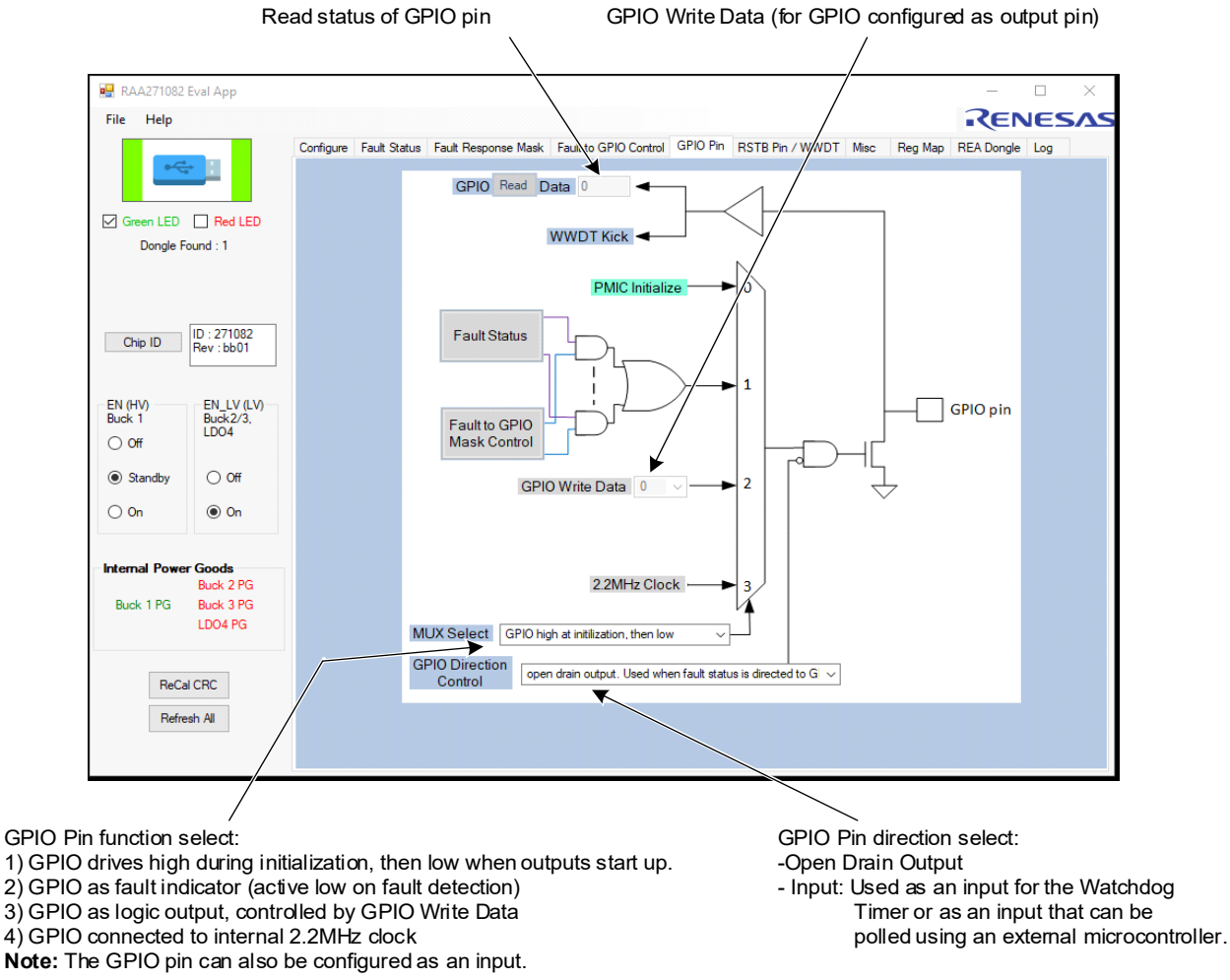

Figure 10. GPIO Pin Tab with Labels

The following are the GPIO options explained in more detail.

- **Read status of GPIO:** This box shows the current logic state of the GPIO pin, whether the GPIO pin is configured as input or output (The value is reflected in register 0xA4, Bit 7). If GPIO is configured as an input, connected for example to an interrupt signal or fault monitor, the input value can be read by a microcontroller using I^2C and used to make fault response decisions at the system level.

- **GPIO Write Data:** If GPIO is selected as a logic output, this bit dictates which logic state (1 or 0) is sent to the pin.
- **GPIO Pin function select:** For all options in this selection (see Figure 10, bottom left), the GPIO pin is configured as an open-drain output and an external pull-up resistor is required. On initial power-up, the GPIO pin defaults to option 1, drives high (open-drain) during initialization and then drives low when initialization is completed. Selecting any other Pin function must be done after initialization is completed. This is also true for setting the pin direction as an input.
- **GPIO Pin direction select:** The GPIO pin can be configured as an output or input, after the initialization is completed at power-up. All the selections in the GPIO Pin function select (Figure 10, bottom left) require the GPIO pin to be configured as an output. If the GPIO pin direction is selected as an input, this overrides the GPIO Pin function selection, and the pin operates as input-only.

2.6 RSTB Pin / WWDT Tab

The RSTB Pin / WWDT tab shown in Figure 9 is selected by clicking the RSTB Pin / WWDT tab in the Tab row. This tab controls operation of the RSTB pin. This tab also controls configuration of the Windowed Watchdog Timer (WWDT).

2.6.1 RSTB Operation and Options

The RSTB pin is a general fault indicator for the device with an active-high/active-low output. In normal operation, RSTB will drive low when any of the outputs falls outside the Undervoltage or Overvoltage threshold selected for that output (which causes the internal PGood signal for that output to be logic low = power not good). However, it is possible to configure RSTB so that it will ignore one or more PGood signals. The outputs which are ignored depend on the Power Sequence order selected from the Configure tab, as shown in Table 2:

Table 2. Ignored Outputs

Option	Power Sequence = Buck2 -> Buck3 -> LDO4	Power Sequence: LDO4 -> Buck2 -> Buck3
0	no PGood signal ignored	no PGood signal ignored
1	LDO4 PGood ignored	Buck3 PGood ignored
2	LDO4, Buck3 PGood ignored	Buck3, Buck2 PGood ignored
3	LDO4, Buck3, Buck2 PGood ignored	Buck3, Buck2, LDO4 PGood ignored

Note: PGood for Vout1 is never ignored. If Vout1 falls outside the UV or OV threshold the RSBT pin is asserted low. Also , there are programmable delays for the detection and assertion of PGood on UV and OV faults, see the Misc Tab for details.

The RSTB pin can also be programmed to be driven low by a Watchdog Timer fault, or by a Sequence fault (the fault in the internal startup sequencer).

RSTB also generally drives low during any fault which later causes output shutdown. For example, if a DAC Compare fault is detected, RSTB immediately drives low, even though the outputs are still in tolerance. When RSTB drives low as a fault indication, it drives low for 200ms and then returns to a logic high state. This is true for all UV and OV faults. For Watchdog timer and Sequence faults, there is a 20ms pulse option that can be selected from the Misc tab.

2.6.2 WWDT Operation and Options

Many options on this tab are related to the WWDT (Windowed Watchdog timer).

The WWDT has many options:

- The WWDT can be enabled or disabled.
- The WWDT features three faults that can trigger a shutdown (restart, too slow, too fast)
- The WWDT fault timing is independently programmable for too-slow and too-fast faults.

- WWDT lockout, a feature that locks the WWDT settings and prevents any future changes.
- Which WWDT faults are sent to the RSTB pin as fault indicators.
- If a WWDT fault occurs, the response can be to shut down all outputs or shut down only LV outputs.

Note: When the count drop-downs are loaded with non-zero values, the WWDT fault detector is armed when it receives a valid WWDT kick. If a WWDT fault is detected, the fault status bit is set high and the fault appears on the Fault Status tab. However, if the WWDT is not enabled (using wwdt_enable), the outputs continue to operate normally.

For the outputs to shut off from a WWDT fault, these steps must be taken:

1. The tick and count for the desired WWDT fault must be selected.
2. One or more fault response masks for the required WWDT must be selected, which allows the device to shut down the outputs. Selection of each fault response is optional.
3. Select which outputs to shut down using the wwdt_reg_dis_sel drop-down. Choices are all outputs or only the LV outputs Buck2/Buck3/LDO4.
4. Choose a Kick Select (GPIO and/or I2C kick).
5. Select which WWDT, if any, asserts the RSTB pin low. Each selection is optional. **Note:** In many cases, RSTB is driven low on a WWDT fault because the outputs are forced to shut down. Enable the WWDT using the wwdt_enable drop-down.
6. Initiate the WWDT by issuing a valid WWDT kick.

After these steps, the WWDT is actively armed and detects and respond to a WWDT fault.

The RSTB Pin/WWDT tab is shown in Figure 11.

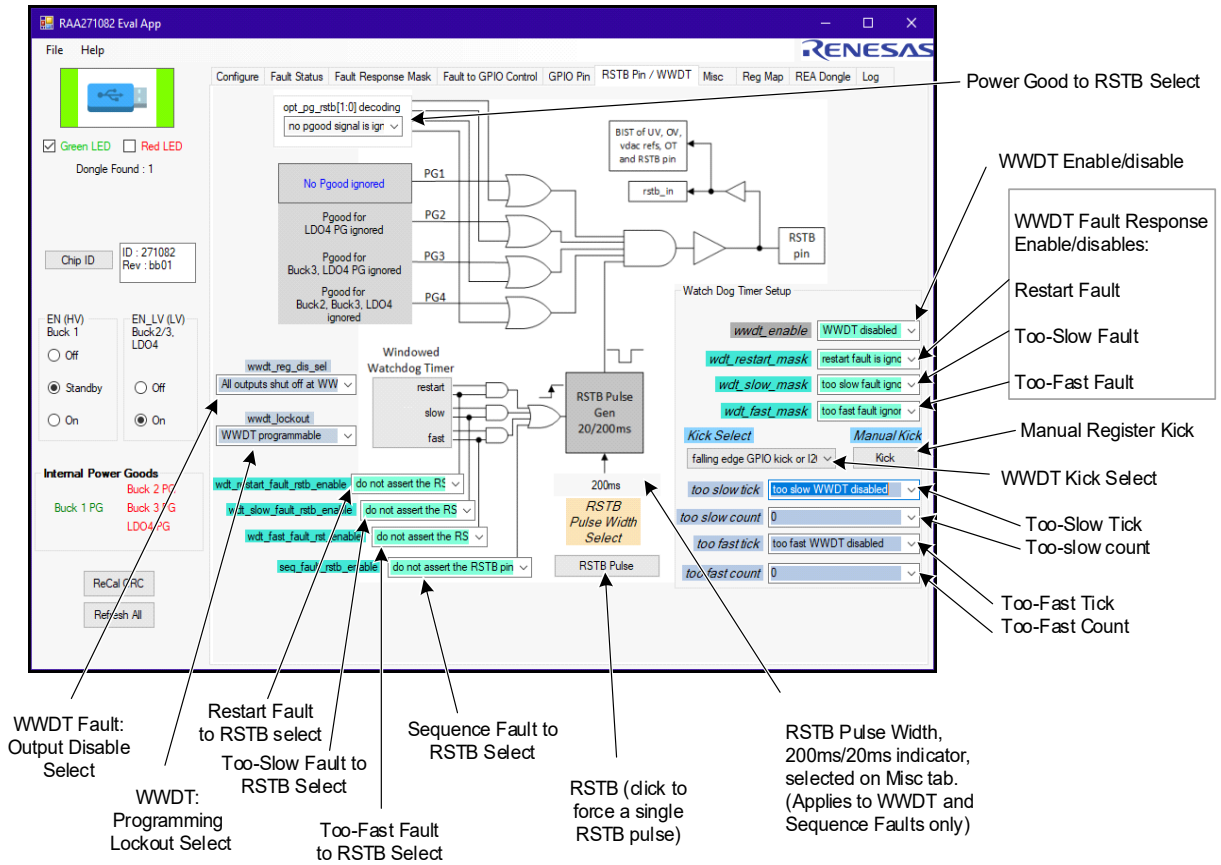

Figure 11. RSTB Pin/WWDT Tab with Labels

The explanations for the drop-downs in Figure 11 are shown below.

From the right side:

- **Power Good selections for RSTB.** The default setting for RSTB is that any output below its UV threshold will generate a RSTB low fault indication. This opt_pg_rstb drop-down allows RSTB to ignore some outputs based on drop-down selection. The options available are determined by the Power Sequence option which is selected on the Configure tab.
- **Enable for the WWDT.**
- **Masks** (to prevent or allow shutdown upon fault) for the three WWDT faults (restart, too slow, too fast)
- **Kick select for WWDT** (I2C register kick and/or GPIO input kick).
- **Manual kick.** Clicking this button sends a WWDT kick to register 0xA3 (KICK_REG).
- **WWDT parameter settings for too-slow and too-fast faults. Note:** The restart fault is simply a too-slow fault with the period set at 2x of the too-slow timing. The tick selects the time interval used for the counter (100usec, 1ms, etc). The count sets the number of ticks used by the WWDT timer.

Example: Set the too-slow tick to 1ms and the too-slow count to 6. The Watchdog timer detects a fault if a time period of 1ms × 6 = 6ms passes without a valid WWDT kick. The too-fast tick and count settings operate in the same manner as too-slow.

From the bottom:

- **WWDT fault output disable select.** This drop-down selects which outputs are shut down due to a WWDT fault. The choices are all outputs shut down or only the LV outputs are shut down (Buck1 remains on).
- **WWDT programming lock-out.** If **WWDT locked out** is selected, this locks all WWDT programming parameters from further changes. The WWDT options remain locked out until the device goes through a power-on reset. This option is prevents a malfunctioning microcontroller from accidentally changing the WWDT parameters.
- **WWDT faults to RSTB, three options:** Restart fault to RSTB, too-slow fault to RSTB, and too-fast fault to RSTB. These drop-downs select whether the RSTB pin drives low when the selected WWDT fault is detected. Each of the three faults can be independently routed or not routed to the RSTB pin.
- **Sequence fault to RSTB:** If selected, the RSTB pin drives low if a sequence fault is detected.
- **RSTB button:** Click this button to force a single RSTB pulse at the RSTB pin. This is equivalent to writing a 1 to Bit 3 of register of 0xA5.
- **RSTB Pulse Width 20ms/200ms indicator.** This display is an indicator only, controlled by the opt_short_fault_wait bit on the Misc tab, in the Misc2 Opt column, which controls register 0x7C (MISC2_OPT), bit 3.

2.7 Misc Tab

The Misc tab shown in Figure 12 is selected by clicking the **Misc tab** in the tab row. This tab controls miscellaneous options that are found in registers 0x7B, 0x7C, and 0x7D of the RAA271082. **Note:** All options on this tab are CRC checked and therefore can be changed only when the device is in Standby mode. After options are selected, a ReCal CRC and Refresh All operation is needed to enable the device to start up with the selection options.

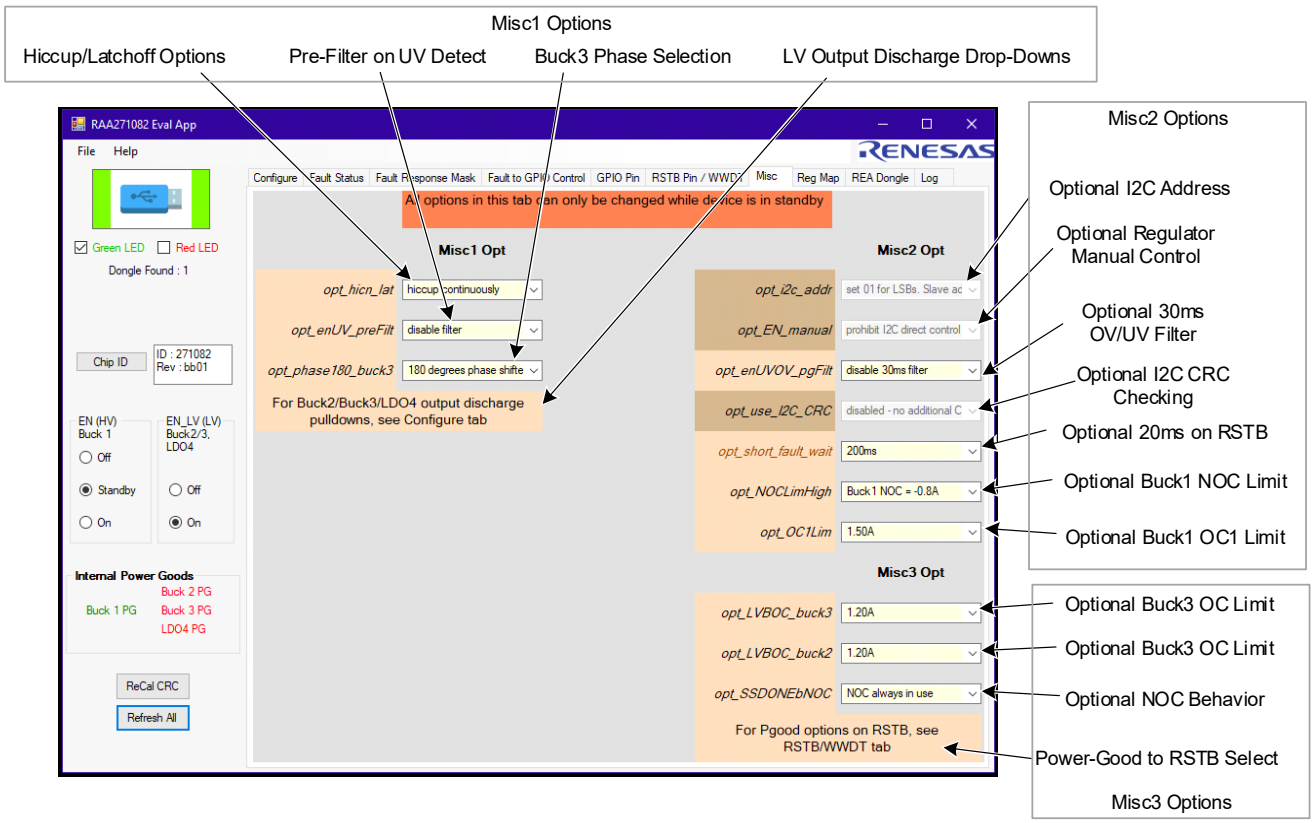

Figure 12. Misc Tab with Labels

The options available on this tab are explained in the following sections.

2.7.1 Misc1 Options – Register 0x7B

Misc1 options are shown in Figure 12 in the Misc1 Options box at the top.

- **Hiccup/latchoff options:** The device has four selections for hiccup/shutdown for response per register 0x7B bits 7,6.

0	Hiccup and retry continuously
1	Hiccup and retry for 10 attempts, then latch off.
2	Hiccup and retry for 5 attempts, then latch off.
3	Latch off on first fault.

- O**ptional pre-filter for UV detection:** The device has four selections for a pre-filter delay on UV detection per register 0x7B bits 5,4. The same delay is applied to all four outputs. **Note:** There is an internal fixed delay of 2 to 3µs for UV detection. The below selections are in addition to this fixed delay.

0	Disable filter: no additional filter delay added.
1	Enable 10µs filter: an additional 10µs delay is added
2	Enable 25µs filter: an additional 25µs delay is added
3	Enable 40µs filter: an additional 40µs delay is added.

These delays affect only the UV detection. OV detection is not affected by this selection.

- **Buck3 Phase selection:** Default operation for the Buck3 switching cycle is to be 180 degrees out of phase with both Buck1 and Buck2. There is an option for have the Buck3 switching cycle to be in phase with Buck2, per register 0x7B bit 0.

The options previously described are all contained in register 0x7B. The remaining options in register 0x7B, the output discharge drop-down for Buck2, Buck3, and LDO4, are in the same register but they are not listed on this tab. The output discharge options for these outputs are shown on the Configure tab.

2.7.2 Misc2 Options – Register 0x7C

Misc2 options are shown in Figure 12, in the Misc2 Options box at the right side.

- **Optional I2C address:** The device has an option for an I^2C address of either 0x4D or 0x4E (register 0x7C Bit 7). However, the GUI presently supports only the address 0x4D and the 0x4E option is disabled. Future versions of the GUI may support this feature. Register 0x7C, Bit 7.
- **Optional manual control of outputs:** This option allows users the ability to control the startup and shutdown of outputs using direct I^2C control instead of using the EN and EN_LV pins. This feature is enabled only through factory programming and is disabled from GUI. Register 0x7C, Bit 6.
- **Optional UV/OV filter:** This is an optional 30ms filter applied to UV and OV, both detection and response. The same filter is applied to all outputs and applies to both UV and OV faults. Register 0x7C, Bit 5.
- **Optional I2C CRC checking:** The device supports CRC checking on I^2C transactions, but it is not supported by the GUI at this time. Register 0x7C, Bit 4.
- **Optional short (20ms) RSTB pulse:** The length of the RSTB pulse can be selected for 20ms instead of the default 200ms by this drop-down. This affects only the WWDT and Sequence faults. For other faults such as OV and UV, the RSTB pulse width is fixed at 200ms. Register 0x7C, Bit 3.
- **Optional NOC1 limit:** This option selects a higher NOC (Negative Overcurrent) limit for Buck1. The default value is 800mA, the optional value is 1A. Register 0x7C, Bit 2.
- **Optional OC1 current limit:** This option selects different Overcurrent (OC1) levels for Buck1. The default value is 1.50A, with options of 1.20A and 1.75A. Register 0x7C Bits 1,0.

2.7.3 Misc3 Options – Register 0x7D

Misc3 options are shown in Figure 12, in the Misc3 Options box at the bottom right side.

- **Optional Buck3 OC:** This option selections different Overcurrent (OC) levels for Buck3. The default value is 1.20A, with options of 0.96A and 1.56A. Register 0x7D Bits 7,6.
- **Optional Buck3 OC:** This option selections different Overcurrent (OC) levels for Buck3. The default value is 1.20A, with options of 0.96A and 1.56A. Register 0x7D Bits 5,4.
- **NOC option for soft-start:** This option selects different behaviors for the NOC detector. The default behavior is that the NOC detector (which truncates the low-side on-time) is always active. The optional behavior is that NOC truncates the low-side on-time only during the soft-start interval. Register 0x7D Bit 2.

2.8 Reg Map Tab

The Reg Map (register map) tab shown in Figure 13 is selected by clicking the **Reg Map tab** in the tab row. This tab displays the names, addresses, and bit names of the registers in the RAA271082. The window area at the left contains a list of all available registers that can be opened or collapsed to view the bit names and assignments. See the *RAAA271082 Datasheet* for more detail on register and bit names and definitions. When the GUI is first powered up, the Reg Map tab has all registers expanded. Each register can be collapsed by clicking the - box to the left of each register name.

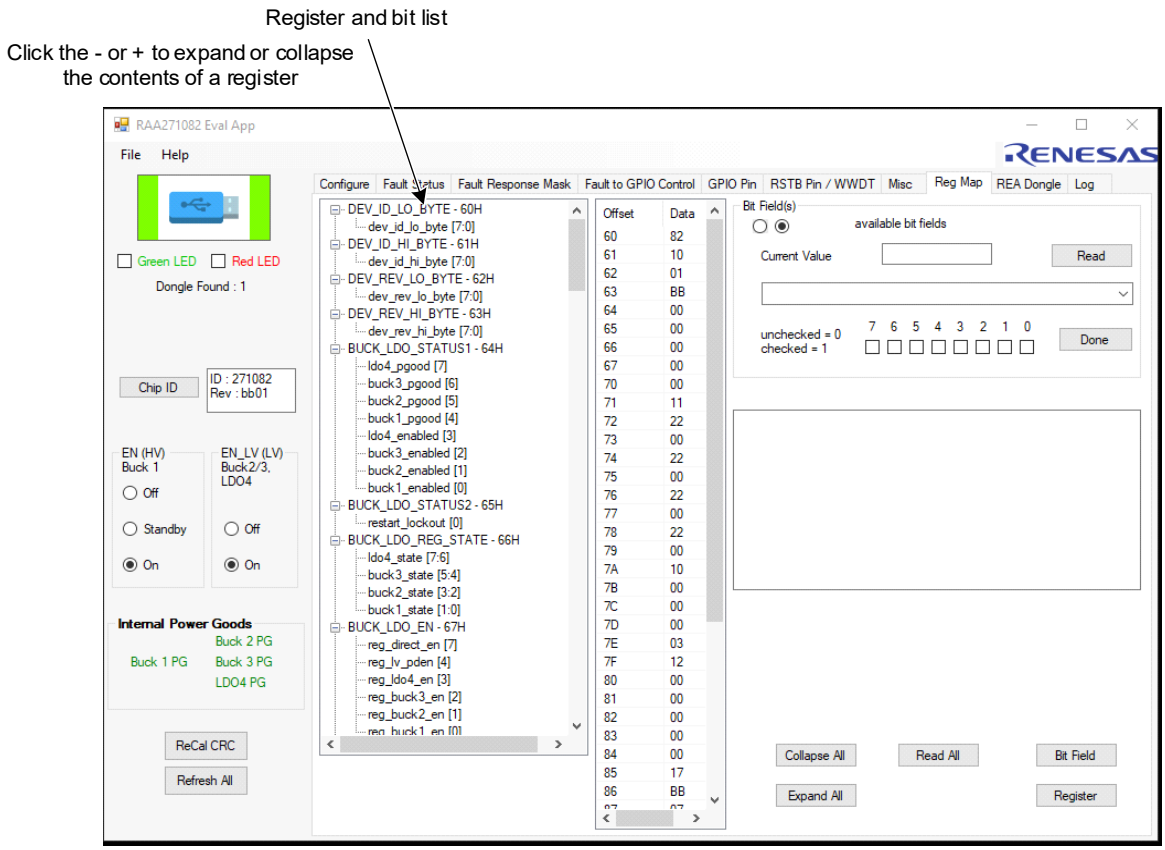

Figure 13. Reg Map Tab with Labels

2.9 REA Dongle tab

The REA Dongle tab shown in Figure 12 below is selected by clicking the REA Dongle tab in the tab row. This tab can be used to perform direct read and write operations on specific registers.

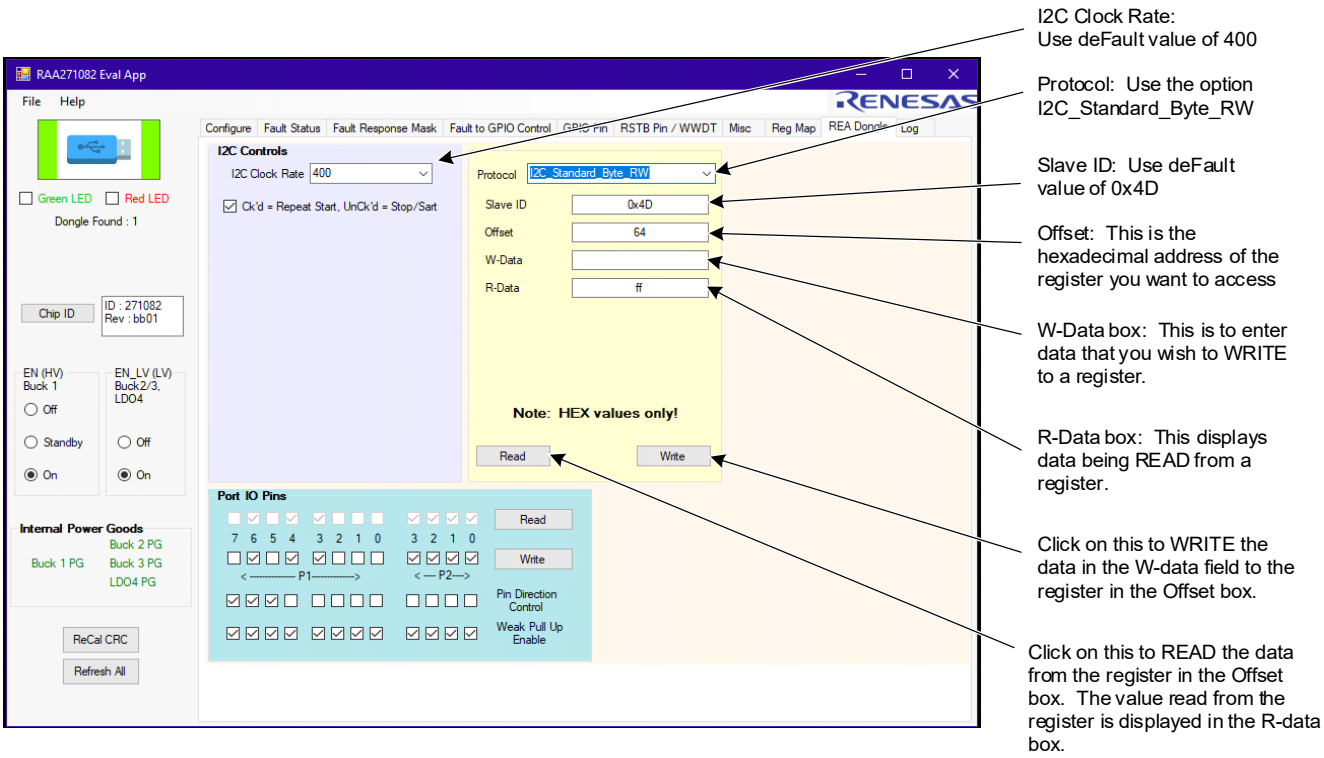

Figure 14. Reg Map tab with Labels

The following are the explanations of the various drop-downs and text boxes in the Reg Map tab.

- **To perform a READ operation on a register:** Type the hexadecimal address of the register in the **Offset** box, and then click the **READ** button. The register contents (value) are displayed in the **R-data** box.
- **To perform a WRITE operation on a register:** Type the hexadecimal address of the register in the **Offset** box, then type the required write value of the register (in hexadecimal) in the **W-data** box, then click the **Write** button. This writes the required value to the register. Click on **READ** to verify that the WRITE operation was successful, by checking the value in the **R-data** box. If the READ operation does not show the required value in the selected register, this indicates one of three possibilities:
  - The register selected is non-writeable under all conditions.
  - The register selected is writeable only when EN has the device placed in Standby mode.
  - The device is not on. (EN is set to Off, or VIN supply is not present).

2.10 Log Tab

The Log tab shown in Figure 13 is selected by clicking the **Log tab** in the tab row. This tab maintains a log of read/write operations done between the GUI and the RAA271082, which is useful for analyzing and understanding the register read/write operations used to configure the device options. For example, clicking Refresh All at any time initiates a read of many registers, and this series of register reads is displayed in the Log window. This Log feature can useful when tracking the relationship between selecting device options and the registers associated with those options.

The Log tab also contains a Clear Log button which clears away all previous read/write information. This is helpful in tracking individual register operations.

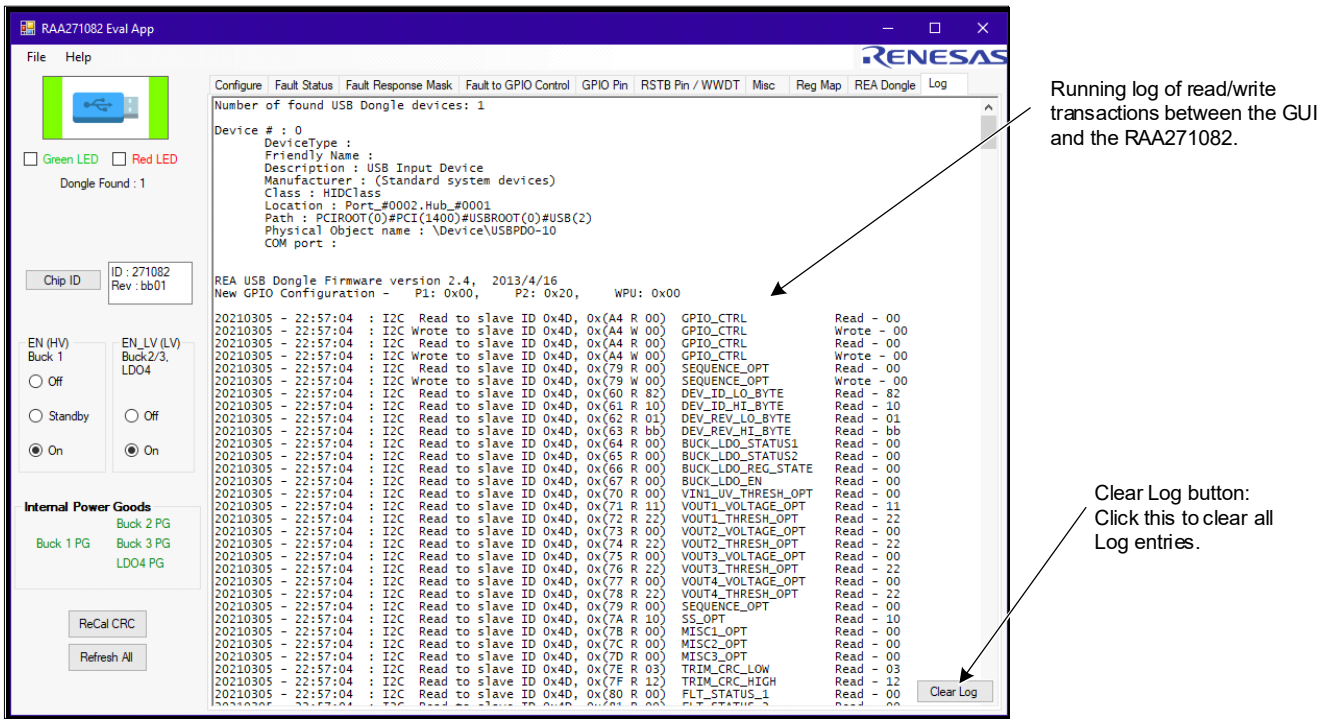

Figure 15. Log Tab with Labels

3. Board Design

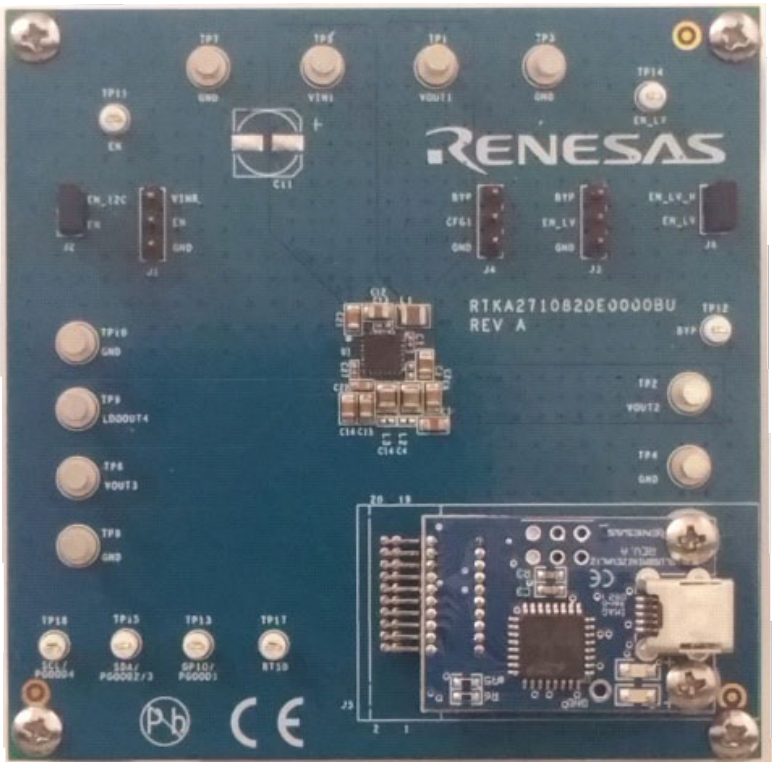

Figure 16. RTKA271082DE0000BU Evaluation Board (Top)

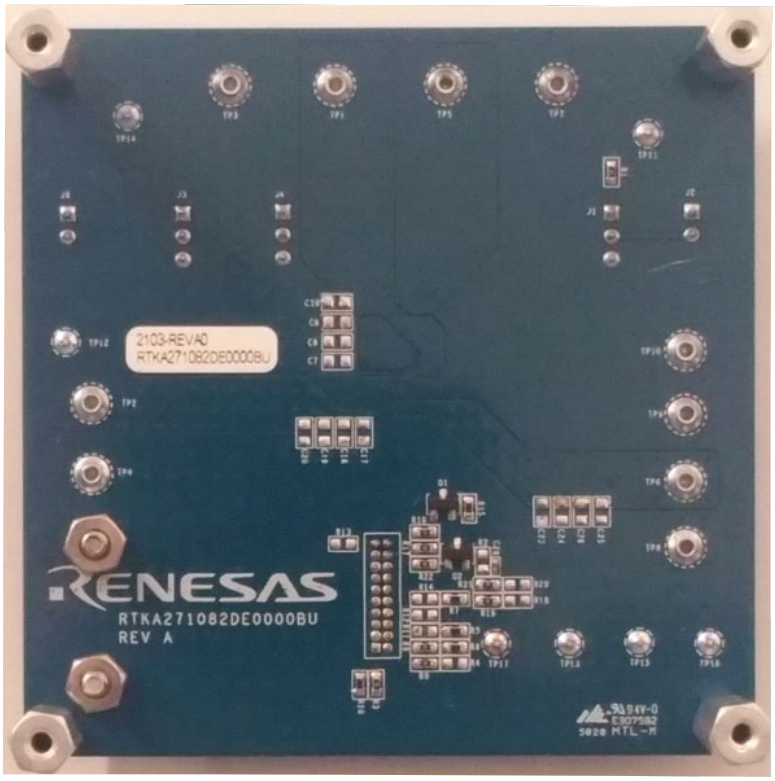

Figure 17. RTKA271082DE0000BU Evaluation Board (Bottom)

3.1 Layout Guidelines

As with all switching regulators, the Printed Circuit Board (PCB) layout requires careful attention to achieve good performance. Proper PCB layout as detailed below minimizes the effects of voltage and current spikes present in fast-switching MOSFET circuits.

- The PCB should have a minimum of four copper layers. Use a full ground plane in the internal layer directly below the top layer. For all components that connect to ground, make sure that each component has one or more vias nearby, to provide a low-impedance path to the ground plane.
- VIN1 input capacitance: Place the input filter capacitor (CIN1) between VIN1 and PGND, as close to the IC pins as possible. Place the high-frequency decoupling capacitor closest to the IC. The loop formed by the input capacitors, VIN1, and PGND must be small to minimize high frequency noise. The copper traces between the capacitors and the IC should be as short and direct as possible.
- Place the Buck1 inductor L1 near the PHASE1 pin of the IC and connect directly to the pin with short, wide copper.
- Place the boot capacitor (CBOOT) next to Pins 5 and 6 and use short, direct copper connections.
- Place the VIN2/3 input capacitor (CIN2/3) near the VIN2/3 pin of the IC. Place the high-frequency decoupling capacitor closest to the IC. Connect the capacitors to the VIN2/3 pin using short, wide copper. Place multiple ground vias at the ground connection of each capacitor, to provide a low-impedance ground path to the ground of the IC (PGND2/3, pin 22).
- Place Buck2 and Buck3 inductors (L2 and L3) next to their respective pins, PHASE2 and PHASE3. Route to the inductors using short, wide copper.
- Place the Buck2 and Buck3 output capacitors (COUT2 and COUT3) near the inductor and connect using short, wide traces. Use multiple vias and copper on other layers if needed to connect from COUT2 or COUT3 to their load circuit.
- Place multiple ground vias at the ground connection of COUT2 and COUT3, to provide a low-impedance ground path to the Buck2/3 ground return at the IC (PGND2/3, pin 22).
- Route the feedback for Buck3 directly from COUT3 to the FB3 pin (Pin 21), as seen in the layout in light blue color. Provide some space clearance between the FB3 trace (which is noise-sensitive) and the high-noise PHASE3 trace.
- Route the feedback for Buck2 on an inner layer, connecting from COUT2 to FB2 (Pin 22). FB2 is a noise-sensitive input. Route the trace so that it avoids passing underneath the inductors L2, L3, or L1, and also avoids passing underneath under the PHASE signals or pins. Renesas recommends routing the trace on an inner layer, going around COUT3, and then routing to Pin 22. VOUT2 (Buck2 output) and the FB2 pin are shown in yellow in Figure 18.
- LDOIN4 and FB1 (Pins 18 and 17) must be connected to VOUT1, which is the output of Buck1 and is connected to the VIN2/3 pin (Pin 1). Use wide copper to route from VOUT1 to LDOIN4. The LDOIN4 pin is the input for the LDOOUT4 output, which dictates that the LDOIN4 trace must carry all the LDO load current. When routing the connection from VOUT1 to LDOIN4, avoid routing underneath any of the inductors and also any PHASE nodes. Renesas recommends using inner layer copper, connecting from VOUT1 to LDOIN4 (all shown in white), routing directly underneath the IC, while avoiding the PHASE and BOOT pins of the IC (Pins 5, 6, 23, 24). Note: The LDOIN4 pin also functions as the overvoltage and undervoltage sense point for Buck1. To minimize I•R voltage drop because of copper resistance, use a wide trace to route to LDOIN4.
- FB1 (Pin 17) is the feedback input for Buck1. This pin ultimately connects to the same net as LDOIN4. It is possible to combine the path for FB1 and LDOIN4 into a single trace, however the trace needs to be wide to minimize I•R voltage drop because of the LDOIN4 loading. Alternatively, a separate trace on an inner layer can route from the VOUT1 output to the FB1 pin. Route this trace away from all high-noise nodes and components, including the inductors, capacitors CIN1 and CIN2/3, and the PHASE and BOOT nodes.
- Place input and output capacitors for the LDO (100nF and CLDOOUT4) near the IC and routed directly with short wide traces. Place multiple ground vias at the ground connection of the capacitors to provide a low-impedance ground path to the ground return at the IC.

- Connect all the grounds pins (Pins 10, 11, and 22) and the thermal PAD (Pin 25) together using a single wide copper pad under the IC. Connect this copper pad to the ground plane using multiple vias, to provide a low-impedance path to the ground plane and also to provide heatsinking through the PCB copper.
- Place the BYP capacitor (CBYP) near the BYP pin (Pin 12). Route to the capacitor using a short, wide PCB trace, for both the BYP and the ground paths. If needed, place multiple ground vias at the ground connection of CBYP, to provide a low-impedance ground path to the ground of the IC (PGND2/3, Pin 22).

An example PCB layout is shown in Figure 18.

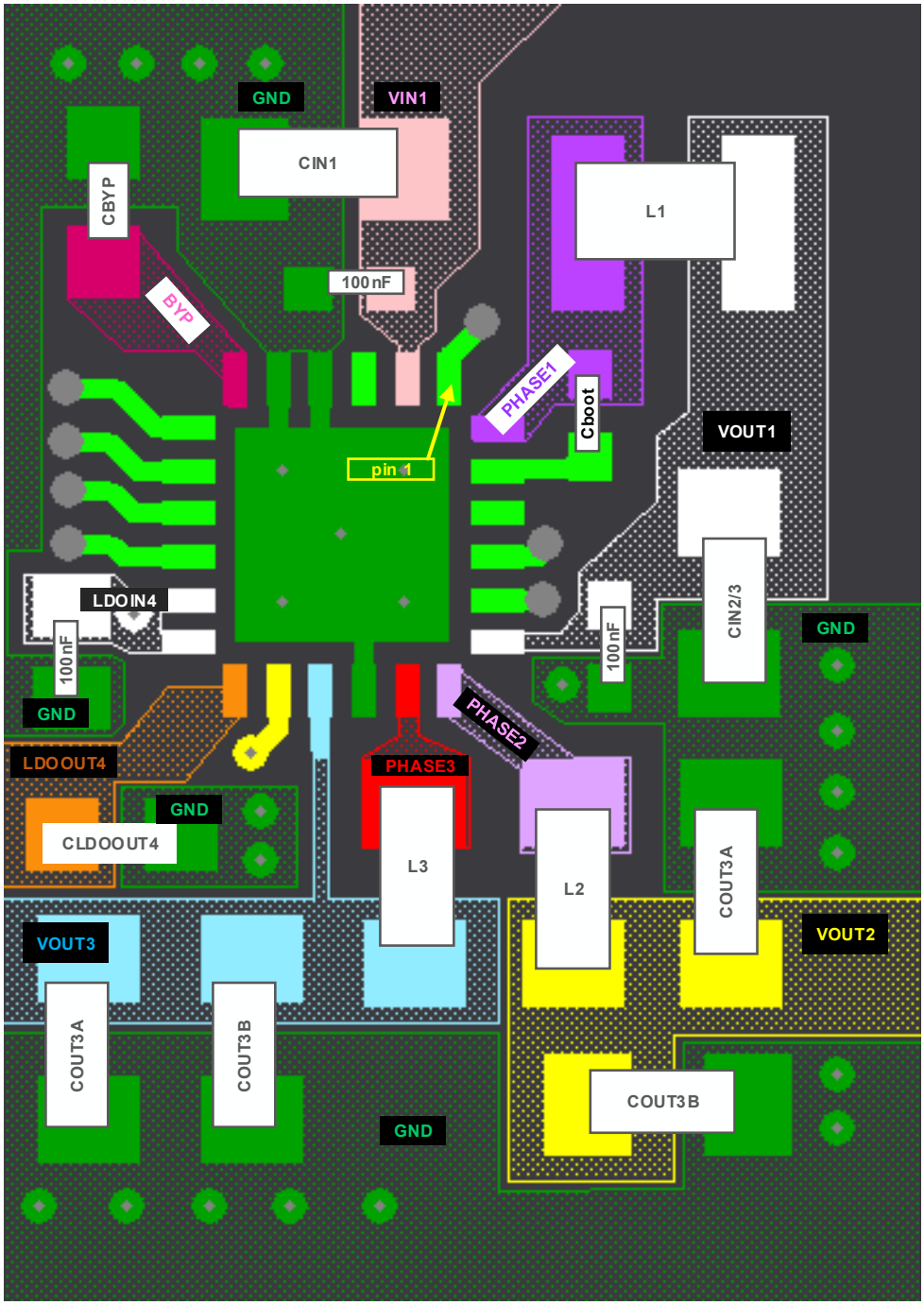

Figure 18. PCB Layout

3.2 Schematic Diagram

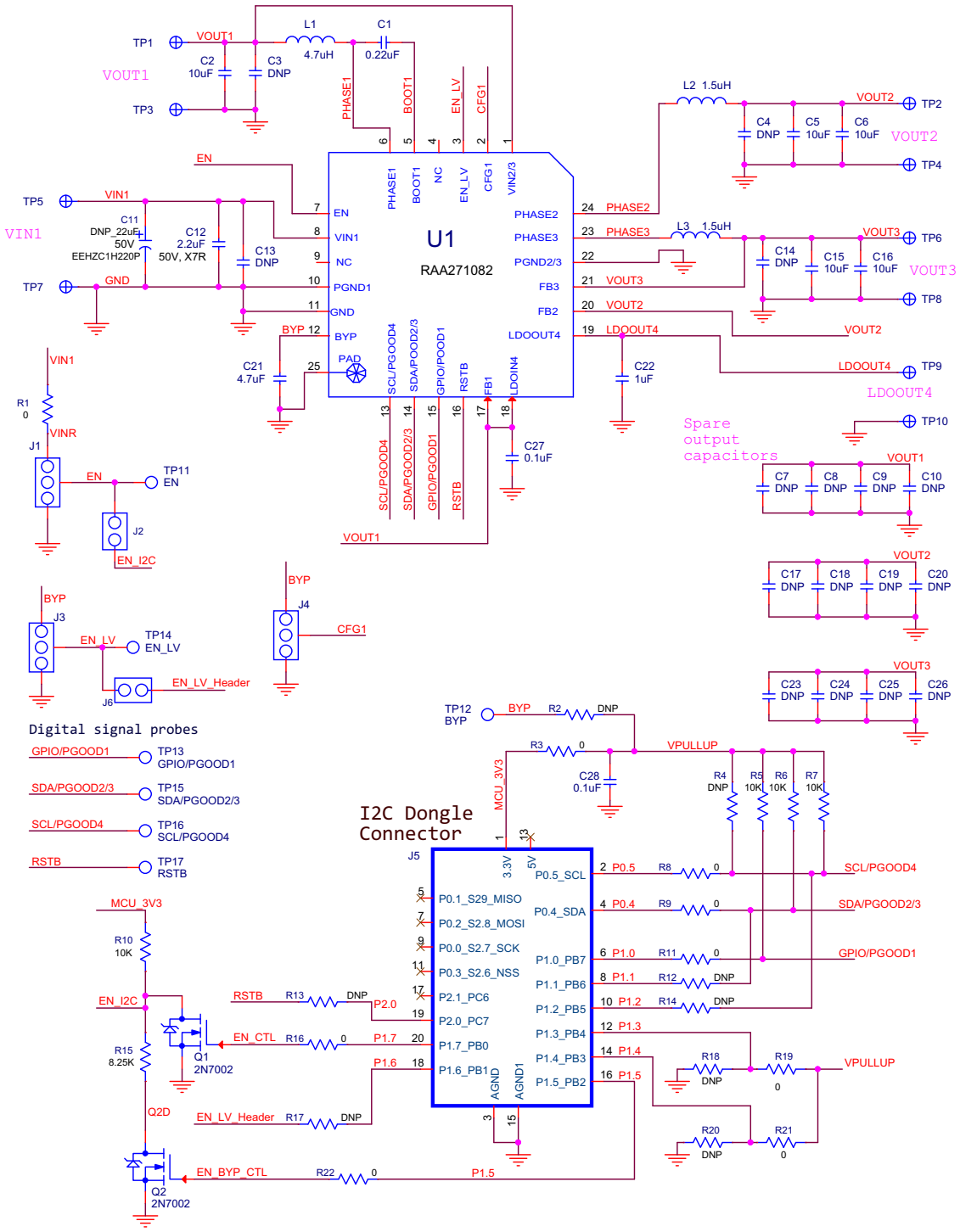

Figure 19. RTKA271082DE0000BU Schematic

3.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	C1	CAP-AEC-Q200, SMD, 0402, 0.22µF, 16V, 10%, X7R, ROHS	Murata	GCM155R71C224KE02D
2	C27, C28	CAP-AEC-Q200, SMD, 0402, 0.1µF, 50V, 10%, X7R, ROHS	Murata	GCM155R71H104KE02D
1	C22	CAP-AEC-Q200, SMD, 0603, 1µF, 25V, 10%, X7R, ROHS	Murata	GCM188R71E105KA64D
5	C2, C5, C6, C15, C16	CAP-AEC-Q200, SMD, 0805, 10µF, 10V, 10%, X7R, ROHS	Murata	GCM21BR71A106KE22K
1	C12	CAP, SMD, 0805, 2.2µF, 50V, 10%, X7R, ROHS	TDK	C2012X7R1H225K125AC
1	C21	CAP, SMD, 0805, 4.7µF, 16V, 10%, X7R, ROHS	Murata	GCJ21BR71C475KA01L
2	L2, L3	COIL-INDUCTOR, AEC-Q200, SMD, 2×1.6mm, 1.5µH, 20%, 2.3A, ROHS	TDK	TFM201610ALMA1R5MTAA
1	L1	COIL-INDUCTOR, AEC-Q200, SMD, 2.5×2mm, 4.7µH, 20%, 1.6A, ROHS	TDK	TFM252012ALMA4R7MTAA
10	TP1-TP10	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
7	TP11, TP12, TP13, TP14, TP15, TP16, TP17	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
3	J1, J3, J4	CONN-HEADER, 1×3, BREAKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
2	J2, J6	CONN-HEADER, 1×2, RETENTIVE, 2.54mm, 0.230×0.120, ROHS"	BERG/FCI	69190-202HLF
1	J5-SEE ASSEMBLY INSTRUCTIONS	CONN-HEADER, TH, 2×10, 1.27mmPITCH, R/A, ROHS	Harwin Inc	M50-3901042
1	U1 *SEE DOCUMENT #1	IC-BYD BATTERY, PMIC, 24P, SCQFN, ROHS	Renesas Electronics	RAA271082A4HNP#MA0
2	Q1, Q2	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	Diodes, Inc.	2N7002-7-F
9	R1, R3, R8, R9, R16, R17, R19, R21, R22	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
4	R5, R6, R7, R10	RES, SMD, 0603, 10K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
1	R15	RES, SMD, 0603, 8.25kΩ, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF8251V
0	R2, R4, R11, R12, R13, R14, R18, R20,	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
1	J5-SEE ASSEMBLY INSTRUCTIONS	PWB-FG, ISLUSBMINIEVAL1Z, ROHS	Renesas Electronics	ISLUSBMINIEVAL1ZFG
2	J5-SEE ASSEMBLY INSTRUCTIONS	SPACER, #4×1/8in, NYLON, ROUND, UNTHREADED, ROHS	Keystone	875
2	J5 (SEE ASSEMBLY INSTRUCTIONS)	WASHER, SPRING LOCK, 4-40, STAINLESS STEEL, ROHS	MCMASTER-CARR	91475A018

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
2	J5-SEE ASSEMBLY INSTRUCTIONS	NUT, 4-40, HEX, 18-8 STAINLESS STEEL, ROHS	MCMASTER-CARR	91841A005
2	J5-SEE ASSEMBLY INSTRUCTIONS	SCREW, 4-40×1/2in, PHILLIPS PAN, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0050 PH
4	Four corners	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40×3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	C11 (EEH-ZC1H220P)	DO NOT POPULATE OR PURCHASE		
0	C3, C4, C13, C14 (GCM155R71H104KE02D)	DO NOT POPULATE OR PURCHASE		
0	C7, C8, C9, C10, C17, C18, C19, C20, C23, C24, C25, C26	DO NOT POPULATE OR PURCHASE		
1	AFFIX TO BACK OF PCB	LABEL-DATE CODE = LINE 1:YRWK-REV#, LINE 2:BOM NAME	Renesas Electronics America	LABEL-DATE CODE

3.4 Board Layout

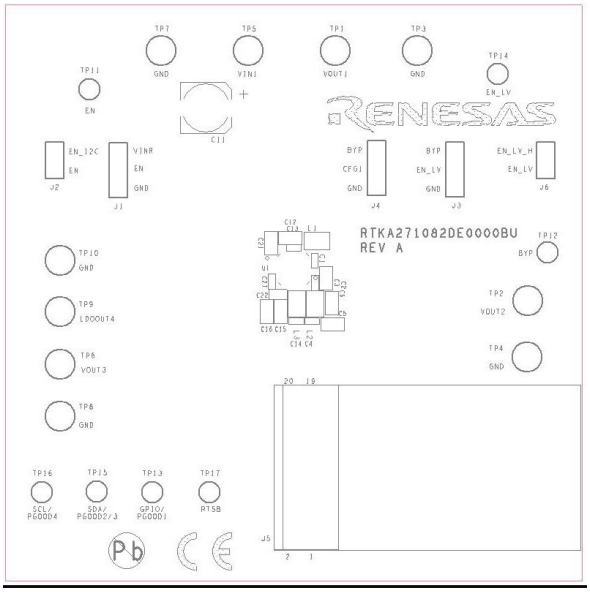

Figure 20. Top Layer Silkscreen

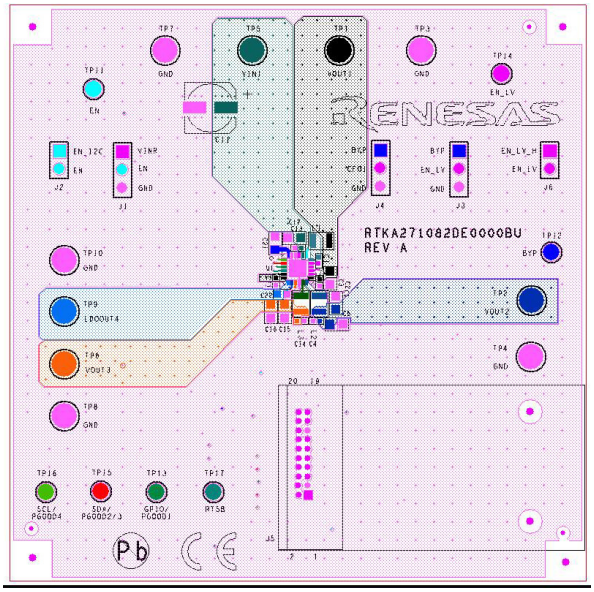

Figure 21. Top Layer Copper and Silkscreen

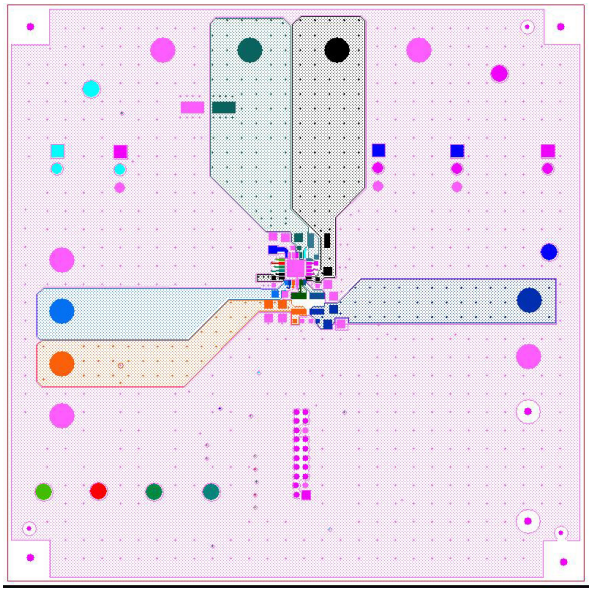

Figure 22. Top Layer

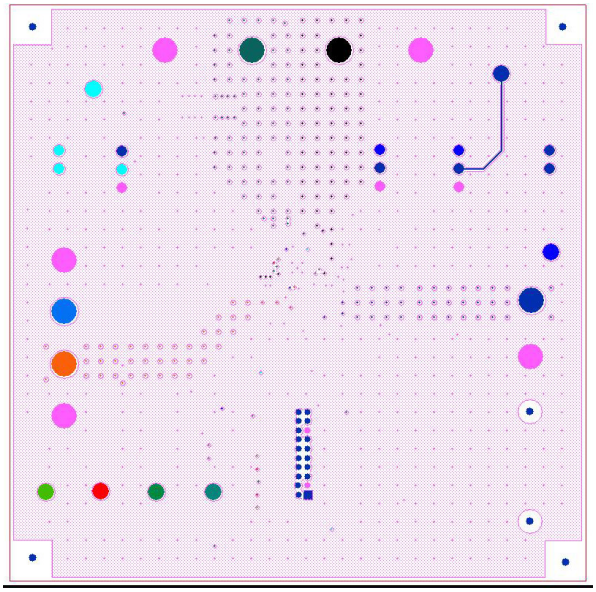

Figure 23. Layer 2

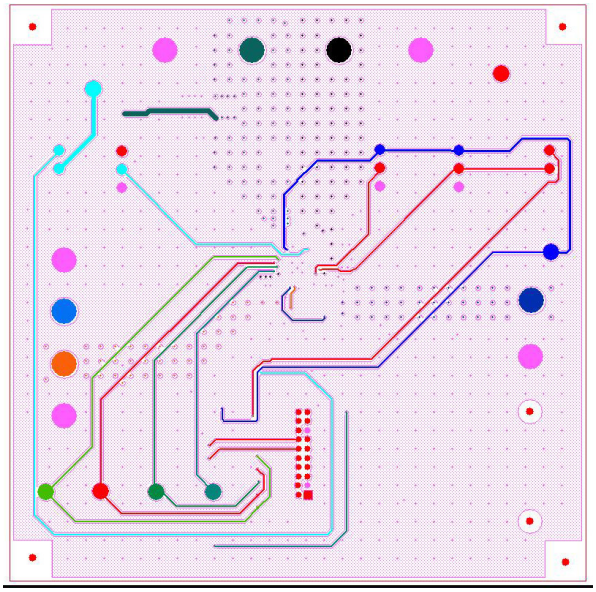

Figure 24. Layer 3

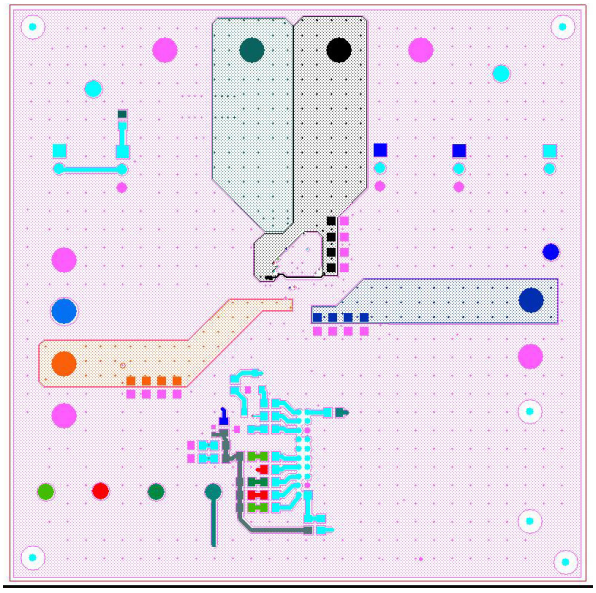

Figure 25. Bottom Layer

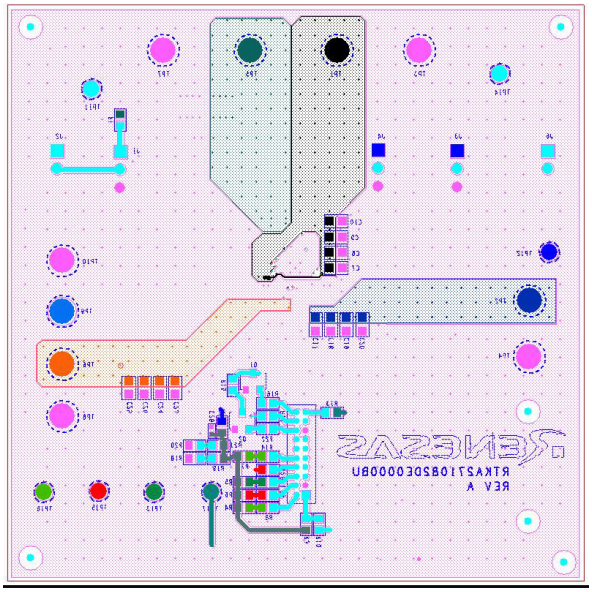

Figure 26. Bottom Layer Copper and Silkscreen

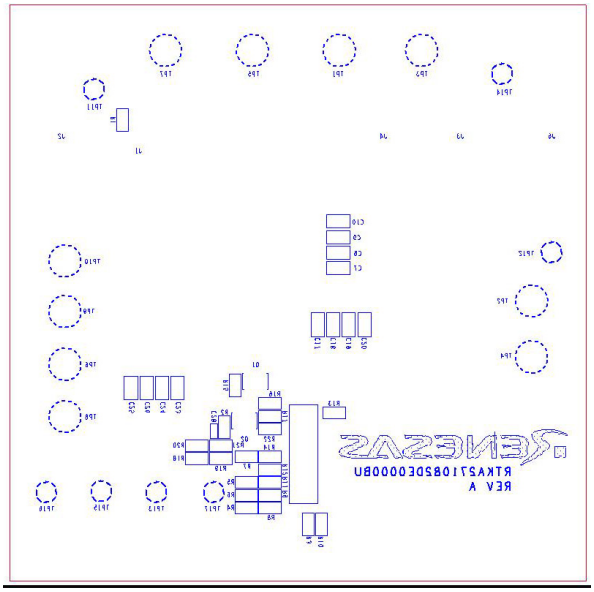

Figure 27. Bottom Layer Silkscreen

4. Typical Performance Graphs

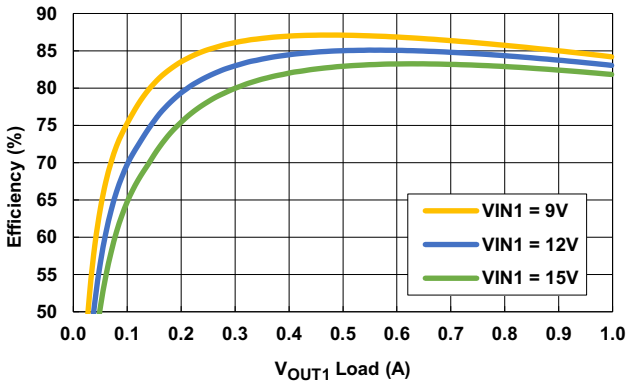

Figure 28. V_{IN} to V_{OUT1} = 3.8V, Efficiency vs Load

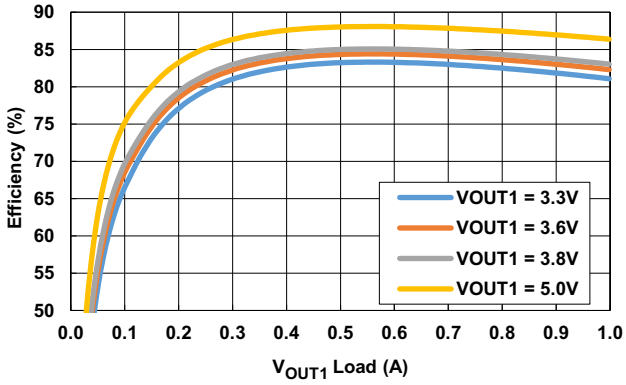

Figure 29. V_{IN} = 12V to V_{OUT1}, Efficiency vs Load

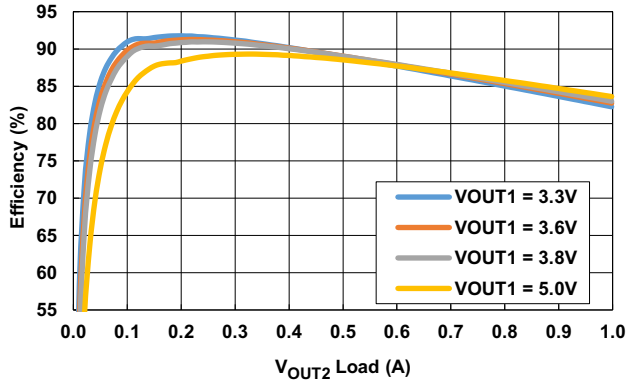

Figure 30. V_{OUT1} to V_{OUT2} = 1.8V, Efficiency vs Load

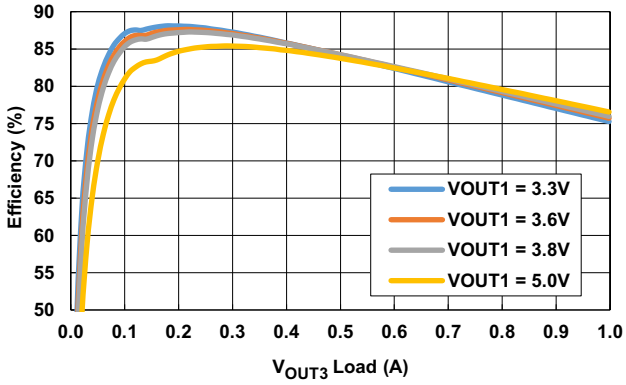

Figure 31. V_{OUT1} to V_{OUT3} = 1.2V, Efficiency vs Load

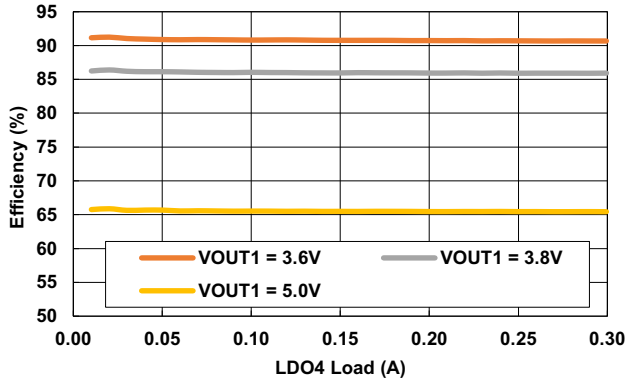

Figure 32. V_{OUT1} to LDO4 = 3.3V, Efficiency vs Load

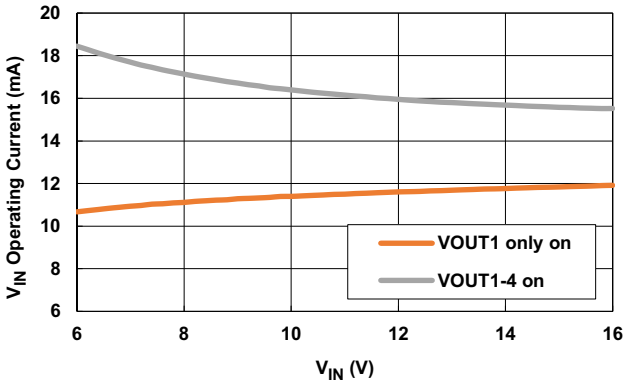

Figure 33. V_{IN} Operating Current, No Load

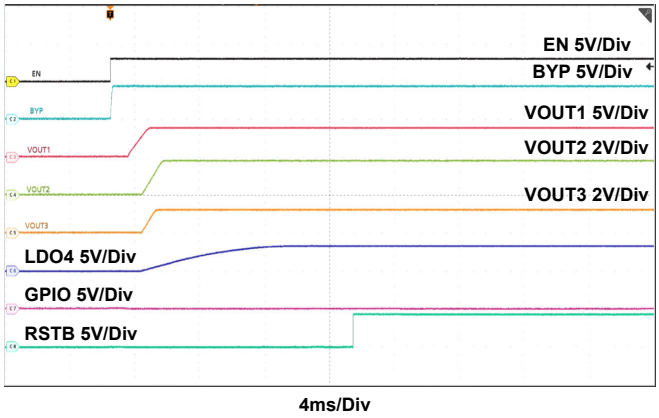

Figure 34. Startup using EN toggle, V_{IN} = 12V

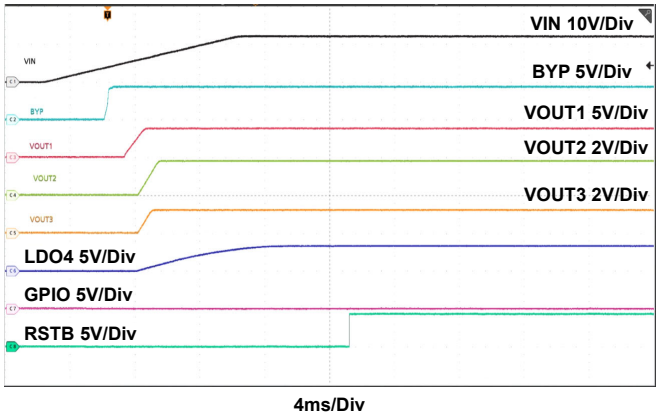

Figure 35. Startup using V_{IN} Ramp, EN Connected to VIN

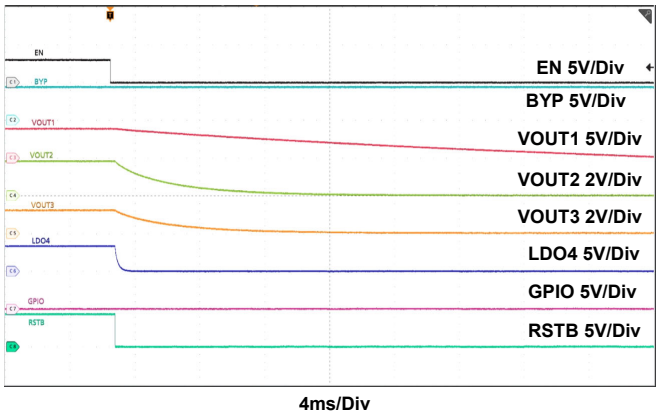

Figure 36. Shutdown using EN toggle, V_{IN} = 12V

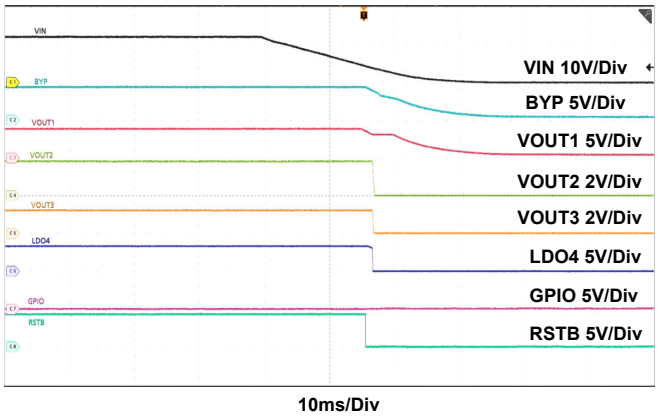

Figure 37. Shutdown using V_{IN} ramp, EN connected to VIN

5. Ordering Information

Part Number	Description
RTKA271082DE0000BU	RAA271082 Evaluation board

6. Revision History

Revision	Date	Description
1.00	Jul 25, 2022	Initial release

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