

ISL81806EVAL1Z

Evaluation Board

The ISL81806EVAL1Z dual-phase evaluation board (shown in [Figure 4](#)) features the ISL81806, an 80V high voltage dual synchronous buck controller, optimized for E-mode GaN FET, with external soft-start, independent enable functions and UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 2MHz helps to optimize the inductor size while the strong gate driver delivers up to 20A for the buck output.

Key Features

- Wide input range: 18V to 80V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Back-biased from output to improve efficiency

Specifications

The ISL81806EVAL1Z dual-phase evaluation board is designed for high current applications. The current rating of the ISL81806EVAL1Z is limited by the FETs and inductor selected. The ISL81806EVAL1Z electrical ratings are shown in [Table 1](#).

Table 1. ISL81806EVAL1Z Electrical Ratings

| Parameter | Rating |
|-----------------------------------|--------------------------------------|
| Input Voltage | 18V to 80V |
| Switching Frequency | 500kHz |
| Output Voltage | 12V |
| Output Current | 20A |
| Average Current OCP Setting Point | 25A (Constant Current Setting Point) |
| Pulse by Pulse OCP Setting Point | 20.5A (Each phase) |
| Hiccup OCP Setting point | 24.5A (Each phase) |

Ordering Information

| Part Number | Description |
|----------------|---|
| ISL81806EVAL1Z | High Voltage Dual Phase Buck Controller GaN FETs Evaluation Board |

Related Literature

For a full list of related documents, visit our website:

- [ISL81806](#) device page

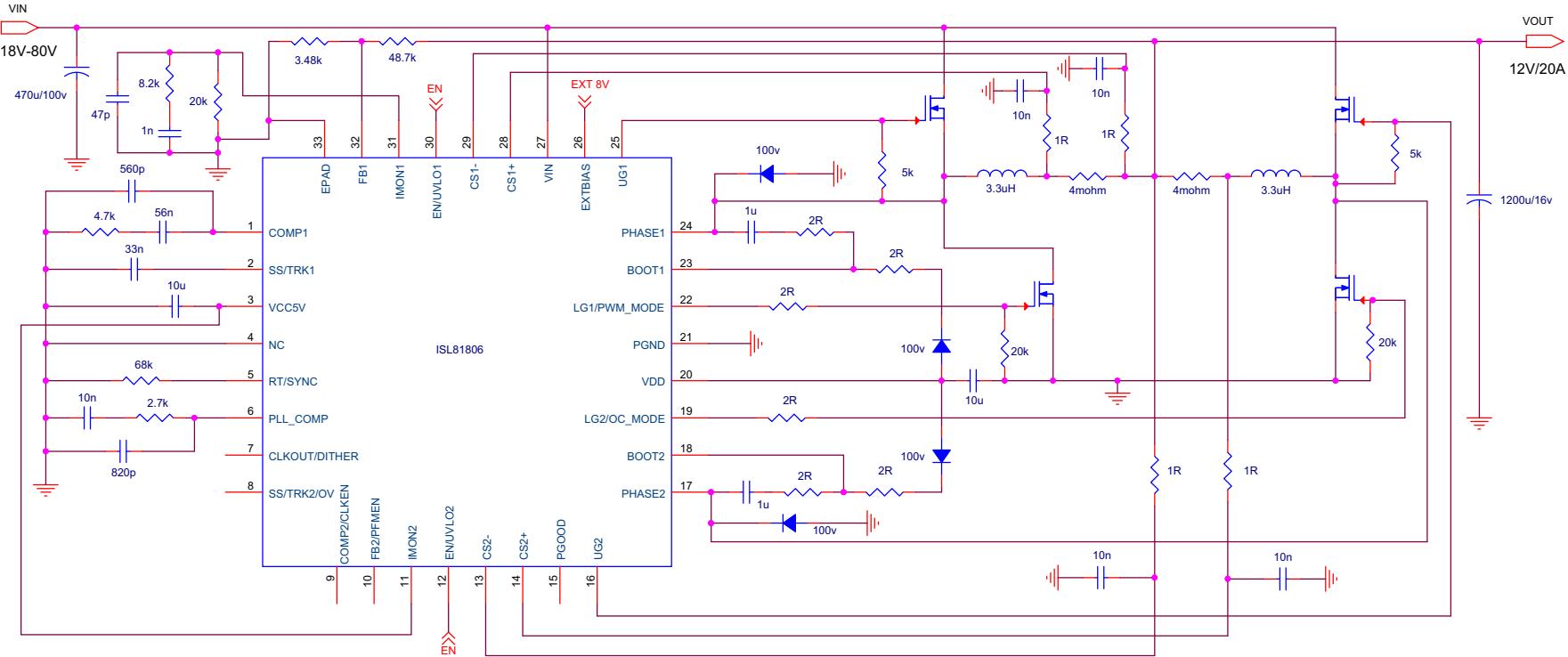


Figure 1. ISL81806EVAL1Z Block Diagram

1. Functional Description

The ISL81806EVAL1Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81806. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in [Figure 3](#), 18V to 80V V_{IN} is supplied to VIN and GND. The regulated 12V output on VOUT and GND can supply up to 20A to the load. Because of the high power efficiency, the evaluation board can run at 20A continuously with airflow 1700LFM at room ambient temperature conditions.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 80V power supply with at least 20A source current capability
- Electronic loads capable of sinking current up to 30A
- Digital Multimeter (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 18V to 80V for an output voltage of 12V. If the output voltage is set to a lower value, the minimum V_{IN} can be reset to a lower value by changing the ratio of R_{10} and R_{11} . The minimum EN threshold that V_{IN} can be set to is 4.5V.

The rated load current is 20A with the OCP point set at 20.5A at room ambient temperature conditions. The operating temperature range of this board is -40°C to +85°C.

Note: Airflow is needed for higher temperature conditions.

1.3 Quick Test Guide

1. Ensure that the circuit is correctly connected to the power supply and electronic loads before applying any power. See [Figure 3](#) for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see [Figure 2](#) for the proper test setup.

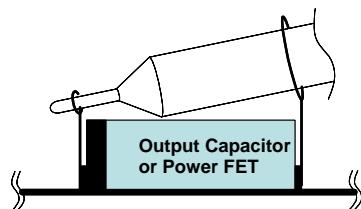


Figure 2. Proper Probe Setup to Measure Output Ripple

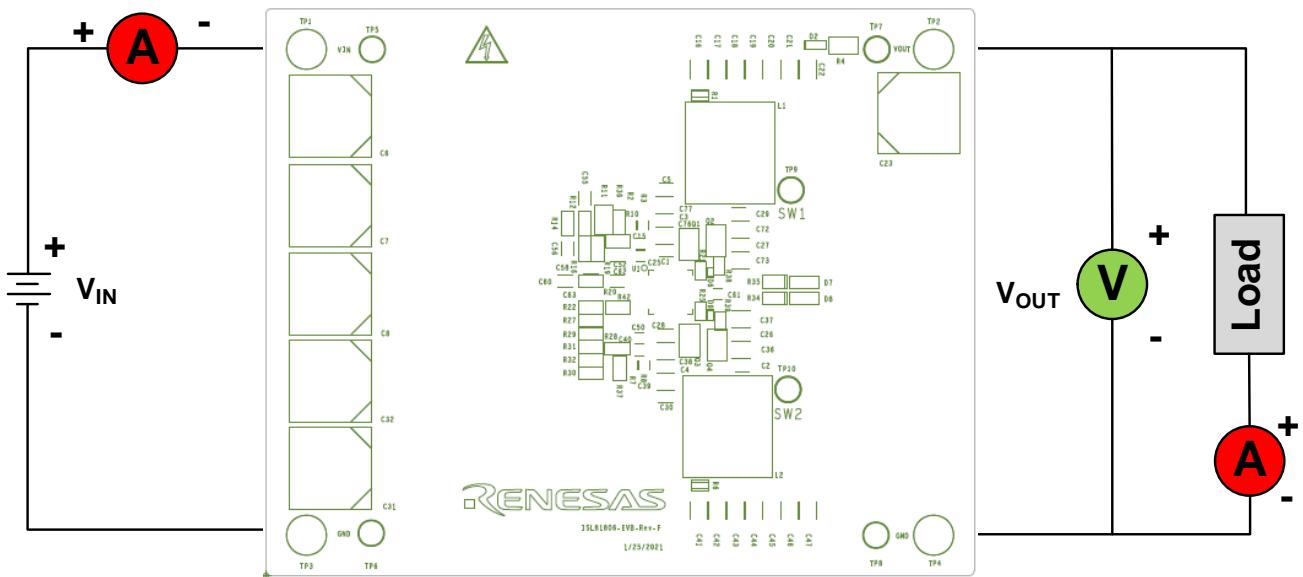


Figure 3. Proper Test Setup

2. Board Design

2.1 PCB Layout Guidelines

Careful attention to the Printed Circuit Board (PCB) layout requirements is necessary for the successful implementation of an ISL81806 based DC/DC converter. The ISL81806 switches at a high frequency; therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81806 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout.

1. Place the input capacitors, GaN FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors very close to the GaN FETs.
2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. **Note: DO NOT** connect them together anywhere else.
3. Keep the loop formed by the input capacitor, the top FET, and the bottom FET as small as possible.
4. Ensure the current paths from the input capacitor to the FETs, the power inductor, and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the FETs Gates. Especially the high side FET. The FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place the VDD bypass capacitor very close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via.
Note: DO NOT connect the PGND pin directly to the SGND EPAD.
7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
8. Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper filled polygons or wide, short traces to connect the junction of the upper FET, lower FET, and output inductor. Keep the PHASE nodes connection to the IC short. **Note: DO NOT** unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
10. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
11. Use a pair of traces with minimum loop for the input or output current sensing connection.

12. Ensure the feedback connection to the output capacitor is short and direct.

2.2 ISL81806EVAL1Z Evaluation Board

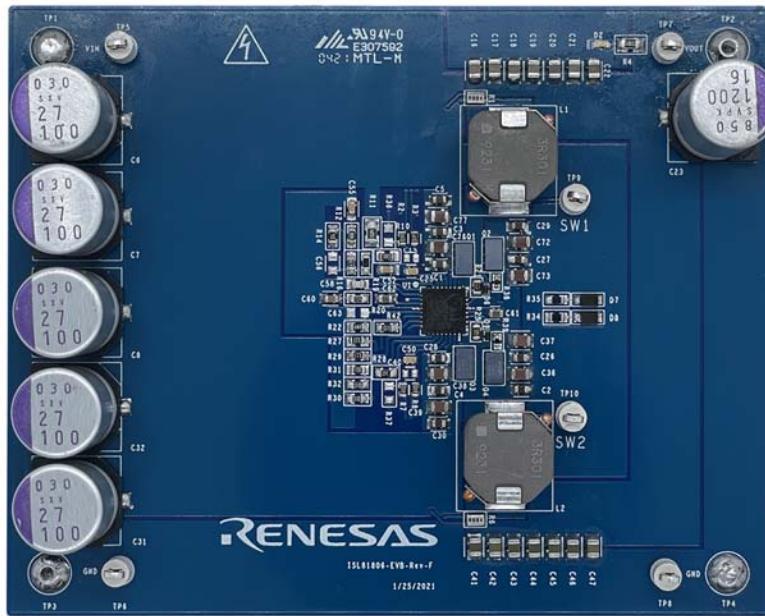


Figure 4. ISL81806EVAL1Z Evaluation Board, Top View

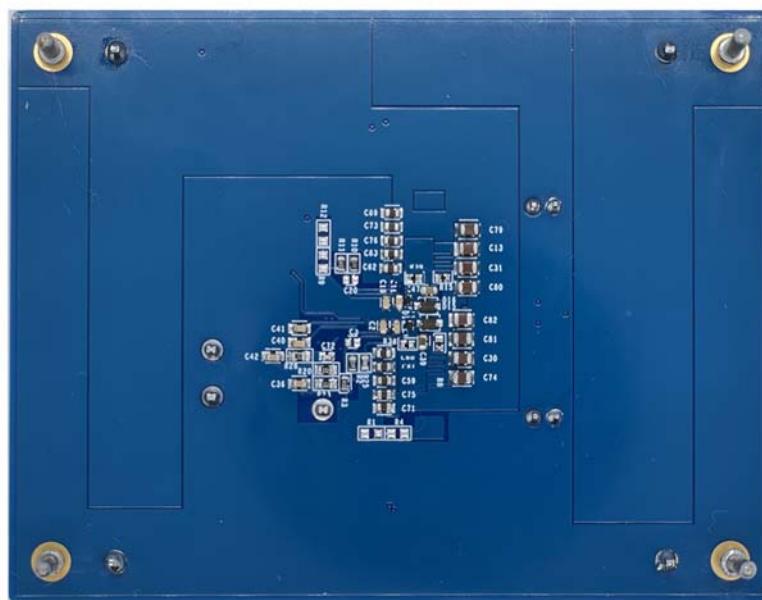


Figure 5. ISL81806EVAL1Z Evaluation Board, Bottom View

2.3 ISL81806EVAL1Z Circuit Schematic

ISL81806EVAL1Z User Manual

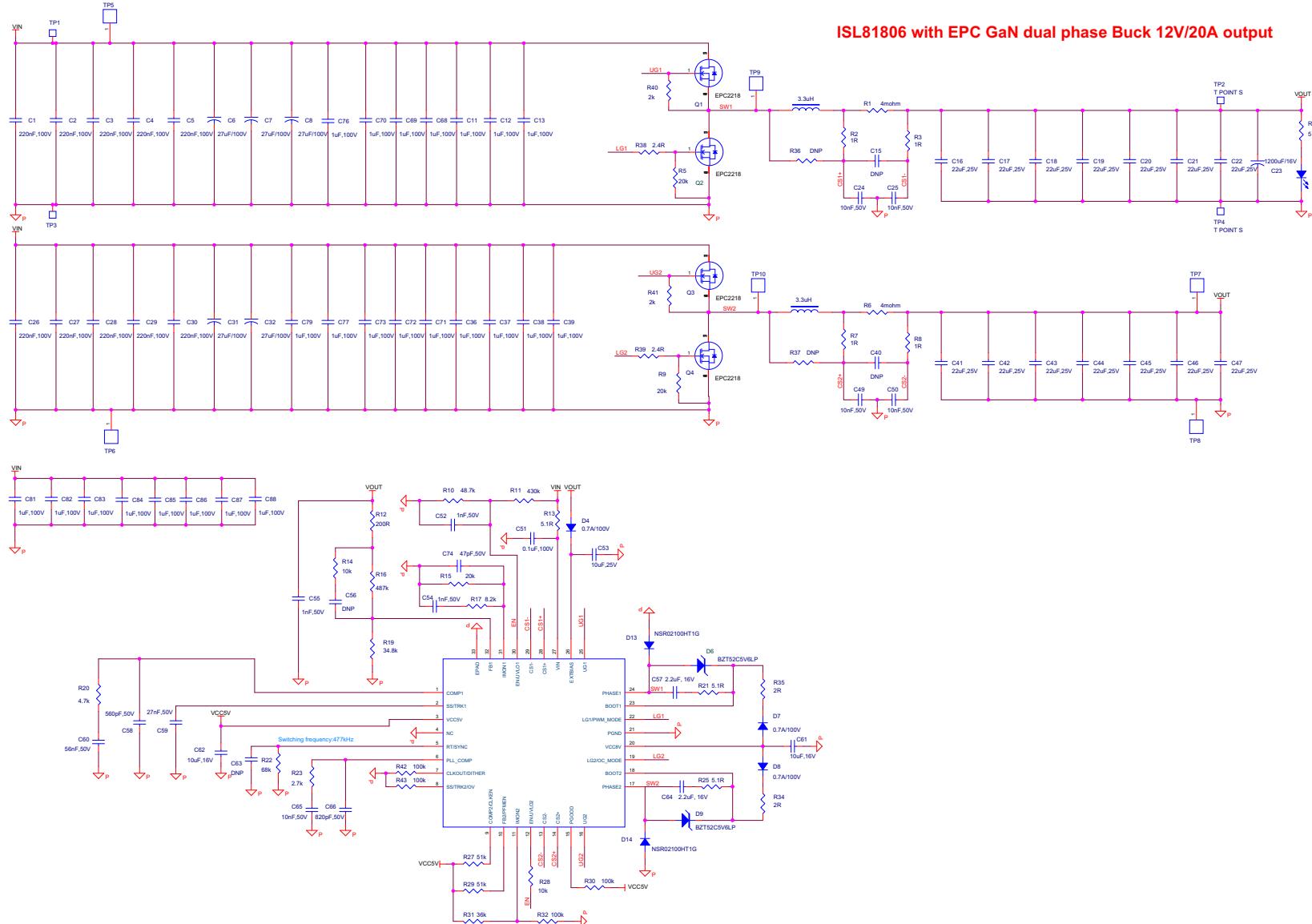


Figure 6. Schematic

2.4 Bill of Materials

| Qty | Reference Designator | Description | Manufacturer | Manufacturer Part |
|-----|--|--|---------------------------------------|-----------------------|
| 1 | | PWB-PCB, ISL81806EVAL1Z, REVF, ROHS | MTL (Multilayer PCB International) | ISL81806EVAL1ZREVFPCB |
| 1 | C65 | CAP, SMD, 0603, 0.01µF, 50V, 5%, C0G/NP0, SOFT TERMINATION, ROHS | TDK | C1608C0G1H103J080AE |
| 3 | C52, C54, C55 | CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS | TDK | C1608X7R1H102K |
| 1 | C51 | CAP, SMD, 0603, 0.1µF, 100V, 10%, X7S, ROHS | TDK | C1608X7S2A104K080AB |
| 14 | C16, C17, C18, C19, C20, C21, C22, C41, C42, C43, C44, C45, C46, C47 | CAP, SMD, 0805, 22µF, 25V, 20%, X5R, LOW ESL, ROHS | TDK | C2012X5R1E226M125AC |
| 24 | C11, C12, C13, C36, C37, C38, C39, C68, C69, C70, C71, C72, C73, C76, C77, C79, C81, C82, C83, C84, C85, C86, C87, C88 | CAP, SMD, 0805, 1µF, 100V, 10%, X7S, ROHS | TDK | C2012X7S2A105K125AB |
| 1 | C66 | CAP-AEC-Q200, SMD, 0603, 820pF, 50V, 5%, C0G/NP0, ROHS | TDK | CGA3E2C0G1H821J080AA |
| 4 | C24, C25, C49, C50 | CAP, SMD, 0402, 0.01µF, 50V, 10%, X7R, ROHS | VENKEL | C0402X7R500-103KNE |
| 1 | C61 | CAP, SMD, 0402, 10µF, 10V, 20%, X5R, ROHS | SAMSUNG | CL05A106MP8NUB8 |
| 2 | C57, C64 | CAP, SMD, 0402, 2.2µF, 25V, 10%, X5R, ROHS | TDK | C1005X5R1E225K050BC |
| 0 | C15, C40 | CAP, SMD, 0402, DNP- PLACE HOLDER, ROHS | | |
| 1 | C62 | CAP, SMD, 0603, 10µF, 16V, 10%, X5R, ROHS | MURATA | GRM188R61C106KAALD |
| 1 | C53 | CAP, SMD, 0603, 10µF, 25V, 20%, X5R, ROHS | TDK | C1608X5R1E106M080AC |
| 1 | C59 | CAP, SMD, 0603, 0.027µF, 50V, 10%, X7R, ROHS | VENKEL | C0603X7R500-273KNE |
| 1 | C74 | CAP, SMD, 0603, 47pF, 50V, 5%, C0G, NP0, ROHS | AVX | 06035A470JAT2A |
| 1 | C58 | CAP, SMD, 0603, 560pF, 50V, 5%, C0G, ROHS | VENKEL | C0603C0G500-561JNE |
| 1 | C60 | CAP, SMD, 0603, 0.056µF, 50V, 10%, X7R, ROHS | MURATA | GRM188R71H563KA93D |
| 0 | C56, C63 | CAP, SMD, 0603, DNP- PLACE HOLDER, ROHS | | |
| 10 | C1, C2, C3, C4, C5, C26, C27, C28, C29, C30 | CAP-AEC-Q200, SMD, 0603, 0.22µF, 100V, 10%, X7S, ROHS | TAIYO YUDEN | HMK107C7224KAHTE |

| Qty | Reference Designator | Description | Manufacturer | Manufacturer Part |
|-----|-------------------------------|---|----------------------------------|-------------------|
| 5 | C6, C7, C8, C31, C32 | CAP-OSCON, SMD, 10.3mm, 27 μ F, 100V, 20%, 30m Ω , POLYMER, ROHS | PANASONIC | 100SXV27M |
| 1 | C23 | CAP, SMD, 10.3mm, 1200 μ F, 16V, 20%, 12m Ω , ALUM.POLYMER, ROHS | PANASONIC | 16SVPK12000M |
| 2 | L1, L2 | COIL-PWR INDUCTOR, AEC-Q200, SMD, 10.5x10, 3.3 μ H, 14.5A, WW, ROHS | TDK | SPM10065VT-3R3M-D |
| 4 | TP1, TP2, TP3, TP4 | CONN-PC PIN, W/FLANGE, TH, 6.55mmPOST, 2.67mmTAIL, ROHS | KEYSTONE | 1377-2 |
| 6 | TP5, TP6, TP7, TP8, TP9, TP10 | CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS | KEYSTONE | 5007 |
| 2 | D6, D9 | DIODE-ZENER, SMD, 0402, 5.6V, 250mW, 7%, 40 Ω , ROHS | DIODES, INC. | BZT52C5V6LP-7 |
| 2 | D13, D14 | DIODE-SCHOTTKY, SMD, SOD-323, 100V, 200mA, ROHS | ON SEMICONDUCTOR | NSR02100HT1G |
| 3 | D4, D7, D8 | DIODE-SCHOTTKY, SMD, 2P, TUMD2M, 100V, 700mA, ROHS | ROHM | RB578VAM100TR |
| 1 | D2 | LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 574nm, 35mcd, ROHS | LITEON/VISHAY | LTST-C191KGKT |
| 1 | U1 | IC-80V PWM CONTROLLER for GaN, 32P, TQFN, 5x5, ROHS | RENESAS ELECTRONICS | ISL81806FRTZ |
| 4 | Q1, Q2, Q3, Q4 | TRANSISTOR-GaNFET, N-CHNL, 100V, 60A, SMD, BUMPED-DIE, ROHS | EPC (Efficient Power Conversion) | EPC2218 |
| 1 | R10 | RES, SMD, 0603, 48.7k, 1/10W, 1%, TF, ROHS | VISHAY/DALE | CRCW060348K7FKEAC |
| 1 | R11 | RES-AEC-Q200, SMD, 0805, 430k, 1/8W, 1%, TF, ROHS | VISHAY/DALE | CRCW0805430KFKEA |
| 4 | R2, R3, R7, R8 | RES, SMD, 0402, 1 Ω , 1/16W, 1%, TF, ROHS | VISHAY/DALE | CRCW04021R00FKED |
| 2 | R38, R39 | RES, SMD, 0402, 2.4 Ω , 1/16W, 1%, TF, ROHS | VISHAY/DALE | CRCW04022R40FKED |
| 2 | R21, R25 | RES, SMD, 0402, 5.1 Ω , 1/16W, 1%, TF, ROHS | YAGEO | AC0402FR-075R1L |
| 2 | R40, R41 | RES, SMD, 0402, 2k, 1/16W, 1%, TF, ROHS | PANASONIC | ERJ-2RKF2001 |
| 2 | R5, R9 | RES, SMD, 0402, 20k, 1/16W, 1%, TF, ROHS | PANASONIC | ERJ2RKF2001 |
| 2 | R34, R35 | RES, SMD, 0603, 2 Ω , 1/10W, 1%, TF, ROHS | YAGEO | 9C06031A2R00FGHFT |

| Qty | Reference Designator | Description | Manufacturer | Manufacturer Part |
|-----|----------------------|---|--------------|----------------------|
| 1 | R13 | RES, SMD, 0603, 5.1Ω, 1/10W, 1%, TF, ROHS | YAGEO | RC0603FR-075R1L |
| 2 | R14, R28 | RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-1002FT |
| 4 | R30, R32, R42, R43 | RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-1003FT |
| 1 | R12 | RES, SMD, 0603, 200Ω, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-2000FT |
| 1 | R15 | RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-2002FT |
| 1 | R19 | RES, SMD, 0603, 34.8k, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-3482FT |
| 1 | R31 | RES, SMD, 0603, 36k, 1/10W, 1%, TF, ROHS | PANASONIC | ERJ-3EKF3602V |
| 1 | R20 | RES, SMD, 0603, 4.7k, 1/10W, 1%, TF, ROHS | YAGEO | 9C06031A4701FKHFT |
| 1 | R16 | RES, SMD, 0603, 487k, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-4873FT |
| 2 | R27, R29 | RES, SMD, 0603, 51k, 1/10W, 1%, TF, ROHS | YAGEO | RC0603FR-0751KL |
| 1 | R22 | RES, SMD, 0603, 68k, 1/10W, 1%, TF, ROHS | YAGEO | RC0603FR-0768KL |
| 1 | R17 | RES, SMD, 0603, 8.2k, 1/10W, 1%, TF, ROHS | ROHM | MCR03EZPFX8201 |
| 0 | R36, R37 | RES, SMD, 0603, DNP-PLACE HOLDER, ROHS | | |
| 1 | R4 | RES, SMD, 0805, 5.1k, 1/8W, 1%, TF, ROHS | PANASONIC | ERJ-6ENF5101V |
| 2 | R1, R6 | RES-AEC-Q200, SMD, 0805-WIDE, 0.004Ω, 1W, 1%, ROHS | SUSUMU | KRL2012E-M-R004-F-T5 |
| 1 | R23 | RES-AEC-Q200, SMD, 0603, 2.7k, 1/4W, 1%, TF, ROHS | VISHAY/DALE | RCS06032K70FKEA |
| 4 | Bottom four corners | BUMPONS, 0.44inWx0.20inH, CYLINDRICAL DOME, BLK, ROHS | 3M | SJ-5003 (BLACK) |

2.5 Board Layout

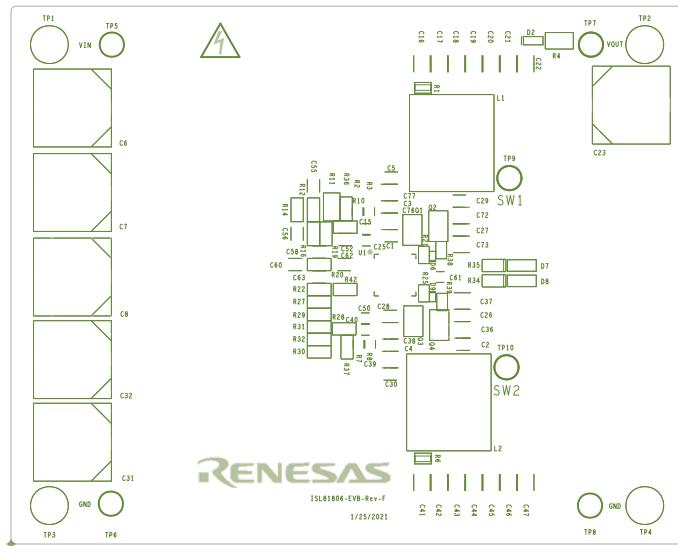


Figure 7. Silkscreen Top

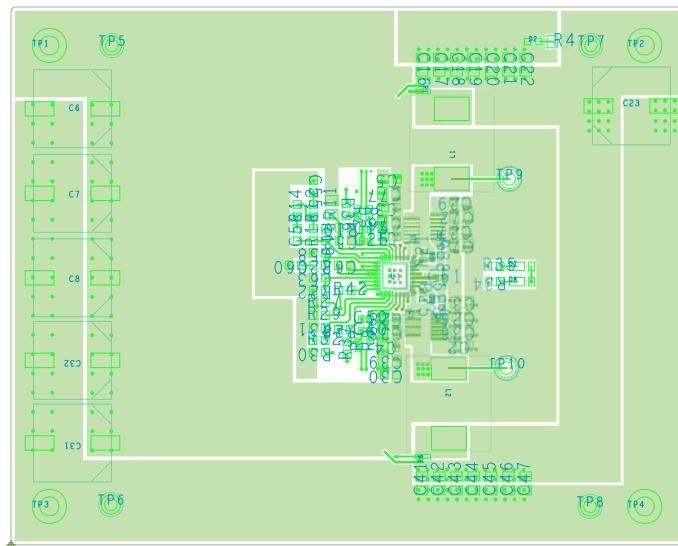


Figure 8. Top Layer

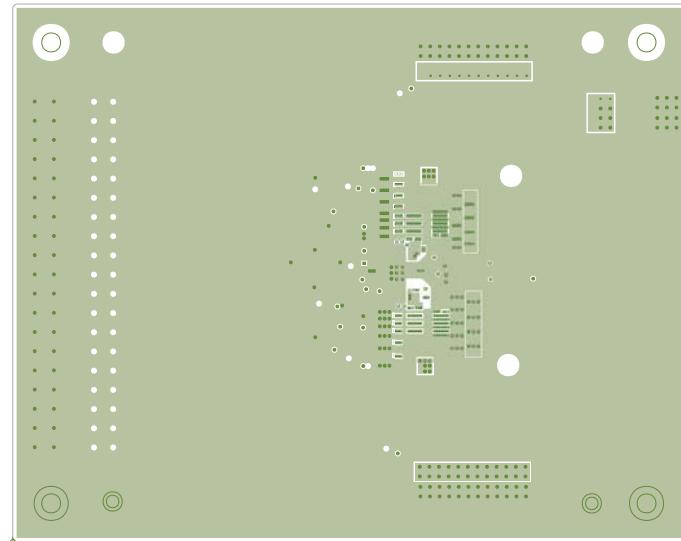


Figure 9. Second Layer (Solid Ground)

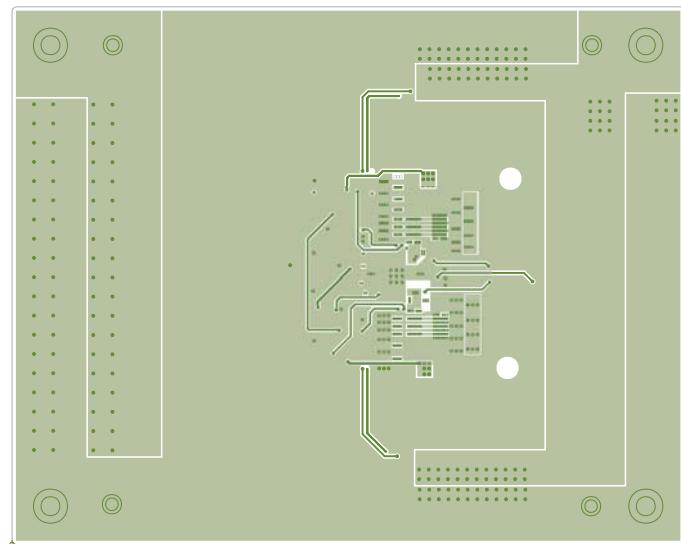


Figure 10. Third Layer

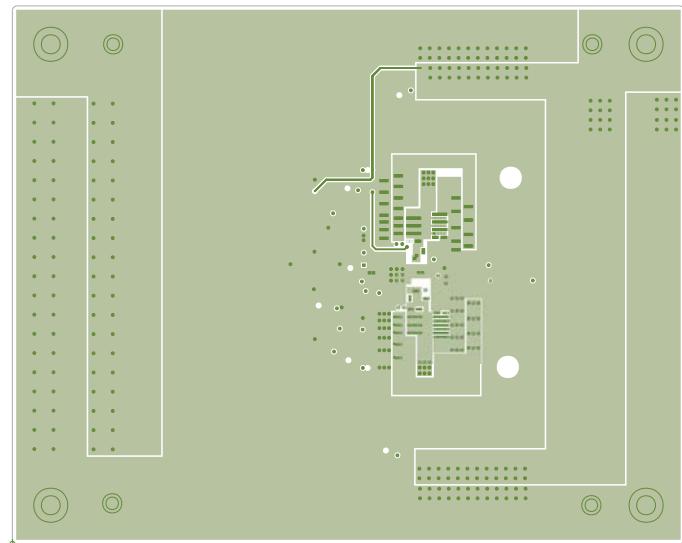


Figure 11. Fourth Layer

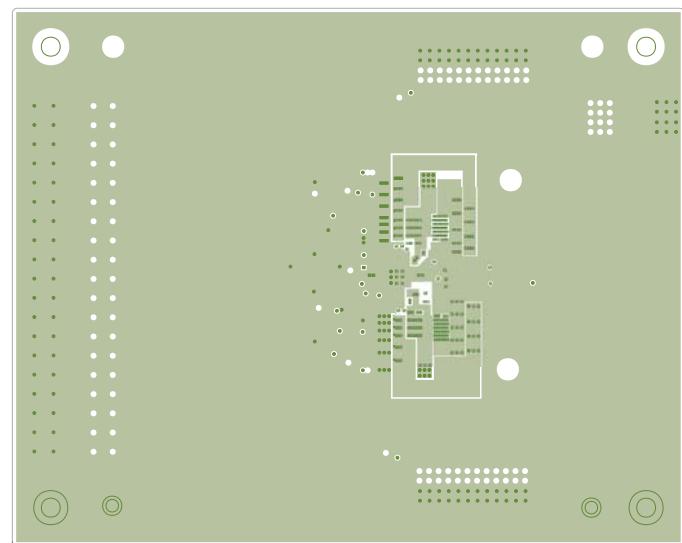


Figure 12. Fifth Layer

Figure 13. Bottom Layer

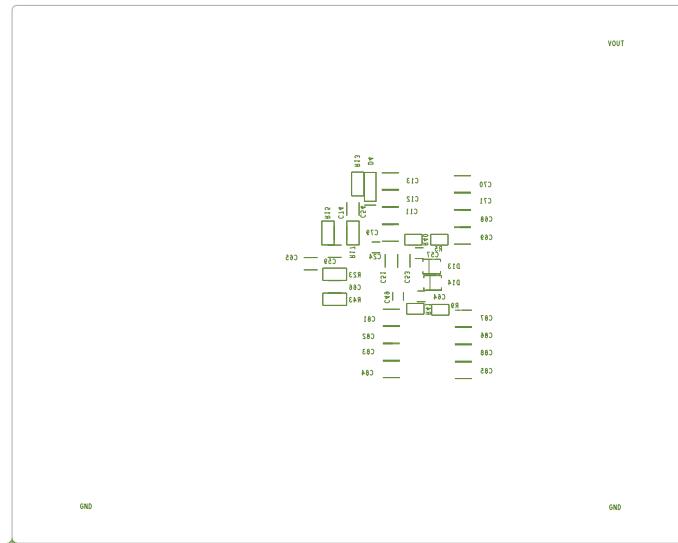


Figure 14. Silkscreen Bottom

3. Design Example

3.1 Design Requirements

| Parameter | Rating |
|------------------------------|------------------|
| Input Voltage | 18V to 80V |
| Switching Frequency | 500kHz |
| Output Voltage | 12V |
| Output Current | 20A |
| Peak Current Limit Set Point | 20.5A per phase |
| Output Mode | Dual phase |
| PWM Mode | Forced PWM |
| OCP Mode | Constant current |

3.2 Frequency Setting

The default switching frequency of the PWM controller is determined by the resistor R_T (R_{22}). It adjusts the default switching frequency from 100kHz to 2MHz. The R_T value for $f_{SW} = 500\text{kHz}$ is calculated using [Equation 1](#).

$$(\text{EQ. 1}) \quad R_T = \left(\frac{34.7}{f_{SW}} - 4.78 \right) = \frac{34.7}{0.5} - 4.78 = 64.62\text{k}\Omega$$

where f_{SW} is the switching frequency in MHz. Select a standard value resistor $R_T = 68\text{k}\Omega$.

3.3 Output Voltage Setting

The output voltage can be set from 0.8V up to a level determined by the feedback voltage divider. A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB_OUT pin. With $V_{OUT} = 12V$ and R_{FBO1} (R_{16}) = 487k, the R_{FBO2} (R_{19}) value is calculated using [Equation 2](#).

$$(\text{EQ. 2}) \quad R_{FBO2} = \frac{0.8V \times R_{FBO1}}{V_{OUT} - 0.8V} = \frac{0.8V \times 487\text{k}\Omega}{12V - 0.8V} = 34.78\text{k}\Omega$$

where R_{FBO1} (R_{16}) is the top resistor of the feedback divider network and R_{FBO2} (R_{19}) is the bottom resistor connected from FB_OUT to ground. Select a standard value resistor $R_{FBO2} = 34.8\text{k}\Omega$.

3.4 UVLO Setting

The ISL81806 has input UVLO protection. When the voltage on the EN/UVLO pin reaches 1.8V, the PWM modulator is enabled. Accurate UVLO feature can be implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} ($R11$) and R_{UV2} ($R10$). The V_{IN} UVP rising threshold is calculated using [Equation 3](#).

$$(\text{EQ. 3}) \quad V_{UVRISE} = \frac{V_{UVLO_THR}(R_{UV1} + R_{UV2}) - I_{LEAK}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(430\text{k}\Omega + 48.7\text{k}\Omega) - 2.8\mu\text{A}(430\text{k}\Omega)(48.7\text{k}\Omega)}{48.7\text{k}\Omega} = 16.49\text{V}$$

The V_{IN} UVP falling threshold is calculated using [Equation 4](#).

$$(EQ. 4) \quad V_{UVFALL} = \frac{V_{UVLO_THR}(R_{UV1} + R_{UV2}) - I_{UVLO_HYST} R_{UV1} R_{UV2}}{R_{UV2}} = \frac{1.8V(430k\Omega + 48.7k\Omega) - 6.8\mu A(430k\Omega)(48.7k\Omega)}{48.7k\Omega} = 14.77V$$

where V_{UVLO_THR} is the 1.8V UVLO rising threshold and I_{UVLO_HYST} is the 6.8 μ A UVLO hysteresis current.

3.5 Soft-Start Capacitor

The soft-start time for dual-phase is set by the value of the soft-start capacitor C_{SS} (C_{59}) connected from SS/TRK1 to GND. The soft-start time with $C_{SS} = 27nF$ is calculated using [Equation 5](#).

$$(EQ. 5) \quad t_{SS} = 0.8V \left(\frac{C_{SS}}{4\mu A} \right) = 0.8V \times \left(\frac{27nF}{4\mu A} \right) = 5.4ms$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

3.6 GaN FETs Considerations

The GaN FETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations. The maximum operation voltage of the GaN FETs in Buck mode is decided by the maximum V_{IN} voltage.

The power loss of the upper and lower GaN FETs for each phase is calculated using [Equation 6](#) and [Equation 7](#). The equations assume linear voltage current transitions and do not model power loss due to the reverse recovery for the body diode of the lower GaN FET.

$$(EQ. 6) \quad P_{UPPERMAX} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{OUT})}{V_{INMAX}} + \frac{(I_{OUT})(V_{INMAX})(t_{SW})(f_{SW})}{2}$$

$$= \frac{(10A)^2(3.2m\Omega)(12V)}{80V} + \frac{(10A)(80V) \left(\frac{1.5nC}{\frac{5V - 1.1V}{8.1\Omega}} + \frac{1.5nC}{\frac{1.1V}{2\Omega}} \right) (477kHz)}{2} = 0.048W + 1.115W = 1.163W$$

$$(EQ. 7) \quad P_{LOWERMAX} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{INMAX} - V_{OUT})}{V_{INMAX}}$$

$$= \frac{(10A)^2(3.2m\Omega)(80V - 12V)}{80V} = 0.272W$$

Ensure that all GaN FETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

3.7 Inductor Selection

The inductor value determines the ripple current of the converter. The ripple voltage is a function of the ripple current and the output capacitor(s) ESR. Assume the ripple current ratio is 80% of the inductor average current at the maximum input voltage and the full output load condition. The inductor value for each phase is calculated using [Equation 8](#).

$$(EQ. 8) \quad L_{INMIN} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(0.8 \times I_{OUTMAX})(V_{INMAX})} = \frac{(80V - 12V)(12V)}{(477\text{kHz})(0.8 \times 10A)(80V)} = 2.67\mu\text{H}$$

The recommended inductor value is $3.3\mu\text{H}$. Then the ripple current and peak current are calculated using [Equation 9](#), [Equation 10](#), and [Equation 11](#).

$$(EQ. 9) \quad \Delta I_{LMAX} = \frac{(V_{INMAX} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{INMAX})} = \frac{(80V - 12V)(12V)}{(477\text{kHz})(3.3\mu\text{H})(80V)} = 6.48\text{A}$$

$$(EQ. 10) \quad I_{LRMS} = \sqrt{(I_{OUTMAX})^2 + \frac{(\Delta I_{LMAX})^2}{12}} = \sqrt{(10\text{A})^2 + \frac{(6.48\text{A})^2}{12}} = 10.17\text{A}$$

$$(EQ. 11) \quad I_{LPKMAX} = \frac{I_{OUTOCP}}{2} + \frac{\Delta I_{LMAX}}{2} = \frac{20\text{A}}{2} + \frac{6.48\text{A}}{2} = 13.24\text{A}$$

The saturation current of the inductor should be larger than OCP point of 20.5A . The heat rating current of the inductor should be larger than 10.17A .

The maximum DC power dissipation in the inductor is calculated using [Equation 12](#).

$$(EQ. 12) \quad P_{LMAX} = (I_{OUT})^2(DCR) = (10\text{A})^2 \times (6\text{m}\Omega) = 0.6\text{W}$$

3.8 Output Capacitor Selection

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in [Equation 13](#).

$$(EQ. 13) \quad C_{OUTMIN} = \frac{L(I_{TRAN})^2}{2(V_{INMIN} - V_{OUT})(\Delta V_{OUT})} = \frac{3.3\mu\text{H} \times (10\text{A} - 0\text{A})^2}{2(18V - 12V)(12V \times \frac{1.5}{100})} = 152.8\mu\text{F}$$

where C_{OUTMIN} is the minimum output capacitor(s) required, I_{TRAN} is the transient load current step, and ΔV_{OUT} is the drop in output voltage allowed during the load transient. Choose a capacitor no less than $152.8\mu\text{F}$ for each phase. A $1200\mu\text{F}$ electrolytic capacitor and $154\mu\text{F}$ MLCC in total are used for each phase on this board.

The output voltage ripple is because of the inductor ripple current and the ESR of the output capacitors as defined by [Equation 14](#).

$$(EQ. 14) \quad V_{RIPPLE} = \Delta I_{LMAX} \times \text{ESR} = 6.48\text{A} \times 5\text{m}\Omega = 32.4\text{mV}$$

3.9 Input Capacitor Selection

The important parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load given in [Equation 15](#).

$$(EQ. 15) \quad I_{RMS} = \sqrt{\left(D - \frac{\text{floor}(2 \times D)}{2}\right) \times \left(\frac{1 + \text{floor}(2 \times D)}{2} - D\right)} \times I_{OUT}$$

where $\text{floor}(2 \times D)$ equals 0 when $D < 0.5$ and equals 1 when $D \geq 0.5$.

The maximum RMS current for two phases in total supplied by the input capacitance occurs at $D = 0.25$ and $D = 0.75$, and only $D = 0.25$ is within the range of this application. Therefore, the maximum AC RMS current is shown in [Equation 16](#).

$$(EQ. 16) \quad I_{RMSMAX} = \sqrt{D \times \left(\frac{1}{2} - D\right)} \times I_{OUTMAX} = \sqrt{0.25 \times \left(\frac{1}{2} - 0.25\right)} \times 10A = 2.5A$$

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the GaN FETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Five 27 μ F electrolytic capacitors with 0.94A rating current and eight 25.2 μ F ceramic capacitors are used to share the 2.5A RMS input current on this board.

3.10 First Level Peak Current Limit and Sense Resistor Selection

The inductor peak current is sensed by the sense resistor R_S (R_1/R_6). When the voltage drop on R_S reaches the set point $V_{OCSET-CS}$ typical 82mV, it triggers the pulse-by-pulse peak current limit. With the current limit set point $I_{OCPP1} = 2 \times I_{OUTMAX} = 20A$ for each phase, the value of the sense resistor is calculated using [Equation 17](#).

$$(EQ. 17) \quad R_S = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{82mV}{20A} = 4.1m\Omega$$

Select a standard value resistor $R_S = 4m\Omega$. Then the actual peak current limit is calculated using [Equation 18](#).

$$(EQ. 18) \quad I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{82mV}{4m\Omega} = 20.5A$$

The maximum power dissipation in R_S is calculated by [Equation 19](#).

$$(EQ. 19) \quad P_{RSMAX} = (I_{OUT})^2 R_S = (10A)^2 (4m\Omega) = 0.4W$$

Therefore, a sense resistor with 1W power rating is sufficient for this application.

3.11 Second Level Hiccup Peak Current Protection

In the output dead short condition especially at high V_{IN} , the inductor current runs away with the minimum on PWM duty. The ISL81806 integrates a second level hiccup type of peak current protection. The second level peak current protection set point I_{OCPP2} is calculated using [Equation 20](#).

$$(EQ. 20) \quad I_{OCPP2} = \frac{V_{OCSET-CS-HIC}}{R_S} = \frac{98mV}{4m\Omega} = 24.5A$$

3.12 Output Average Overcurrent Protection and R_{IM} Selection

The ISL81806 provides either constant current or hiccup type of overcurrent protection for output average current. The OCP mode is set by a resistor connected between the LG2/OC_MODE pin and ground. With output constant current/hiccup set point $I_{OUTOCP} = 25A$ for two phases in total, the current monitoring resistor R_{IM} (R_{15}) is calculated using [Equation 21](#).

$$(EQ. 21) \quad R_{IM} = \frac{1.2}{I_{OUTOCP} \times R_S \times Gm_{CS} + 2 \times I_{CSOFFSET}} = \frac{1.2V}{25A \times 4m\Omega \times 200\mu S + 2 \times 20\mu A} = 20k\Omega$$

where $I_{CSOFFSET}$ is the output current sense op amp internal offset current, typical $20\mu A$. Select a standard value resistor $R_{IM} = 20k\Omega$. (R_{IM} Should be within 17k to 24k to ensure good current sharing.)

3.13 Output Mode Selection

The IMON2 pin voltage is set to be higher than 3V, and the IC is set for one output dual-phase application. The original IMON2 current monitor function pin is disconnected from the IMON2 pin and internally connected to the IMON1 pin.

3.14 PWM Mode Selection

The ISL81806 can be set to either forced PWM mode or DE mode. The mode is set by a resistor $R_{PWMMODE}$ (R_5) connected between the LG1/PWM_MODE pin and GND. The boundary resistor value for $R_{PWMMODE}$ is calculated using [Equation 22](#).

$$(EQ. 22) \quad R_{PWMMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than $30k\Omega$ sets the converter to forced PWM mode, while a resistor higher than $30k\Omega$ sets the converter to DE mode. Considering the tolerance in all temperature ranges, Renesas recommends using $20k\Omega$ to set Forced PWM mode and $39k\Omega$ to set DE mode. With a GaN FET application, there is an approximately $1M\Omega$ resistance between the drain and the gate. The pre-bias voltage on the VOUT supplies to the gate using this $1M\Omega$ resistor. The equation must be corrected by this factor. Most importantly, the gate voltage must be kept lower than the minimum gate threshold voltage of the GaN FET, which is typically 0.8V to avoid GaN FET damage in the initial stage.

3.15 Overcurrent Protection Mode Selection

The ISL81806 is set to either a constant current or hiccup type of overcurrent protection for output average current by selecting a different value of the resistor R_{OCMODE} (R_9) connected between LG2/OC_MODE and GND. The boundary resistor value for R_{OCMODE} is calculated using [Equation 23](#).

$$(EQ. 23) \quad R_{OCMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than $30k\Omega$ sets the converter to constant current mode, while a resistor higher than $30k\Omega$ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges, Renesas recommends using $20k\Omega$ to set constant current and $39k\Omega$ to set the Hiccup mode. With a GaN FET application, there is an approximately $1M\Omega$ resistance between the drain and the gate. The pre-bias voltage on the VOUT supplies to the gate using this $1M\Omega$ resistor. The equation must be corrected by this factor. Most importantly, the gate voltage must be kept lower than the minimum gate threshold voltage of the GaN FET, which is typically 0.8V to avoid GaN FET damage in the initial stage.

3.16 Phase Lock Loop (PLL)

The PLL of the ISL81806 ensures the wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting. The external compensation network of R_{PLL} (R_{23}), C_{PLL1} (C_{65}), and C_{PLL2} (C_{66}) are needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7k Ω for R_{PLL} , 10nF for C_{PLL1} , and 820pF for C_{PLL2} .

3.17 Feedback Loop Compensation

Due to the current loop feedback, the modulator has a single pole response with -20dB slope at a frequency determined by the load using [Equation 24](#).

$$(EQ. 24) \quad F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} = \frac{1}{2\pi \cdot \frac{12V}{10A} \cdot 1354\mu F} = 98\text{Hz}$$

where R_O is load resistance and C_O is total load capacitance for each phase. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

[Figure 15](#) shows a Type 2 amplifier and its response, along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region between the zero and the pole. The R_{COMP} , C_{COMP1} , and C_{COMP2} network connected on the Gm regulator output COMP pin is needed to compensate the loop for stable operation. The loop stability can be affected by many different factors such as V_{IN} , V_{OUT} , load current, switching frequency, inductor value, output capacitance, and the compensation network on the COMP pin.

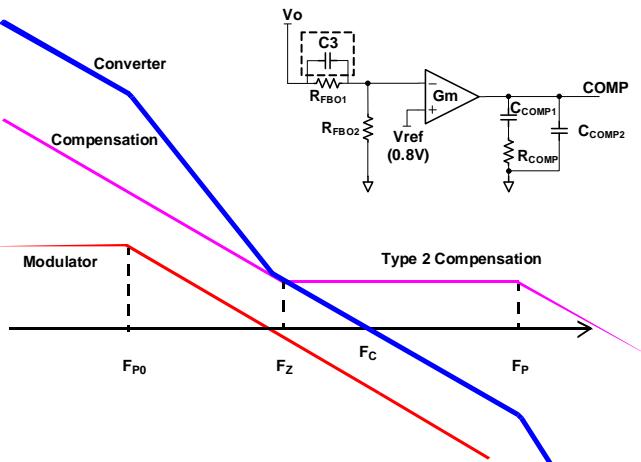


Figure 15. Feedback Loop Compensation

High amplifier zero frequency gain and modulator gain are chosen to satisfy most typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high-frequency gain. The crossover frequency F_C is usually about 1/10 to 1/30 of switching frequency. To fulfill the various applications, large value capacitors are used on the output side. Therefore, a reasonable target crossover frequency F_C in this application is 4kHz.

The compensation zero F_Z is usually placed between F_{PO} and F_C . Setting F_Z to 0.5kHz, with C_{COMP1} (C_{60}) = 56nF, the R_{COMP} (R_{20}) is calculated using [Equation 25](#).

$$(EQ. 25) \quad R_{COMP} = \frac{1}{2\pi \cdot F_Z \cdot C_{COMP1}} = \frac{1}{2\pi \cdot 1.6\text{kHz} \cdot 56\text{nF}} = 4.74\text{k}\Omega$$

Select a standard value resistor $R_{COMP} = 4.7\text{k}\Omega$. A larger C_{COMP1} makes the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. Lower R_{COMP} improves stability but slows the loop response.

A high-frequency pole F_P is placed by a capacitor C_{COMP2} (C_{58}) in parallel with R_{COMP} and C_{COMP1} . Set the frequency of this pole at about 7 to 10 times of crossover frequency F_C to provide attenuation of switching ripple and noise on COMP, while avoiding excessive phase loss at the crossover frequency. For a target $F_P = 60\text{kHz}$, the C_{COMP2} is calculated using [Equation 26](#).

$$(EQ. 26) \quad C_{COMP2} = \frac{1}{2\pi \cdot R_{COMP1} \cdot F_P} = \frac{1}{2\pi \cdot 4.7\text{k}\Omega \cdot 60\text{kHz}} = 564.7\text{pF}$$

Select a standard value capacitor $C_{COMP2} = 560\text{pF}$.

Some phase boost can be achieved by connecting capacitor C_{56} in parallel with the upper resistor R_{FBO1} of the divider. These values provide a good starting point for the compensation design, and the final compensation network should be optimized with bench test.

4. Typical Performance Curves

$V_{IN} = 48V$, $T_A = 25^\circ C$, unless otherwise noted.

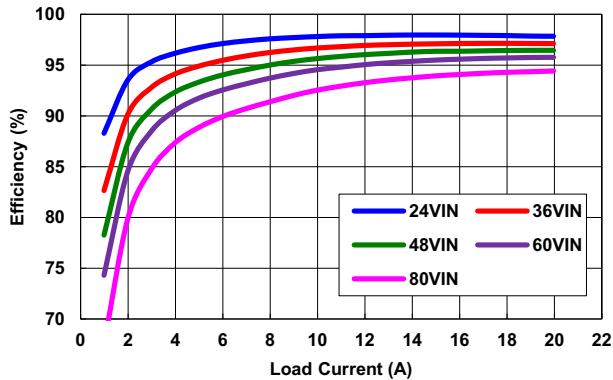


Figure 16. Efficiency, CCM

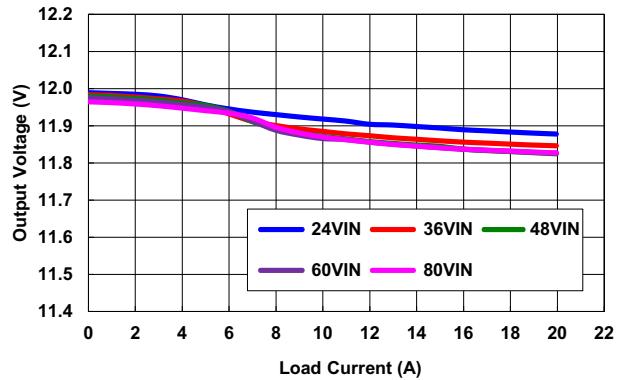


Figure 17. Load Regulation, CCM

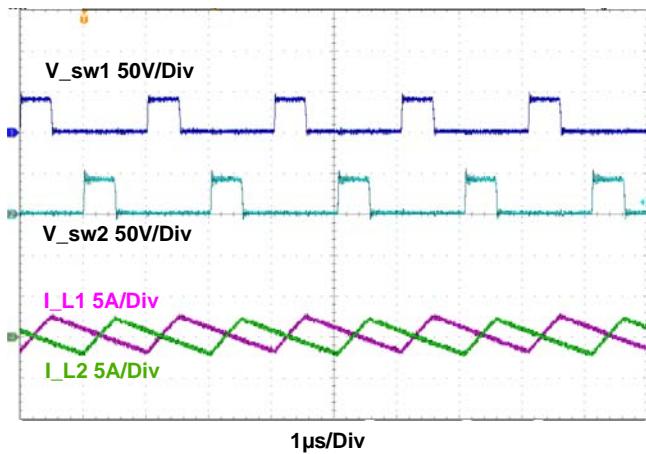


Figure 18. Dual-Phase Waveforms,
 $V_{IN} = 48V$, $I_{OUT} = 0A$, CCM Mode

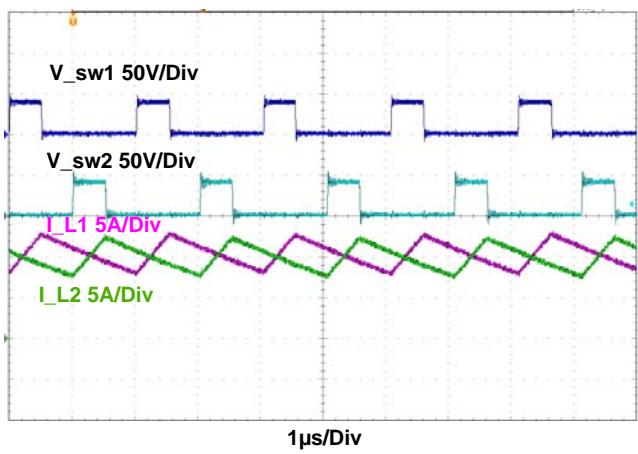


Figure 19. Dual-Phase Waveforms,
 $V_{IN} = 48V$, $I_{OUT} = 20A$, CCM Mode

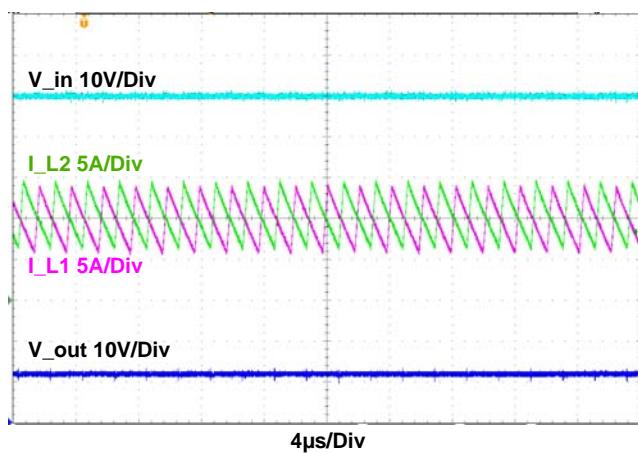


Figure 20. $V_{IN} = 80V$, $V_{OUT} = 12V$, $I_{OUT} = 20A$

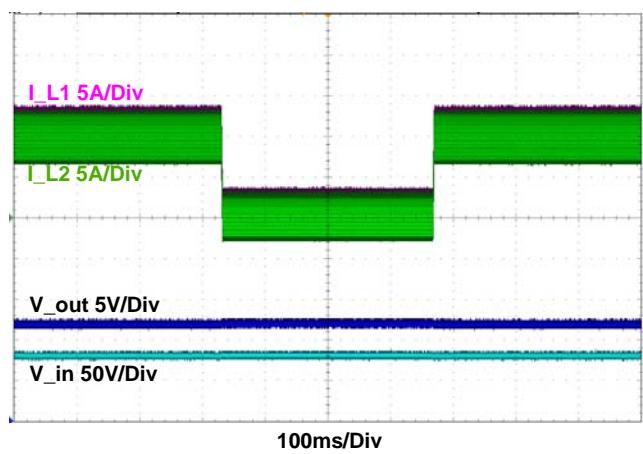


Figure 21. Load Transient, $V_{IN} = 80V$, $I_{OUT} = 0A$ to $20A$,
CCM

$V_{IN} = 48V$, $T_A = 25^\circ C$, unless otherwise noted. (Cont.)

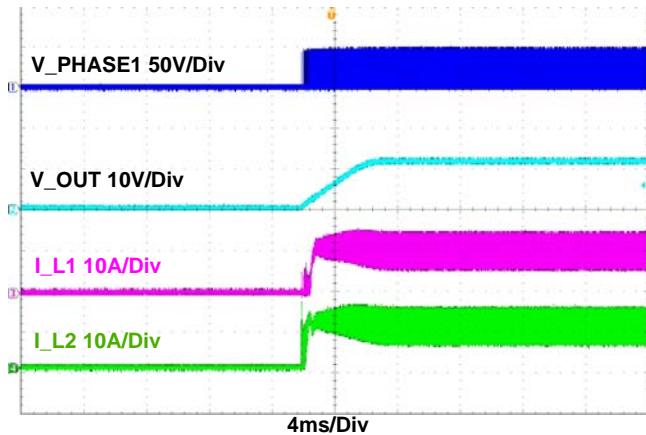


Figure 22. Start-Up $V_{IN} = 48V$, $I_{OUT} = 20A$, CCM

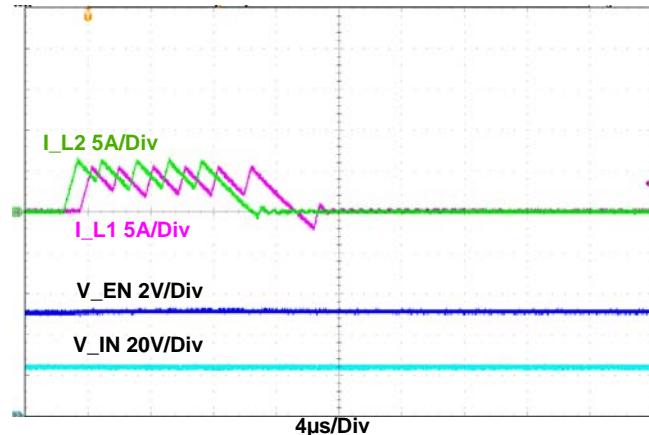


Figure 23. Burst Mode, $V_{IN} = 24V$

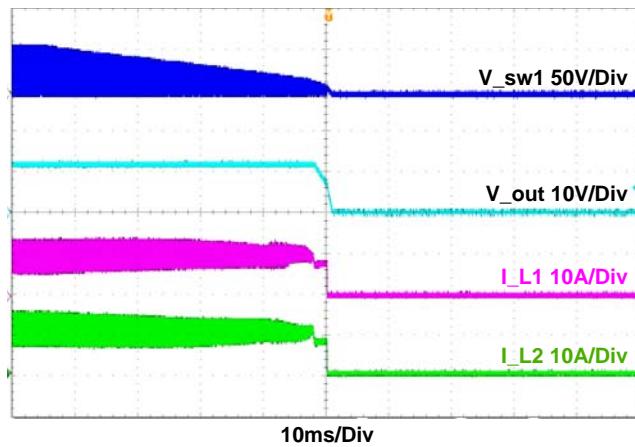


Figure 24. Shutdown Waveform, $V_{IN} = 60V$, $I_{OUT} = 20A$, CCM

5. Revision History

| Rev. | Date | Description |
|------|--------------|---|
| 1.1 | May 13, 2021 | In 1. Functional Description, corrected “ambient room” to “room ambient”. Removed OCP Set Point and added Peak Current Limit Set Point to 3.1 Design Requirements. Updated 3.3, 3.8, 3.13, 3.14. Updated 4. Typical Performance Curves: Figure 16, 17, 20, 22, and 23. |
| 1.0 | Feb 10, 2021 | Initial release |

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