User Manual

DA1453x Pro-Development Kit Hardware Description

UM-B-169

Abstract

Renesas DA1453x Pro-development kit supports the family of DA1453x SoC. This user manual describes the system functions of the hardware as well as the guidelines of how to enable or disable features of the DA1453x Pro-development kit.

DA1453x Pro-Development Kit Hardware Description

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1 Terms and Definitions

UART	Universal Asynchronous Receiver Transmitter
GPIO	General Purpose Input Output (pin)
JTAG	Joint Test Action Group
RF	Radio Frequency
IC	Integrated Circuit
NP	Not Populated
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembled
SoC	System on Chip
SWD	Serial Wire Debug
DK	Development Kit
Pro-DB	Pro Daughterboard
Pro-MB	Pro Motherboard
OTP	One-Time Programmable Memory
POR	Power-On Reset

2 References

[1] DA14531 Datasheet, Renesas.

[2] DA14535 Datasheet, Renesas.

[3] UM-B-083, SmartSnippets Toolbox User Manual, User Manual, Renesas.

[4] AN-B-075, DA14531 Hardware Guidelines, Application Note, Renesas.

[5] AN-B-098, DA14535 Hardware Guidelines, Application Note, Renesas

[6] UM-B-114, DA14531 Devkit Pro Hardware, User Manual, Renesas.

Note 1 References are for the latest published version, unless otherwise indicated.

3 Introduction

This document describes the hardware of DA1453x Pro-Development Kit (Pro-Devkit). The DA1453x Pro-Devkit is available as a set of a Pro motherboard, a Pro daughterboard with four variants (according to IC type and/or package), and the power measurement module PMM2. The complete system is shown in Figure 1.

The DA1453x Pro-Devkit, when combined with the Software Development Kit (SDK) and Smart Snippets tools, provides an easy to use and complete platform for software/hardware development.

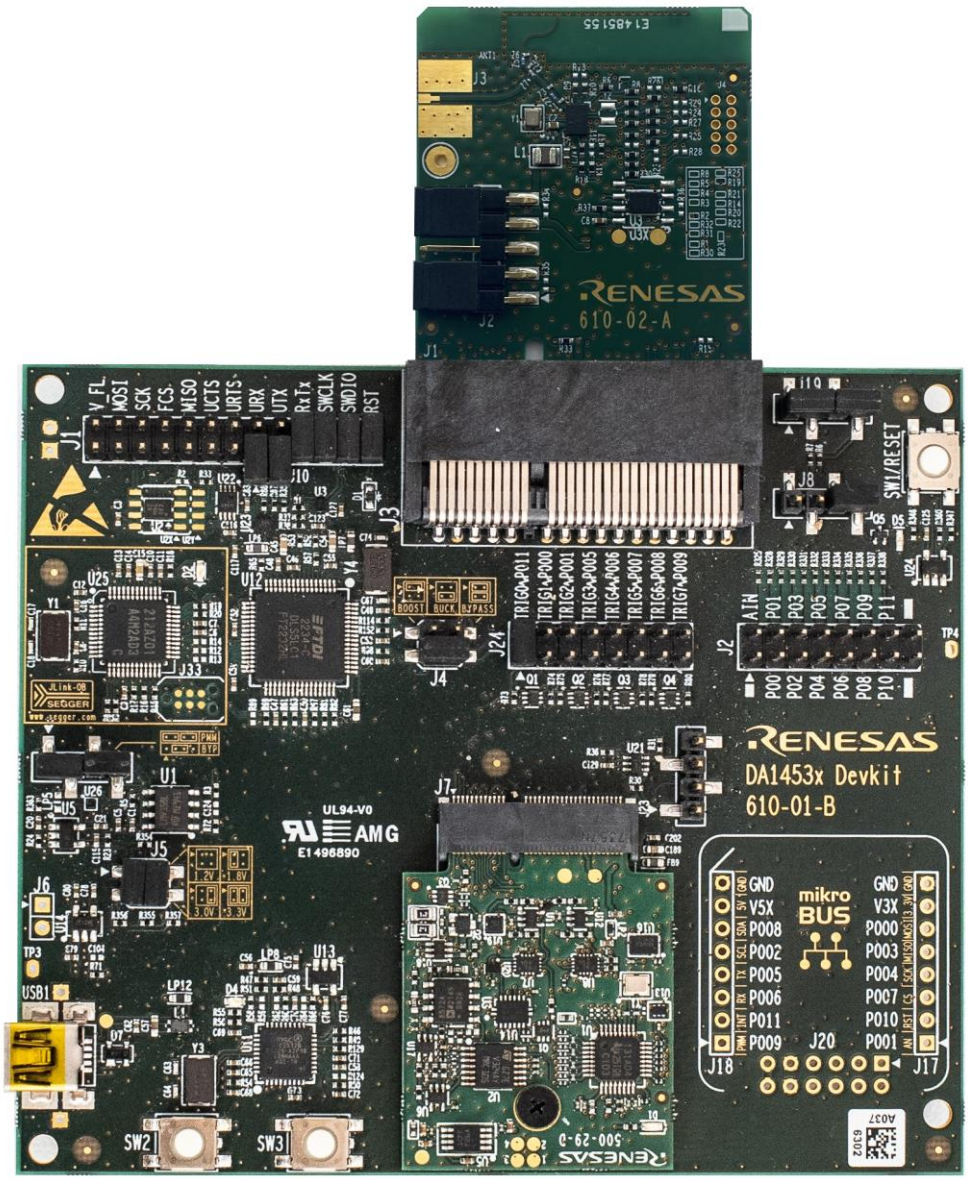

Figure 1. The DA1453x Pro-Devkit

The following sections describe the system setup, the different available configuration options, as well as the tools provided to debug, develop, and evaluate the system performance.

3.1 Features of DA1453x Pro-DB

- Embedded printed antenna.
- RF port output (connector not included)

- Current measurement port to connect external measurement equipment.
- Onboard place holder of a 2-Mbit SPI data Flash for DA14531, DA14533 and DA14535
- Onboard JTAG connector
- Support for coin cell battery (battery holder not included).

3.2 Features of DA1453x Pro-MB

- A slot to connect a DA1453x Pro-DB which hosts one of the:
  - DA14531-FCGQFN24
  - DA14531-WLCSP17
  - DA14533- FCQFN22
  - DA14535-FCGQFN24
- A slot for attaching a power measurement module (PMM2)
- Single USB port to provide power and data interfacing to a PC (USB1)
- Onboard JTAG debugger
- Virtual 4-wire UART port
- Onboard 2-Mbit SPI data Flash AT25DF021A-MAHN-T
- Multiple voltage options (1.25 V, 1.8 V, 3.0 V, and 3.3V) to supply the DA1453x DBs
- User LEDs and push buttons (to be used with a DA14531/5 FCGQFN24 PRO-DB)
- Voltage translation for the JTAG and UART signals eliminates current leakage during operation.

3.3 DA1453x Pro-Devkit hardware block diagram

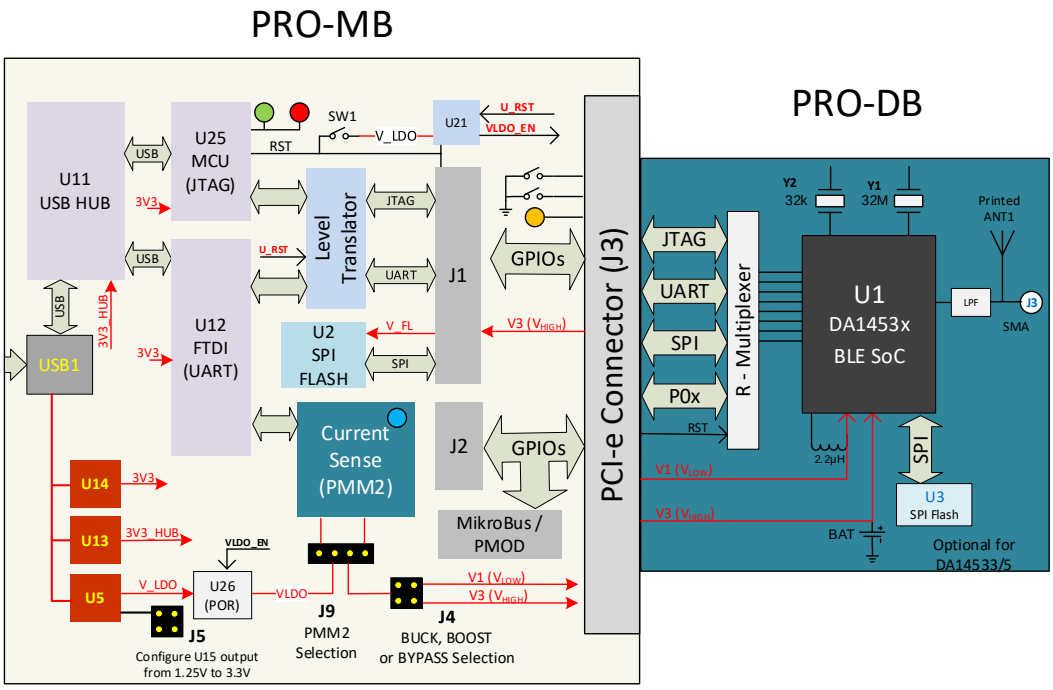

Figure 2. Block diagram of the Pro DA1453x Dev-Kit Platform

4 Getting to Know DA1453x Pro-Devkit

4.1 DA1453x Pro-Devkit hardware components

The DA1453x Pro-Development kit consists of the following parts:

Pro-MB

- PCBA reference number 610-01-B

Pro-DB with following variants

- FCGQFN24 Pro-DB: SoC DA14531-FCGQFN24. PCBA reference number 376-04-F
- WLCSP17 Pro-DB: SoC DA14531-WLCSP17. PCBA reference number 376-05-E
- FCQFN22 Pro-DB: SoC DA14533-FCQFN22. PCBA reference number 610-05-A
- FCGQFN24 Pro-DB: SoC DA14535-FCGQFN24. PCBA reference number 610-02-A

PMM2

- Power measurement module, PMM2. PCBA reference number 500-29-E

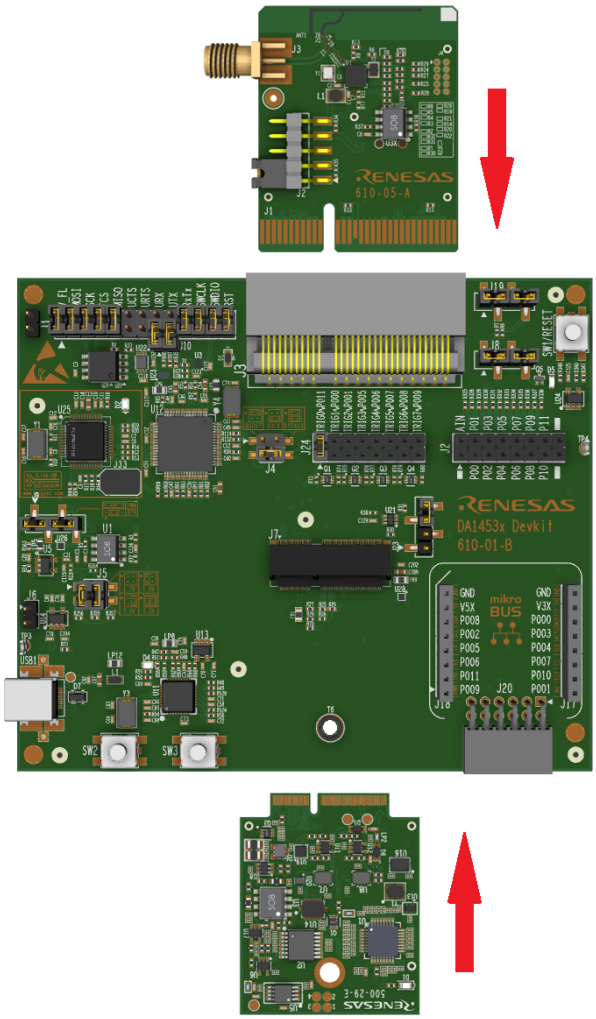

Figure 3. DA1453x complete system of Pro-MB, Pro-DB and PMM2

Table 1. Pro-Dev-Kit part numbers and description

Part number	Description
DA14531-00OGDB-P	DA14531 WLCSP17 Pro-DB. Bluetooth Low Energy DA14531 WLCSP17 Pro-daughterboard
DA14531-00FXDB-P	DA14531 FCGQFN24 Pro-DB Bluetooth Low Energy DA14531 FCGQFN24 Pro-daughterboard
DA14533 Pro-DB	DA14533, FCQFN22 Pro-DB Bluetooth Low Energy DA14533 FCQFN22 Pro-daughterboard
DA14535-00FXDB-P	DA14535, FCGQFN24 Pro-DB Bluetooth Low Energy DA14535 FCGQFN24 Pro-daughterboard
DA1453x Pro-MB	DA1453x Bluetooth Low Energy Development Pro-MB
DA14535-00FXDEVKT-P	DA14535 DK-Pro Bluetooth Low Energy Development Kit Pro for DA1453x, including Pro-MB and Pro-DB.

4.2 Jumper settings

Table 2. Headers and jumper settings of DA1453x Pro-Daughterboard

HDR	Function of headers	Jumper Options		Default Jumper setting
J1	Supply DA1453x SoC	Supply VBAT_Hi	J2:1-2	Mounted 1-2
		Supply VBAT_Lo	J2:4-5	Mounted 4-5

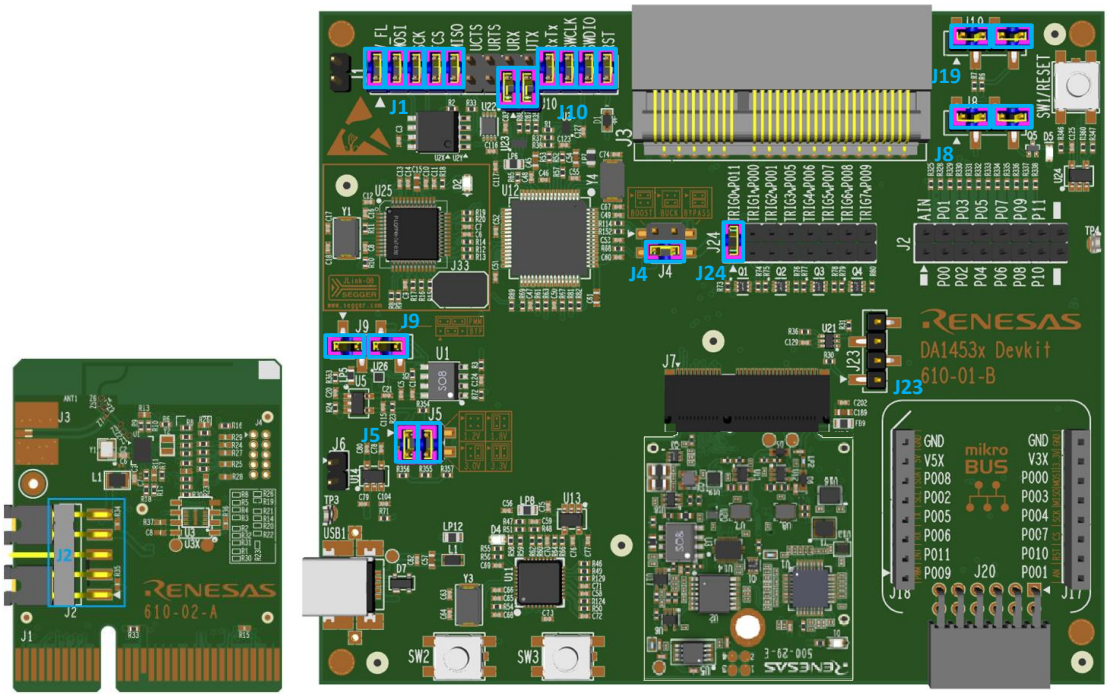

Figure 4. Default jumper settings for DA1453x Pro-Devkit

Table 3. Headers and jumper settings of DA1453x Pro-Motherboard

HDR	Function of headers	Jumper options		Default jumper setting
J1 and J10	DA1453x Pro-Devkit System setup	Enable SPI Data Flash on Pro-Motherboard	Mount pos. 1-2 Mount pos. 3-4 Mount pos. 5-6 Mount pos. 7-8 Mount pos. 9-10	SPI Flash Enabled Mounted 1-2 Mounted 3-4 Mounted 5-6 Mounted 7-8 Mounted 9-10
		Enable SWD	Mount pos. 21-22 Mount pos. 23-24	SWD Enabled Mounted 21-22 Mounted 23-24
		Enable Reset	Mount pos. 25-26	Reset Enabled Mounted 25-26
		Enable 2-UART	Mount pos. 15-16 Mount pos. 17-18	Not mounted
		Enable 4-UART	Mount pos. 11-12 Mount pos. 13-14 Mount pos. 15-16 Mount pos. 17-18	Not mounted
		Enable Single UART	Mount pos. J1.16-**J10**.1 Mount pos. J1.18-**J10**.2	Single UART Enabled Mounted J1.16 - **J10**.1 Mounted J2.18 - **J10**.2
J4	Selection of Mode DA1453x SoC power configuration	BOOST	Mount pos. 1-2	**BUCK** Mounted 3-4
		BUCK	Mount pos. 3-4	
		BYPASS	Mount pos. 1-2 Mount pos. 3-4	
J5	Voltage levels of V_{LDO} V_{LDO} generates V1 and V3	1.2 V	Mount no jumper	**3.3 V** Mounted 1-3 Mounted 2-4
		1.8V	Mount Pos. 1-3	
		3.0 V	Mount pos. 2-4	
		3.3 V	Mount pos.1-3 Mount pos. 2-4	
J6	Force Power Enable for supplying Pro-Devkit with a power source without USB data connection	Force Power_Enable	Mount pos. 1-2	Not mounted 1-2
J8	Reset sourced from R7FA4M2AD3CFL (implemented from Segger software)	Enable Reset	Mount pos. 1-2	Mounted 1-2
	LED, D5 connection to P0_9	Enable LED connection	Mount pos. 3-4	Mounted 3-4

HDR	Function of headers	Jumper options		Default jumper setting
J9	Power Measurement Module PMM2	PMM2 Bypass	Mount pos. 2-3	*PMM2 mounted* Mounted 1-2 Mounted 3-4 *PMM2 not mounted* Mounted 2-3
		PMM2 Enable	Mount pos.1-2 Mount pos. 3-4	
J19	Enable Push buttons SW2 and SW3	Enable SW2	Mount pos.1-2	Mounted 1-2
		Enable SW3	Mount pos.2-3	Mounted 3-4
J23	Reset source options	Activate Reset driven from Debugger (U_RSTn)	Mount pos.1-2	Not Mounted 1-2
		Activate POR functionality when pressing SW1 push button	Mount pos. 3-4	Not Mounted 3-4
J24	Software Trigger activation	TRIG_0 mapped to P0_11 TRIG_1 mapped to P0_0 TRIG_2 mapped to P0_1 TRIG_3 mapped to P0_5 TRIG_4 mapped to P0_6 TRIG_5 mapped to P0_7 TRIG_6 mapped to P0_8 TRIG_7 mapped to P0_9	Mount pos.1-2 Mount pos.3-4 Mount pos.5-6 Mount pos.7-8 Mount pos. 9-10 Mount pos.11-12 Mount pos.13-14 Mount pos.15-16	Mounted 1-2

4.3 DA1453x Pro-Devkit default setup

The default configuration of DA1453x Pro-Devkit is enabled by applying the appropriate jumpers to the DA1453x Pro-MB:

- Reset is enabled.
- JTAG is enabled.
- Single wire UART is enabled.
- SPI data flash (populated on Pro-MB) Dual UART or full UART are not enabled.
- Crystal 32.768 kHz is not mounted on DA1453x Pro-DB.

Table 4. DA1453x Pro-DB and Pro-MB signals assignment (default)

DA14531-FCGQFN24 376-04-x	DA14531-WLCSP17 376-05-x	DA14535-FCGQFN24 610-02-x	DA14533-FCQFN22 610-05-x	Function	Mikrobus PMOD	Trigger signals	Position on Pro-MB connector(s)
P0_0	P0_0	P0_0	P0_0	RST/MOSI	X_MOSI,	TRIG_1	J1:4, J1:12, J1:26, J2:3, J24:4
P0_1	P0_1	P0_1	P0_1	FCS	X_AN	TRIG_2	J1:8, J2:4, J24:6
P0_2	P0_2	P0_2	P0_2	SW_CLK	X_SCL,		J1:22, J2:5
P0_3	P0_3	P0_3	P0_3	MISO (Note 1)	X_MISO		J1:10, J2:6
P0_4	P0_4	P0_4	P0_4	SCK	X_CLK		J1:6, J2:7
P0_5	P0_5	P0_5	P0_5	RxTx (Note 2)	X_TX	TRIG_3	J1:20, J2:8, J24:8
P0_6		P0_6		P0_6	X_RX	TRIG_4	J2:9, J24:10
P0_7		P0_7	P0_7	P0_7	X_CSn	TRIG_5	J2:10, J24:12
P0_8		P0_8	P0_8	P0_8	X_SDA	TRIG_6	J2:11, J24:14
P0_9		P0_9		P0_9	X_PWM	TRIG_7	J2:12, J24:16
P0_10		P0_10	P0_10	SW_DIO/ SW3-Button	X_RSTn		J1:24, J2:13, J19:3,
P0_11		P0_11		SW2-Button	X_INT	TRIG_0	J2:14, J19:1, J24:2

Note 1 For DA14531-WLCSP17 (376-05-x), P0_3 is assigned as RxTx.

Note 2 For DA14531-WLCSP17(376-05-x), P0_5 is assigned as SW_DIO.

5 DA1453x Pro-DB

The system on DA1453x Pro-DB consists of the DA1453x SoC, XTALs, power section, and radio section. The system block diagram is presented in Figure 5 and the actual component's location in Figure 6 for DA14531 and DA14535 and Figure 7 for the DA14533.

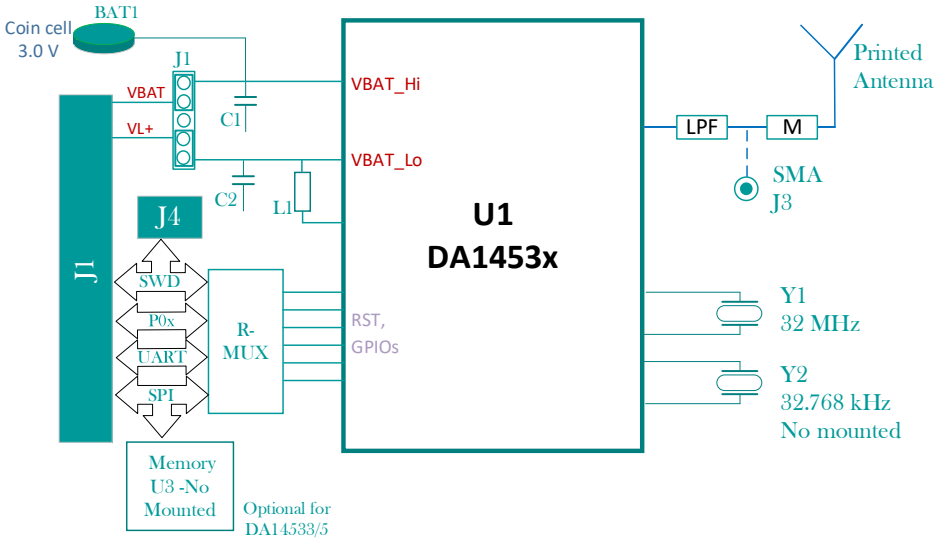

Figure 5. System block diagram of DA1453x Pro-DB

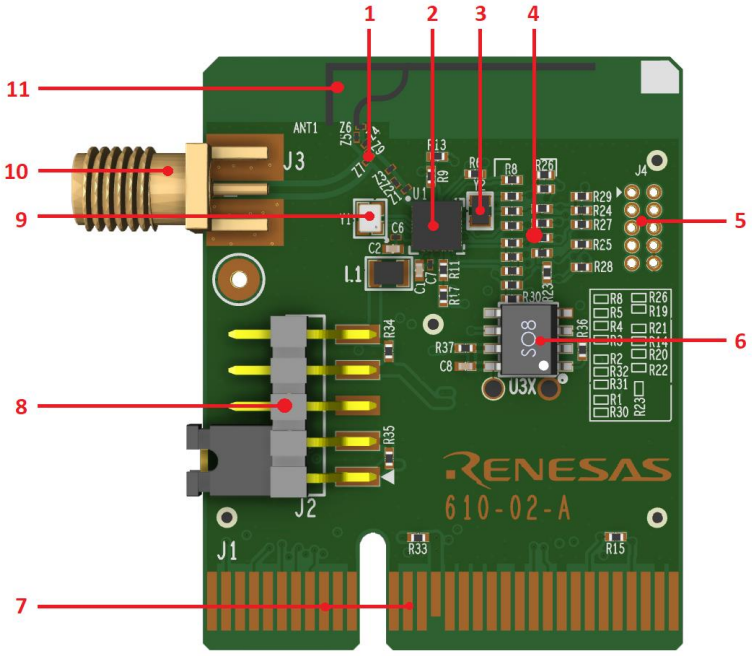

Figure 6. DA14531 and DA14535 Component's placement

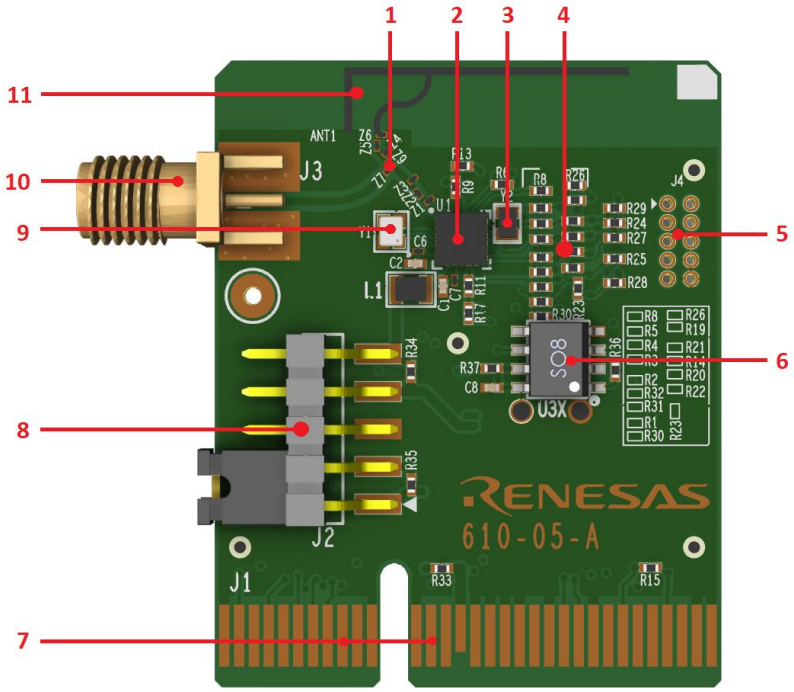

Figure 7. DA14533 Component's placement

Components:

1. Antenna selection network
2. DA1453x SoC (U1)
3. 32.768 kHz XTAL (Y2 - Not mounted)
4. R-Multiplexer
5. Debug Connector
6. SPI Flash (Not mounted for DA14531 & DA14535)
7. Interface Connector with DA1453x Pro-MB
8. Current Measurement Points
9. 32 MHz XTAL (Y1)
10. SMA Connector (Not mounted)
11. Embedded Printed Antenna

- **BLE SoC (U1)**: DA1453x is an ultra-low power SoC integrating a 2.4 GHz transceiver and an ARM CortexM0+TM microcontroller with 64 kB of RAM and 12 kB of One-Time Programmable memory (OTP).
- **32 MHz XTAL (Y1)**: The main clock of the system is generated from a 32 MHz XTAL which is connected to th**e internal clock oscillator. The selected crystal for DA14535 is the XRCGB32M000F1SBAR0** of Murata, whereas for DA14533 the XRCGE32M000FBA2FR0 of Murata is used.
- **32.768 kHz XTAL (Y2, NP)**: A crystal of 32.768 kHz can be placed on the pins P0_3 and P0_4 of DA1453x. A crystal that can be used is the ECS-.327-7-12QS-TRfrom ECS. In most applications the DA1453x can run with good accuracy with its internal RC oscillator (RCX) and therefore the XTAL32k is not needed. For applications with more demanding accuracy/drift characteristics, such as timekeeping, using the XTAL32k is considered a suitable solution.

  By default, XTAL32k is not assembled on Pro-DB. Internal RC clock is used. P0_3 and P0_4 pins are assigned to other SPI data flash (mounted on Pro-MB).

- **RF section:** see section 5.2.
- **R-Multiplexer:** a group of 0 Ω configuration resistors can be placed/removed as needed to hardwire various peripherals to the DA1453x pins as desired. See section 5.3.
- **SPI Flash:** see section 5.4.

5.1 Power section of Pro-DB

The DA1453x Pro-DB can operate in the Buck mode (supplied VBAT_HIGH with 1.8 V to 3.6 V) or in the Boost mode (supplied VBAT_LOW with 1.2 V to 1.65 V). The available voltage levels provided by DA1453x Pro-MB are:

- 1.25 V
- 1.8 V
- 3 V
- 3.3 V

A jumper must be applied between pins 1 and 2 on header J2. This jumper shorts the VH+ and VH- for the VBAT_Hi pin of the DA1453x SoC.

For the Boost mode, the jumper must be applied between pins 3 and 4 on header J2. This jumper short VL+ and VL- for the VBAT_Lo pin of the DA1453x SoC.

Both jumpers should be mounted.

For any other voltage level, the DA1453x Pro-DB must be supplied from external power supply.

Right angle J2 header can be used to connect external ammeter and measure the power consumption of the DA1453x Pro-DB, or to externally power supply the Pro-DB when in stand-alone (not mounted on a DA1453x Pro-MB).

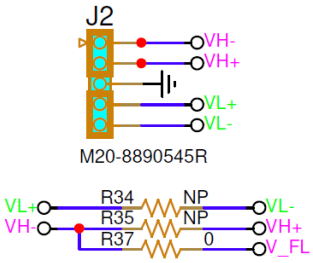

Figure 8. Current measurement connector, J2

Current measurement for:

- Buck mode: connect ammeter at J2 pin 1-2
- Boost mode: connect ammeter at J2 pin 4-5.

Power supplied externally (for example, Benchtop power supply) for:

- Buck mode: connect GND to J2 pin 3 and power supply voltage from 1.8 V to 3.6 V at pin 1.
- Boost mode: connect GND to J2 pin 3 and power supply voltage from 1.25 V to 1.65 V at pin 5.

5.2 RF section

A printed F-antenna (ANT1) is used as the radiating element for the DA1453x Pro-DB.

The DA1453x RFIO pin is connected to the printed antenna through an RF strip-line and a matching circuit.

To perform conducted RF measurements, proceed with the following hardware modifications (Figure 10):

1. Remove Z9
2. Assemble Z7 = 10 pF
3. Assemble J3, SMA Female Socket 50 Ω Board Edge (142-0761-861) of Cinch Connectivity Solutions Johnson).

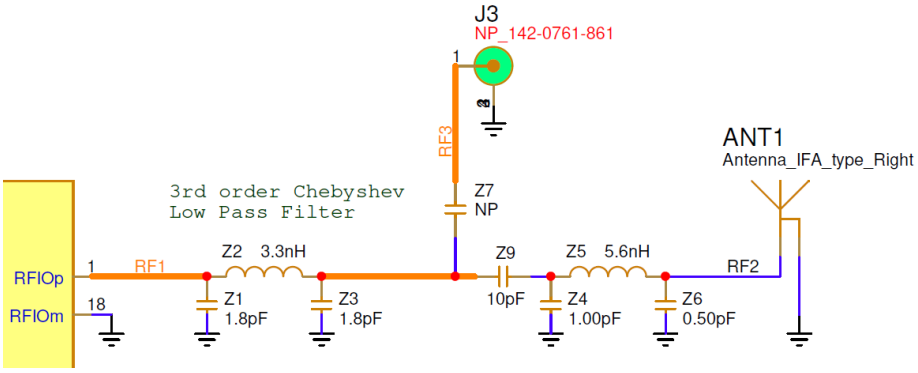

Figure 9. RF section of DA1453x Pro-DB

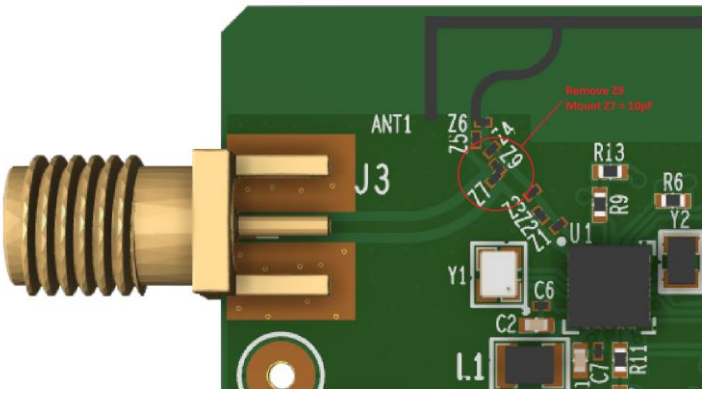

Figure 10. Modifications required for performing RF measurements

5.3 R-Multiplexer

Different combinations of GPIOs assignment can be selected through the R-multiplexer. The default setup is shown in Figure 11. Depending the setup of the R-Multiplexer on the DA1453x Pro-DB, modifications on software may also require.

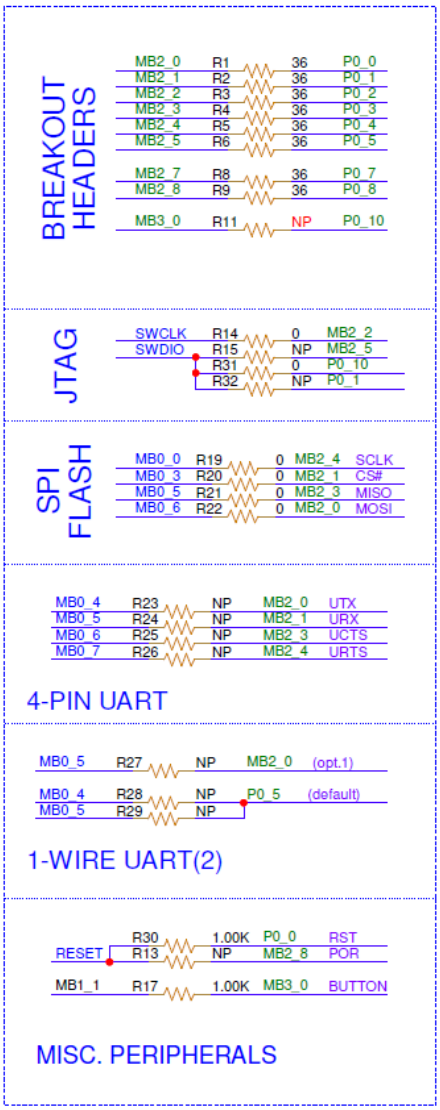

Figure 11. R-Multiplexer default setup

5.4 SPI Data flash on Pro-DB

The DA14533 Pro-DB (610-05-x) and the DA14535 Pro-DB (610-02-x) have the option to support SPI flash (U3 or U3x) as shown in Figure 12. The proposed part is the AT25DF021A-MAHN-T for the DA14535 Pro-DB and the Winbond W25X20CV for the DA14533 Pro-DB (610-05-x). By default, the SPI Flash is not mounted on the Pro-DB.

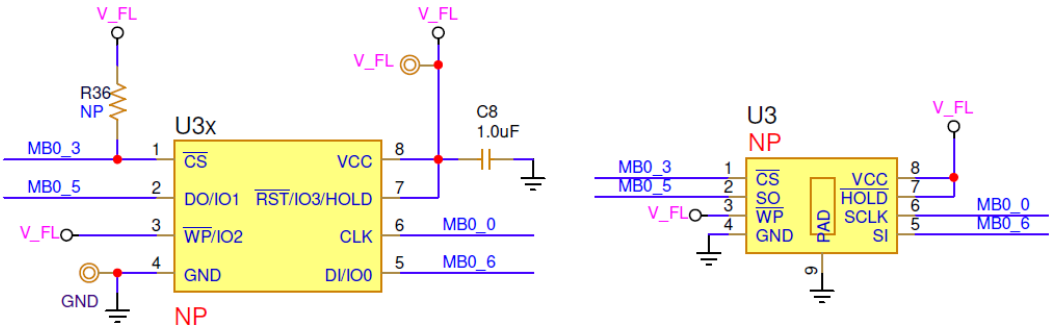

Figure 12. Optional SPI-Flash on the DA14533, DA14535 Pro-DB

NOTE
If memory is mounted on Pro-DB, you must ensure that resistor R19 to R22 (see Figure 11) are mounted and the jumpers on J1 header on Pro-MB (Jumpers at positions 1-2, 3-4, 5-6, 7-8 and 9-10) are removed.

6 DA1453x Pro-MB

The block diagram and the actual component locations of the Pro-MB are shown in Figure 13 and Figure 14, respectively.

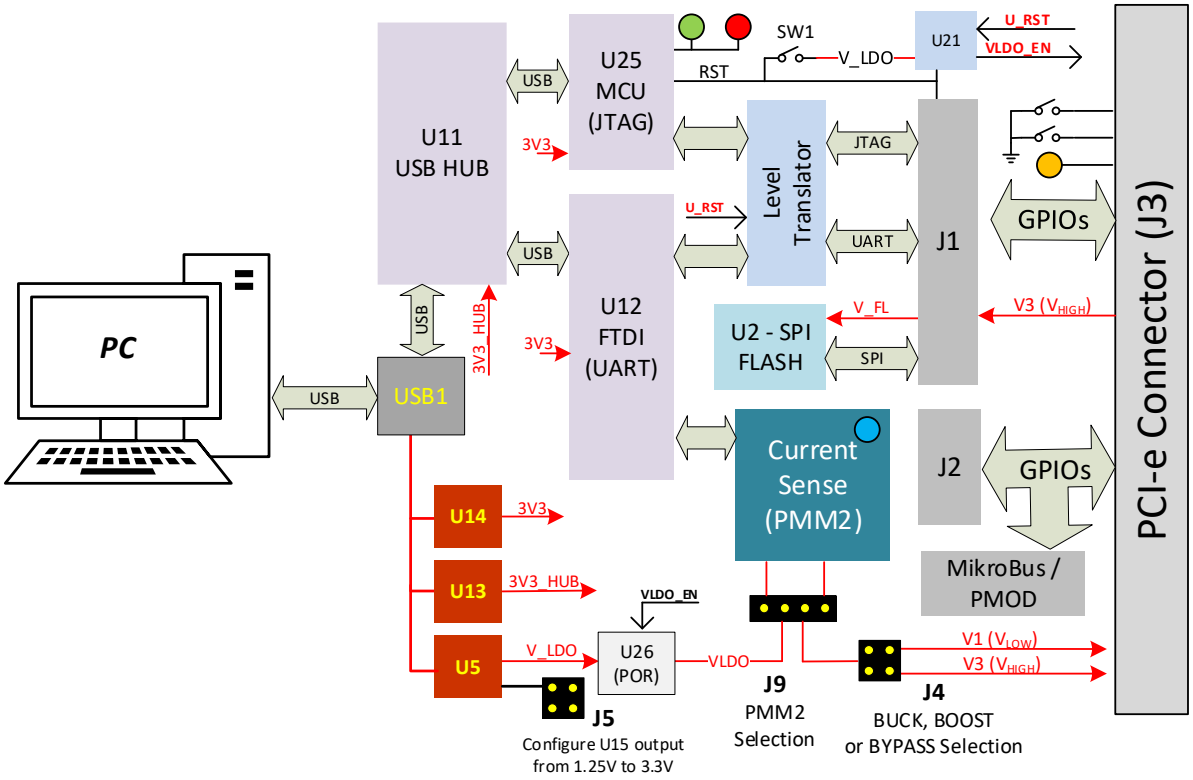

Figure 13. DA1453x Pro-MB block diagram

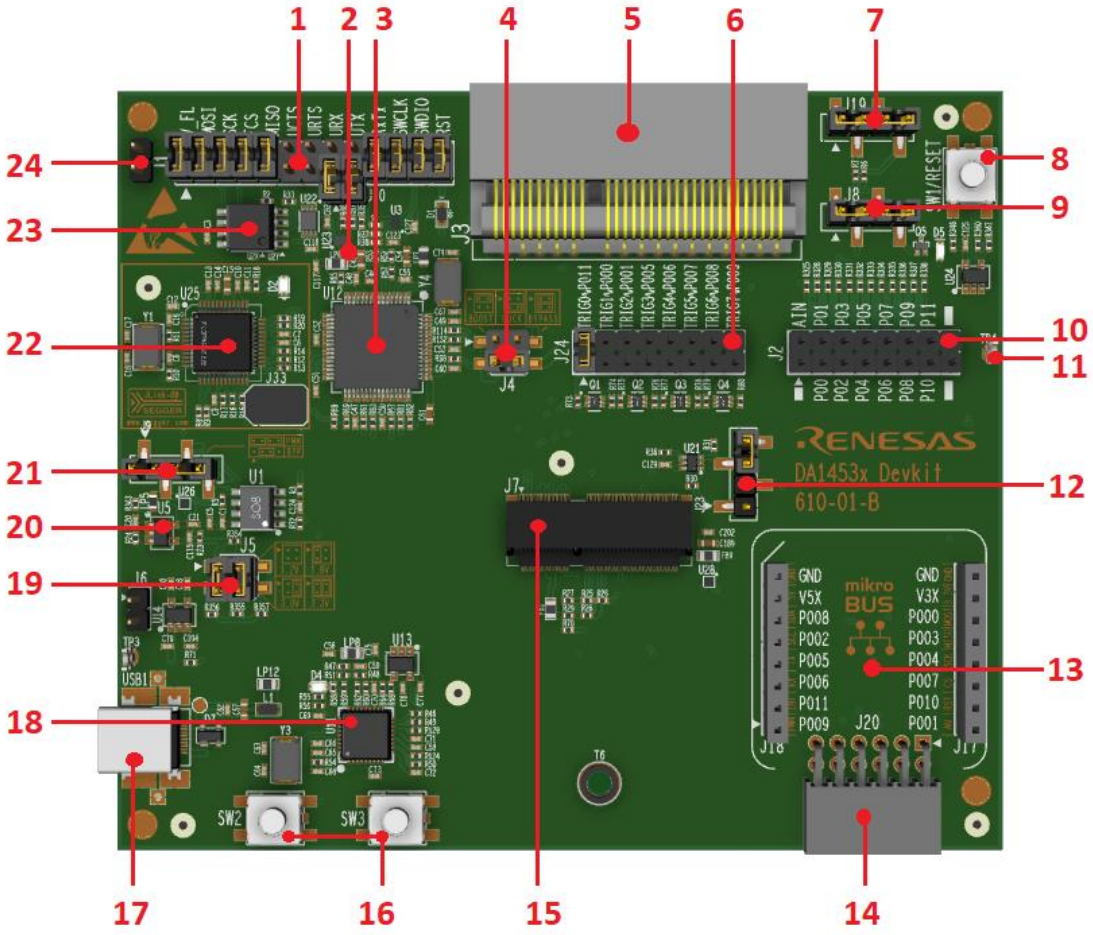

Figure 14. Pro-MB (610-01-A)

- **Configuration header (J1)**: wiring of the available peripherals to the DA1453x pins is done with the help of jumpers on J1 (for default configurations) or with jumper wires from J1 to J2 when custom pin assignments of the peripherals to DA1453x pins are desired.
  - **RxTx single wire UART (J10)**: generates RxTx single wire UART by shorting UTX and URX through a 1 KΩ resistor. Jumpers must be applied from J10.1 to J1.15 and from J10.2 to J15.17.
- **Voltage translators (U3, U22, U23):** transfer the data between DA1453x and FTDI (U12)/JTAG (U25) in proper voltage level.
- **USB to UART (U12)**: provides communication between DA1453x UART port and PC. It also transfers the current measurement samples to PC.
- **DCDC configuration (J4)**: selects either Boost, Buck, or Bypass mode for DA1453x. See Section 6.1.4.
- **Pro-DB mating header (J3)**: an interface mating connector for the DA1453x Pro-DB.
- **Software trigger options (J24):** configures the pin assignment for trigger through SmartSnippets Toolbox software application (when PPM2 is mounted).
- **Push button selection header (J19)**: configures the assignment of onboard push buttons to certain DA1453x pins.
- **Reset push button (SW1)**: push button used to reset DA1453x.
  - **P0**_0 must be configured as RST pin to generate reset from push button SW1.

- **User LED and C-Trig (J8)**: enables use of the onboard LED (D5) and the software cursor.
- **GPIO monitoring header (J2)**: exposes all the pins of the Pro-DB to allow wiring for custom configurations as well as monitoring of the hardware signals.
- **GND test point (TP4):** can be used as GND point for external instruments connection such as oscilloscope.
- **Reset options (J23):** additional reset options (POR, software reset).
- **MikroBus interface connector (J17 and J18)**: sockets for plugging in MikroBus interface add-on boards. It is multiplexed with PMOD (to be used with DA1453x).
- **PMOD (J20)**: socket for plugging in PMOD interface add-on boards. It is multiplexed with MikroBUS (to be used with DA1453x).
- **PMM2 interface connector (J7)**: PMM2 interface male connector. Using this current measurement circuit monitors the current consumption of Pro-DB through SmartSnippets Toolbox software application.
- **Push buttons (SW2 and SW3)**: general use push buttons.
- **USB connector (USB1)**: mini-USB connector for power supply and data interfacing to the PC.
- **USB hub (U11)**: connects JTAG and UART interfaces to the PC.
- **VLDO selection (J5)**: selects the output voltage generated for the Pro-DB board (1.25 V, 1.8 V, 3.0 V, or 3.3 V).
- **Adjustable LDO (U5):** provides power to DA1453x Pro-DB. Adjustable.
- **PMM2 selection (J26)**: enables the current sense circuit (default PMM2 is not mounted). Also, it allows the simultaneous connection of an external current measurement instrument to measure and profile the current consumption of D1453x.
- **USB to JTAG (U4)**: provides communication between DA1453x JTAG and PC.
- **SPI Flash (U2):** on-board SPI Flash (AT25DF021A-MAHN-T) connected with DA1453x through J1 configuration header.
- **GND Test Point (J21):** can be used as GND point for external instruments connection such as oscilloscope.

6.1 Power section

The power tree of the DA1453x Pro-MB is shown in Figure 15.

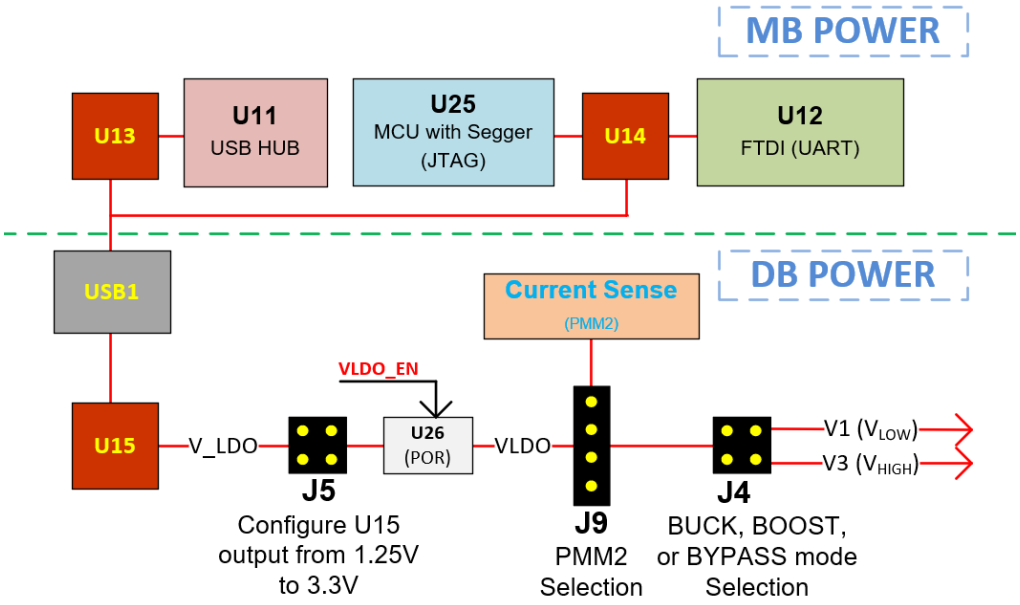

Figure 15. DA1453x Pro-MB power tree block diagram

The power tree of the DA1453x Pro-MB, as shown in Figure 15, consist of two routes, one is used to power supply he components of the DA1453x Pro-MB and the other is used to power supply the DA1453x Pro-DB and its components.

6.1.1 DA1453x Pro-DB power circuit

The DA1453x Pro-DB is powered from the adjustable LDO (U5). The output voltage of the U5 can be configured from the jumpers on the J5 header and provide the following voltage levels:

- 1.25 V
- 1.8 V
- 3.0 V
- 3.3 V

NOTE
Consider the DA1453x Pro-DB mode (Buck, Boost, or By-pass) before selecting the U5 output voltage. The 1.25 V used for the Boost mode, while from 1.8 V (and above) is used for Buck and By-Pass modes. The mode selection is described in Section 6.1.4.

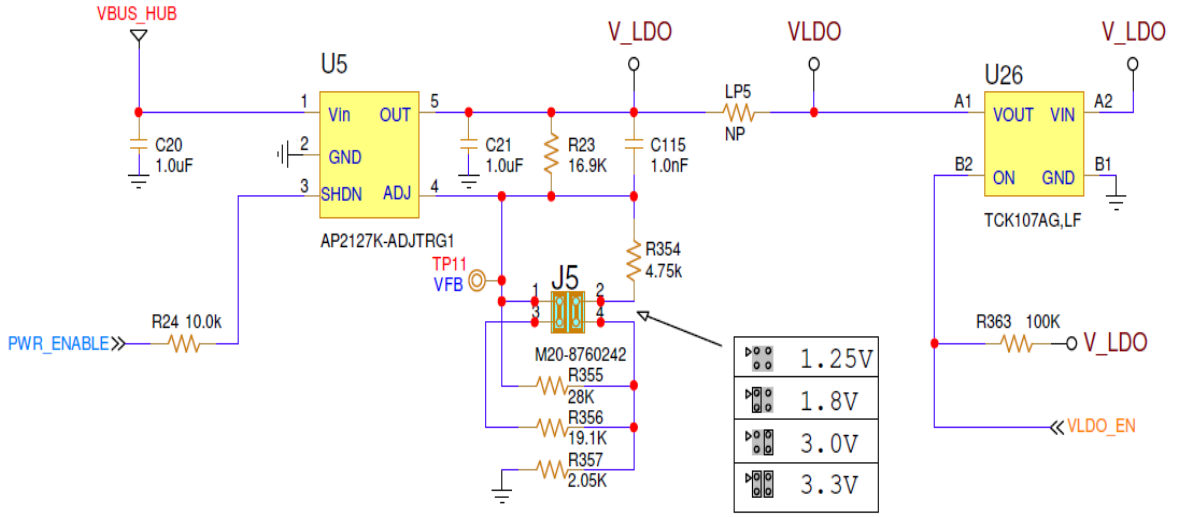

Figure 16. DA1453x Pro-DB power circuit

The configuration for the jumpers of the J5 header is presented on the top mask of the DA1453x Pro-MB as shown in the Figure 17.

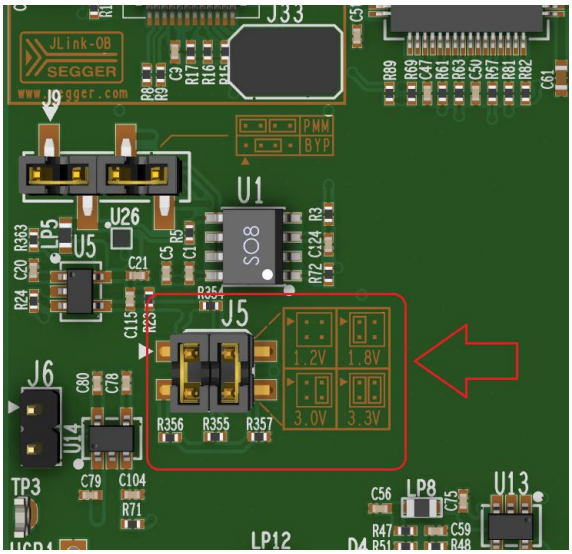

Figure 17. J5 header configuration

6.1.2 U26 (POR)

To generate the Power ON Reset function for the DA1453x Pro-DB the load switch U26 is used as shown in Figure 16. By default, the load switch is always ON and can be disabled when B2 pin is connected to GND. More details for the POR functionality, see Section 6.5.

6.1.3 PMM2

PMM2 is an external module which can be attached on the DA1453x Pro-MB. The usage of this module is to measure the current consumption of the DA1453x Pro-DB as well as to monitor signals and various power rails. The PMM2 is connected to J7, M.2 Socket and stabilized with a screw at T6 point, as shown in Figure 18 and Figure 19.

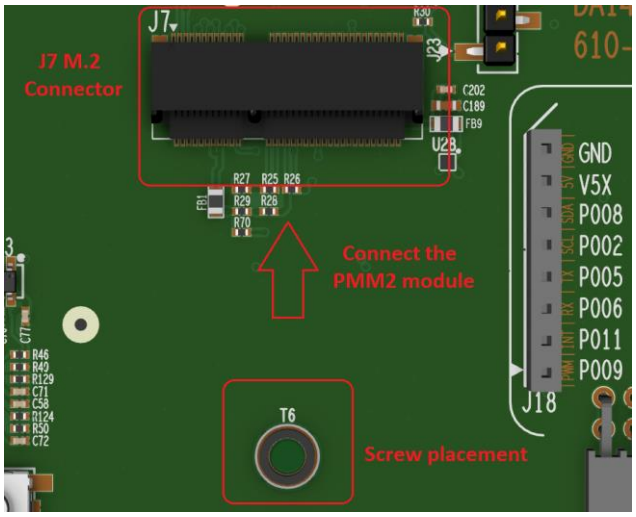

Figure 18. PMM2 slot

NOTE
SmartSnippets Toolbox software application is required for the monitoring of the voltages and the signals triggering.

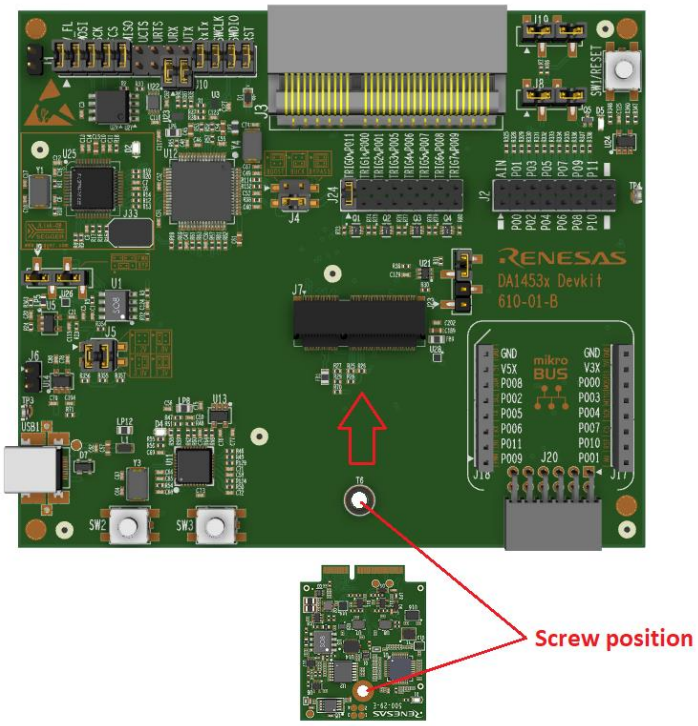

Figure 19. How to mount the PMM2 on the DA1453x Pro-MB

Even if the PPM2 is mounted on the DA1453x Pro-MB, you can either include or exclude it from the system, by configuring the jumpers on J9 header. On the top mask of the DA1453x Pro-DB is described the jumper configuration for the J9 header, as shown in Figure 20.

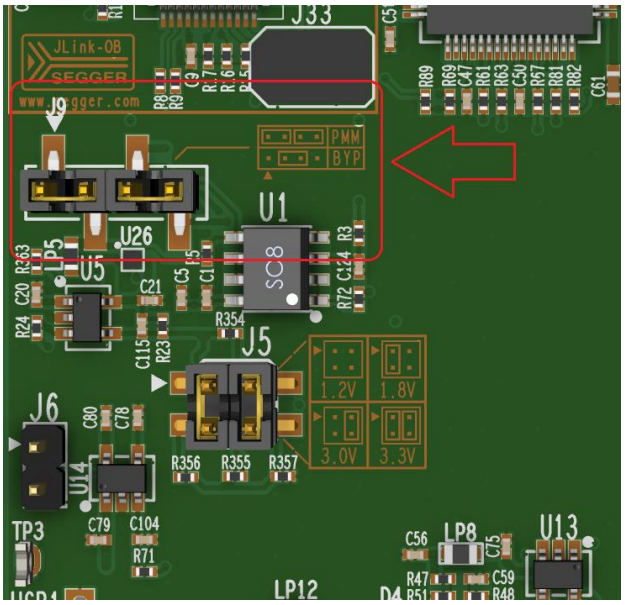

Figure 20. J9 header configuration

6.1.4 Mode selection (Buck, Boost, By-Pass)

By applying proper jumper at J4 header, you can select among buck, boost, or bypass mode of operation of the DA1453x DC-DC converter. The supply pins are:

- Jumper pin 1-2 → Boost mode, V1 is connector to VBAT_LOW
- Jumper pin 3-4 → Buck mode, V3 is connector to VBAT_HIGH
- Jumper pin 1-2 and pin 3-4 → Bypass mode, V3 is connector to VBAT_HIGH and V1 is connector to VBAT_LOW (DA1453x DC-DC converter is disabled).

NOTE
The Buck mode is the default selected mode.

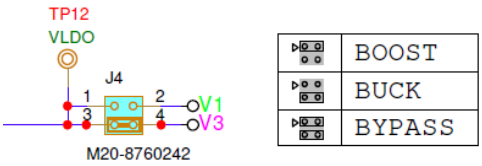

Figure 21. J4 header mode selection

On the top mask of the DA1453x Pro-MB is described the jumper configuration for the J4 header, as show in Figure 22. No modifications required on DA1453x Pro-DB.

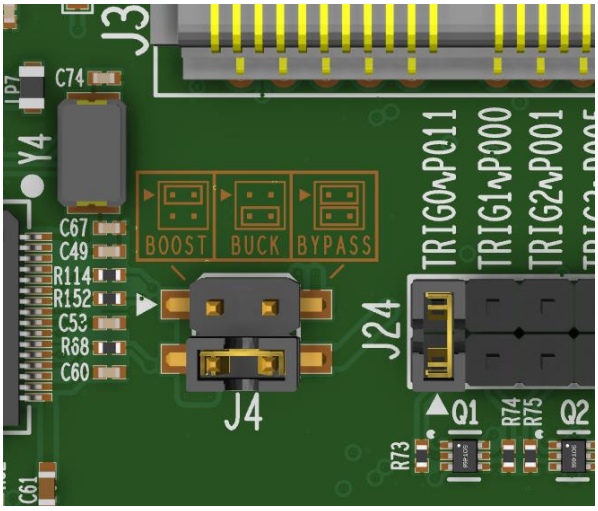

Figure 22. J4 header configuration

6.2 USB HUB

The USB HUB of DA1453x Pro-MB is implemented by U11(Figure 23), USB2512B. This chip is supplied with 3.3 V from U13 (Figure 24).

The signal PWR_ENABLE is generated from U11 and it is an active high signal. It enables the power components (LDOs and DCDC converter) for UART, JTAG, and the current sensing circuit. The system powers up only after the USB HUB is enumerated properly.

USB HUB operation is indicated through the green LED D4 on DA1453x Pro-MB. A 24 MHz crystal (Y3) is required for chip operation.

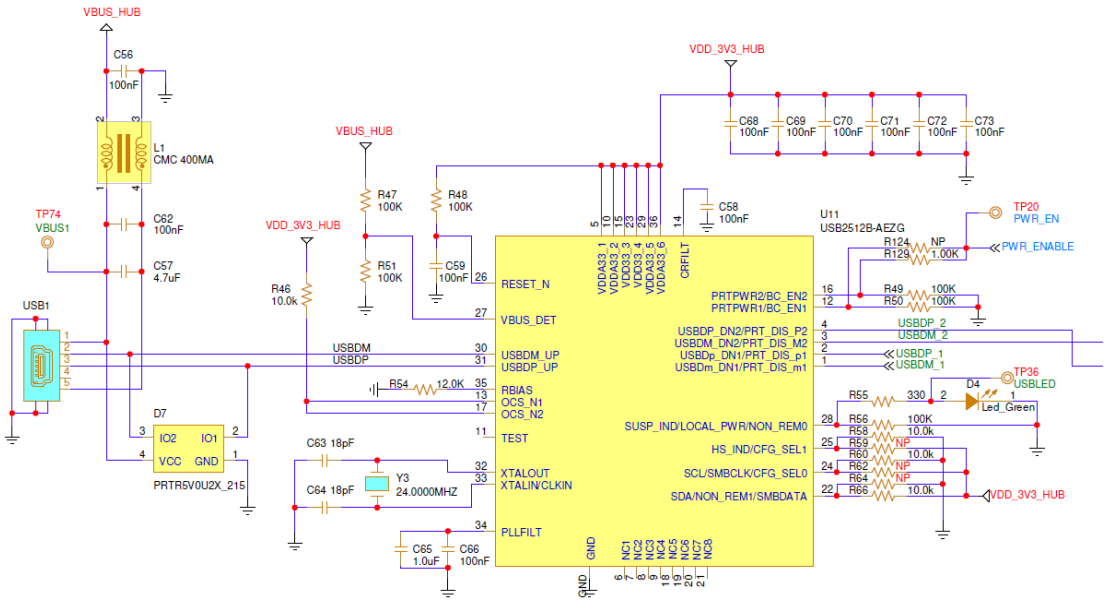

Figure 23. USB HUB circuitry

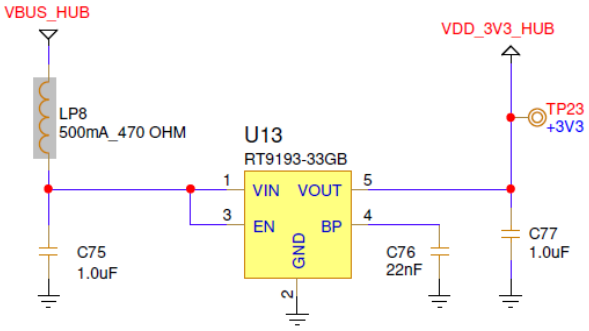

Figure 24. USB HUB power supply

6.3 USB to UART

The USB to UART function is implemented by U12, FT2232HL (Figure 25). A 12 MHz crystal (Y4) is required for the chip operation. This chip is supplied with 3.3 V from U14 (Figure 26). U14 can be enabled manually from J6 header. Not in use by default.

U12 functions are the following:

- Connecting a PC to the UART port of DA1453x SoC
- Connecting a PC to the power measurement module PMM2:
  - SPI connection with ADC (U8)
  - Up to 8 triggers including Software cursor triggering (C_TRIG)
- Reset capability of the DA1453x SoC through the T_RESET signal (not enabled).

UART signals are connected to the DA1453x SoC through voltage translators as described in Section 6.5, these can be accessed by the breakout header J2 as described in Section 6.11.

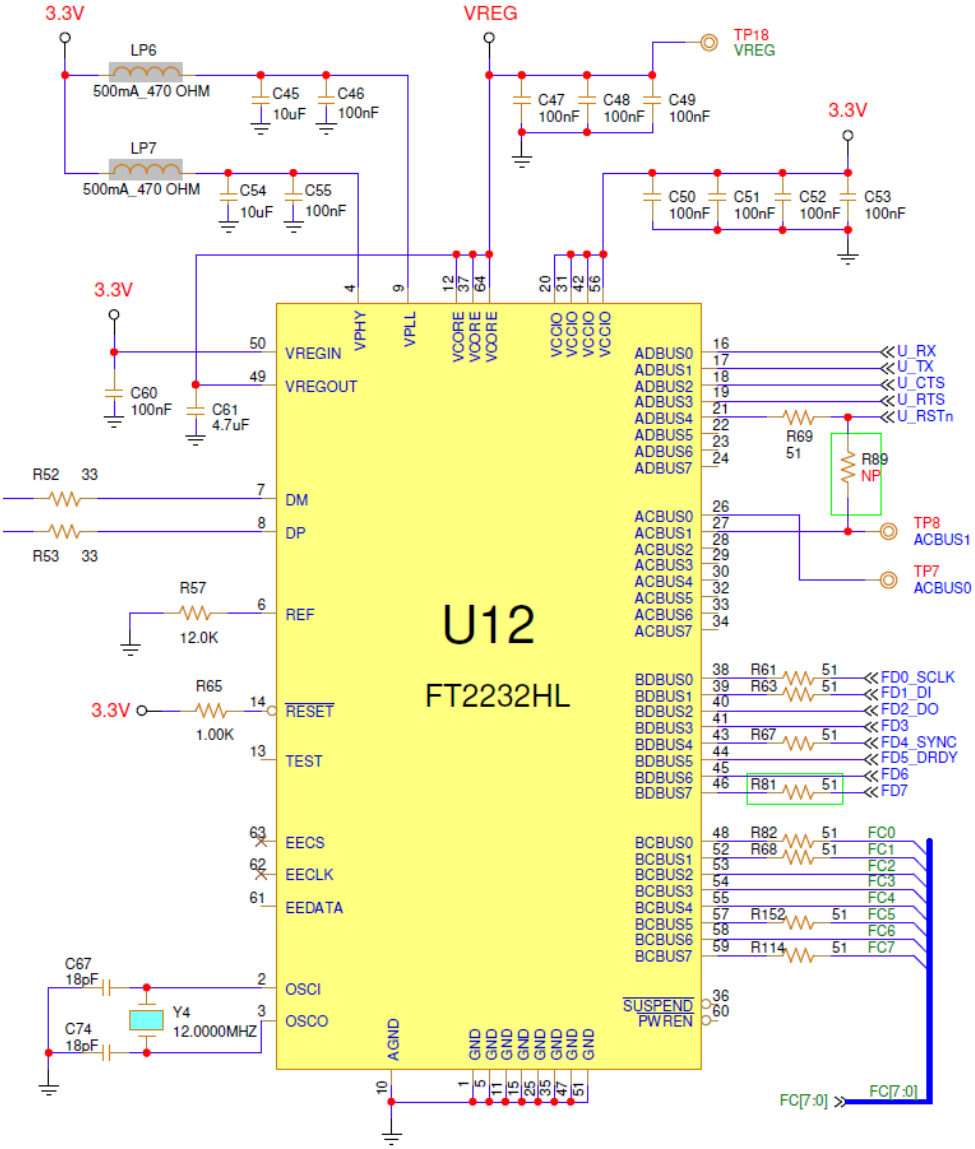

Figure 25. USB to UART circuitry

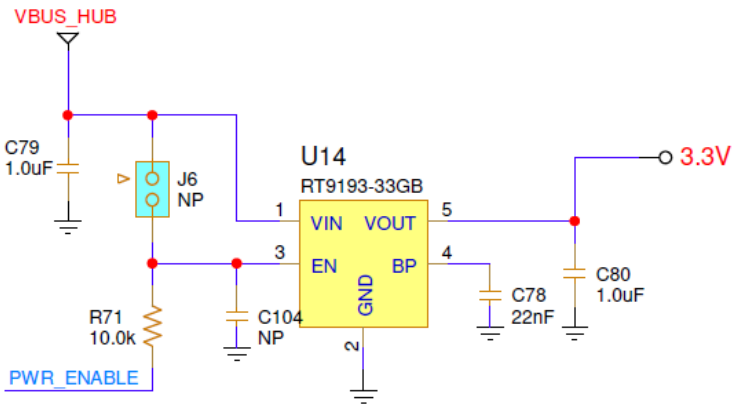

Figure 26. USB to UART power supply

6.4 USB to JTAG

The USB to JTAG function is implemented by U25, R7FA4M2AD3CFL (Figure 27). On the ROM of U4, software from SEGGER is loaded. Its operation is indicated through the green LED D2 on the DA1453x Pro-MB. This chip is supplied with 3.3 V from U14 (Figure 26). U14 can be enabled manually from J6 header. Not in use by default.

U25 functions are the following:

- Connecting a PC to the JTAG signals SWCLK, SWDIO of DA1453x SoC
- Reset capability of the DA1453x SoC through the T_RESET signal.

JTAG signals are connected to the DA1453x SoC through voltage translators as described in Section 6.6, these can be accessed by the breakout header J2 as described in Section 6.11.

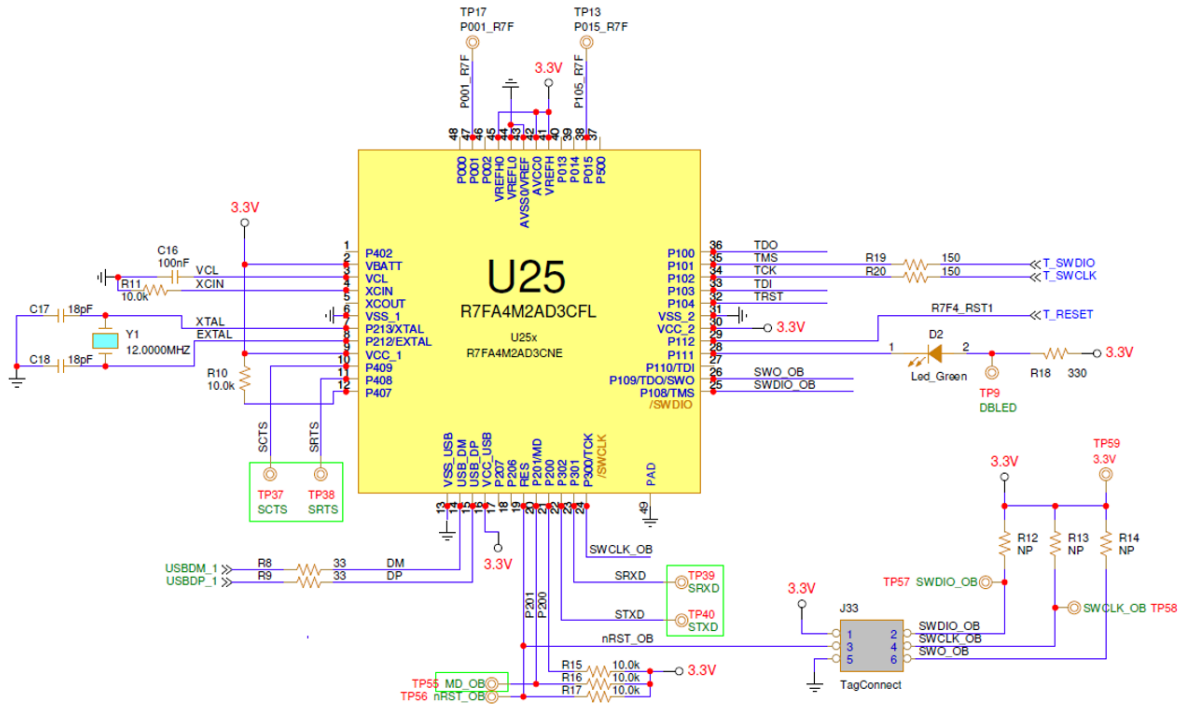

Figure 27. USB to JTAG (U25)

6.5 Reset function

At power-on and before booting in the chip, reset is active high, and it is assigned to on P0_0. After booting, reset assignment and operation is handled by software.

DA1453x Pro-DB reset signal provided by the Pro-MB is connected to P0_0 through a 1 kΩ resistor, reset can be enabled:

- By pressing the push button SW1
- From JTAG interface (T_RST)
- By the U_RSTn signal from UART – not enabled (a jumper must be placed at J23 pin 1-2 and – software required for enabling this feature.

NOTE
To enable reset on an application, P0_0 must be enabled in both hardware and software. To generate POR, a jumper must be placed at J23 pin 3-4 and press the SW1 push button.

The block diagram of the reset circuit is presented in Figure 28, the circuit schematic in Figure 29 and the actual position of the SW1 and J23 Header in Figure 30.

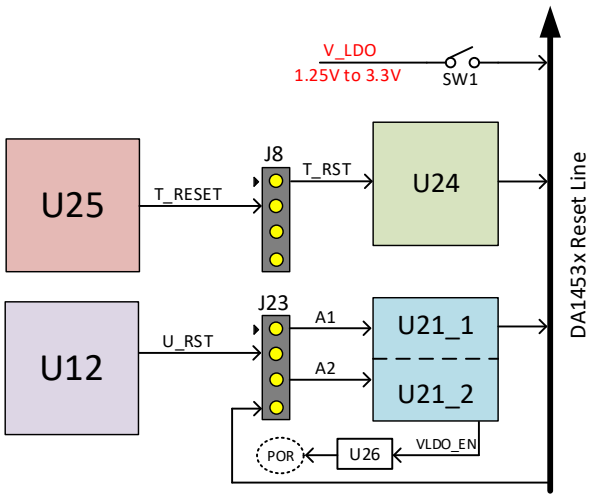

Figure 28. Reset circuit block diagram

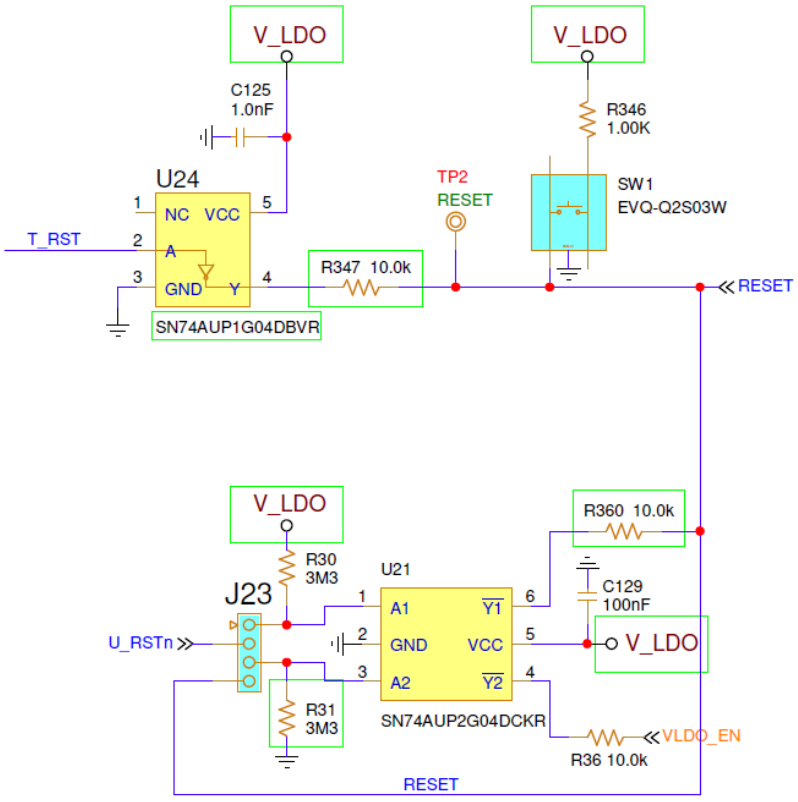

Figure 29. Reset circuit on DA1453x Pro-MB

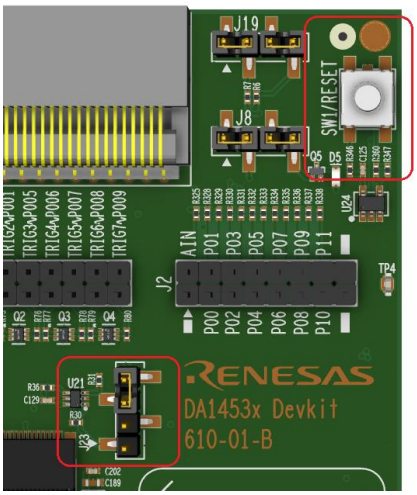

Figure 30. Position of the SW1 and J23 header on the DA1453x Pro-MB

6.6 Voltage translator

Voltage translation is applied to the UART and JTAG signals. The voltage translation is from 3.3 V to V_{DDIO} and vice versa.

The V_{DDIO} is generated from U1A, where V3 (V_{BAT_HIGH}) is used as a reference. Consequently, there is no additional power consumption on the power circuitry of DA1453x Pro-MB due to voltage translation.

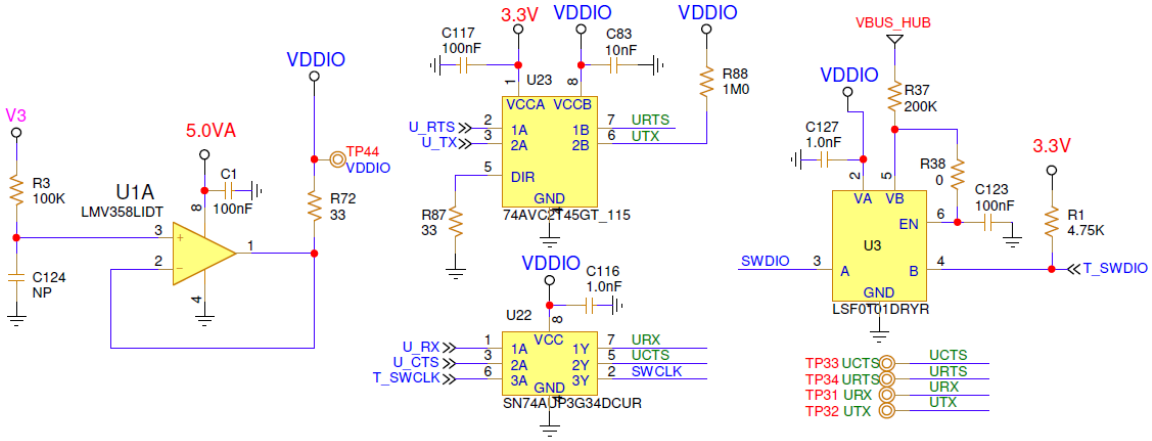

Figure 31. Voltage translator circuitry

6.7 SPI data flash

SPI data flash is enabled by default. The SPI data flash is the AT25DF021A-MAHN-T from Renesas (2 Mbit) and is located on the DA1453x Pro-MB.

Ext-SPI Slave mode is used to connect the DA1453x to SPI data flash. The SPI data flash can be isolated or connected on the system if the appropriate jumpers are removed or mounted respectively from J1 configuration header. The configuration for the SPI data flash is presented in Table 5. The circuit schematic is shown in Figure 32, The jumper configuration of the J2 header is highlighted in Figure 33 and Figure 34, and the SPI data flash position on the DA1453x Pro-MB is shown in Figure 34.

Table 5. Configuration settings for SPI data flash in DA1453x Pro-MB

SPI data flash pin	Enabled by jumpers	DA1453x Pro-DB pins	Comments
MOSI	J1 pin 3-4	P0_0	
FCS	J1 pin 7-8	P0_1	
MISO	J1 pin 9-10	P0_3	
SCK	J1 pin 5-6	P0_4	
V_FL	J1 pin 1-2	V3	Flash voltage. It is supplied with the voltage rail of the V_{BAT_HIGH}

Note 1 If the SPI data flash on the DA1453x Pro-DB is mounted and is used as primary flash, the SPI data flash from the DA1453x Pro-MB must be disconnected from the system. All the above jumpers must be removed.

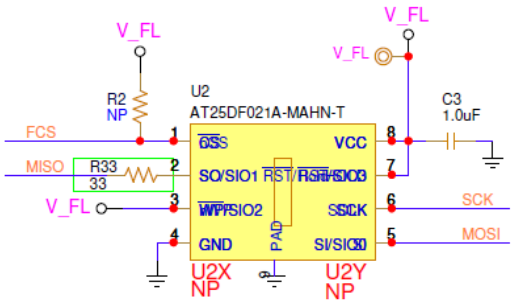

Figure 32. SPI data flash schematic

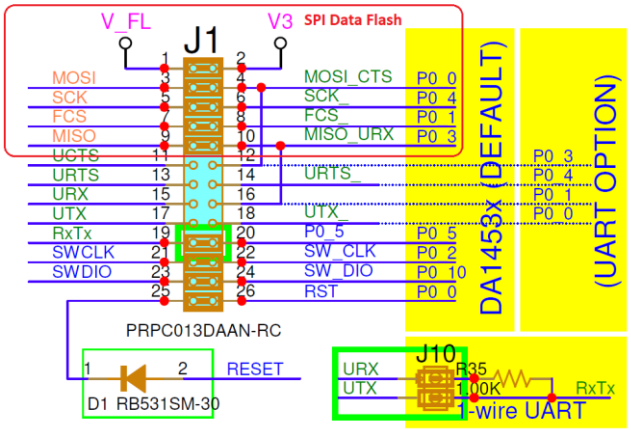

Figure 33. Jumper configuration at J1 header on Pro-MB

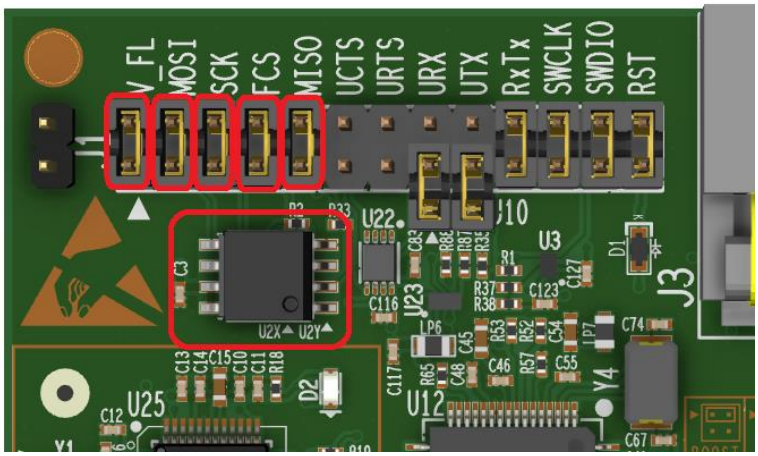

Figure 34. SPI data flash and configuration jumpers position

6.8 Configuration headers J1 and J10

Header J1 and J10 configuration define the communication interface between the DA1453x Pro-MB and DA1453x Pro-DB. You can choose if the SPI data flash is to be included in the system, the type of the UART connection (single wire UART or 2 wire UART or flow control), JTAG and Reset access. This header can also be used for monitoring and for debugging/measuring.

The default pin assignment is presented in Figure 35 and the default jumper configuration in Figure 36.

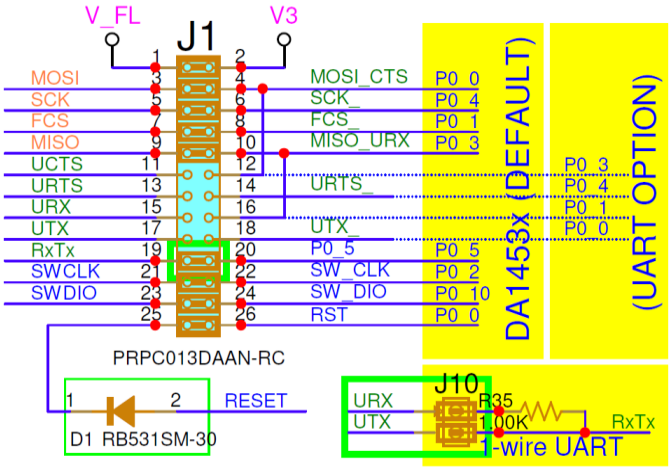

Figure 35. J1 pin assignment (including J10)

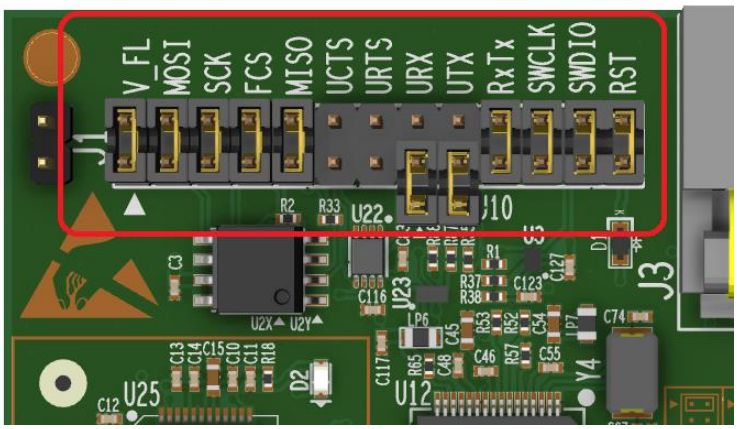

Figure 36. J1 default jumper configuration

The default configuration, (Figure 36) is:

- SPI data flash
- Single wire UART
- JTAG access
- Reset access.

NOTE
Consider configuring the software accordingly to support the above hardware features. If a DA1453x Pro-DB with a Flash is plugged on the Pro-MB, the following jumpers must be removed: ● J1 1:2 ● J1 3:4 ● J1 5:6 ● J1 7:8 ● J1 9:10

Pro SPI flash signals on the Pro-MB must not be used and should be kept isolated to avoid conflict with correlated signals on Pro-DB.

6.9 UART configuration

Any GPIO pin can be set as UART in the DA1453x SoC. In the DA1453x Dek-Kit specific pins are used for UART signals. The dev-kit supports three different modes of UART:

- Single-wire UART (default)
- Two-wire UART
- Flow control UART.

The UART signal assignment is shown in

Table 6.

Table 6. UART signals assignment in DA1453x Dev-Kit

Pro-MB signal	Function	Pro-DB signal	Comments
UTX	Two-wire UART or Full UART Transmit – boot UTX	P0_1	Used for SPI data Flash

Pro-MB signal	Function	Pro-DB signal	Comments
URX	Two-wire UART or Full UART Receive – boot URX	P0_0	Used for SPI data Flash
UCTS	Two-wire UART or Full UART Clear To Send	P0_3	Used for SPI data Flash
URTS	Two-wire UART or Full UART Request To Send	P0_4	Used for SPI data Flash
RxTx	Single-Wire UART Receive and Transmit – boot-TxRx	P0_5	

SPI data flash and two-wire UART or full UART use same DA1453x GPIOs. This is valid for the data flash memory located either on Pro-MB or on Pro-DB. Consequently, when a two-wires or four-wires UART is used, SPI data flash can't be used and vice versa.

6.9.1 Single-wire UART

Single-wire UART is the default configuration on the DA1453x DevKit and it is assigned to P0_5 for both RX and TX as shown in Figure 37. The jumper configuration is highlighted in Figure 38.

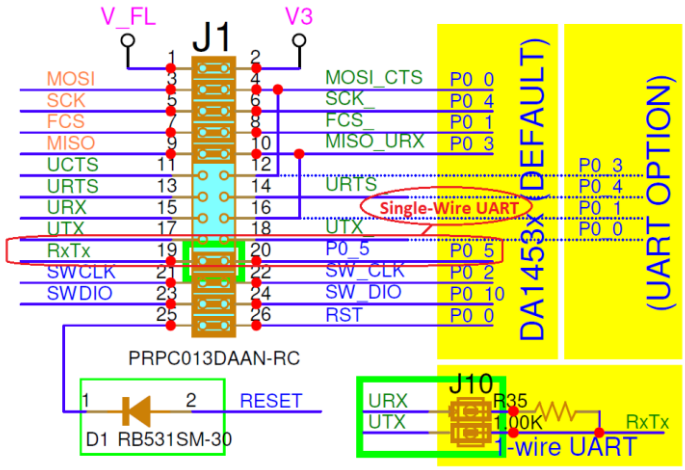

Figure 37. Single-wire UART jumper configuration at J1 header on Pro-MB

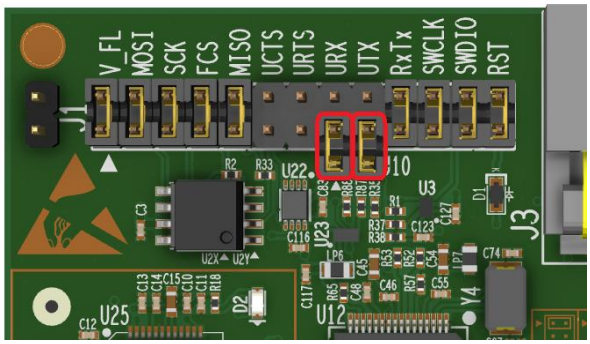

Figure 38. Single-wire UART configuration jumpers position

6.9.2 Two-wires UART

Two-wire UART pins are multiplexed with FCS (chip select) and MOSI of the SPI bus. The jumpers of the SPI flash must be removed. The two-wire UART jumper configuration is highlighted in Figure 39 and Figure 40.

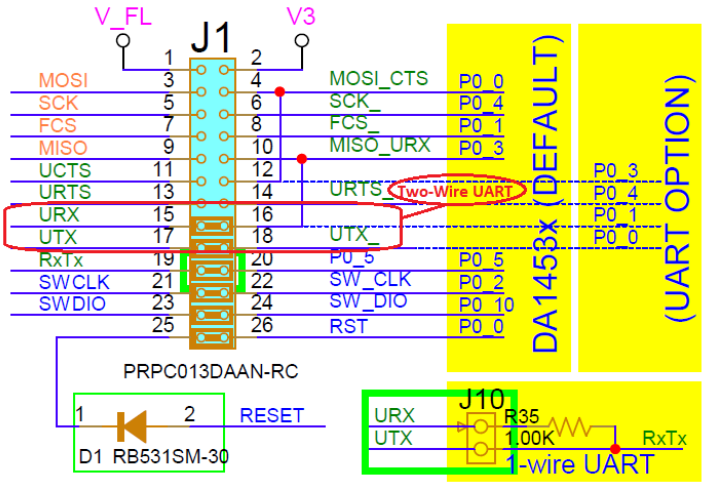

Figure 39. Two-wires UART jumper configuration at J1 header on Pro-MB

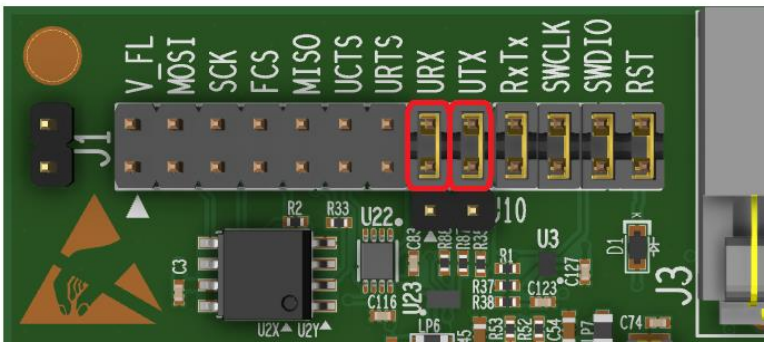

Figure 40. Two-wires UART configuration jumpers position

By placing the jumpers, UTX and URX are driven from signals P0_0 and P0_1 respectively. These signals are not connected to the correspondent pins of DA1453x SoC. You must modify the Pro-DBs by mounting resistors R23 and R24 (both equal to 0Ω).

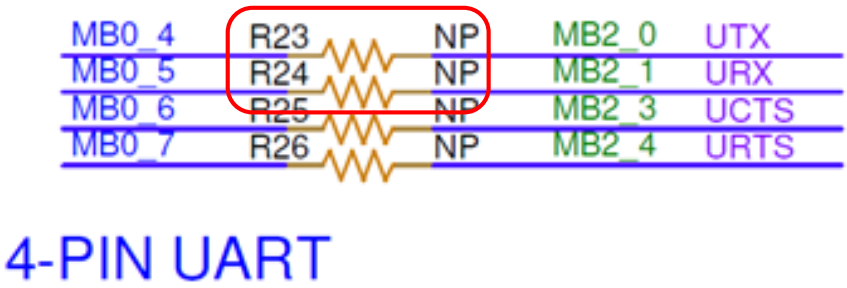

Figure 41. Enable two-wires UART on Pro-DB

Alternatively, you can use a jumper wire for connecting the appropriate signals, without modifying Pro-DBs:

- J1:4 to J1:17 for UTX
- J1:8 to J1:15 for URX

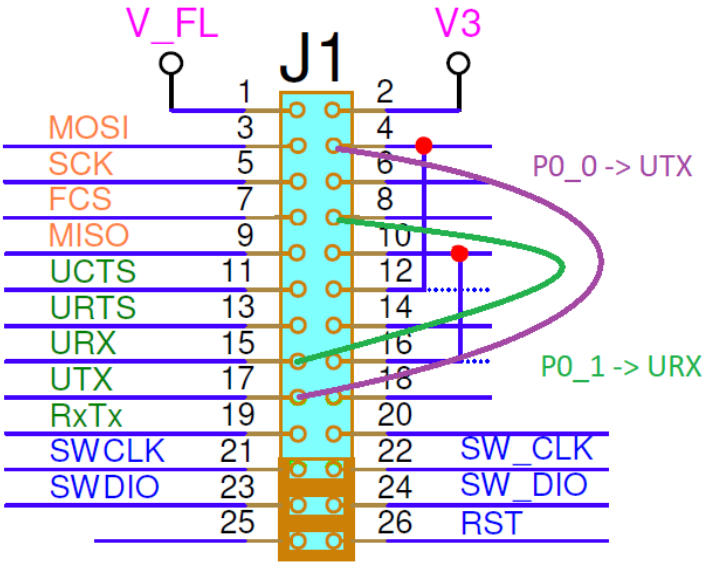

Figure 42. Enabling two-wires UART with jumper wires

6.9.3 Four-wires UART/UART with flow control

Four-wires UART pins UTX, URX, URTS, and UCTS are multiplexed with MOSI, FCS, SCK, and MISO of the SPI bus, respectively. The jumpers of the SPI flash must be removed. The Full-wire UART jumper configuration is highlighted in Figure 43 and Figure 44.

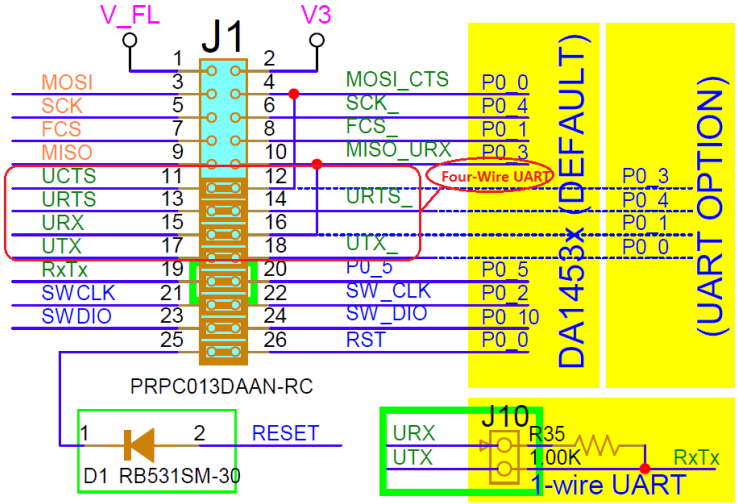

Figure 43. Full-wire UART jumper configuration at J1 header

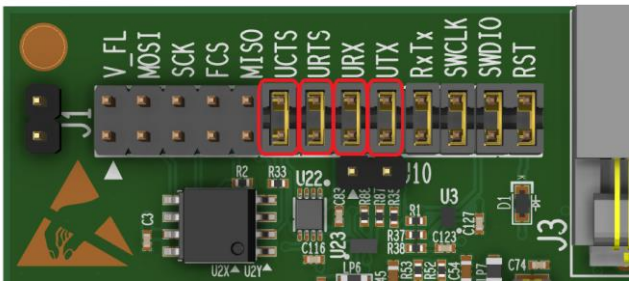

Figure 44. Four UART configuration jumpers position

By placing the jumpers, UART signals are driven from signals P0_0 to P0_4. These signals are not connected to the correspondent pins of DA1453x SoC. You must modify the Pro-DBs by mounting resistors R23 to R26 (both equal to 0Ω) and to remove resistors R19 to R22.

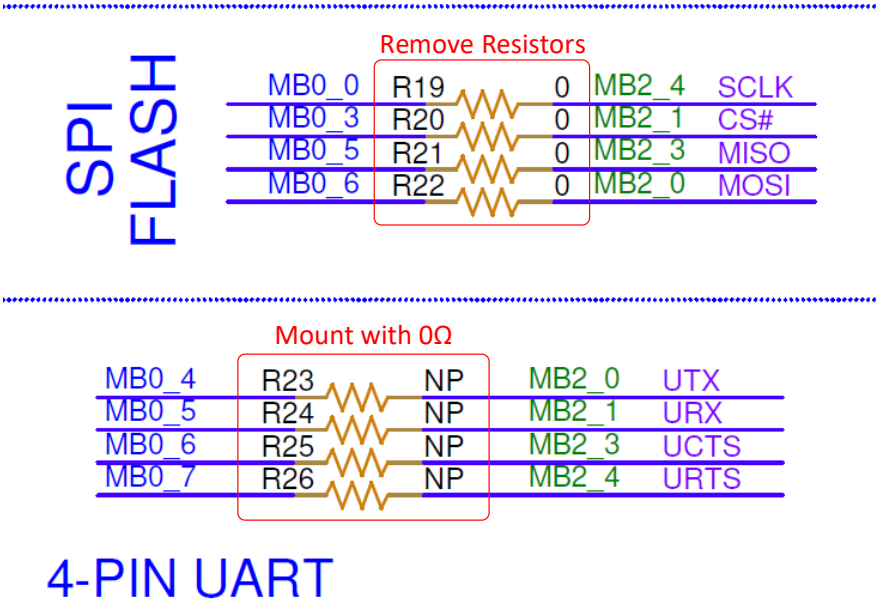

Figure 45. Enable two-wires UART on Pro-DB

Alternatively, you can use a jumper wire for connecting the appropriate signals, without modifying Pro-DBs:

- J1:4 to J1:17 for UTX
- J1:8 to J1:15 for URX
- J1:10 to J1:11 for UCTS
- J1:6 to J1:13 for URTS.

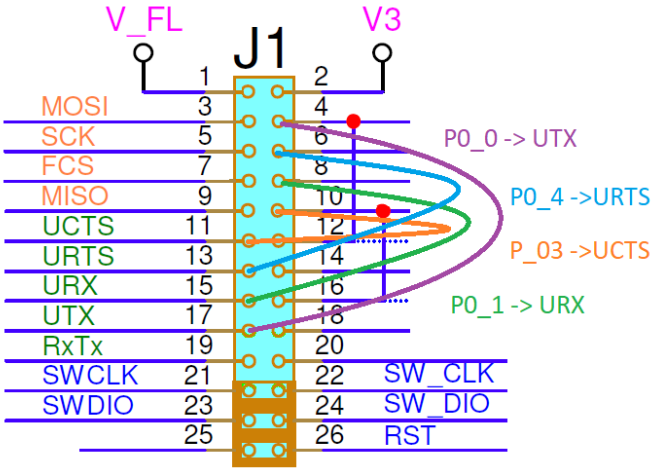

Figure 46. Enabling two-wires UART with jumper wires

6.10 JTAG configuration

JTAG uses the Serial Wire Debug (SWD) protocol and consists of the SWDIO and SWCLK lines. The JTAG signal assignment is shown in Table 7.

Table 7. UART signals assignment in DA1453x Dev-Kit

Pro-MB signal	Function	Pro-DB signal	Comments
SWCLK	Serial Wire Clock	P0_2	
SWDIO	Serial Wire Data Input Output	P_10	On the WLCSP package the SWDIO assigned to P0_5.

Note 1 JTAG and UART cannot be used in parallel for the WLCSP versions of the DA1453x SoC without software modification.

The JTAG jumper configuration is highlighted in Figure 47 and Figure 48.

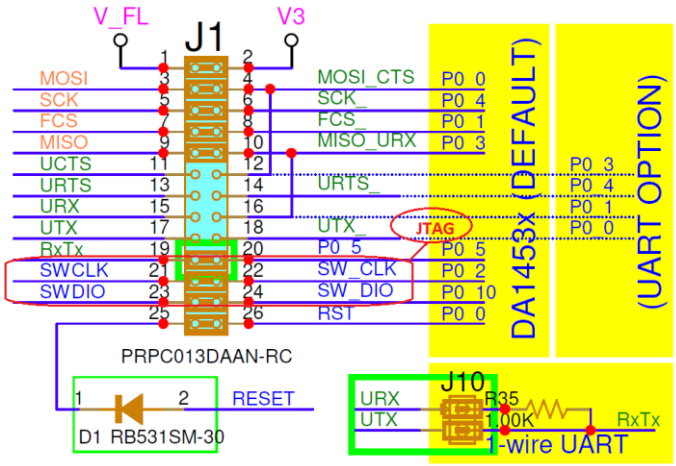

Figure 47. JTAG jumper configuration at J1 header

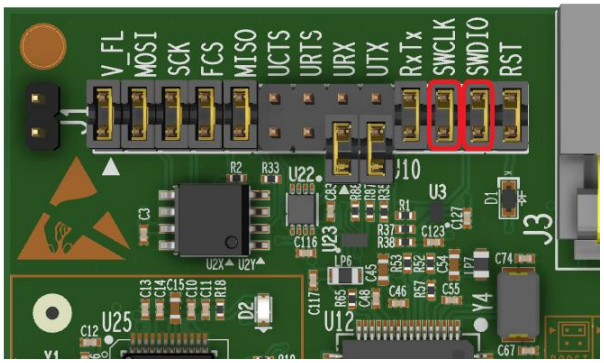

Figure 48. JTAG configuration jumpers position

6.11 Breakout header J2

All P0_X GPIOs of the DA1453x Pro-DBs are diverted also to the DA1453x Pro-MB for monitoring on the breakout header J2 of the Pro-MB. The schematic of the J2 is shown in Figure 49 and the position of the J2 header on DA1453x in Figure 50.

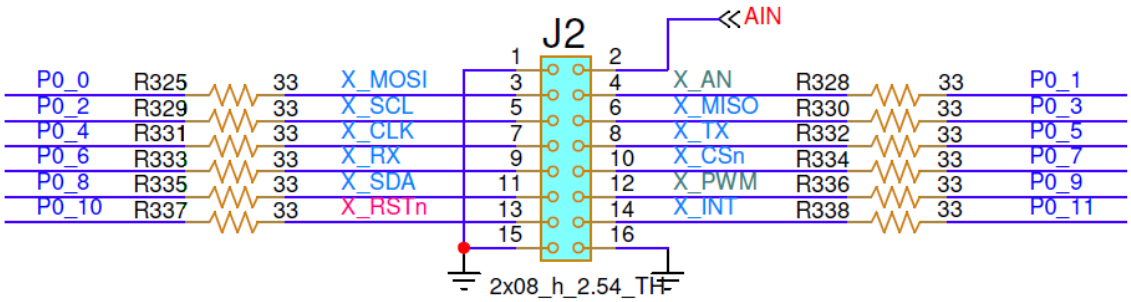

Figure 49. J2 schematic

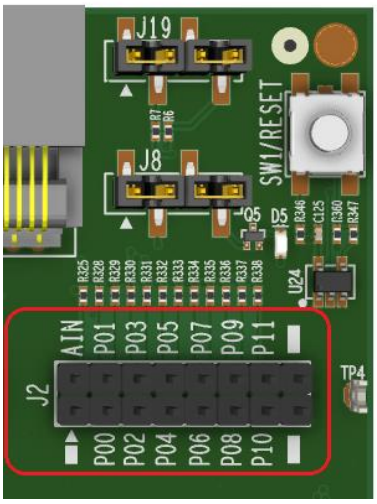

Figure 50. J2 position on DA1453x Pro-MB

6.12 Push buttons

There are two available push buttons on the DA1453x Pro-MB, the SW2 and SW3. The SW2 is assigned to P0_11 and the SW3 to P0_10. The WLCSP versions of the DA1453x SoC do not support any push button whereas DA14533 supports only the SW3.

By default, the jumpers on J19 are mounted. The circuit schematic is shown in Figure 51 the position of the push buttons in Figure 52, and the position of the J19 header in Figure 53.

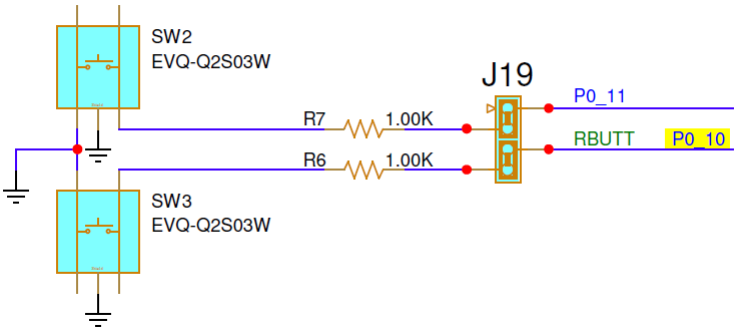

Figure 51. Push buttons SW2 and SW3

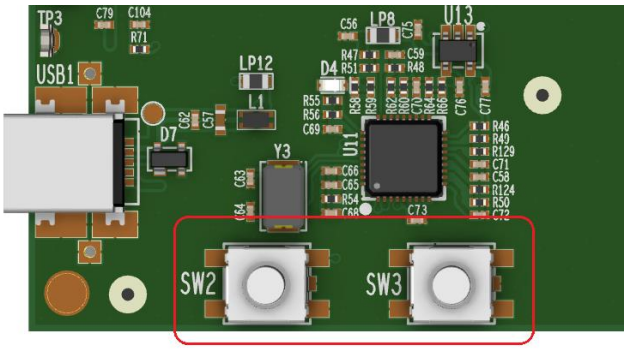

Figure 52. Push buttons position on the DA1453x Pro-MB

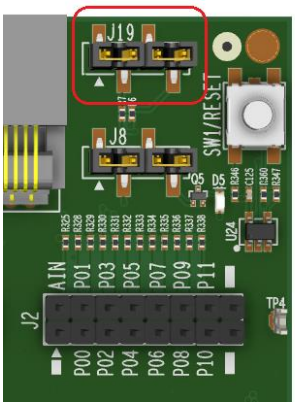

Figure 53. J19 header position on the DA1453x Pro-MB

6.13 User LED

The user LED (D5) is supported only from DA14531 and DA14535 FCQFN packages. The user LED is assigned to P0_9. The circuit schematic is shown in Figure 54 and the position of the user LED on the DA1453x Pro-MB in Figure 55. The jumper on the J8 header (pin 3-4) is mounted by default.

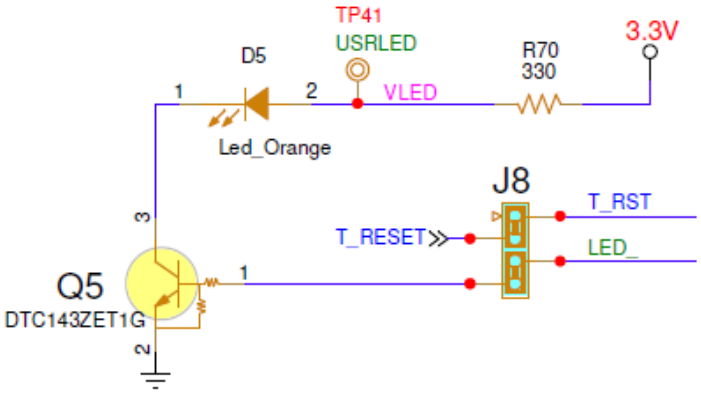

Figure 54. User LED (D5)

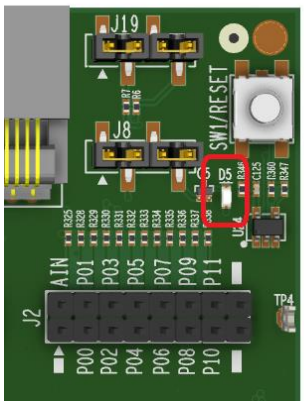

Figure 55. User LED position

6.14 MikroBus interface

DA1453x Pro-MB can support one MikroBus module. The MikroBus slot is compatible with MikroBus standard click boards for additional expandability requirements. Two female headers (8 position 0.100", through hole, socket type) are mounted (by default) on J17 and J18. The schematic circuit is shown in Figure 56 and the position of the MikoBus slot in Figure 57.

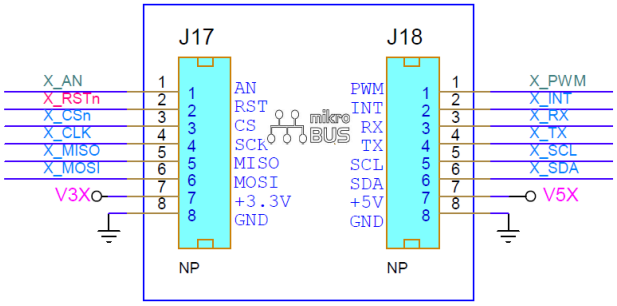

Figure 56. MikroBus slot

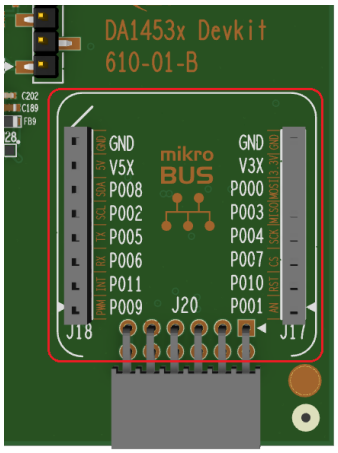

Figure 57. MikroBus position on the DA1453x Pro-MB

6.15 PMOD interface

DA1453x Pro-MB can support one PMOD module. The female header (J20) is mounted (by default). The schematic circuit is shown in Figure 58 and the position of the MikoBus slot in Figure 59.

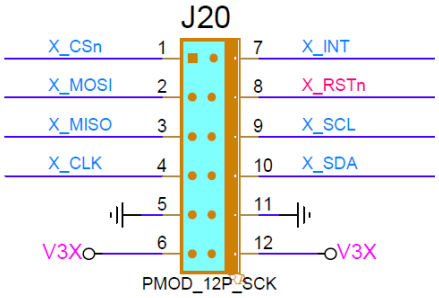

Figure 58. PMOD slot

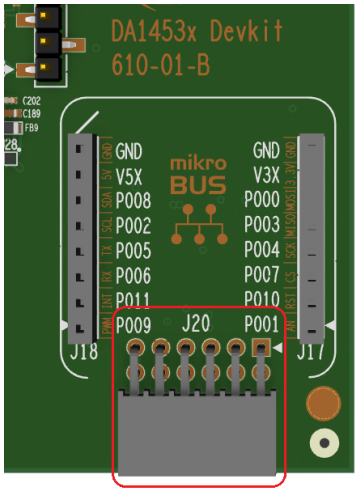

Figure 59. PMOD position on the DA1453x Pro-MB

GPIOs and Pin Assignment and Functions of DA1453x DK Pro.

All P0_X GPIOs of the DA1453x Pro-DBs are diverted also to the DA1453x Pro-MB for monitoring.

On the breakout headerJ2 of the Pro-MB, you can monitor the P0_X GPIOs mainly used for the MikroBUS, PMOD interface.

6.16 Measurements and software triggers

On DA1453x Development kit, you can monitor the critical current and voltages of the system. This is implemented with a power measurement circuitry which consists of the power measurement module (PMM2) and the monitoring circuit, which resides on the DA1453x Pro-Motherboard. With the aid of the Power profiler of Renesas Smart Snippets Toolbox, a good visualization of the system current drawn and various voltages is provided. Measurements are quite accurate, but for precise measurements, use an external calibrated instrument.

PMM2 features are:

- DA1453x current measurement (1 uA-100 mA at 128 kHz)
- Measurement of two additional system currents (voltage rails V3x and V5x for Mikrobus/PMOD)
- 2x DA1453x system voltage measurement
- 8 x DA1453x system voltage monitoring
- Monitoring and measuring up to 8 Digital signals with capability to be configured as software triggers.

The block diagram of PMM2 is shown in Figure 60. The analog frontend and ADC converter are implemented on the PMM2 module, whereas the SPI to USB bridge (FT2232H, U12) and digital signals reside on the motherboard.

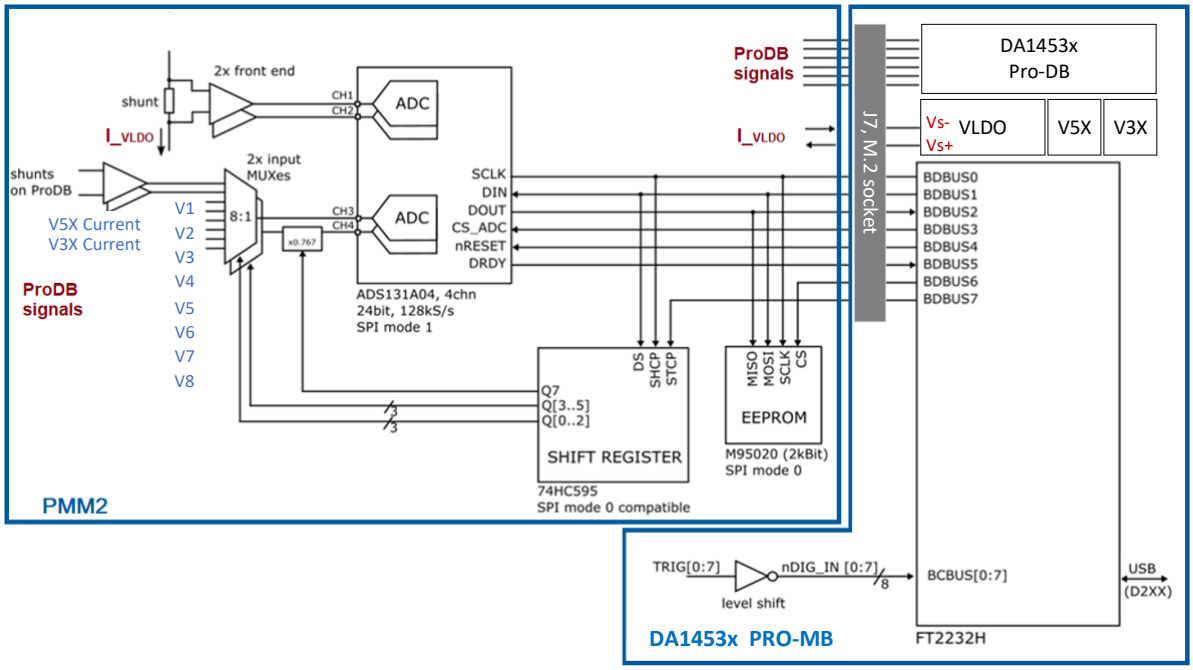

Figure 60. Power measurement module (PMM2) block diagram

An EEPROM is also provided on the module to store production data and allow autodetection from the host software.

The power measurement module (PMM2) is connected to Pro-Motherboard through J7, M.2 socket. PMM2 is supplied from 3.3 V and VCM through power switch U24.

The DA1453x does not employ shunt voltage drop compensation. The voltage drop on the PMM2 is $V_{PMM2\_dropout}=2.4*I_{VBAT}$. Use cases for the DA1453x rarely draw more than 40-50 mA of current in which case the max voltage drop of about 100 mV due to the PMM2 should not cause problems.

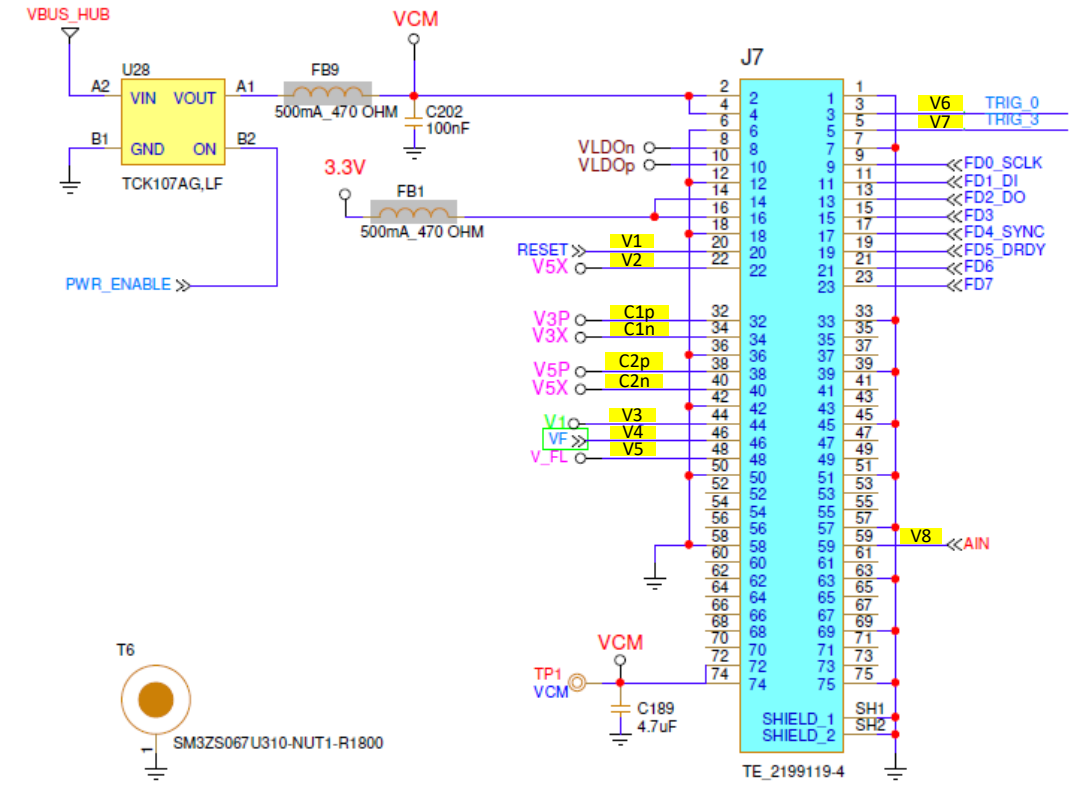

Figure 61. Current measurement socket (M2)

Table 8. Monitored power sources

PMM2 pins (Note 1)	**DA1453x signals**	**Comments**
V1	Reset	Reset line, applied on pin J7.20
V2	V5X	5 V rail powering MikroBUS. It is connected to USB1 through a 0.1Ω resistor and filter L1.
V3	V1	This is voltage rail is connected to the VBAT_Low of the DA1453x SoC. When, VLOW. It is applied on pin J7.44. Sourced from Pro-Daughterboard when DA13453x is configured in BUCK or BYPASS mode. Sourced from Pro-Motherboard when DA13453x is configured in BOOST mode.
V4	VF	It is a sample of the voltage that is supplied to DA1453x SoC. It is applied on pin J7.46. Sourced from Pro-Motherboard.
V5	VFL	The supply voltage of Flash that is located on the Pro-Motherboard. It is applied on pin J7.48.
V6	TRIG_0	Pin P0_11 or another signal connected on J24.1. Applied on pin J7.3.
V7	TRIG_3	Pin P0_5 or another signal connected on J24.7. Applied on pin J7.5.
V8	AIN	Any signal connected on J2.2 with a jump wire. Applied on J7.59.

PMM2 pins (Note 1)	DA1453x signals	Comments
VLDOp, VLDOn	Vs+, Vs-	DA1453x VBAT_x current measurement. Sourced from Pro-Motherboard. Current enters PMM2 from Vs+ (pin J7.10) and exits from Vs- (pin J7.8).
C1p, C1n	V3P, V3X	3.3 V voltage rail. V3X current measurement. The current drawn from PMOD.
C2p, C2n	V5P, V5X	5 V voltage rail. V5X current measurement. The current drawn from MikroBUS or PMOD.

Note 1 See PMM2 daughterboard pinout.

There are eight TRIG options defined (TRIG_0 to TRIG_7).

As shown in Figure 62, suitable jumper block (J7) allows you to directly select any of the available signals. Any other GPIO can be used as a trigger source by connecting a TRIG pin on J7 with a jumper wire to the desired position at breakout header (J2).

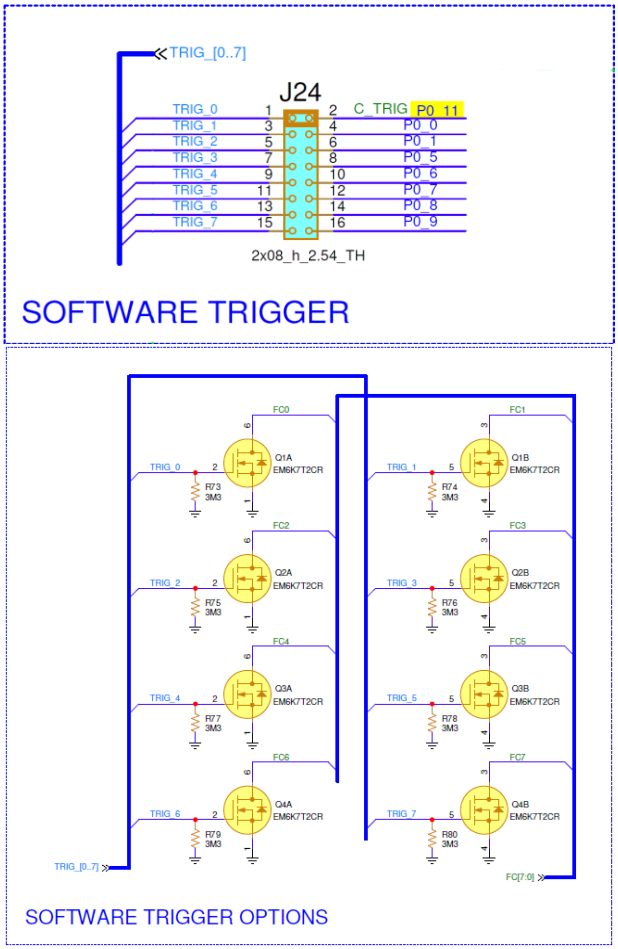

Figure 62. Selection jumper block (J24) and buffer MOSFETS for I/O levels compatibility

The dual Mosfets Q1 to Q4 buffer the signals to provide compatibility with 1.2 to 5 V I/O levels.

Renesas Smart Snippets Toolbox is required for capturing the waveforms of DA1453x system. By using Power profiler, you can monitor simultaneously, on separated windows, the DA1453x VBAT current, two analog waveforms (voltages or currents) and up to eight digital signals, Figure 63.

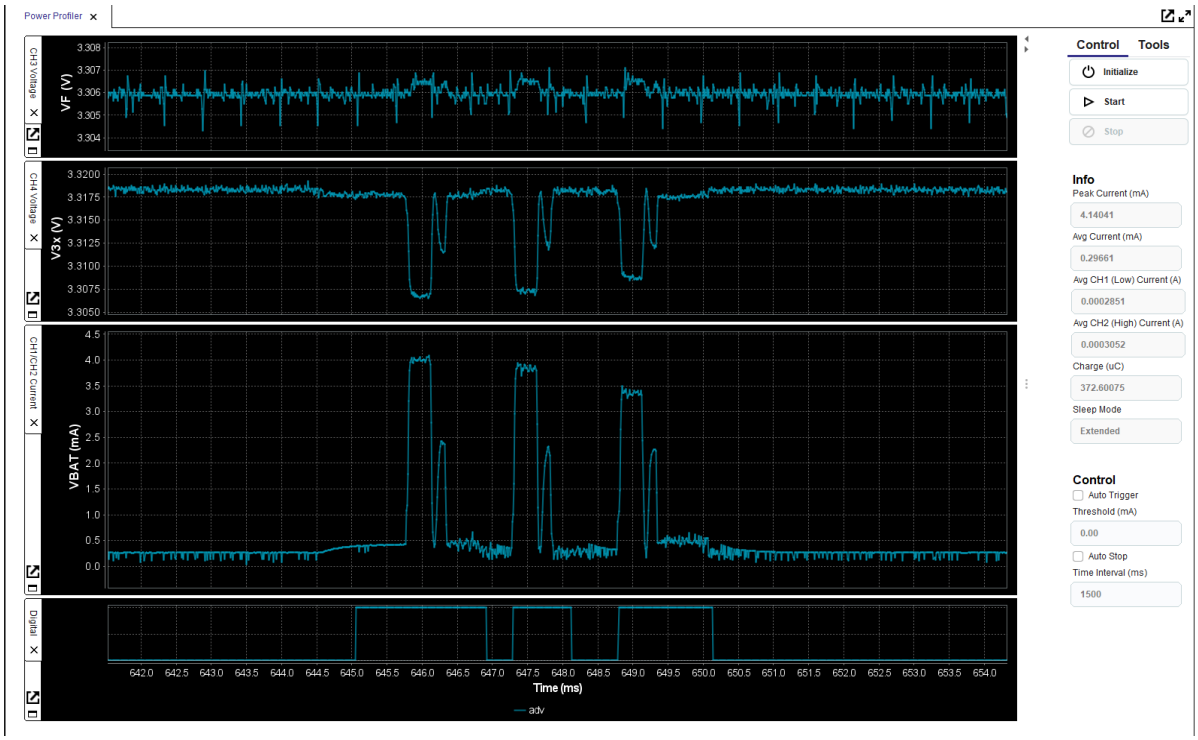

Figure 63. DA1453x waveforms, captured from Power profiler of SmartSnippet Toolbox

This functionality, coupled with the digital trigger signals allows profiling the power footprint of software operations and provides you a better insight of how the system works. Digital signals can be used either as monitoring signals or as triggers to start/stop capture of data so the user can isolate specific events. The trigger functionality is implemented in SDK.

7 The Power Measurement Module 2 (PMM2), (500-29-x)

The power measurement module (PMM2) is an external add-on board that is interfaced (connected) on the Pro-Motherboard via connector J7.

The current measurement unit has the following features:

- Full scale range 640 mA at 3 V (for currents > 50-100 mA dropout compensation is recommended – not implemented in the DA1453x Pro-Devkit)
- Measure accurately down to 1 µA
- Dedicated hibernation mode to measure down to 100 nA
- Current sense resistors
  - 2.4 Ω in series to VLDO (located on PMM2)
  - 0.1 Ω in series for measuring current on C1p/C1n (located externally to PMM2)
  - 0.1 Ω in series for measuring current on C2p/C2n (located externally to PMM2)
- Analog processing blocks
- Fast quad channel 24-bit ADC with SPI interface
- FTDI chip for transferring data to the PC
- Software trigger inputs
- System voltage measurement
- External analog input 5 V.

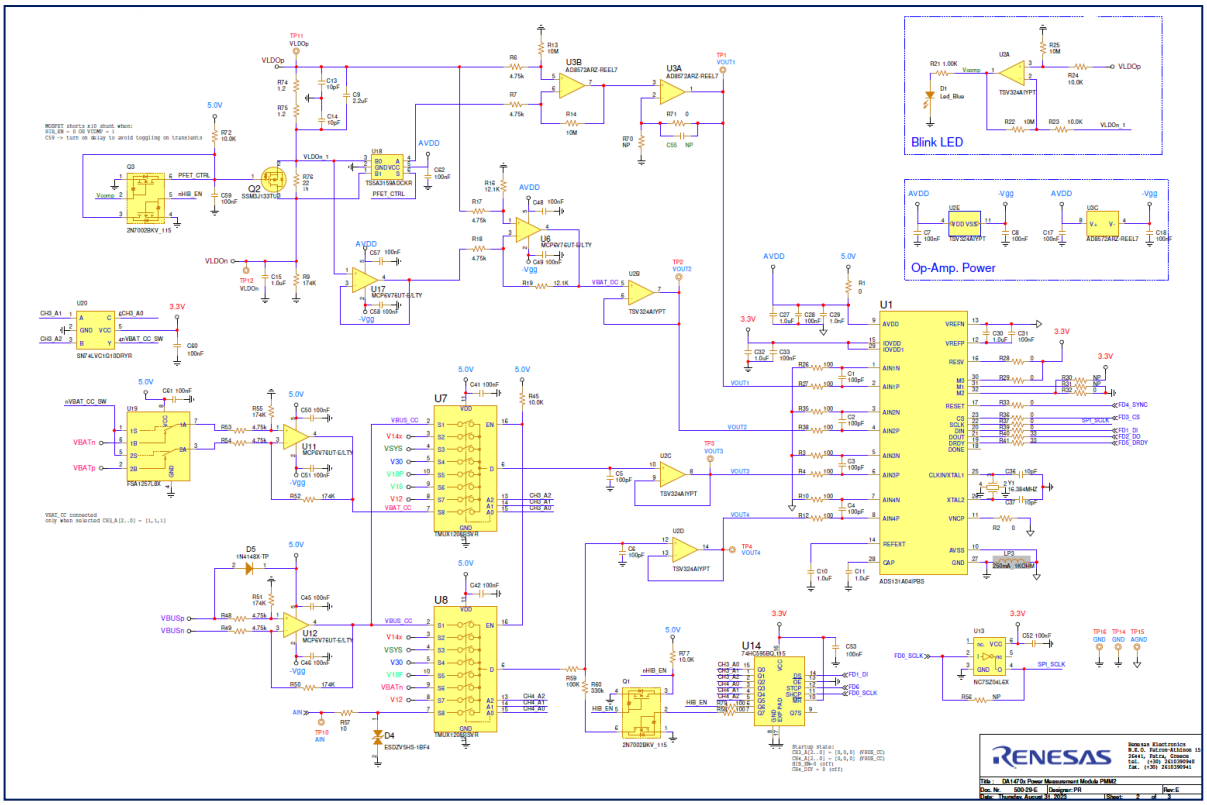

Figure 64. PMM2 current measurement circuit PMM2

The input to the circuit is the voltage across the sense resistors R74 and R75. The voltage across the sense resistors is sampled simultaneously by two differential amplifier stages and is converted by the ADC to a digital value. The low range has a conversion gain of 5053 V/A and covers from 1 µA up to about 790 µA. The high scale has a conversion gain of 6.114 V/A and covers up to about 600 mA

depending on the VBAT voltage. Both channels are sampled simultaneously, and the host software selects the correct channel using a threshold of 750 µA. R9 provides a constant offset which helps avoid the nonlinear region of the low scale. A blue LED serves as a visual indicator of the range. It switches on close to 750 µA and allows you to have a quick indication of the state of the system (on when active, off when sleeping).

Multiplexers U7 and U8 select among the available system voltages and feed channels 3 and 4 of the ADC. A divider formed by R59 and R60 can be selected on CH4 to allow for 5 V input signal range (the full-scale voltage of the ADC is 4 V). Two analog front ends around U11 and U12 are provided for measuring the C1 (VBATp/n) and C2 (VBUSp/n) currents. The switch in front of U11 prevents the leakage current of the differential amplifier stage from C1 (VBATp/n) to be measured as system current.

A shift register and associated logic control the multiplexers and the rest of the functions of the module. An EEPROM memory is used to store production data and allows the host software to autodetect the module. Charge pump U6 generates a slightly negative voltage (-230 mV) to allow the output of the frontend OPAMPs to reach true zero.

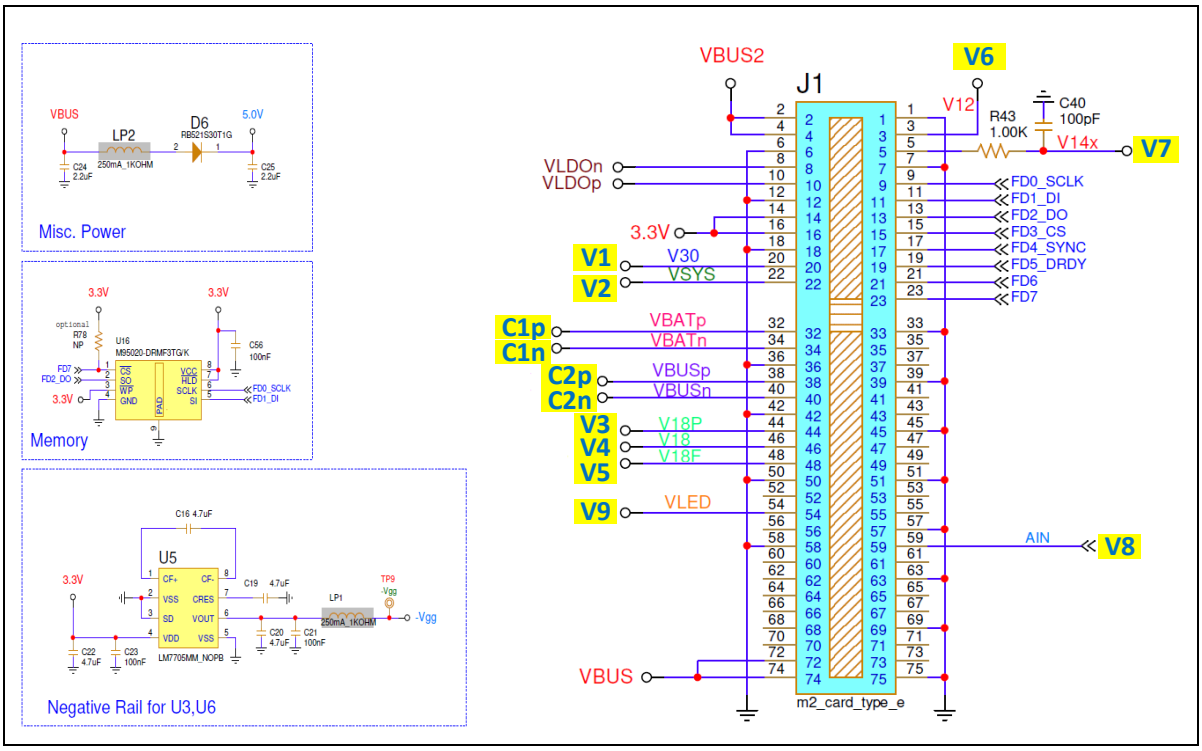

Figure 65. PMM2 on board peripherals (power supply, memory and so on)

The circuit can be set in a low current measurement mode from the host (hibernation mode). This is useful to measure the current of the SoC in hibernation (shipping) mode, which is in the order of some hundreds of nA. The measurement range of the circuit in this mode is from 100 nA to 60 µA. This is achieved with a significantly larger sense resistor (R76) which is shorted by Q2 in normal operation. In hibernation mode, Q2 switches off and R76 is placed in series with R74 and R75 forming a 24.4 Ω sense resistor. The lower sampling point of the low range is moved to the terminals of this series combination with the help of analog switch U18. The high range connections remain unchanged, and it monitors the current through R74 and R75 only. To avoid excessive voltage drop due to the large sense resistor, in case the system wakes up and draws large currents, the LED indicator output also overrides the control of Q2 when the measured current exceeds ~600-700 µA. This ensures that the system can wake up normally and its operation is not affected by the hibernation mode. The hibernation mode is intended for measuring low level and mostly stable currents.

The offset of the circuit can be calibrated in the Smart Snippets Toolbox software. The procedure necessitates disconnecting the daughterboard either physically or by sliding the daughterboard power selection switch to the right.

Sampling rate is by default 128 kS/s but can be further reduced to 84 kS/s when using slower machines or lower speed USB ports. All analog and digital signals are sampled simultaneously.

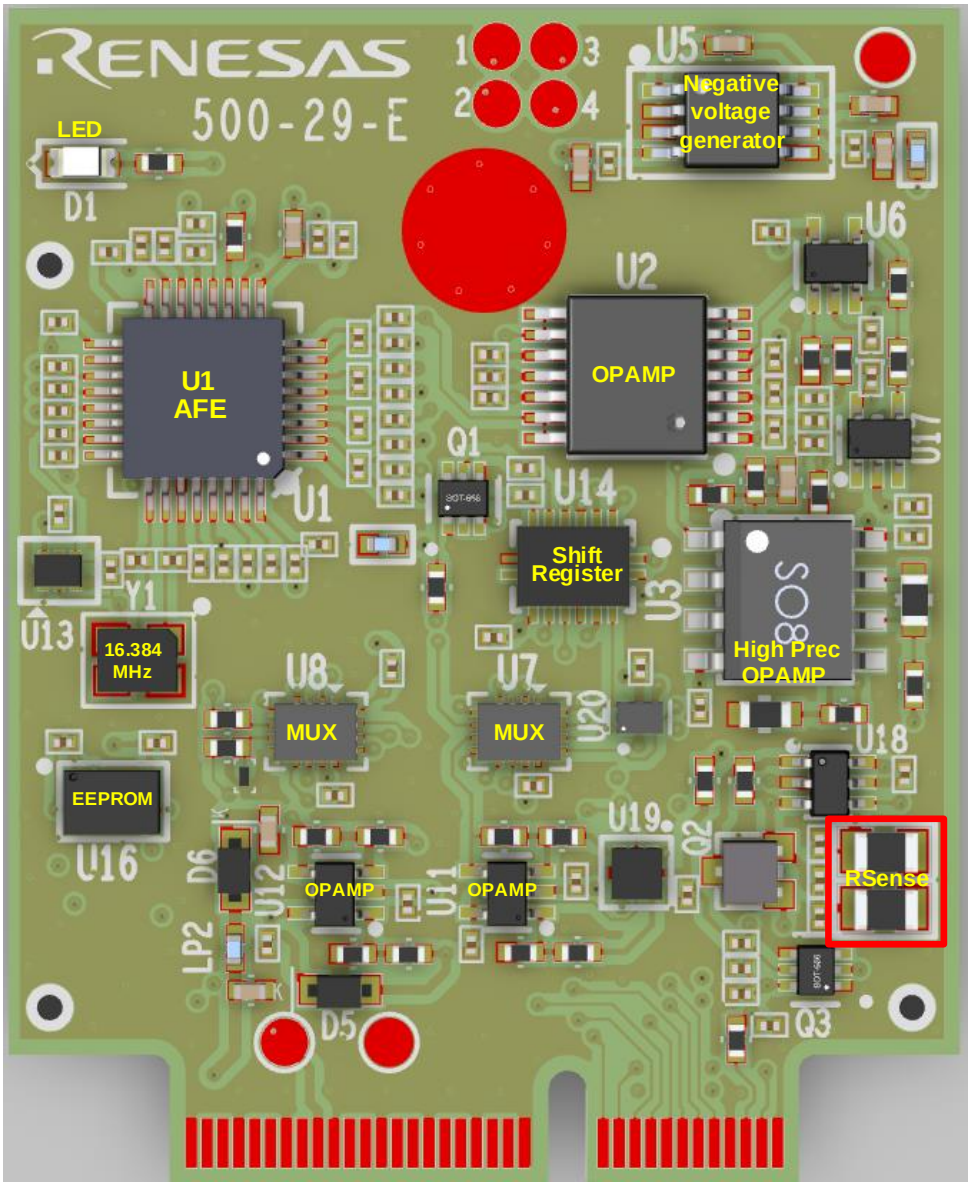

Figure 66. Current measurement unit PCBA (TOP)

7.1 Accuracy of current measurement for VBAT system (VLDO)

The total measuring range of the current measurement circuit of the power measurement module two is 100 nA to 500 mA for VLDO= 3 V, implemented into two scales. The current measurement range is covered by two operating modes, the default (1 µA to 500 mA) and the hibernation mode (100 nA to 60 µA). Switching from default to hibernation mode is done manually over Smart Snippets Toolbox (a version supporting this mode must be used).

The circuit accuracy is measured by applying a constant current, monitoring the same current with an external instrument and the ADC of the PMM2 module, then comparing the two. In general, the inaccuracy presented in the current measurement circuit is less than 5% (practically less than 2%) in most of the current range, (Table 9). The values presented in Figure 67 are averages of multiple points.

Table 9. Accuracy of the current measurement circuit

Channel	Range	Error (%)	Comment
CH1/CH2: VBAT current hibern.	100 nA-60 µA	±15% at 100 nA, <±2% at 1µA-60 µA	Mode automatically overridden in hardware if current > ~750 µA
CH1/CH2: VBAT current active	1 µA-640 mA	±10% at 1 µA, <±2% at 100 µA-640 mA	2 ranges [1µA-750 µA/750 µA-640 mA]
CH3, CH4 current: C1p/n, C2p/n	1 mA-1 A	±5%	Range and accuracy depend on external R_{sense}. Values shown with 0.1 Ω/1% shunt
CH3 voltage	0-4 V	±2%	
CH4 voltages	0-4 V/0-5 V	±2%	0-5 V range available with 0.776x divider enabled

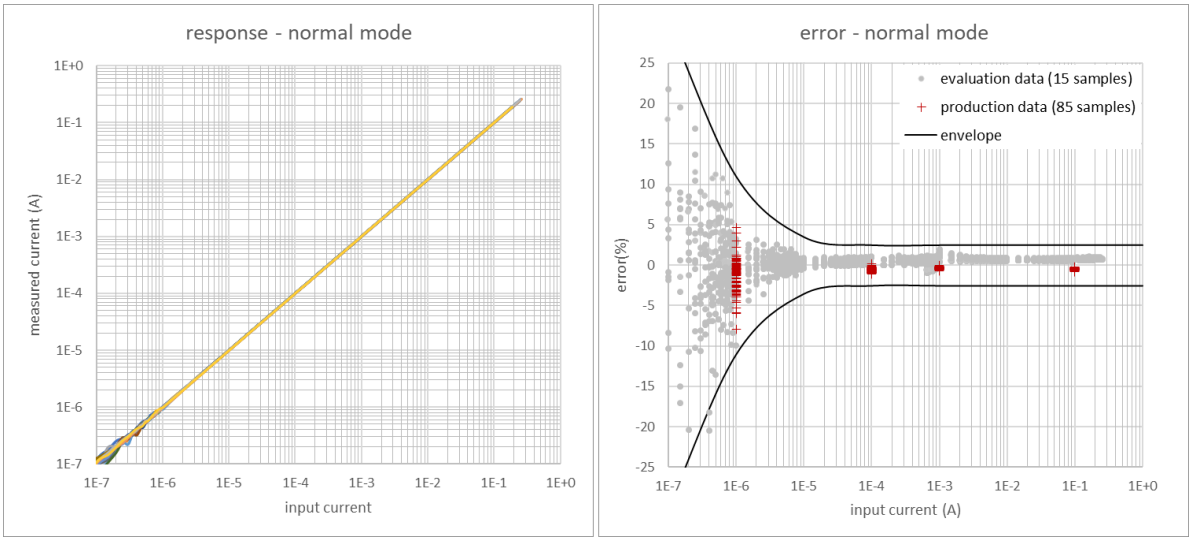

Figure 67. Normal mode (1 µA to 640 mA at 3.3 V) data after offset calibration

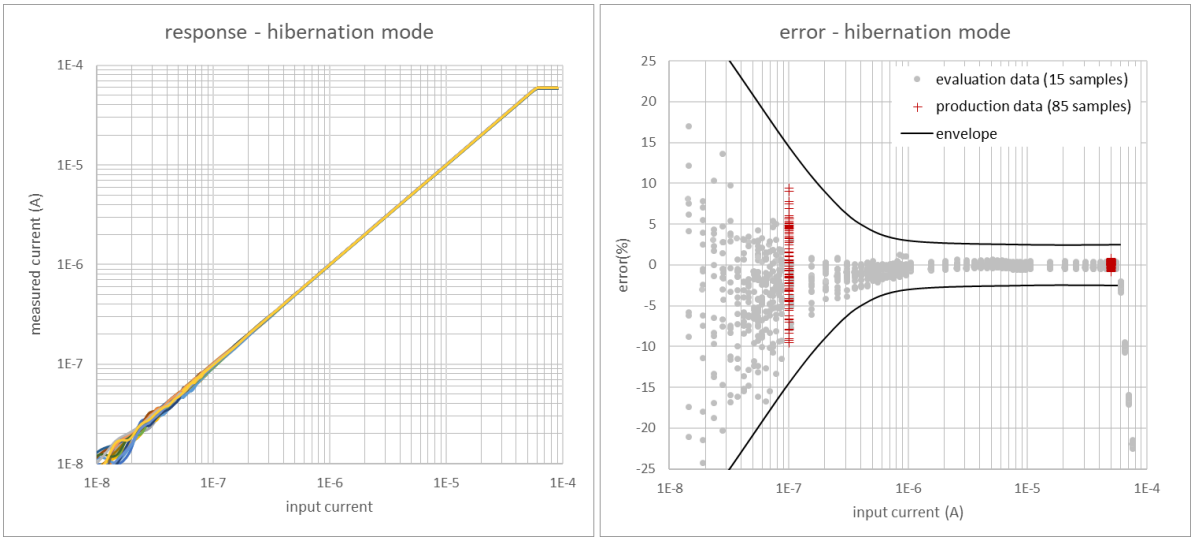

Figure 68. Hibernation mode (100 nA to 60 µA at 3.3 V) data after offset calibration

Appendix A Schematics

A.1 DA1453x Pro motherboard (610-01-B), schematic.

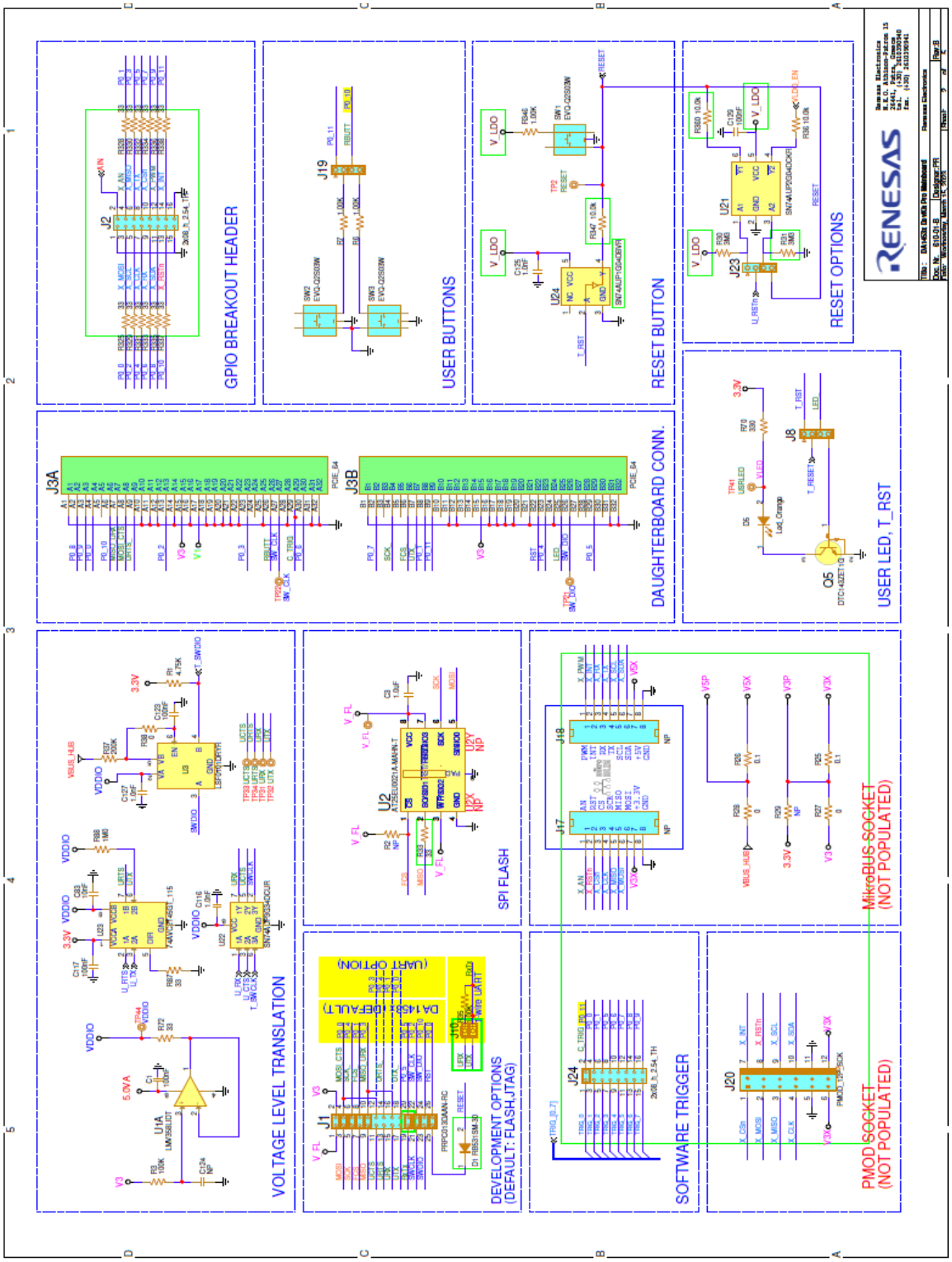

Figure 69. DA1453x Pro-MB (610-01-B), GPIO connectivity, voltage translators, and data flash

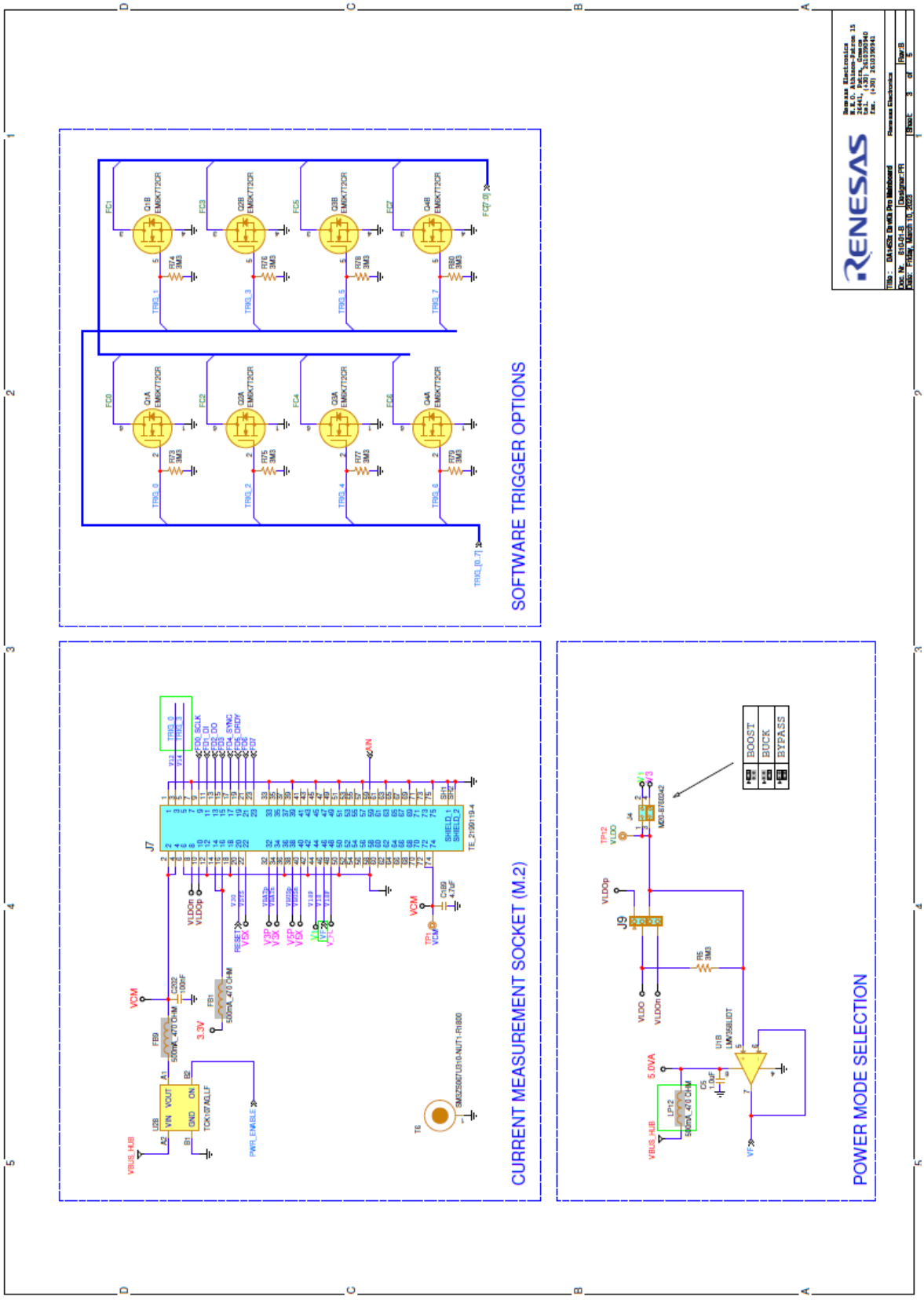

Figure 70. DA1453x Pro-MB (610-01-B), PMM2 interface

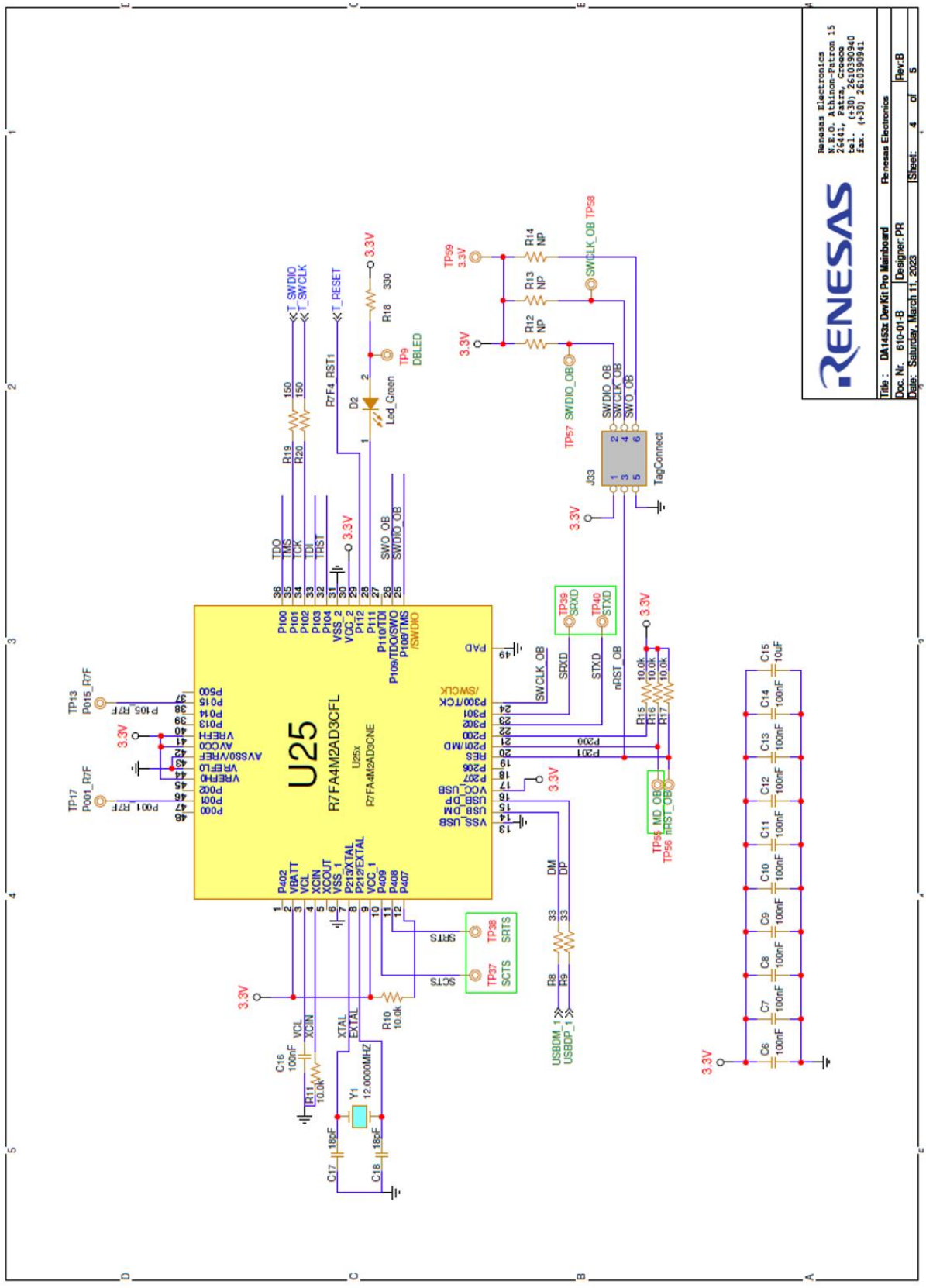

Figure 71. DA1453x Pro-MB (610-01-B), the MCU with segger implementation

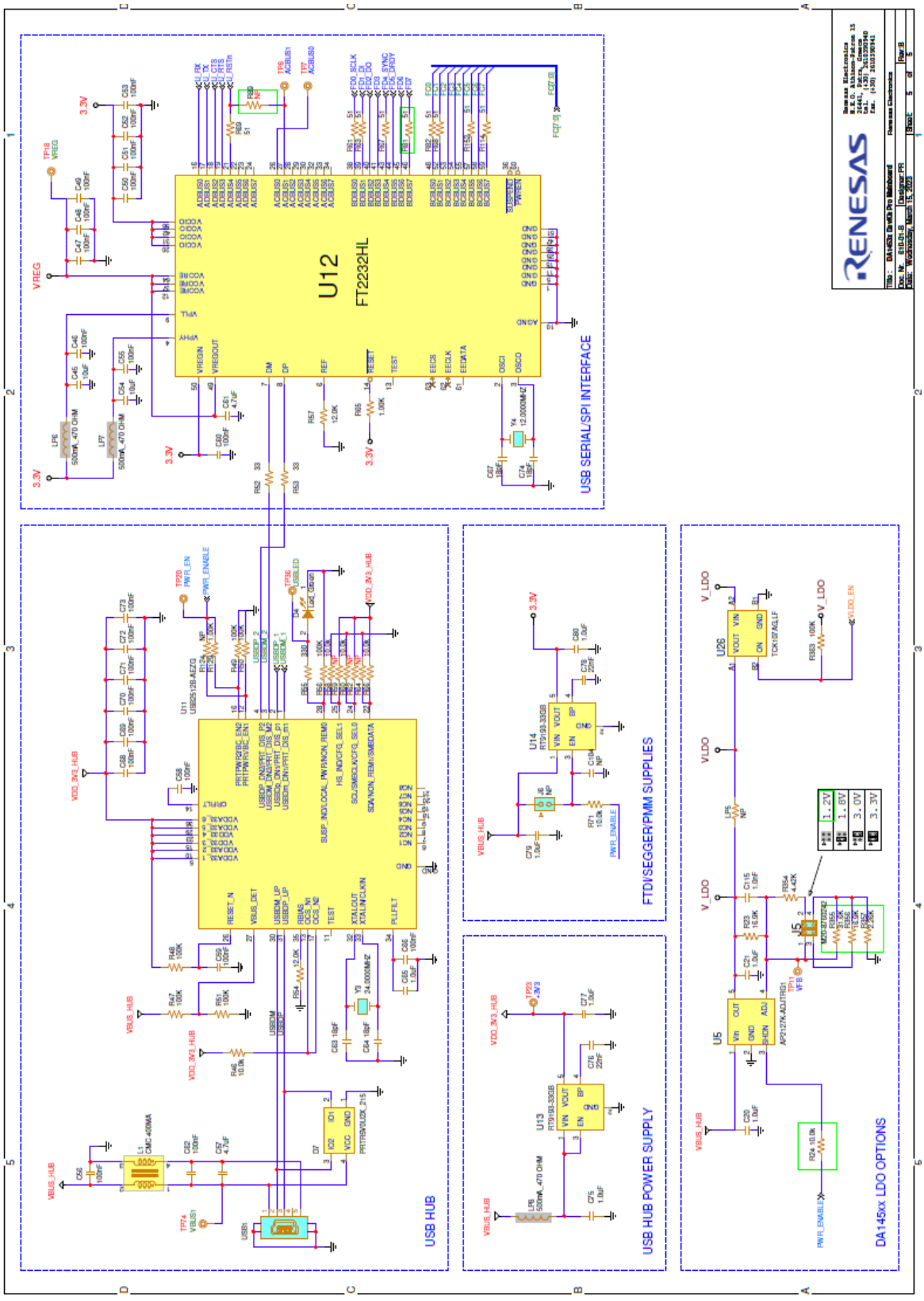

Figure 72. DA1453x Pro-MB (610-01-B), USB hub, UART and power section

A.2 DA14535 Pro daughterboard (610-02-A), schematic

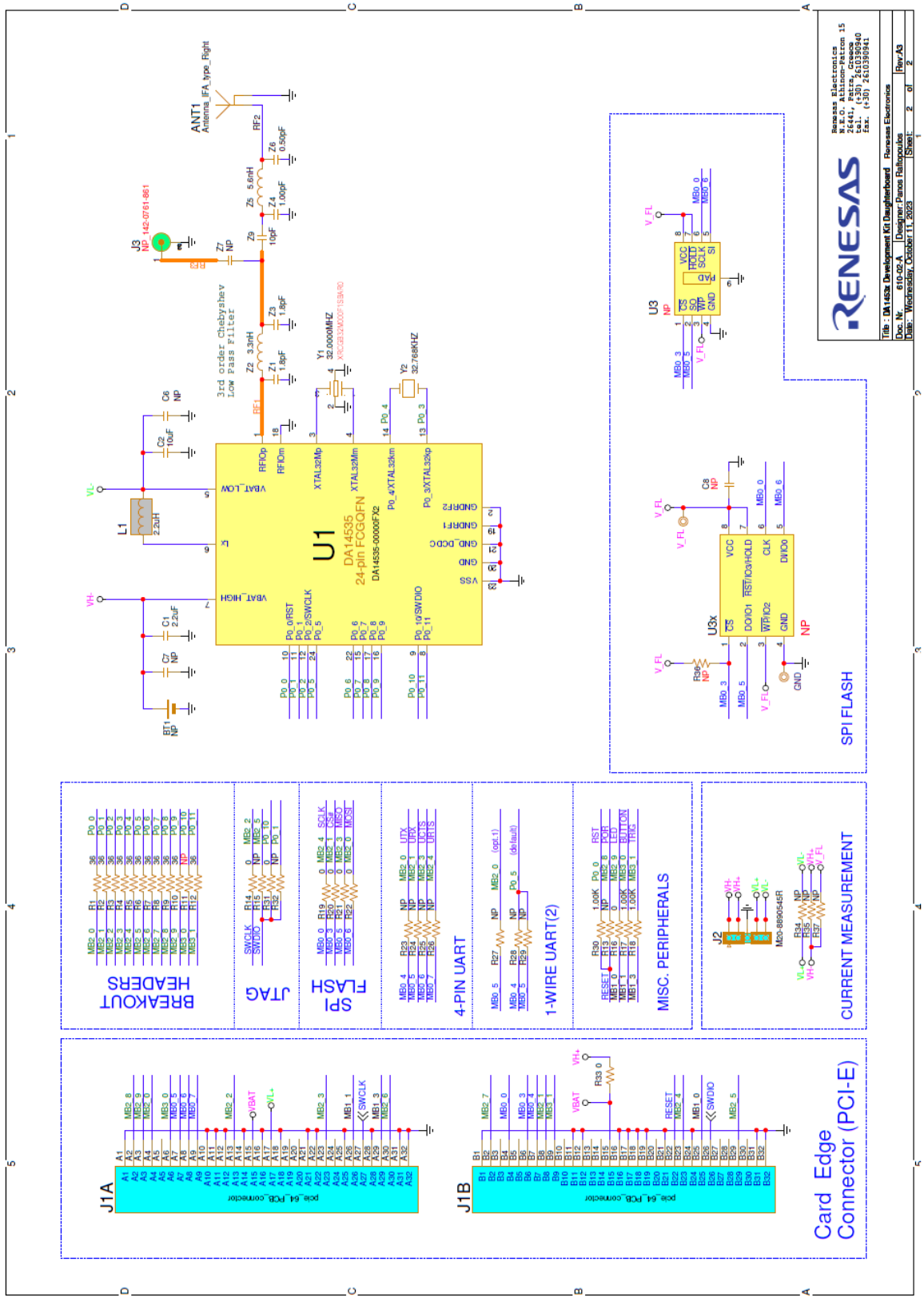

Figure 73. DA14535 Pro-DB (610-02-A)

A.3 DA14533 Pro daughterboard (610-05-A), schematic

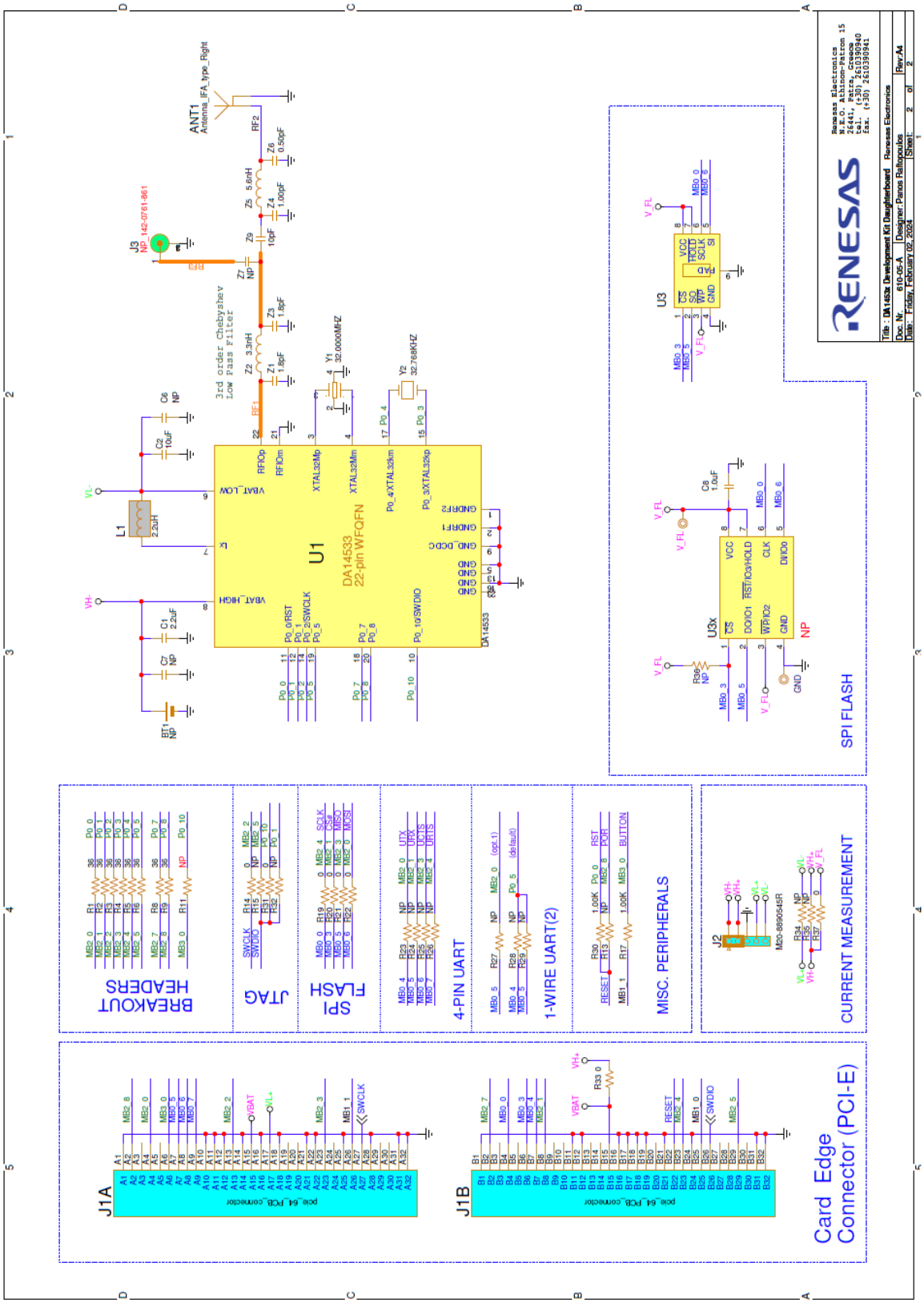

Figure 74. DA14533 Pro-DB (610-05-A)

A.4 PMM2, Power measurement module (500-29-E), schematic

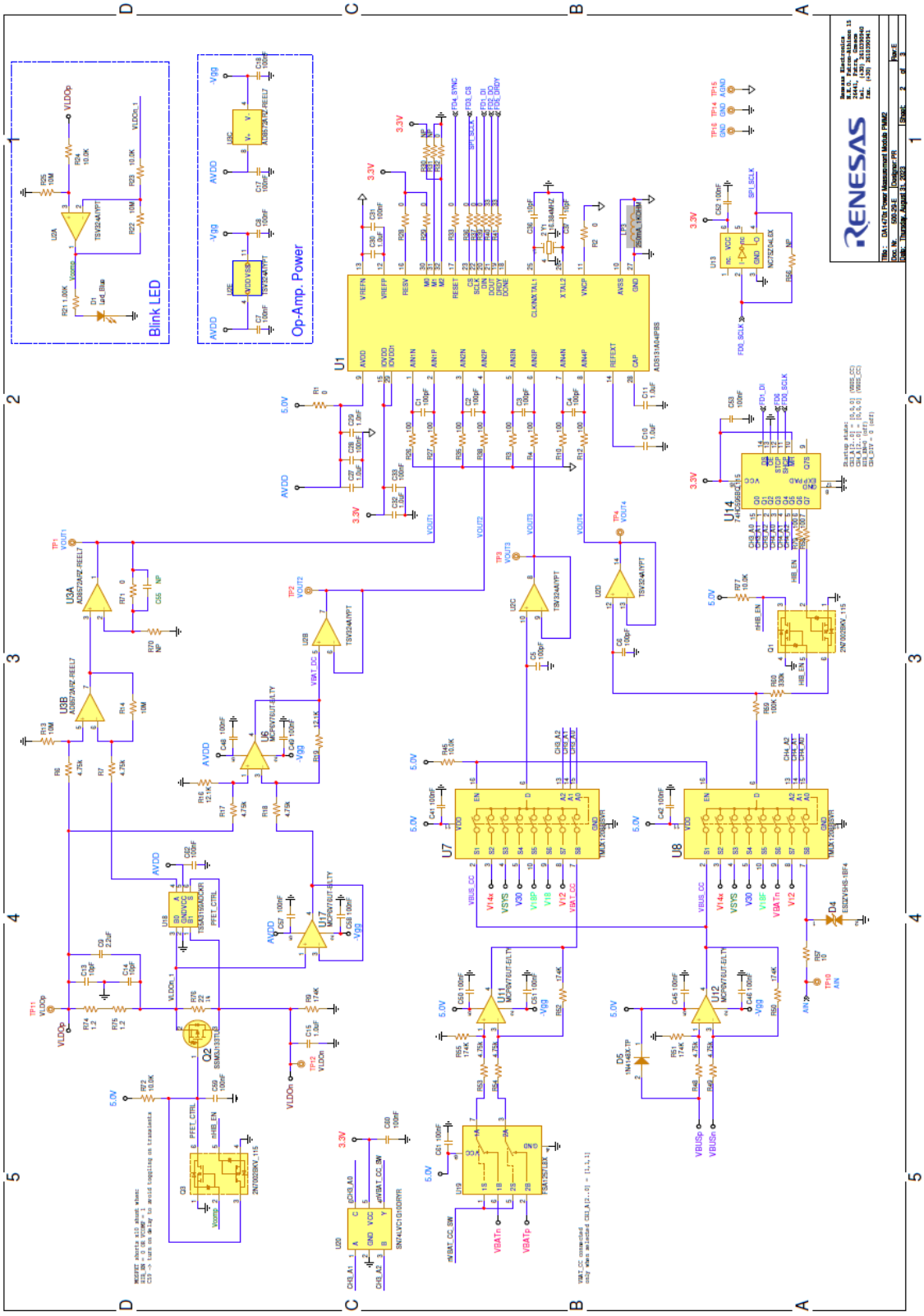

Figure 75. PMM2 (500-29-E), main circuit

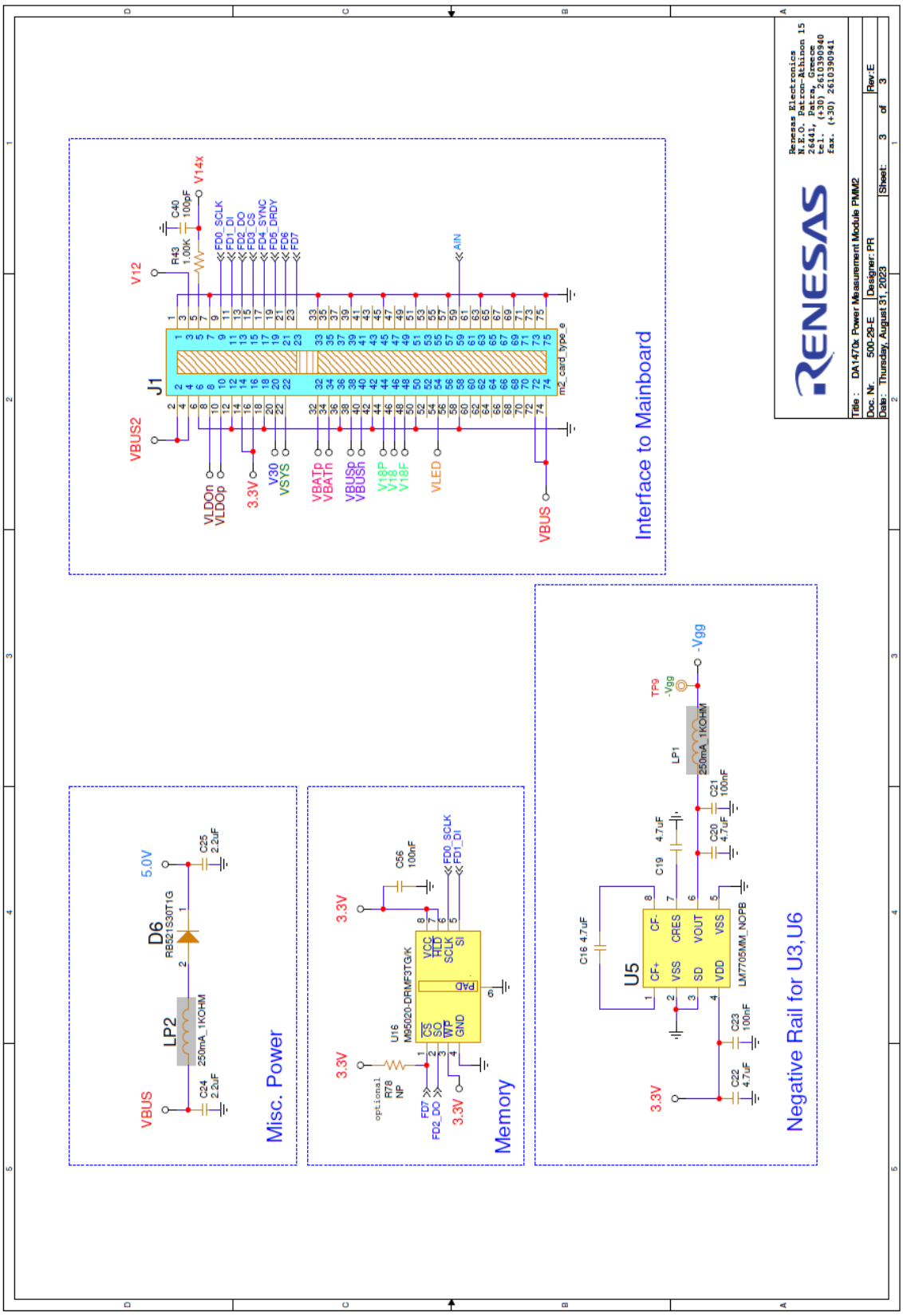

Figure 76. PMM2 (500-29-E), mating connector, power supply and EEPROM

Revision History

Revision	Date	Description
1.0	Feb 9, 2024	Initial version.

DA1453x Pro-Development Kit Hardware Description

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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