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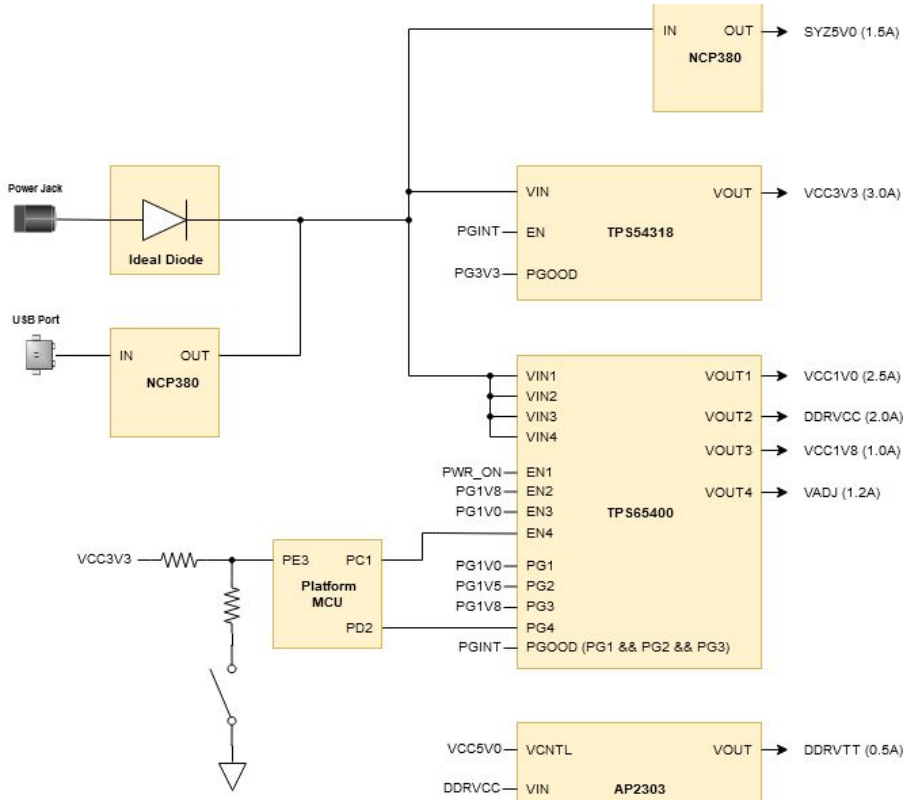
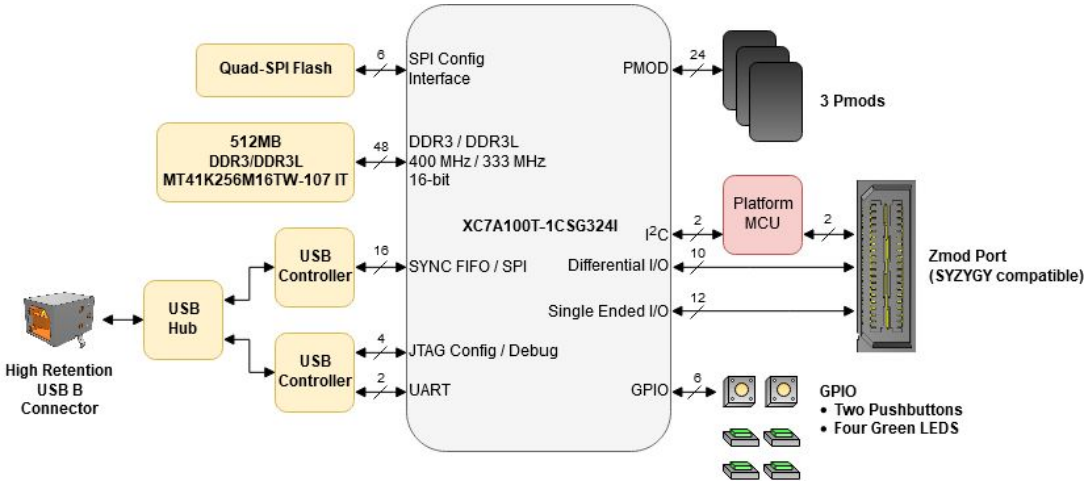
Power Tree



Block Diagram



DDRVCC Select

DDRVCC = 1.35V with switch in on position
DDRVCC = 1.5V with switch in off position

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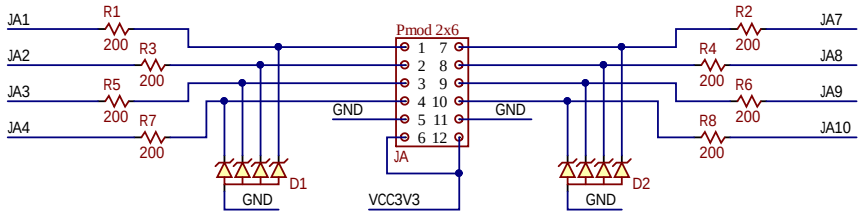
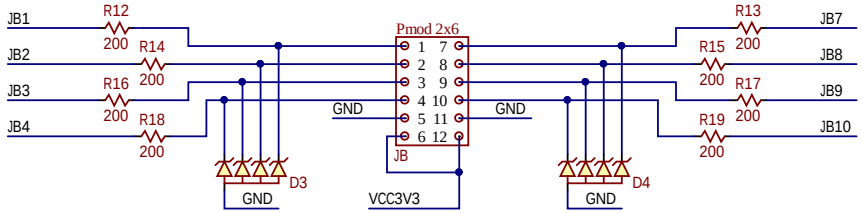
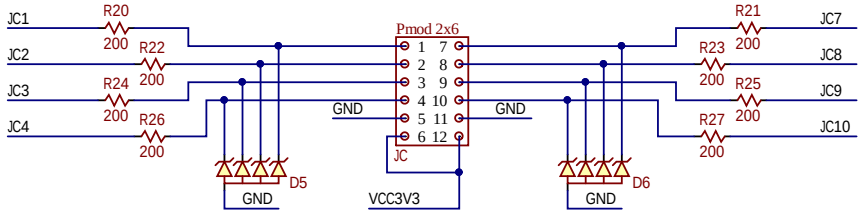
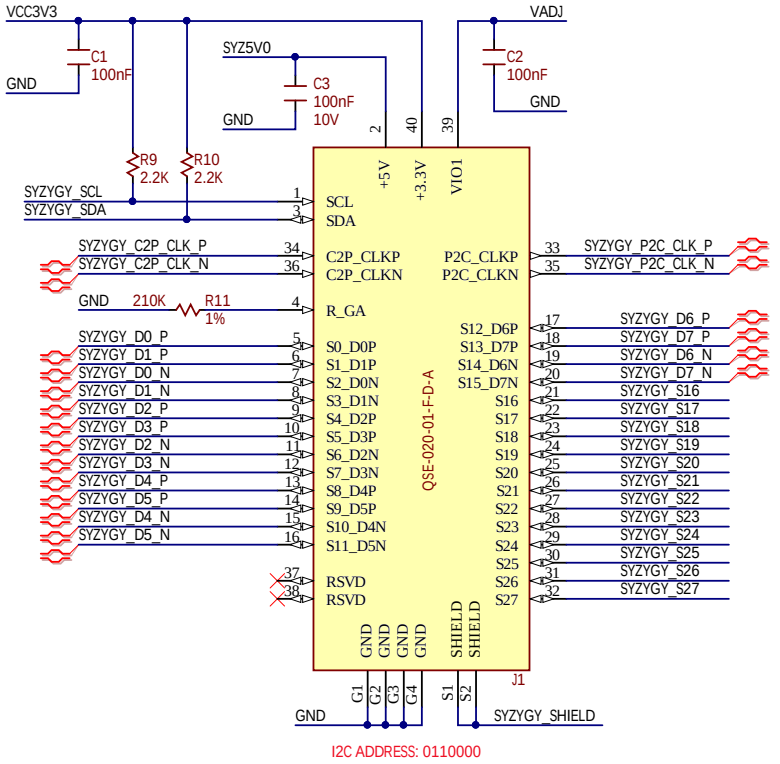
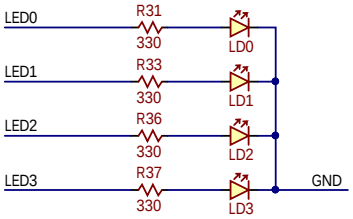


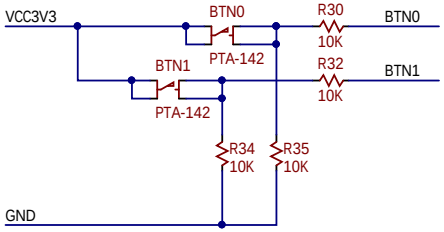


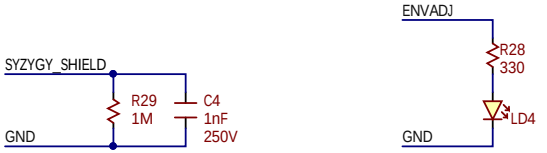




I2C ADDRESS: 0110000







Foot F1 Foot F2 Foot F3 Foot F4

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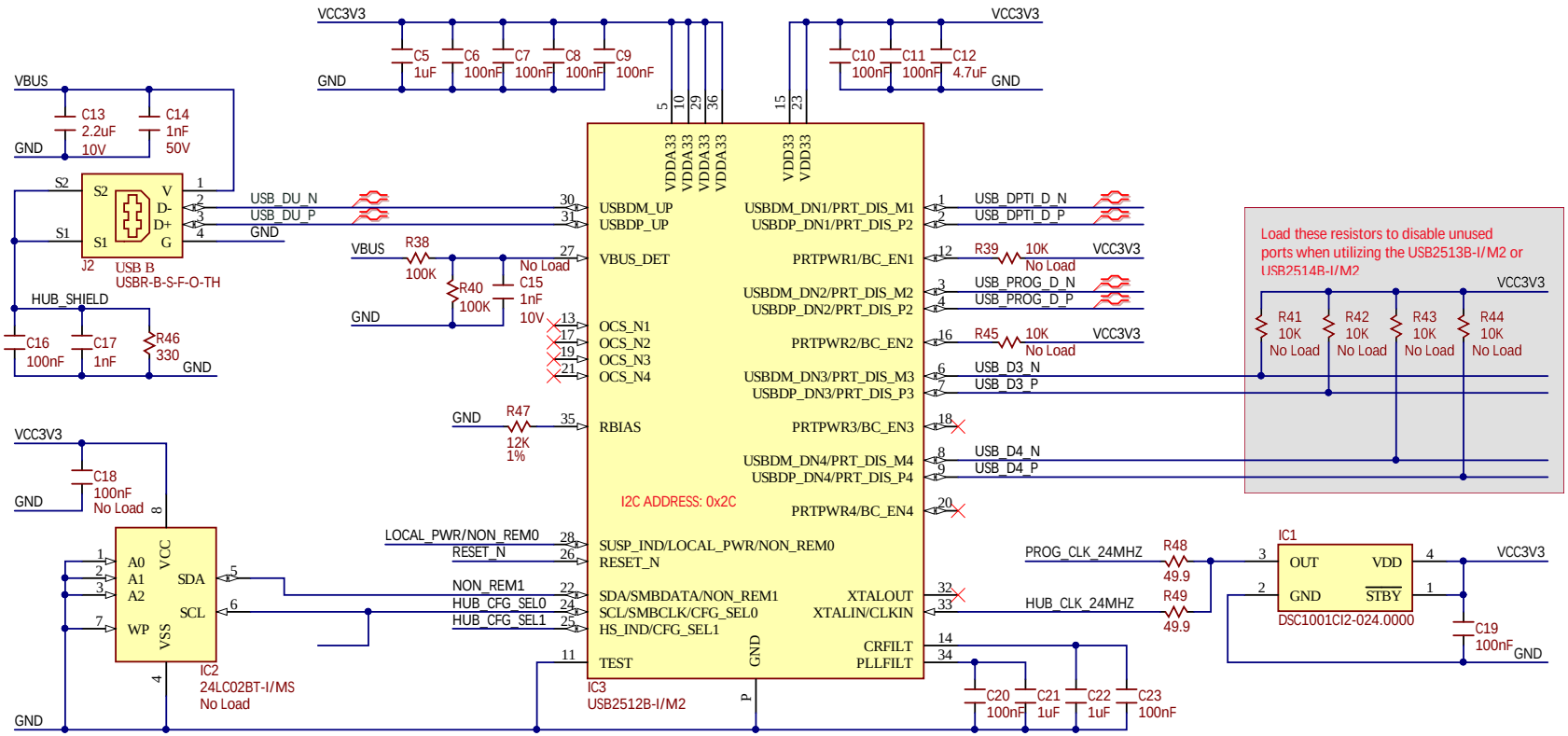
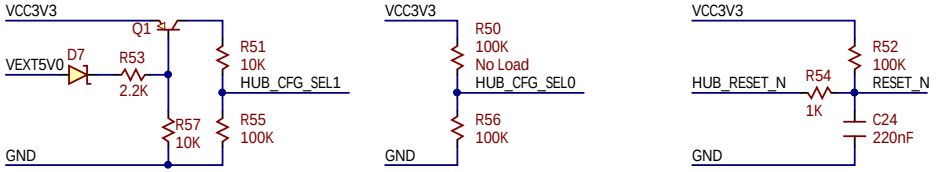
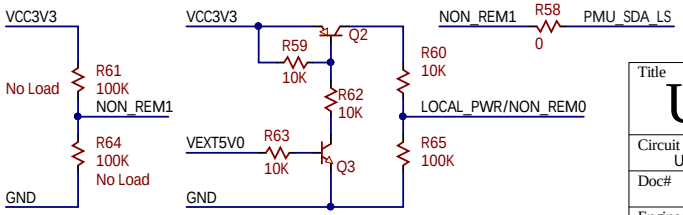


CFG_SEL1	CFG_SEL0	Hub Configuration
0	0	Default Configuration, Strapping Enabled, Self Powered
0	1	Configured via SMBus, Strapping disabled
1	0	Default Configuration, Strapping Enabled, Bus Powered
1	1	Configured via I2C EEPROM, Strapping disabled



Note: CFG_SELx and NON_REMx are sampled on the rising edge of RESET_N

NOM_REM1	NOM_REM0	Port Configuration
0	0	All ports are removable
0	1	Port 1 is non-removable
1	0	Ports 1 and 2 are non-removable
1	1	When available, ports 1, 2, and 3 are non-removable



Note: Use of LOCAL_PWR requires the hub to be configured via SMBus or EEPROM.

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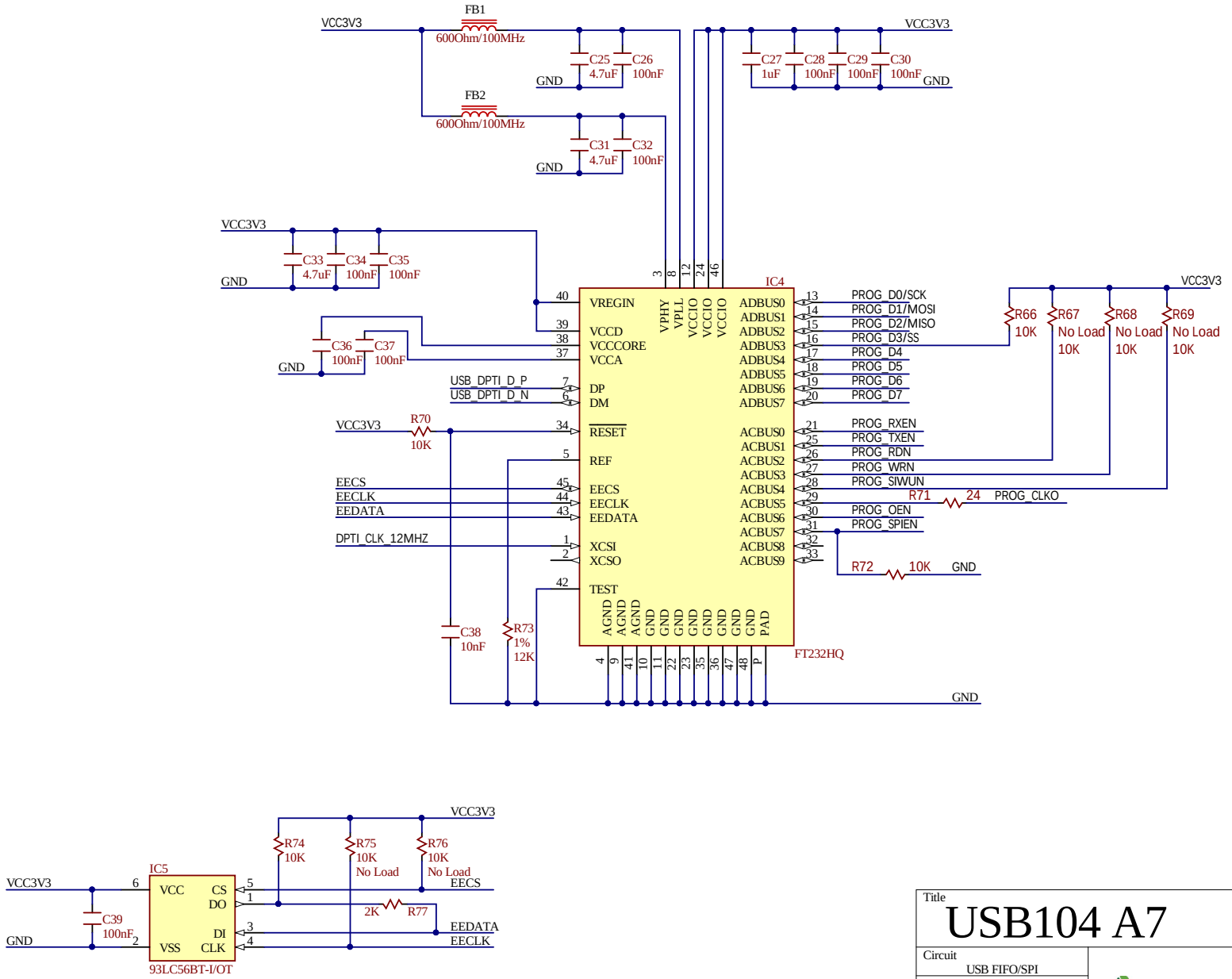

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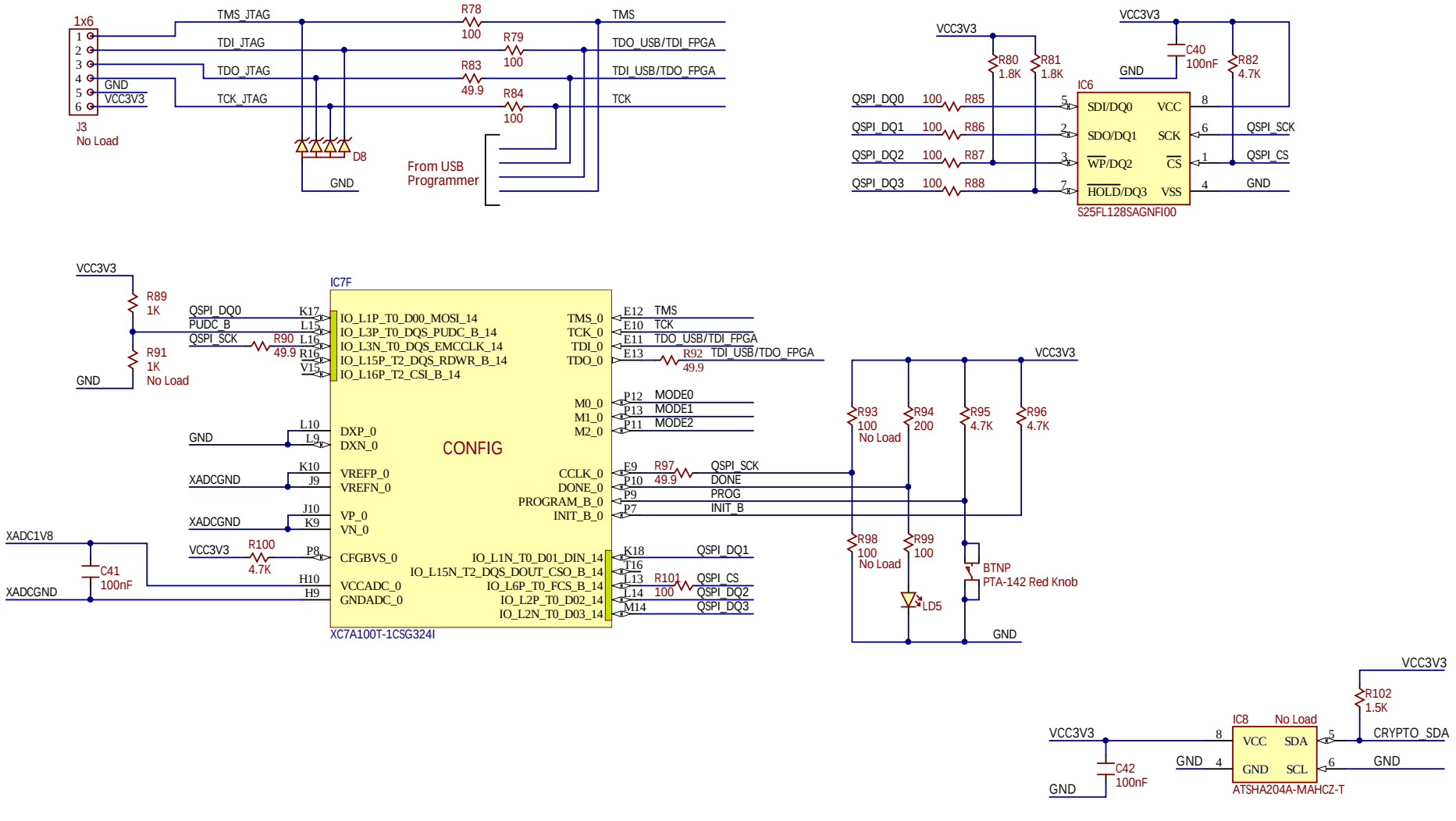

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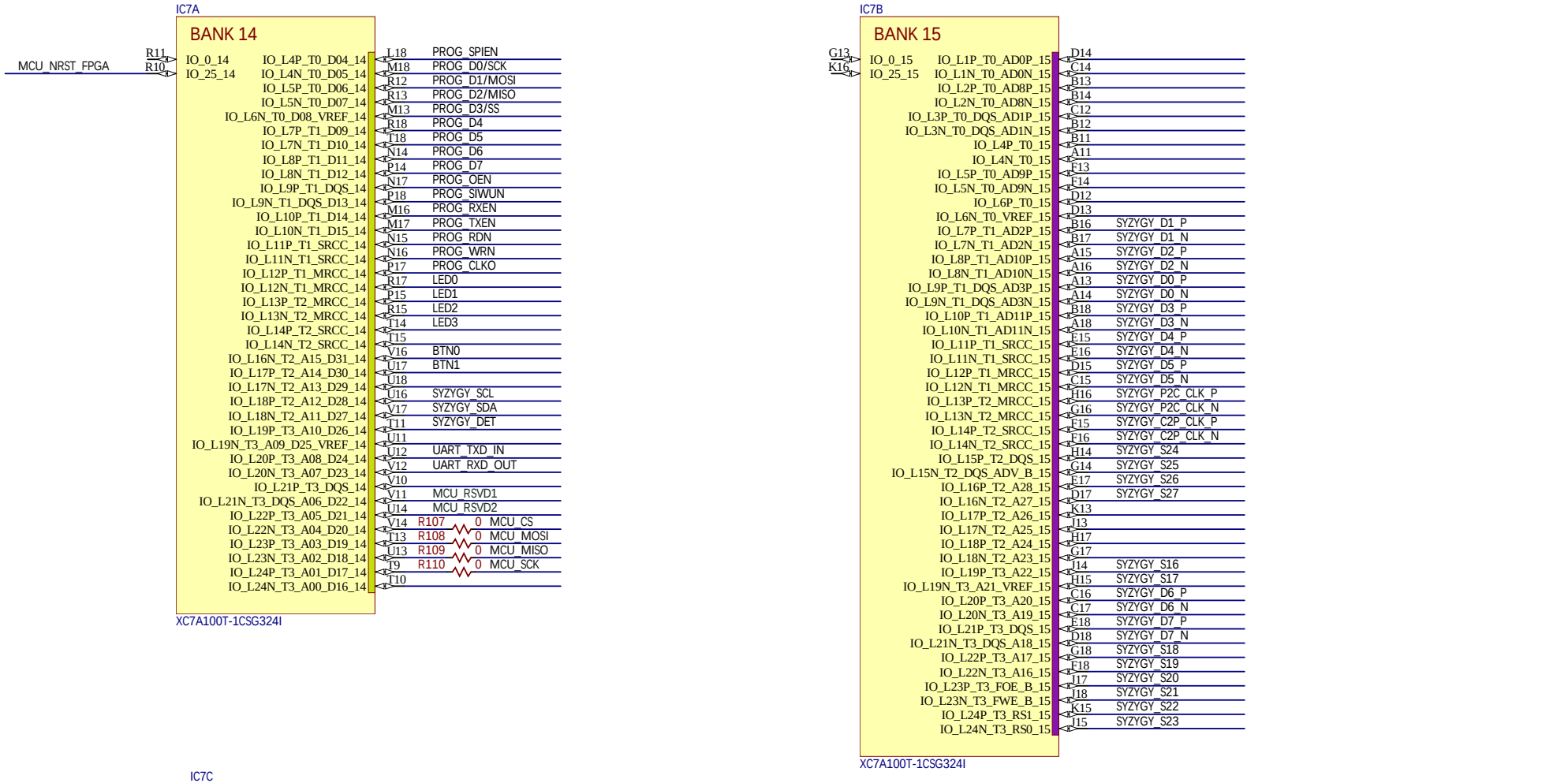

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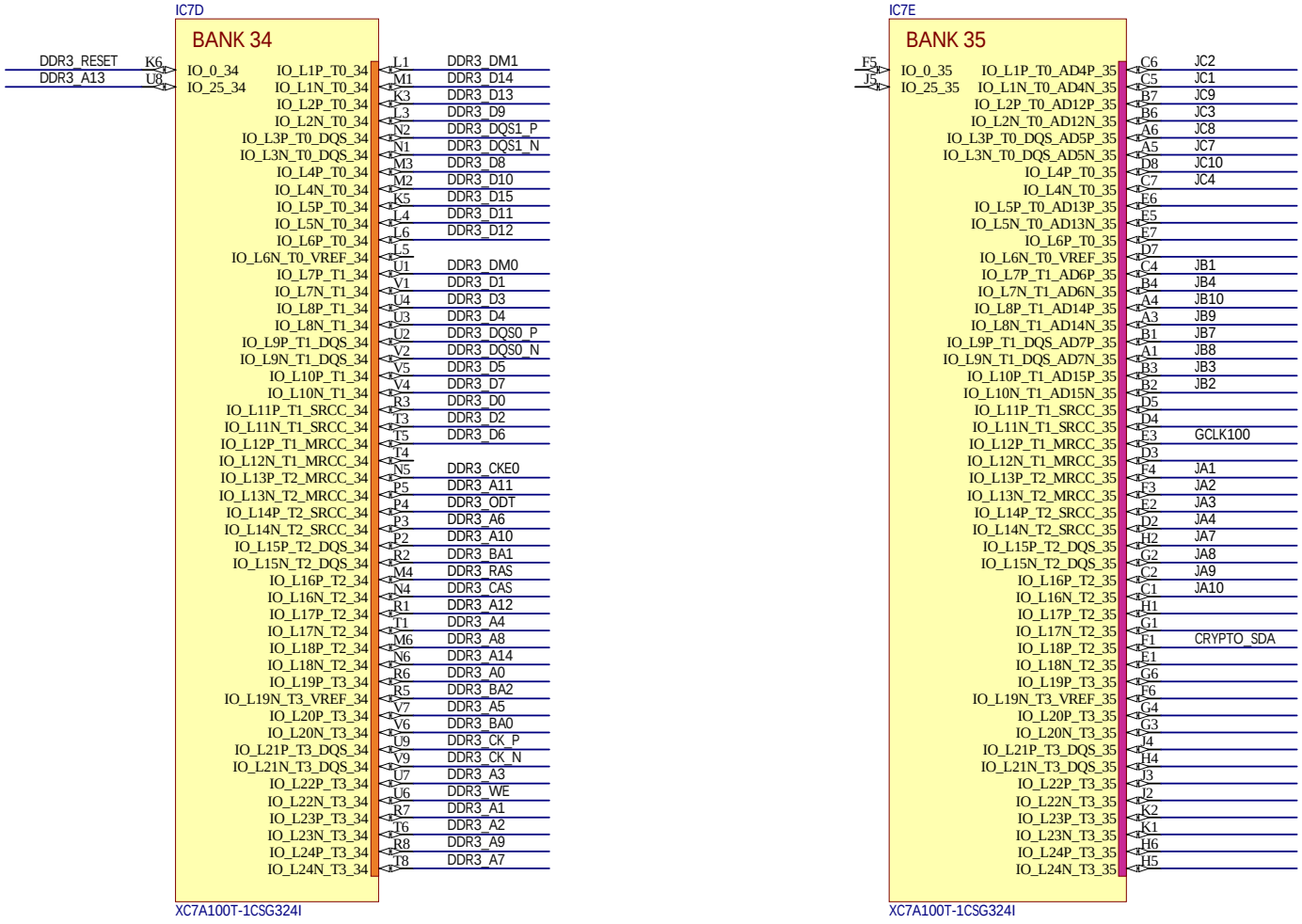

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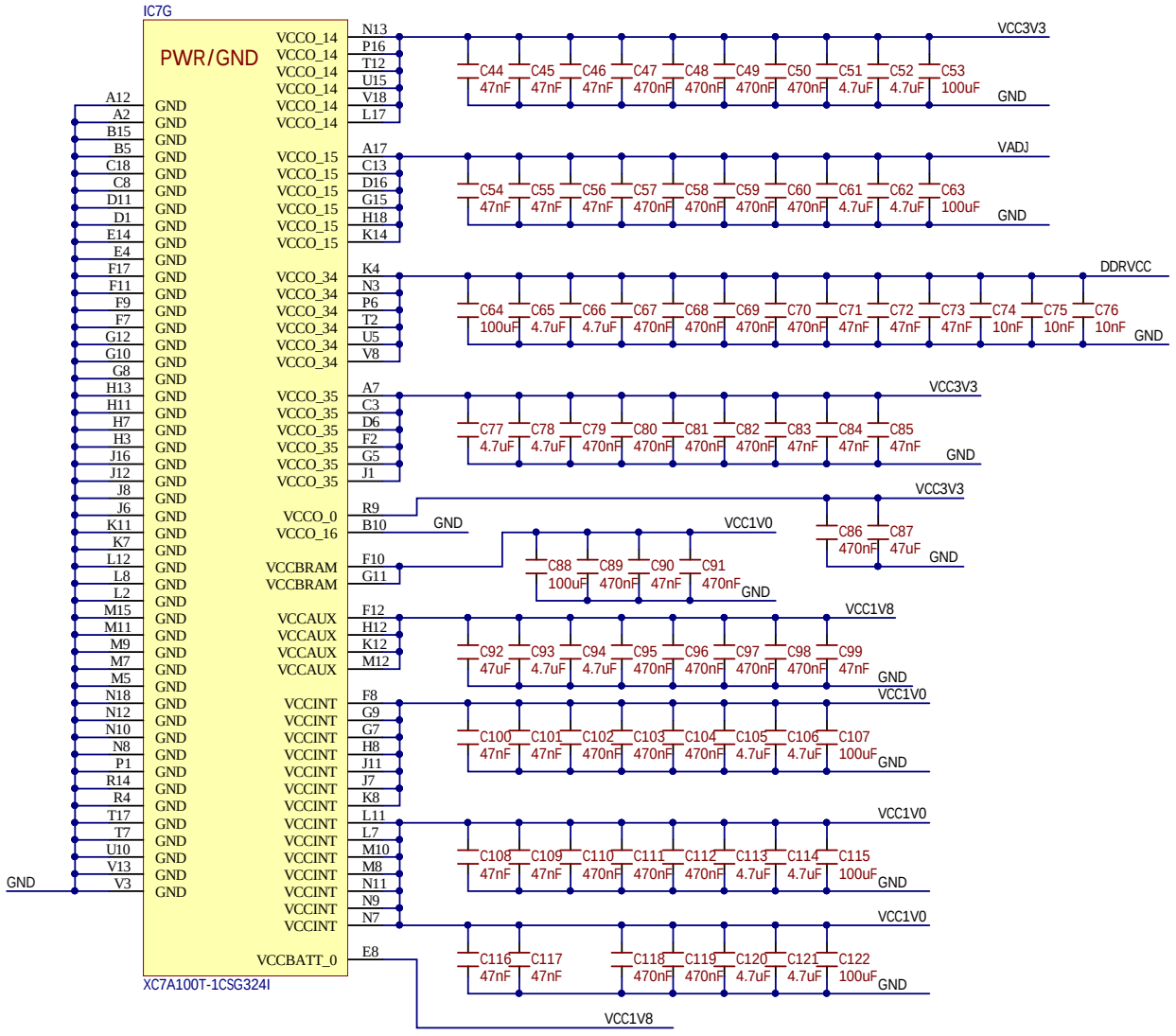

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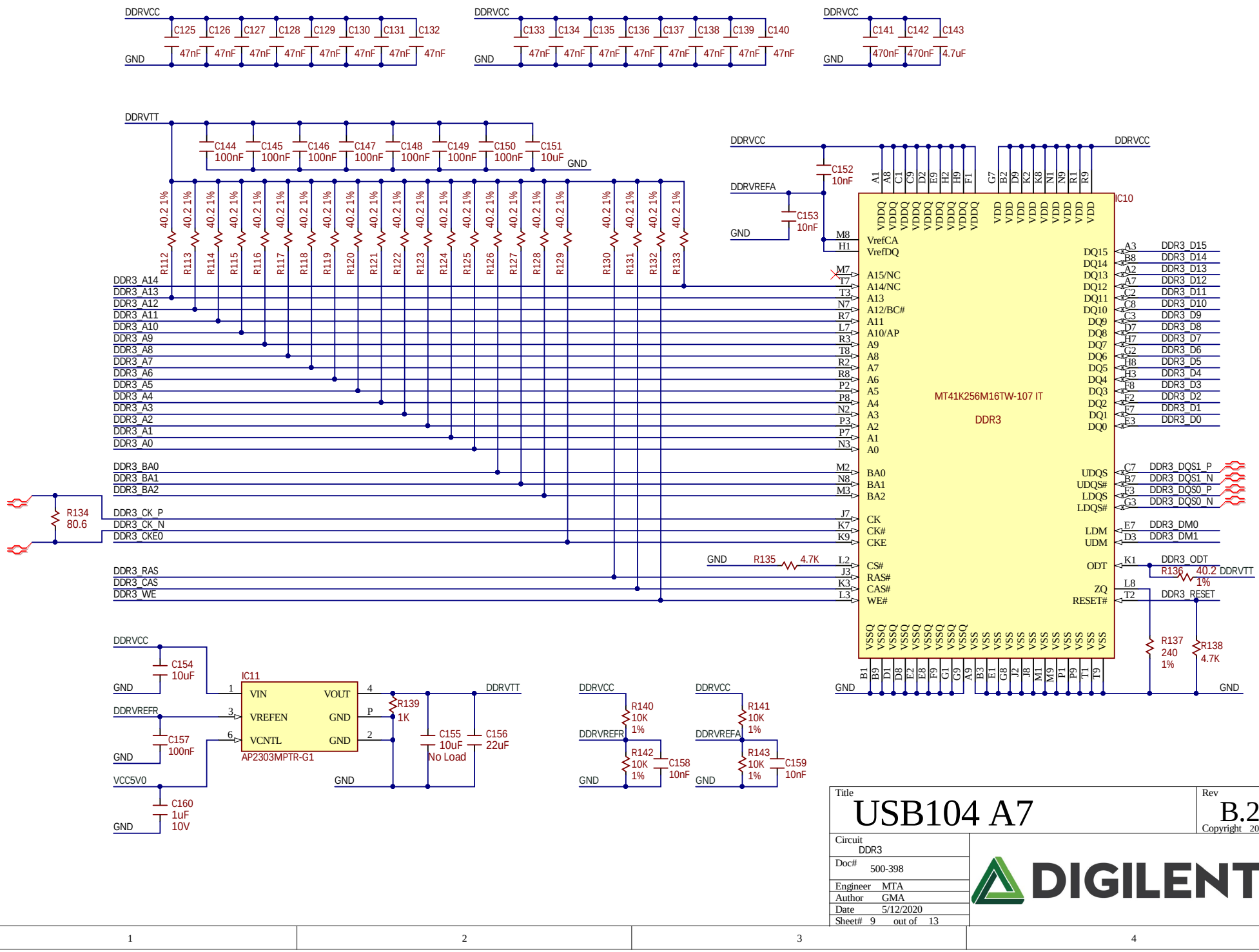
DDRVCC
C125 C126 C127 C128 C129 C130 C131 C132
GND
47nF 47nF 47nF 47nF 47nF 47nF 47nF 47nF
DDRVCC
C133 C134 C135 C136 C137 C138 C139 C140
GND
47nF 47nF 47nF 47nF 47nF 47nF 47nF 47nF
DDRVCC
C141 C142 C143
GND
470nF 470nF 4.7uF
DDRVTT
C144 100nF C145 100nF C146 100nF C147 100nF C148 100nF C149 100nF C150 100nF C151 10uF
GND
DDRVCC
C152 10nF
DDRVREFA
C153 10nF
GND
IC10
MT41K256M16TW-107 IT
DDR3
VrefCA
VrefDQ
A15/NC
A14/NC
A13
A12/BC#
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BA0
BA1
BA2
CK
CK#
CKE
CS#
RAS#
CAS#
WE#
ODT
ZQ
RESET#
UDQS
UDQS#
LDQS
LDQS#
LDM
UDM
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
DDR3_D15 DDR3_D14 DDR3_D13 DDR3_D12 DDR3_D11 DDR3_D10 DDR3_D9 DDR3_D8 DDR3_D7 DDR3_D6 DDR3_D5 DDR3_D4 DDR3_D3 DDR3_D2 DDR3_D1 DDR3_D0
DDR3_DQS1_P DDR3_DQS1_N DDR3_DQS0_P DDR3_DQS0_N
DDR3_DM0 DDR3_DM1
DDR3_ODT
R136 40.2 1%
DDRVTT
DDR3_RESET
R137 240 1%
R138 4.7K
GND
R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133
40.2 1%
DDR3_A14 DDR3_A13 DDR3_A12 DDR3_A11 DDR3_A10 DDR3_A9 DDR3_A8 DDR3_A7 DDR3_A6 DDR3_A5 DDR3_A4 DDR3_A3 DDR3_A2 DDR3_A1 DDR3_A0
DDR3_BA0 DDR3_BA1 DDR3_BA2
R134 80.6
DDR3_CK_P DDR3_CK_N DDR3_CKE0
GND R135 4.7K
DDR3_RAS DDR3_CAS DDR3_WE
DDRVCC
C154 10uF
GND
DDRVREFR
C157 100nF
GND
VCC5V0
C160 1uF 10V
GND
IC11
VIN VOUT
VREFEN GND
VCNTL GND
AP2303MPTR-G1
R139 1K
C155 10uF No Load
C156 22uF
DDRVTT
GND
DDRVCC
R140 10K 1%
DDRVREFR
R142 10K 1%
C158 10nF
GND
DDRVCC
R141 10K 1%
DDRVREFA
R143 10K 1%
C159 10nF
GND
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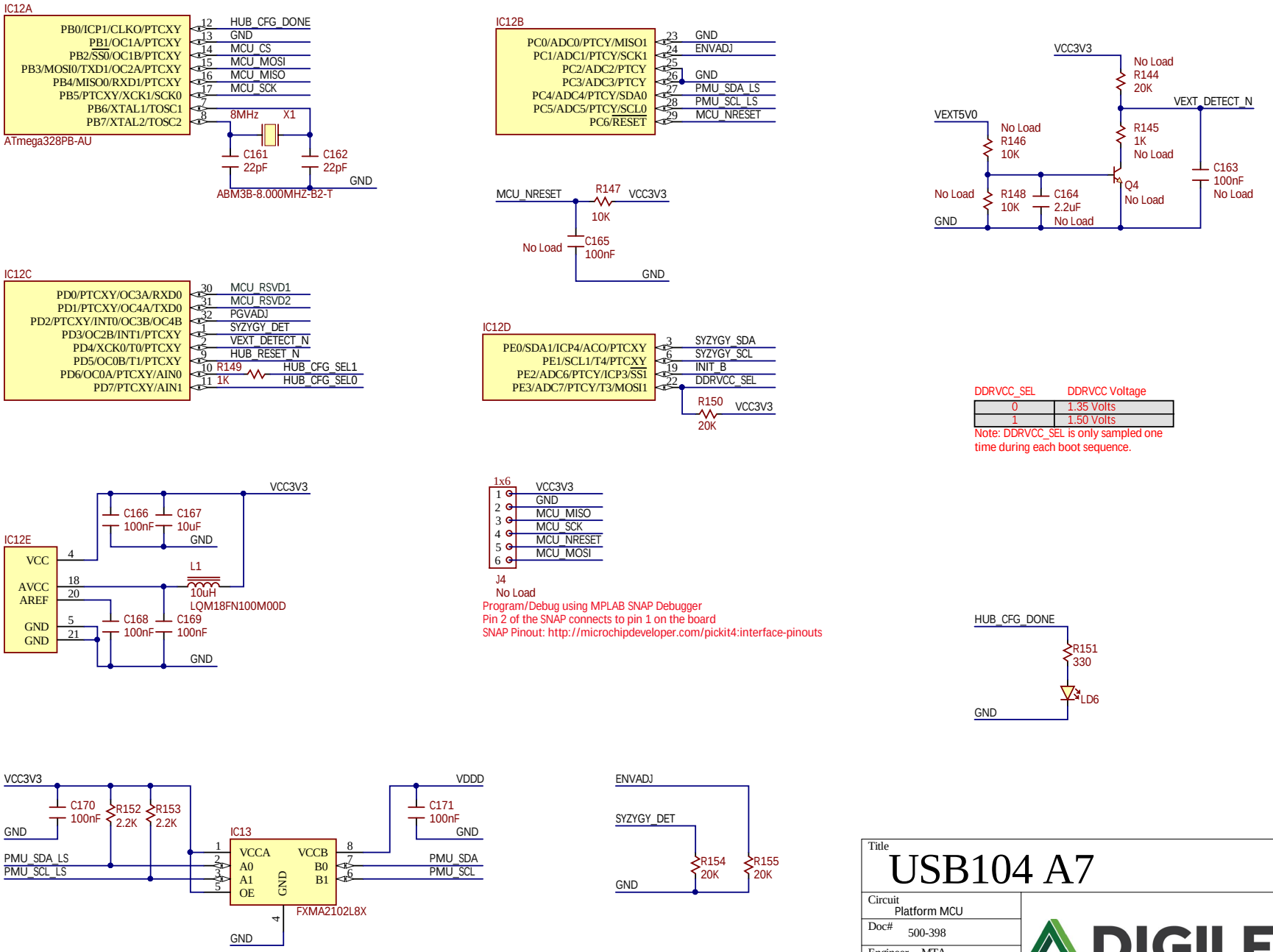
IC12A
PB0/ICP1/CLKO/PTCXY
PB1/OC1A/PTCXY
PB2/SS0/OC1B/PTCXY
PB3/MOSI0/TXD1/OC2A/PTCXY
PB4/MISO0/RXD1/PTCXY
PB5/PTCXY/XCK1/SCK0
PB6/XTAL1/TOSC1
PB7/XTAL2/TOSC2
12 HUB_CFG_DONE
13 GND
14 MCU_CS
15 MCU_MOSI
16 MCU_MISO
17 MCU_SCK
8MHz
X1
C161 22pF
C162 22pF
GND
ATmega328PB-AU
ABM3B-8.000MHZ-B2-T
IC12B
PC0/ADC0/PTCY/MISO1
PC1/ADC1/PTCY/SCK1
PC2/ADC2/PTCY
PC3/ADC3/PTCY
PC4/ADC4/PTCY/SDA0
PC5/ADC5/PTCY/SCL0
PC6/RESET
23 GND
24 ENVADJ
25
26 GND
27 PMU_SDA_LS
28 PMU_SCL_LS
29 MCU_NRESET
MCU_NRESET
R147 10K
VCC3V3
C165 100nF
No Load
GND
VCC3V3
No Load R144 20K
VEXT_DETECT_N
VEXT5V0
No Load R146 10K
R145 1K No Load
C163 100nF No Load
Q4 No Load
No Load R148 10K
C164 2.2uF No Load
GND
IC12C
PD0/PTCXY/OC3A/RXD0
PD1/PTCXY/OC4A/TXD0
PD2/PTCXY/INT0/OC3B/OC4B
PD3/OC2B/INT1/PTCXY
PD4/XCK0/T0/PTCXY
PD5/OC0B/T1/PTCXY
PD6/OC0A/PTCXY/AIN0
PD7/PTCXY/AIN1
30 MCU_RSVD1
31 MCU_RSVD2
32 PGVADJ
1 SYZYGY_DET
2 VEXT_DETECT_N
9 HUB_RESET_N
10 R149 HUB_CFG_SEL1
11 1K HUB_CFG_SEL0
IC12D
PE0/SDA1/ICP4/ACO/PTCXY
PE1/SCL1/T4/PTCXY
PE2/ADC6/PTCY/ICP3/SS1
PE3/ADC7/PTCY/T3/MOSI1
3 SYZYGY_SDA
6 SYZYGY_SCL
19 INIT_B
22 DDRVCC_SEL
R150 20K
VCC3V3
DDRVCC_SEL
DDRVCC Voltage
0
1.35 Volts
1
1.50 Volts
Note: DDRVCC_SEL is only sampled one time during each boot sequence.
IC12E
VCC
AVCC
AREF
GND
GND
4
18
20
5
21
C166 100nF
C167 10uF
GND
L1 10uH LQM18FN100M00D
C168 100nF
C169 100nF
GND
VCC3V3
1x6
1 VCC3V3
2 GND
3 MCU_MISO
4 MCU_SCK
5 MCU_NRESET
6 MCU_MOSI
J4
No Load
Program/Debug using MPLAB SNAP Debugger
Pin 2 of the SNAP connects to pin 1 on the board
SNAP Pinout: http://microchipdeveloper.com/pickit4:interface-pinouts
HUB_CFG_DONE
R151 330
LD6
GND
VCC3V3
C170 100nF
R152 2.2K
R153 2.2K
GND
PMU_SDA_LS
PMU_SCL_LS
IC13
VCCA
A0
A1
OE
GND
VCCB
B0
B1
1
2
3
5
8
7
6
4
FXMA2102L8X
VDDD
C171 100nF
GND
PMU_SDA
PMU_SCL
GND
ENVADJ
SYZYGY_DET
R154 20K
R155 20K
GND
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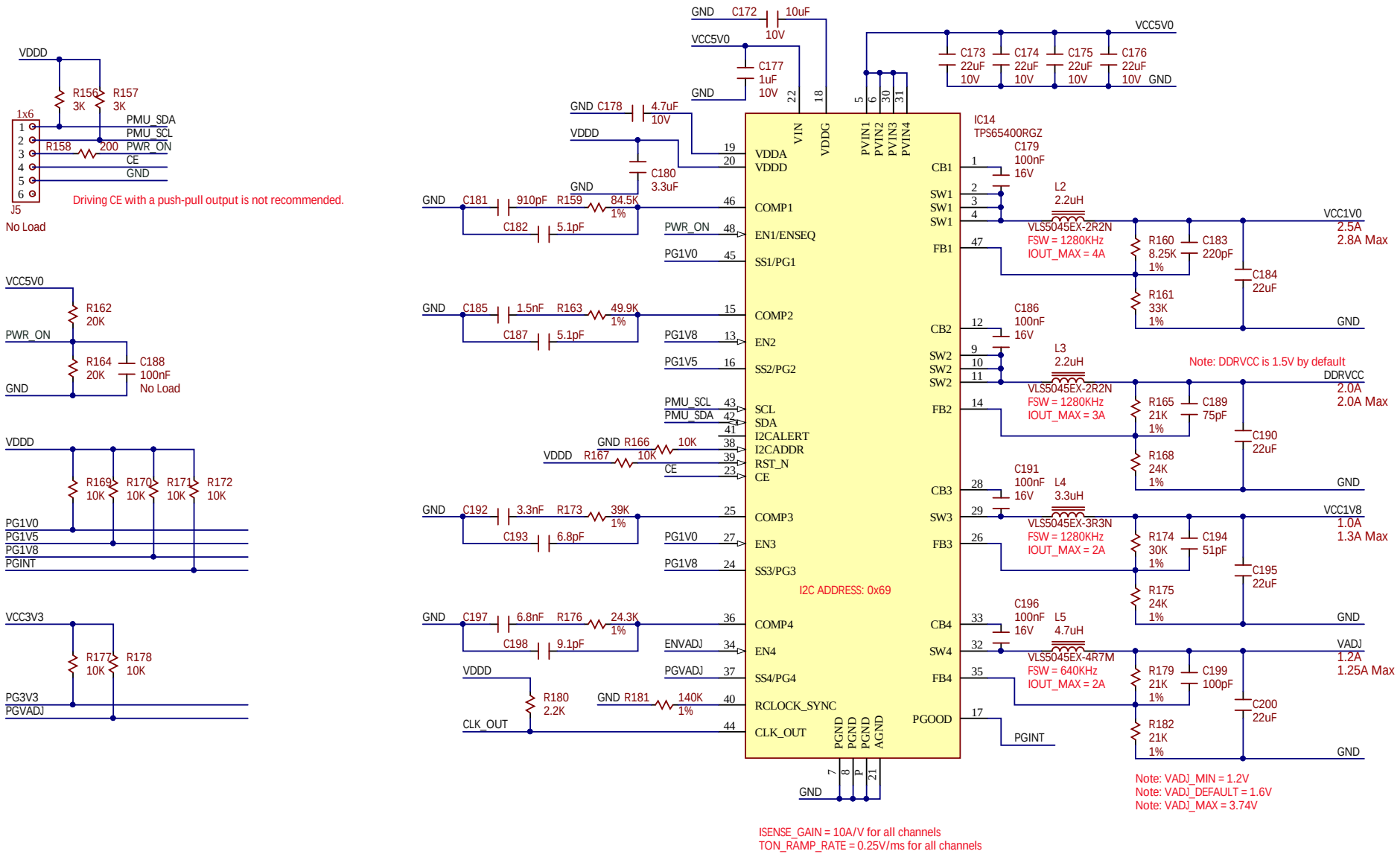

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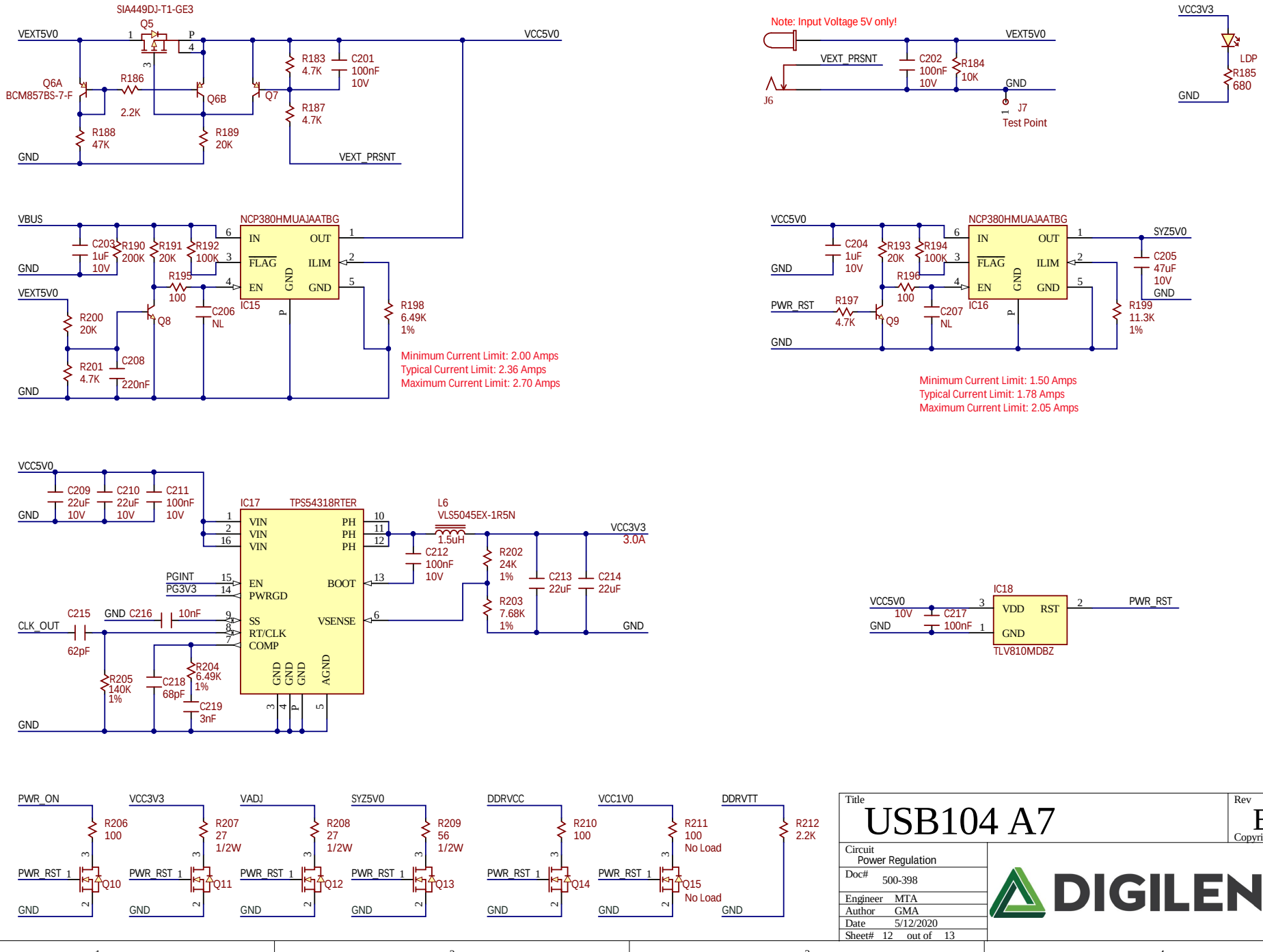

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