60V Low I_Q No-Opto Isolated Flyback Controller

FEATURES

- **Wide Input Voltage Range: 4.5V to 60V**
- **Low Quiescent Current**
  - **120µA in Sleep Mode**
  - **390µA in Active Mode**
- **Quasi-Resonant Boundary Mode Operation at Heavy Load**
- Low Ripple Burst Mode® Operation at Light Load
- Minimum Load < 0.5% (Typ) of Full Output
- V_{OUT} Set with a Single External Resistor
- 8V Gate Drive for External NFET
- No Transformer Third Winding or Opto-Isolator Required for Regulation
- Accurate EN/UVLO Threshold and Hysteresis
- Internal Compensation and Soft-Start
- Output Short-Circuit Protection
- 6-Lead TSOT-23 Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Isolated Telecom, Automotive, Industrial, Medical Power Supplies
- Isolated Auxiliary/Housekeeping Power Supplies

DESCRIPTION

The LT®8306 is a micropower isolated flyback controller in a 6-lead ThinSOT™ package. By sampling the isolated output voltage directly from the primary-side flyback waveform, the part requires no third winding or opto-isolator for regulation. The output voltage is programmed with a single external resistor. Internal compensation and soft-start further reduce external component count. Boundary mode operation provides a small magnetic solution with excellent load regulation. Low ripple burst mode operation maintains high efficiency at light load while minimizing the output voltage ripple. The LT8306 drives a low side N-channel power MOSFET with 8V gate drive.

The LT8306 has a wide input voltage range of 4.5V to 60V. The high level of integration and the use of boundary and low ripple burst modes result in a simple-to-use, low component count, and high efficiency application solution for isolated power delivery.

TYPICAL APPLICATION

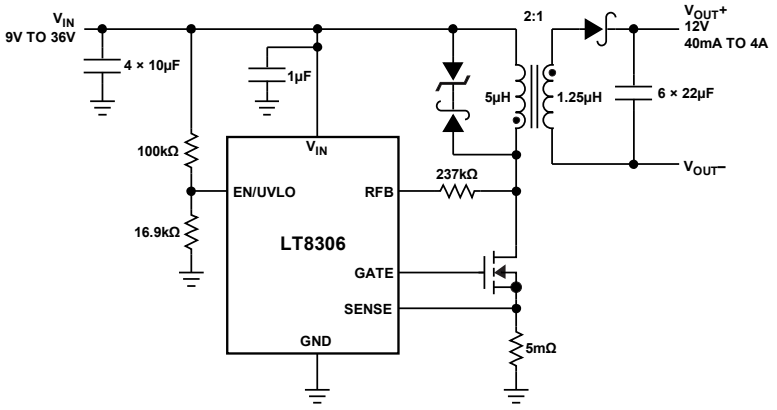

Figure 1. 9V to 36V Input, 12V/4A Output Isolated Flyback Converter

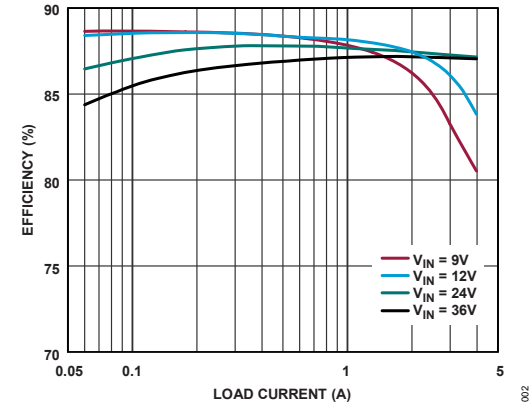

Figure 2. Efficiency vs. Load Current

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REVISION HISTORY

Revision Number	Revision Date	Nature of Change	Page Number
Rev 0	1/23	—	—
Rev A	7/23	Updated Ordering Guide	28

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C [3] V_{IN} = 12V, EN/UVLO = V_{IN}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range	V_{IN}	-40°C ≤ T_J ≤ 150°C	4.5		60	V
V_{IN} Quiescent Current	I_Q	$V_{EN/UVLO}$ = 0.2V		1	2	µA
		In Sleep Mode (Gate Off)		120		
		In Active Mode (Gate On)		390		
EN/UVLO Shutdown Threshold	$V_{EN/UVLO}$		0.2	0.55	0.9	V
EN/UVLO Enable Threshold	$V_{EN/UVLO}$	Falling	1.204	1.228	1.248	V
EN/UVLO Enable Hysteresis	$V_{EN/UVLO}$			18		mV
EN/UVLO Hysteresis Current	I_{HYS}	$V_{EN/UVLO}$ = 1.1V	2.1	2.5	2.9	µA
		$V_{EN/UVLO}$ = 1.3V	-0.1	0	0.1	
Minimum Switching Frequency	f_{MIN}		7.5	10	12.5	kHz
Maximum Switching Frequency	f_{MAX}		360	400	440	kHz
Minimum Switch-On Time	$t_{ON(MIN)}$			200		ns
Minimum Switch-Off Time	$t_{OFF(MIN)}$			630		ns
SENSE Maximum Current Threshold	$V_{SENSE(MAX)}$		85	95	105	mV
SENSE Minimum Current Threshold	$V_{SENSE(MIN)}$		9	17	25	mV
SENSE Overcurrent Threshold	$V_{SENSE(OVER)}$			160		mV
SENSE Pin Current	I_{SENSE}	V_{SENSE} = 0V, Out of Pin		35		µA
GATE Drive Voltage	V_{GATE}		7.5	8	8.5	V
GATE Rise Time	$t_{GATE(RISE)}$	C_L = 3.3nF, 10% to 90%		60		ns
GATE Fall Time	$t_{GATE(FALL)}$	C_L = 3.3nF, 90% to 10%		30		ns
R_{FB} Regulation Current	I_{RFB}	-40°C ≤ T_J ≤ 150°C	97.5	100	102.5	µA
R_{FB} Regulation Current Line Regulation	I_{RFB}	4.5V ≤ V_{IN} ≤ 60V		0.02	0.1	%

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}	-0.3V to 60V
EN/UVLO	-0.3V to V_{IN}
R_{FB} Current [1]	-2mA to 200µA
GATE [2]	-0.3V to 10V
SENSE	-0.3V to 0.3V
Operating Junction Temperature Range [3, 4] LT8306R	-40°C to 150°C
Storage Temperature Range	-65°C to 150°C

1 Do not force any voltage on the R_{FB} pin.

2 Do not apply a positive or negative voltage source to the GATE pin or permanent damage may occur.

3 The LT8306R is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

4 The LT8306R includes overtemperature protection to protect the device during momentary overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

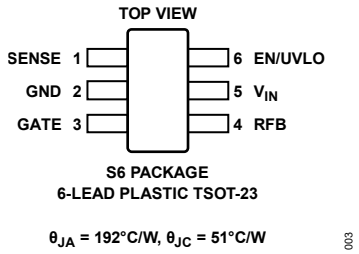

Figure 3. Pin Diagram

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	SENSE	Current-Sense Comparator Input. Kelvin connect this pin to the positive terminal of the current-sense resistor in the source of the bottom MOSFET. Connect the negative terminal of the current-sense resistor to the ground plane close to the chip.
2	GND	Ground. Tie this pin directly to the ground plane.
3	GATE	MOSFET Gate Drive. Drives the gate of N-channel MOSFET with a voltage swing from the ground to an internal 8V supply voltage.
4	R_{FB}	Input Pin for External Feedback Resistor. Connect a resistor from this pin to the transformer primary SW node. The ratio of the R_{FB} resistor to an internal 10k resistor, times a trimmed 1.0V reference voltage, determines the output voltage (plus the effect of any non-unity transformer turns ratio). Minimize trace area at this pin.
5	V_{IN}	Input Supply. The V_{IN} pin supplies current to the internal circuitry and serves as a reference voltage for the feedback circuitry connected to the R_{FB} pin. Locally bypass this pin to the ground with a ceramic capacitor.
6	EN/UVLO	Enable/Undervoltage Lockout. The EN/UVLO pin is used to enable the LT8306. Pull the pin below 0.2V to shut down the LT8306. This pin has an accurate 1.228V threshold and can be used to program a V_{IN} undervoltage lockout (UVLO) threshold using a resistor divider from V_{IN} to the ground. A 2.5µA hysteresis current allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

TYPICAL PERFORMANCE CHARACTERISTICS

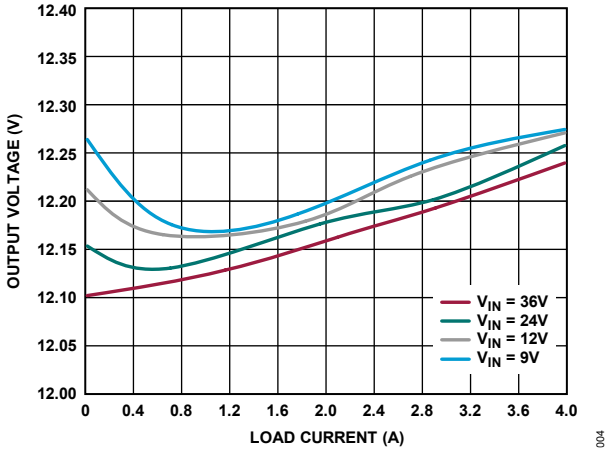

Figure 4. Output Load and Line Regulation

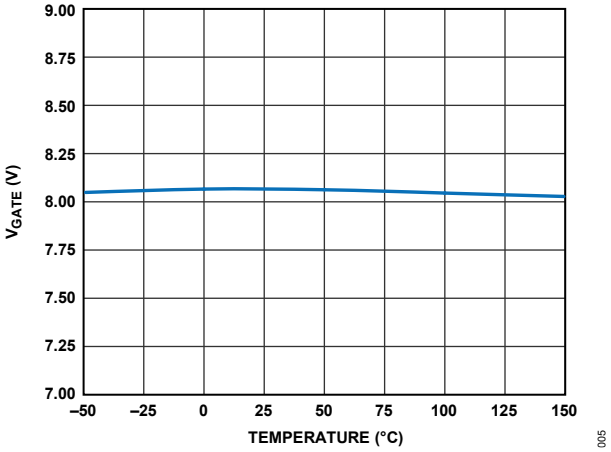

Figure 5. GATE Drive Voltage

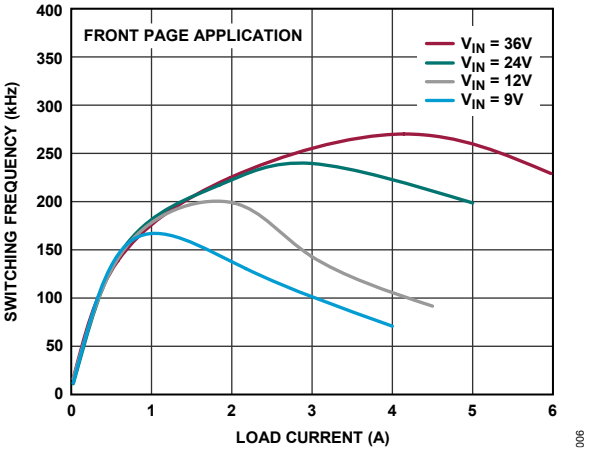

Figure 6. Switching Frequency vs. Load Current

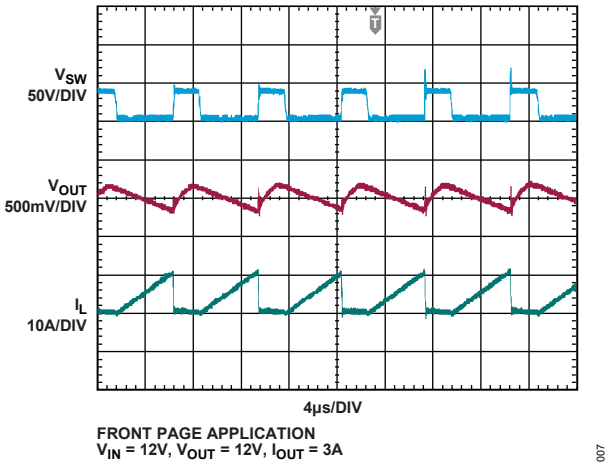

Figure 7. Boundary Mode Waveforms

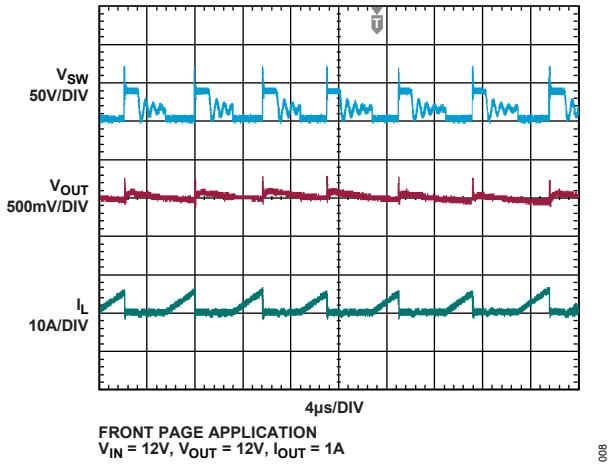

Figure 8. Discontinuous Mode Waveforms

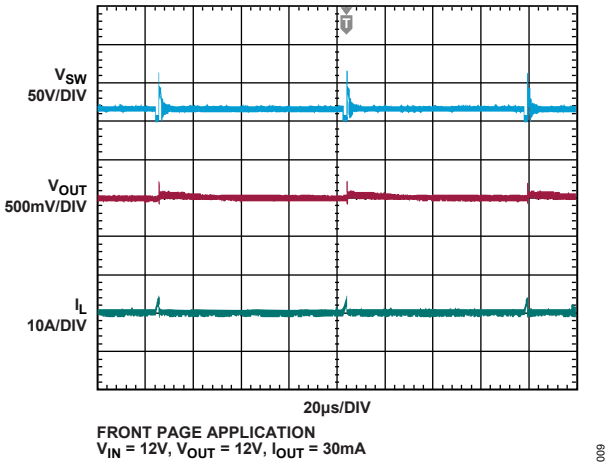

Figure 9. Burst Mode Waveforms

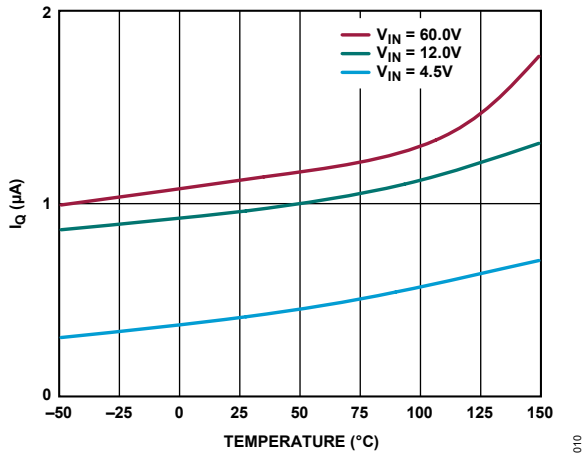

Figure 10. V_{IN} Shutdown Current

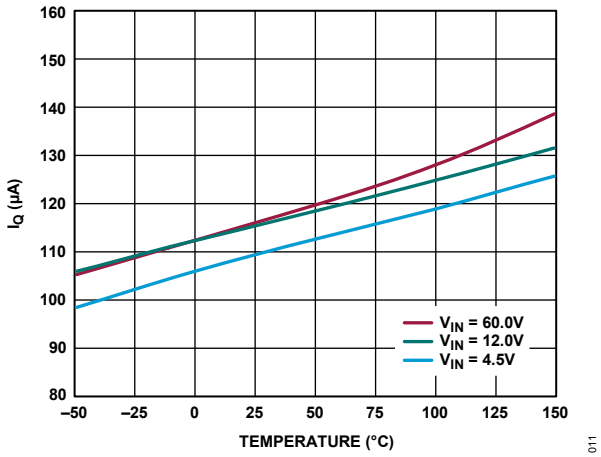

Figure 11. V_{IN} Quiescent Current, Sleep Mode

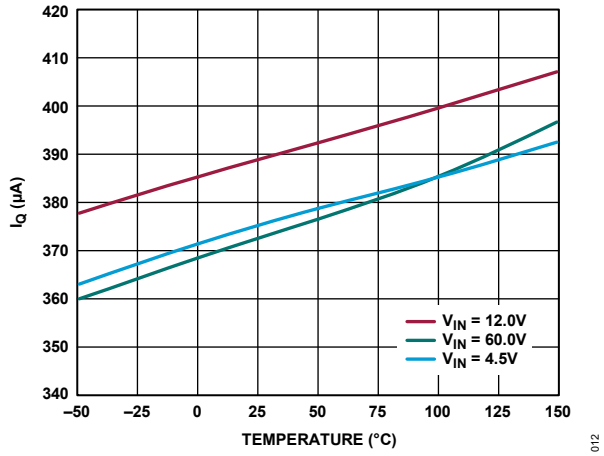

Figure 12. V_{IN} Quiescent Current, Active Mode

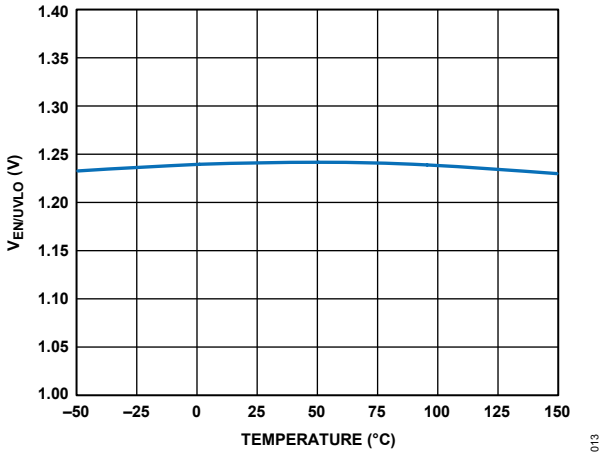

Figure 13. EN/UVLO Enable Threshold

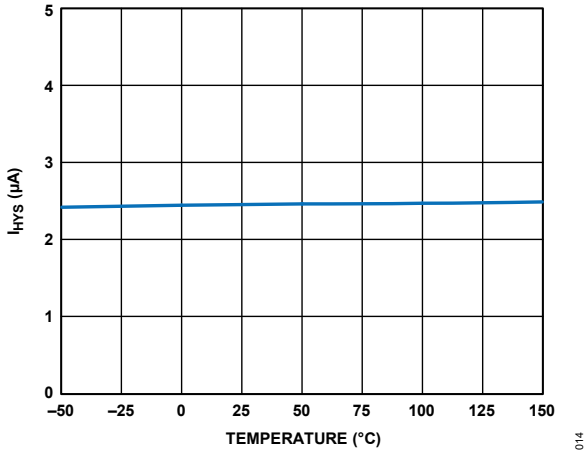

Figure 14. EN/UVLO Hysteresis Current

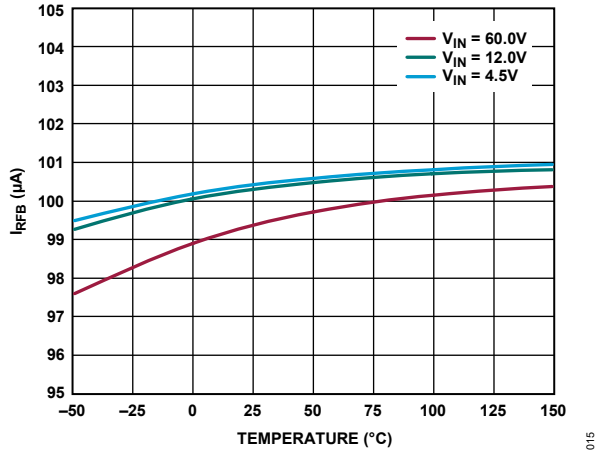

Figure 15. R_{FB} Regulation Current

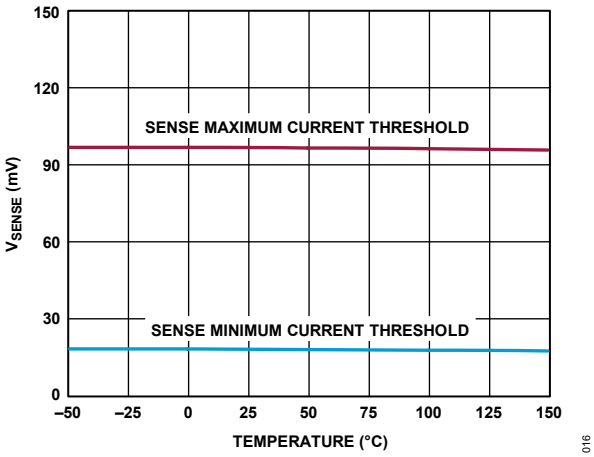

Figure 16. SENSE Current Threshold

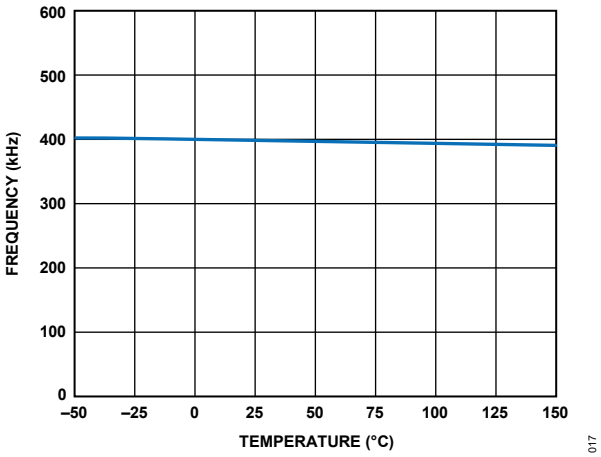

Figure 17. Maximum Switching Frequency

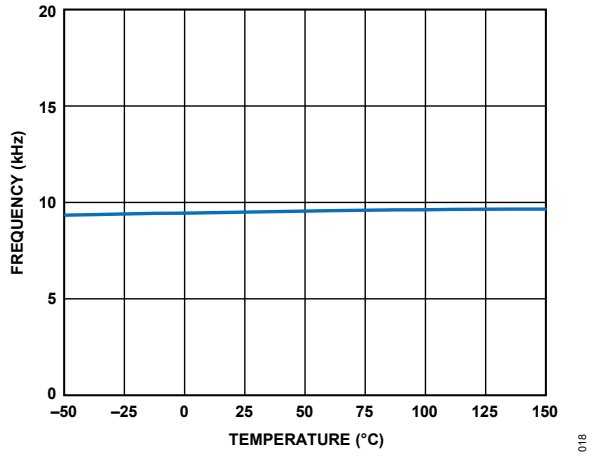

Figure 18. Minimum Switching Frequency

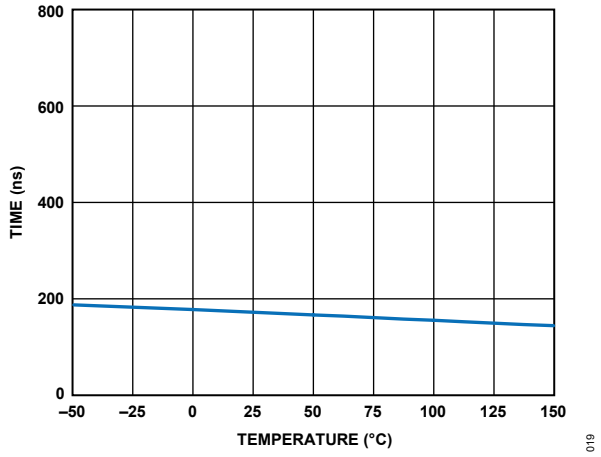

Figure 19. Minimum Switch-On Time

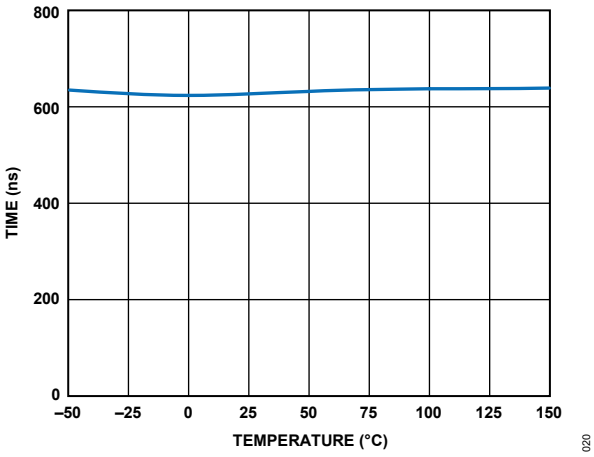

Figure 20. Minimum Switch-Off Time

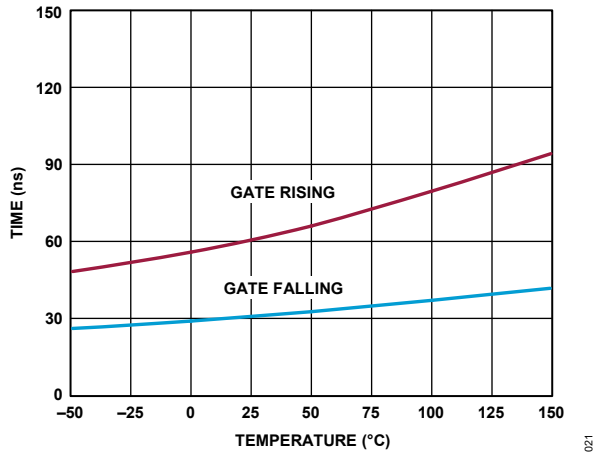

Figure 21. Gate Rising and Falling Time

BLOCK DIAGRAM

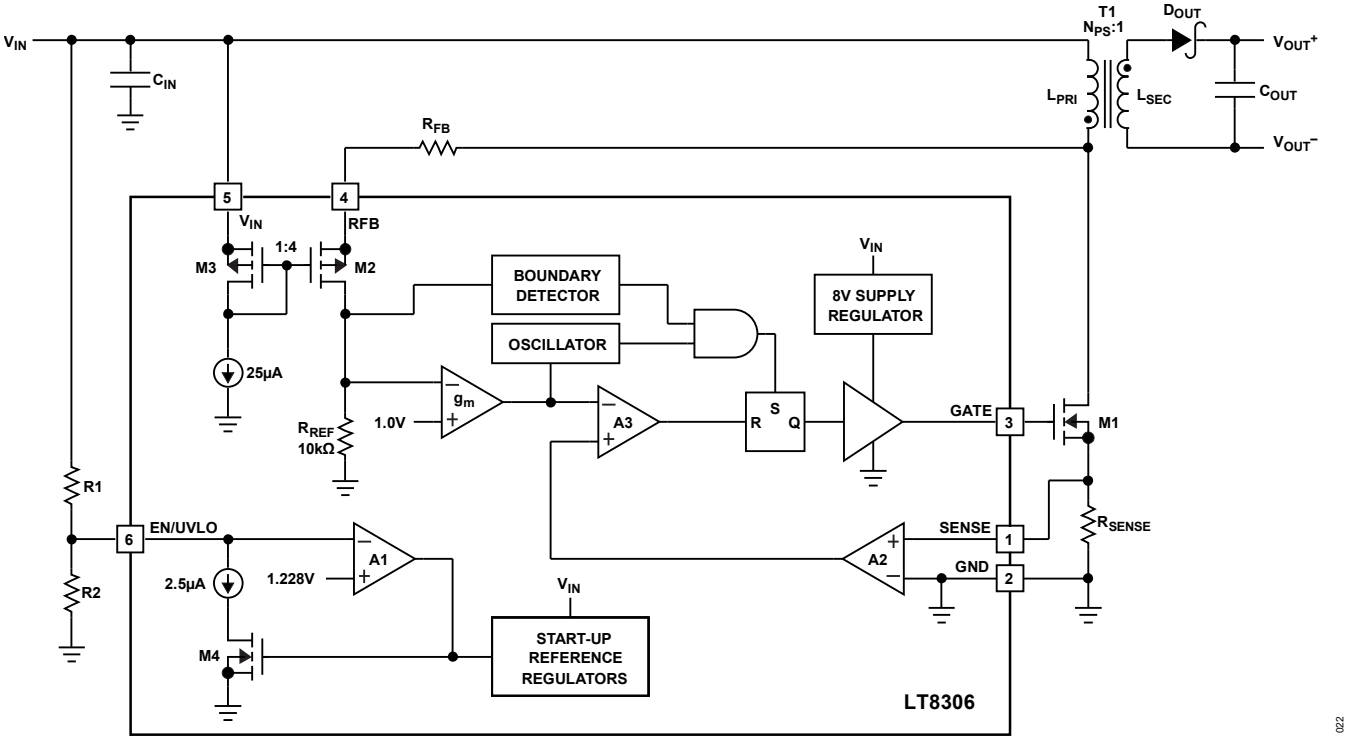

Figure 22. Block Diagram

THEORY OF OPERATION

The LT8306 is a current-mode switching regulator controller designed specially for the isolated flyback topology. The key problem in isolated topologies is how to communicate the output voltage information from the isolated secondary side of the transformer to the primary side for regulation. Historically, opto-isolators or extra transformer windings communicate this information across the isolation boundary. Opto-isolator circuits waste output power, and the extra components increase the cost and physical size of the power supply. Opto-isolators can also cause system issues due to limited dynamic response nonlinearity, unit-to-unit variation, and aging over life. Circuits employing extra transformer windings also exhibit deficiencies, as using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The LT8306 samples the isolated output voltage through the primary-side flyback pulse waveform. In this manner, neither opto-isolator nor extra transformer winding is required for regulation. Since the LT8306 operates in either the boundary conduction mode or discontinuous conduction mode, the output voltage is always sampled on the R_{FB} pin when the secondary current is zero. This method improves load regulation without the need of external load compensation components.

The LT8306 is a simple-to-use isolated flyback controller housed in a 6-lead TSOT-23 package. The output voltage is programmed with a single external resistor. By integrating the loop compensation and soft-start inside, the part further reduces the number of external components. As shown in the Figure 22, many of the blocks are similar to those found in traditional switching regulators including reference, regulators, oscillator, logic, current amplifier, current comparator, and an N-channel MOSFET gate driver. The novel sections include a flyback pulse sense circuit,

a sample-and-hold error amplifier, and a boundary mode detector, as well as the additional logic for boundary conduction mode, discontinuous conduction mode, and low ripple burst mode operation.

Boundary Conduction Mode Operation

The LT8306 features boundary conduction mode operation at heavy load, where the chip turns on the primary power switch when the secondary current is zero. Boundary conduction mode is a variable frequency, variable peak-current switching scheme. The power switch turns on and the transformer primary current increases until an internally controlled peak current limit. After the external MOSFET turns off, the voltage on the drain of the MOSFET rises to the output voltage multiplied by the primary-to-secondary transformer turns ratio plus the input voltage. When the secondary current through the output diode falls to zero, the voltage on the drain of the MOSFET falls below V_{IN}. A boundary mode detector senses this event and turns the external MOSFET back on.

Boundary conduction mode returns the secondary current to zero every cycle, so parasitic resistive voltage drops do not cause load regulation errors. Boundary conduction mode also allows the use of smaller transformers compared to continuous conduction mode and does not exhibit subharmonic oscillation.

Discontinuous Conduction Mode Operation

As the load gets lighter, boundary conduction mode increases the switching frequency and decreases the switch peak current at the same ratio. Running at a higher switching frequency up to several MHz increase switching and gate charge losses. To avoid this scenario, the LT8306 has an additional internal oscillator that clamps the maximum switching frequency to be less than 400kHz (typ). Once the switching frequency hits the internal frequency clamp, the part starts to delay the switch turn-on and operates in discontinuous conduction mode. Since the LT8306 integrates the control loop compensation and power supply rails internally without any external capacitors, there can be some jittering behavior in the discontinuous conduction mode operation.

Low Ripple Burst Mode Operation

Unlike traditional flyback converters, the LT8306 must turn on and off at least for a minimum amount of time and with a minimum frequency to allow accurate sampling of the output voltage. The inherent minimum switch current limit and minimum switch-off time are necessary to guarantee the correct operation of specific applications. As the load gets very light, the LT8306 starts to fold back the switching frequency while keeping the minimum switch current limit. So, the load current can decrease while still allowing minimum switch-off time for the sample-and-hold error amplifier. Meanwhile, the part switches between the sleep mode and active mode, thereby reducing the effective quiescent current to improve light load efficiency. In this condition, the LT8306 operates in low ripple burst mode. The 10kHz (typ) minimum switching frequency determines how often the output voltage is sampled and the minimum load requirement.

APPLICATIONS INFORMATION

Output Voltage

The R_{FB} resistor as depicted in the block diagram is an external resistor used to program the output voltage. The LT8306 operates like traditional current-mode switchers, except in the use of a unique flyback pulse sense circuit and a sample-and-hold error amplifier, which sample and therefore regulate the isolated output voltage from the flyback pulse. The operation is as follows: when the power switch M1 turns off, its drain voltage rises above the V_{IN} supply. The amplitude of the flyback pulse, i.e., the difference between it and the V_{IN} supply, is given as:

$$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \bullet ESR) \bullet N_{PS} \quad (1)$$

V_F = Output diode forward voltage

I_{SEC} = Transformer secondary current

ESR = Total impedance of secondary circuit

N_{PS} = Transformer effective primary-to-secondary turns ratio

The flyback voltage is then converted to a current, I_{RFB}, by the R_{FB} resistor and the flyback pulse sense circuit (M2 and M3). This current, I_{RFB}, also flows through the internal 10k R_{REF} resistor to generate a ground-referred voltage. The resulting voltage feeds to the inverting input of the sample-and-hold error amplifier. Since the sample-and-hold error amplifier samples the voltage when the secondary current is zero, the (I_{SEC} • ESR) term in the V_{FLBK} equation is assumed to be zero.

The internal reference voltage, V_{REF}, feeds the non-inverting input of the sample-and-hold error amplifier. The relatively high gain in the overall loop causes the voltage at the R_{REF} resistor to be nearly equal to the internal reference voltage V_{REF}. The resulting relationship between V_{FLBK} and V_{REF} is expressed with Equation 2 or Equation 3.

$$\left(\frac{V_{FLBK}}{R_{FB}}\right) \bullet R_{REF} = V_{REF} \quad (2)$$

$$V_{FLBK} = R_{FB} \bullet \left(\frac{V_{REF}}{R_{REF}}\right) = I_{RFB} \bullet R_{FB} \quad (3)$$

V_{REF} = Internal reference voltage = 1.00V

I_{RFB} = R_{FB} regulation current = 100µA

Combination of Equation 1 and Equation 3 yields Equation 4 for V_{OUT}, in terms of the R_{FB} resistor, transformer turns ratio, and diode forward voltage.

$$V_{OUT} = 100\mu A \bullet \left(\frac{R_{FB}}{N_{PS}}\right) - V_F \quad (4)$$

Output Temperature Coefficient

The first term in Equation 3 does not have a temperature dependence, but the output diode forward voltage V_F has a significant negative temperature coefficient (−1mV/°C to −2mV/°C). Such a negative temperature coefficient produces approximately 200mV to 300mV voltage variation on the output voltage across temperature.

For higher voltage outputs, such as 12V and 24V, the output diode temperature coefficient has a negligible effect on the output voltage regulation. For lower voltage outputs, such as 3.3V and 5V, however, the output diode temperature coefficient does count for an extra 2% to 5% output voltage regulation. For tight output voltage regulation across temperature, refer to other ADI parts with integrated temperature compensation features.

Selecting the Actual R_{FB} Resistor Value

The LT8306 uses a unique sampling scheme to regulate the isolated output voltage. Due to the sampling nature, the scheme contains repeatable delays and error sources, which affect the output voltage and force a re-evaluation of the R_{FB} resistor value. Therefore, a simple two-step process is required to choose the feedback resistor R_{FB}.

Rearrangement of the expression for V_{OUT} in the Output Voltage section yields the starting value for R_{FB} in Equation 5.

$$R_{FB} = \frac{N_{PS} \bullet (V_{OUT} + V_F)}{100\mu A} \quad (5)$$

V_{OUT} = Output voltage

V_F = Output diode forward voltage = ~0.3V

N_{PS} = Transformer effective primary-to-secondary turns ratio

Power up the application with the starting R_{FB} value and other components, and measure the regulated output voltage, $V_{OUT(MEAS)}$. Adjust the final R_{FB} value according to Equation 6.

$$R_{FB(FINAL)} = \frac{V_{OUT}}{V_{OUT(MEAS)}} \bullet R_{FB} \quad (6)$$

Once the final R_{FB} value is selected, the regulation accuracy from board to board for a given application is very consistent, typically under ±5% when including device variation of all the components in the system (assuming resistor tolerances and transformer windings matching within ±1%). However, if the transformer or the output diode is changed, or the layout is dramatically altered, there may be some change in V_{OUT}.

Output Power

Because the MOSFET power switch is located outside the LT8306, the maximum output power is primarily limited by external components. Output power limitations can be separated into three categories: voltage limitations, current limitations, and thermal limitations.

The voltage limitations in the flyback design are primarily the MOSFET switch $V_{DS(MAX)}$ and the output diode reverse-bias rating. Increasing the voltage rating of either component typically decreases application efficiency if all else is equal, and the voltage requirements on each of those components is directly related to the windings ratio of the transformer, the input and output voltages, and the use of any additional snubbing components. The MOSFET $V_{DS(MAX)}$ must theoretically be higher than $V_{IN(MAX)} + (V_{OUT} \bullet N_{PS})$, though leakage inductance spikes on both the drain

of the MOSFET and the anode of the output diode may more than double that requirement (see Leakage Inductance and Snubbers section for more details on snubbers). Figure 23 illustrates several MOSFET voltage ratings and the effect on the available output power (the MOSFET current limit and output voltage are fixed, and the turns ratio is continuously optimized for V_{IN}). Increasing the MOSFET rating increases the possible windings ratio and or maximum input voltage, and can increase the available output power for a given application. Both figures, Figure 23 and Figure 24, assume no leakage inductance and high efficiency.

The current limitation on output power delivery is generally constrained by transformer saturation current in higher power applications, although the MOSFET switch and output diode need to be rated for the desired currents as well. Increasing the peak current on the primary side of the flyback by reducing the R_{SENSE} resistor is the primary way to increase output power, and power delivered increases linearly with current limit, as shown in Figure 24, until parasitic losses begin to dominate. However, once the saturation current of the transformer is exceeded, the energy coupling between the primary and the secondary is reduced and incremental power is not delivered to the output. In addition, the primary inductance drops, the SENSE pin overcurrent threshold may trip due to a corresponding rapid rise in current, and the transformer has to absorb the energy not transferred through the saturated core, leading to heating. Some manufacturers may not specify the rated saturation current, but it is a necessary specification when trying to minimize transformer size and maximize output power and efficiency. Also necessary for proper design is data on saturation current over temperature. The saturation of typical power ferrites may reduce by over 20% from 25°C to 100°C.

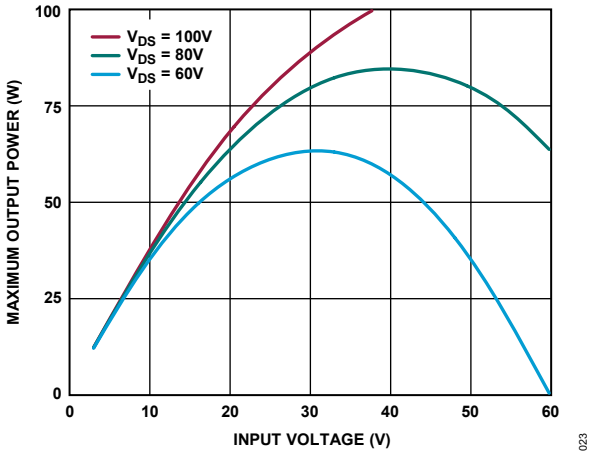

Figure 23. Maximum Output Power at $12V_{OUT}$ with a 10A I_{LIM} and Maximum V_{DS} = 60V, 80V, 100V

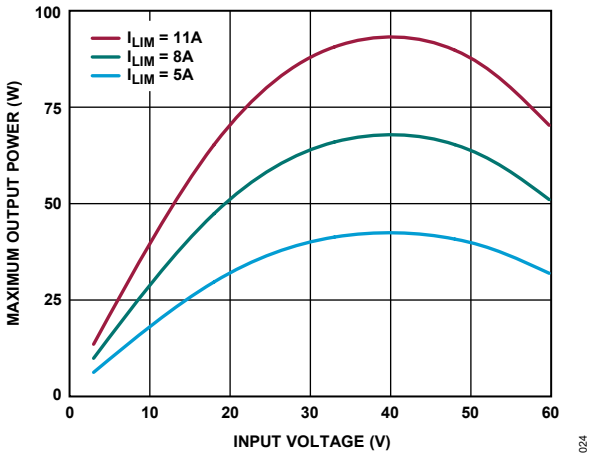

Figure 24. Maximum Output Power at 12V_{OUT} with 80V $V_{DS(MAX)}$ and I_{LIM} = 5A, 10A, 15A

The thermal limitation in flyback application for lower output voltages is dominated by losses in the output diode, with resistive and leakage losses in the transformer increasing as a percentage basis of loss as the output voltage is increased. As power level increases, the output diode and transformer may exceed their rated temperature specifications. Minimizing RMS output diode current, selecting a diode with minimal forward drop at expected currents, and minimizing parasitic resistances and leakage inductance in the transformer keep those components below their maximum temperatures while maximizing efficiency. The following section discussing transformer selection further helps to focus on minimizing losses in the output diode.

While active current in the LT8306 itself is low (approximately 390µA from V_{IN}), the current required to drive the external MOSFET ($f_{SW} \cdot Q_G$), drawn from V_{IN} through the LT8306 internal low dropout (LDO), dissipates (V_{IN} – 8V) • f_{SW} • Q_G. If that power is high enough, it causes significant heating of the LT8306 and triggers the overtemperature protection.

Primary Inductance Requirement

The LT8306 obtains output voltage information from the external MOSFET drain voltage when the secondary winding conducts current. The sample-and-hold error amplifier needs a minimum of 630ns to settle and sample the reflected output voltage. The 630ns includes 440ns minimum demagnetizing time and 190ns sample time. To ensure proper sampling, the secondary winding needs to conduct current for a minimum of 440ns. Equation 7 gives the minimum value for primary-side magnetizing inductance.

$$L_{PRI} \geq \frac{(V_{OUT}+V_F) \bullet R_{SENSE} \bullet t_{DEMAG(MIN)} \bullet N_{PS}}{V_{SENSE(MIN)}} \qquad (7)$$

$V_{SENSE(MIN)}$ = Sense minimum threshold = 17mV (typ)

$t_{DEMAG(MIN)}$ = Minimum demagnetize time = 440ns

N_{PS} = Ratio of primary windings to secondary windings

In addition to the primary inductance requirement for the minimum demagnetize time, the LT8306 has minimum switch-on time that prevents the chip from turning on the power switch shorter than approximately 200ns. This minimum switch-on time is mainly for leading-edge blanking the initial switch turn-on current spike. If the inductor

current exceeds the desired current limit during that time, oscillation may occur at the output as the current control loop loses its ability to regulate. Therefore, follow Equation 8 relating to maximum input voltage to select the primary-side magnetizing inductance.

$$L_{PRI} \geq \frac{V_{IN(MAX)} \bullet R_{SENSE} \bullet t_{ON(MIN)}}{V_{SENSE(MIN)}} \qquad (8)$$

$t_{ON(MIN)}$ = Minimum switch-on time = 200ns

In general, choose a transformer with its primary magnetizing inductance about 30% larger than the values calculated above. A transformer with much larger inductance has a bigger physical size and may cause instability at light load.

Selecting a Transformer

Transformer specification and design is perhaps the most critical part of successfully applying the LT8306. In addition to the usual list of guidelines dealing with high frequency isolated power supply transformer design, carefully consider the following information.

Analog Devices has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT8306. Table 4 shows the details of these transformers.

Turns Ratio and RMS Diode Current

Note that when choosing the R_{FB} resistor to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. In contrast, the use of simple ratios of small integers, e.g., 3:1, 2:1, 1:1, provides more freedom in settling total turns and mutual inductance.

While the turns ratio can be selected to maximize output power for a given current limit, minimizing the turns ratio and increasing the current limit often increases efficiency and better utilizes the saturation current of a given transformer. Figure 25 shows the maximum output power using three transformers with different windings ratio that have the same output inductance and peak output current, illustrating that increasing current while decreasing turns ratio can deliver more power.

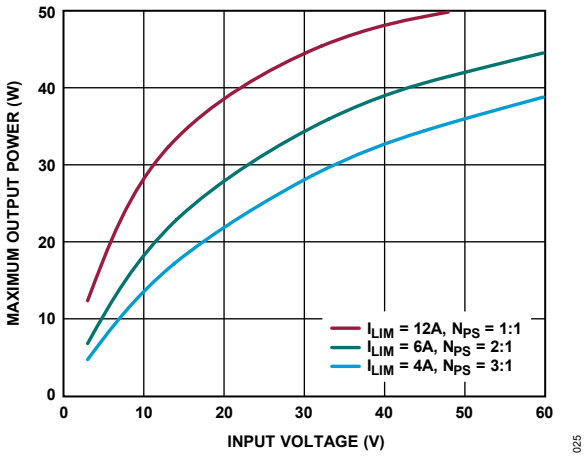

Figure 25. Maximum Output Power at 12V Out Using Three Transformers with Equal Peak Output Current and Secondary Inductance

Table 4. Predesigned Transformers

TRANSFORMER PART NUMBER	DIMENSIONS (W × L × H) (mm)	L_{PRI} (µH)	L_{LKG} (µH)	N_P:N_S	R_{PRI} (mΩ)	R_{SEC} (mΩ)	VENDOR	TARGET APPLICATION		
								V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
10393-T174-VER3	32.6 × 27.0 × 15.0	5	0.1	2:1	10	6.5	Sumida	9 to 36	12	4
12322-T351-VER2	17.0 × 14.0 × 8.5	10	0.15	1:1.5:0.5	55	160/40	Sumida	7 to 18	18/6	0.3/0.1
11338-T259-VER2	24.5 × 17.6 × 9.1	2.4	0.09	1:1	10	10	Sumida	7 to 18	12	2
PA1835NL	29.2 × 21.8 × 11.4	4.5	0.2	3:1	9.5	5	Pulse Electronics	18 to 36	5	7
750311911	25.0 × 22.2 × 16.0	6.78	0.1	1:3:3:3:3	20	450	Wurth Electronics	8 to 36	+15/–8	0.2

Note: Typical specifications, unless otherwise noted.

There are two significant constraints on the turns ratio. First, the MOSFET drain voltage equals the maximum input supply plus the output voltage multiplied by the windings ratio plus some amount of overshoot caused by leakage inductance. Second, increasing the turns ratio increases the RMS diode current, lowering the efficiency. This efficiency limitation is worse at lower output voltages when the diode forward voltage is significant compared to the output voltage. To calculate RMS diode current, Equation 9 and Equation 10 are needed; Equation 9 to calculate the duty cycle, D, and Equation 10 to calculate the RMS current of a triangle waveform.

$$D = \frac{(V_{OUT}+V_F)\bullet N_{PS}}{V_{IN}+(V_{OUT}+V_F)\bullet N_{PS}} \quad (9)$$

$$I_{DIODE(RMS)} = \sqrt{\frac{(I_{LIM}\bullet N_{PS})^2\bullet(1-D)}{3}} \quad (10)$$

In a typical application such as the 5V, 7A output in the last page, it is recommended to work with a secondary-side synchronous rectifier driver for high efficiency.

Saturation Current

The current in the transformer windings should not exceed its rated saturation current. Energy injected once the core is saturated is not transferred to the secondary and instead is dissipated in the core. When designing custom transformers to be used with the LT8306, the transformer manufacturers should always specify the saturation current.

Winding Resistance

Resistance in either the primary or secondary windings reduces overall power efficiency. Good output voltage regulation is maintained independent of winding resistance due to the boundary/discontinuous conduction mode operation of the LT8306.

Leakage Inductance and Snubbers

Transformer leakage inductance on either the primary or secondary causes a voltage spike to appear on the primary after the MOSFET switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. Minimize transformer leakage inductance.

In most cases, proper selection of the external MOSFET and a well-designed transformer eliminates the need for snubber circuitry, but in some cases the optimal MOSFET may require protection from this leakage spike.

To clamp and damp the leakage voltage spikes, a (RC + DZ) snubber circuit in Figure 26 is recommended. The RC (resistor-capacitor) snubber quickly damps the voltage spike ringing and provides great load regulation and EMI performance. And, the DZ (diode-Zener) ensures well-defined and consistent clamping voltage to protect the drain of MOSFET from exceeding its absolute maximum rating voltage.

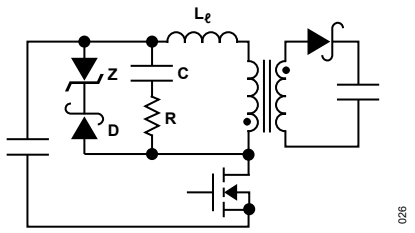

Figure 26. (RC + DZ) Snubber Circuit

The recommended approach for designing an RC snubber is to measure the period of the ringing at the MOSFET drain when the MOSFET turns off without the snubber and then add capacitance (starting with something in the range of 100pF) until the period of the ringing is 1.5 to 2 times longer. The change in period determines the value of the parasitic capacitance, from which the parasitic inductance can be determined from the initial period, as well. Similarly, estimate initial values using stated switch capacitance and transformer leakage inductance. Once the value of the drain node capacitance and inductance is known, add a series resistor to the snubber capacitance to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance using the observed periods (t_{PERIOD} and $t_{PERIOD(SNUBBER)}$) and snubber capacitance ($C_{SNUBBER}$) is given by Equations 11 to 13.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBER)}}{t_{PERIOD}}\right)^2 - 1} \quad (11)$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} \cdot 4\pi^2} \quad (12)$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}} \quad (13)$$

Note that energy absorbed by a snubber is converted to heat and is not delivered to the load. In high voltage or high current applications, the snubber may need to be sized for thermal dissipation.

For the DZ snubber, take proper care when choosing both the diode and Zener diode. Schottky diodes are typically the best choice, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. Choose a diode that has a reverse-voltage rating higher than the maximum rating voltage of MOSFET. Choose the Zener diode breakdown voltage to balance power loss and switch voltage protection. The best compromise is to choose the largest voltage breakdown with enough margin. Use Equation 14 to make the proper choice.

$$V_{ZENER(MAX)} = V_{DS(MAX)} - V_{IN(MAX)} \quad (14)$$

The power loss in the DZ snubber determines the power rating of the Zener diode.

Leakage Inductance and Output Diode Stress

The output diode may also see increased reverse voltage stresses from leakage inductance. While it nominally sees a reverse voltage of the input voltage divided by the winding's ratio plus the output voltage when the MOSFET power switch turns on, the capacitance on the output diode and leakage inductance cause an LC tank, which may ring beyond that expected reverse voltage. Implement an RC snubber or RCD clamp to reduce the voltage spike if it is desirable to use a lower reverse voltage diode.

Secondary Leakage Inductance

In addition to the previously described effects of leakage inductance in general, leakage inductance on the secondary in particular exhibits an additional phenomenon. It forms an inductive divider on the transformer secondary that effectively reduces the size of the primary-referred flyback pulse used for feedback. This increases the output voltage target by a similar percentage. Note that unlike leakage spike behavior, this phenomenon is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations), this can be accommodated by adjusting the R_{FB} resistor.

Selecting a Current-Sense Resistor

The external current-sense resistor optimizes the current limit behavior for the application under consideration. As the current-sense resistor is varied from several ohms down to tens of milliohms, peak switch current goes from a fraction of an ampere to tens of amperes. Take care to ensure proper circuit operation, especially with small current-sense resistor values. The sense resistor value is calculated using Equation 15.

$$R_{SENSE} = \frac{95mV}{I_{LIM}} \quad (15)$$

For example, a peak MOSFET switch current of 5A requires a sense resistor of 0.019Ω. Note that the instantaneous peak power in the sense resistor is 1W, and rate it accordingly. The LT8306 has only a single sense line to this resistor. Therefore, any parasitic resistance in the ground side connection of the sense resistor increases its apparent value. In the case of a 0.025Ω sense resistor, 1mΩ of parasitic resistance causes 4% reduction in peak switch current. Therefore, do not ignore resistance of printed circuit copper traces and vias.

Another issue for proper operation of the current-sense circuitry is avoiding prematurely tripping the SENSE threshold while slewing the MOSFET drain when the GATE pin goes high. The LT8306 does not begin to compare the SENSE pin voltage with the target threshold until at least 200ns has passed. This should be entirely sufficient for most

applications, but premature tripping of SENSE comparator may occur in cases where MOSFET with very high Q_G is used with a series resistor at the GATE pin.

Output Short Circuits and SENSE Pin Over Current

When the output is heavily overloaded or shorted to ground, it reflects a very low output voltage back to the primary side of the transformer, which causes the LT8306 to turn the external MOSFET on after the internal blanking time instead of the secondary current that has discharged.

Under this condition, the LT8306 runs into the continuous conduction mode at maximum switching frequency. If the sampled R_{REF} voltage is still less than 0.6V after internal soft-start, the LT8306 stops switching for a long time and then initiates a new soft-start cycle. If the sampled R_{REF} voltage is larger than 0.6V after internal soft-start, the switch current may run away and the voltage at the SENSE pin exceeds the 95mV maximum current limit threshold. Once the SENSE voltage hits 160mV over the current limit threshold, the LT8306 also stops switching for a long time and then initiates a new soft-start cycle. Under either condition, the new soft-start cycle throttles back both the switch current limit and switch frequency. The output short-circuit protection prevents the switch current from running away and limits the average output diode current.

High Drain Capacitance and Low Current Operation

When designing applications with some combination of a low current limit (I_{LIM} < 1A), a high secondary-to-primary turns ratio (N_{PS} <1), multiple output windings, or very capacitive output diodes, it is important to minimize the capacitance reflected onto the primary winding and on the drain of the external MOSFET. After the MOSFET turns off during each switching cycle, the primary current charges that capacitance to slew the MOSFET drain until the secondary begins to deliver power, and if the drain node does not slew and remain below V_{IN} within approximately 440ns once the GATE pin goes low and the MOSFET turns off, the LT8306 may detect that the current in the secondary is zero and turn the MOSFET back on, causing the LT8306 to switch continuously while delivering very little power to output. This results in the drop of the output voltage at lighter loads. This problem can be prevented by maximizing N_{PS} (minimizing ratio of secondary windings to primary windings), increasing the peak drain current (minimizing R_{SENSE}), and minimizing the output diode and transformer capacitance.

Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.228V with 18mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.228V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are given by Equations 16 and 17.

$$V_{IN(UVLO^+)} = \frac{1.246V \bullet (R1+R2)}{R2} + 2.5\mu A \bullet R1 \qquad (16)$$

$$V_{IN(UVLO^-)} = \frac{1.228V \bullet (R1+R2)}{R2} \qquad (17)$$

Figure 27 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on and puts the LT8306 in shutdown with quiescent current less than 2µA.

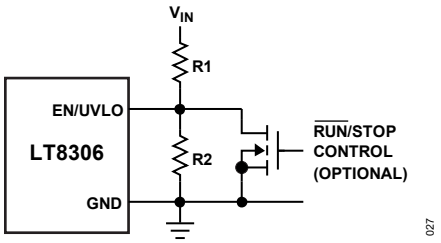

Figure 27. Undervoltage Lockout (UVLO)

Minimum Load Requirement

The LT8306 recovers output voltage information using the flyback pulse that occurs once the external MOSFET turns off and the secondary winding conducts current. To regulate the output voltage, the LT8306 needs to sample the flyback pulse. The LT8306 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum delivery of energy creates a minimum load requirement on the output of approximately 0.5% of maximum load. The minimum operating frequency at minimum load is approximately 10kHz.

Alternatively, use Zener diodes sufficiently rated to handle the minimum load power to provide a minimum load without decreasing efficiency in normal operation. When selecting a Zener diode for this purpose, the Zener voltage should be high enough that the diode does not become the load path during transient conditions, but the voltage must still be low enough that the MOSFET and output voltage ratings are not exceeded when the Zener functions as the minimum load.

Design Example

Use the following design example as a guide to design the application for the LT8306. The design example involves designing a 12V output with 4A load current and an input range from 9V to 36V.

Step 1: Select the Transformer Turns Ratio

Transformer turns ratio affects the requirements for the MOSFET switch V_{DS} rating, output diode reverse bias rating, output power capability, and efficiency of the overall converter. Because the output diode and currents are high in this application, optimize efficiency by minimizing the RMS diode current. Typical efficiency in a variety of applications is 85% to 90% and due to compromises made for the wide input voltage range, an efficiency of 85% is assumed for calculating output power. This assumption can be revised once the application is tested. The following equations evaluate each of the important criteria.

$$N_{PS} = N_P / N_S \quad (18)$$

$$N_{PS} = \frac{D_{MAX} \bullet V_{IN}}{(1 - D_{MAX}) \bullet (V_{OUT} + V_F)} \quad (19)$$

$$V_{DS(MAX)} \geq V_{IN(MAX)} + V_{OUT} \bullet N_{PS} \quad (20)$$

$$V_{R(DIODE)} \geq \frac{V_{IN(MAX)}}{N_{PS}} + V_{OUT} \quad (21)$$

$$I_{OUT(MAX)} \approx 0.85 \bullet (1 - D) \bullet N_{PS} \bullet \frac{I_{LIM}}{2} \quad (22)$$

$$I_{DIODE(RMS)} = \sqrt{(I_{LIM} \bullet N_{PS})^2 \bullet (1 - D)/3} \quad (23)$$

where, D_{MAX} is typically between 0.45 to 0.65

V_F = Output diode forward voltage = ~0.3V

Rearrange the equation for output power to solve for the current limit, I_{LIM}, which can be solved at the nominal or the minimum V_{IN} depending on application requirements. In this application, the 4A load requirement is set at V_{IN} = 9V to reduce operating stresses at higher input voltage. Table 5 shows the results of the equation in this application.

Evaluating the results of Table 5, the 1:2 turns ratio looks demanding in terms of diode reverse-voltage requirements (a diode with higher reverse bias capability generally has a larger forward drop and therefore lower application efficiency) and primary side currents, and only decreases the output diode RMS current by 13% from the 1:1 case. However, on evaluating the minimum and maximum inductance requirements in step 3, even the 1:1 case does not allow for enough on-time from maximum V_{IN} for the range of inductance that provides sufficient off-time. For that reason, a 2:1 turns ratio is selected, easing the requirement on the output diode reverse voltage rating in process.

Table 5. Voltage Stresses, Output Capability, and Diode Current vs. Turns Ratio in 36V V_{IN} to 12V, 4A Application

N_{PS}	$V_{DS(MAX)}$	$V_{R(DIODE)}$	D (V_{IN} = 12V)	D (V_{IN} = 9V)	I_{LIM} (4A OUT AT V_{IN} = 9V)	$I_{DIODE(RMS)}$ (V_{IN} = 12V)
0.5	42	84	0.34	0.41	30.9	6.5
1	48	48	0.51	0.58	21.7	7.5
2	60	30	0.67	0.73	17.1	9.2
3	72	24	0.75	0.80	15.6	10.7

Step 2: Calculate the Sense Resistor Value

Calculate the sense resistor by Equation 24.

$$R_{SENSE} = \frac{95mV}{I_{LIM}} \quad (24)$$

The desired 17.1A current limit leads to non-standard value of 0.0055Ω, so the current limit is increased to use a standard 0.005Ω value and I_{LIM} of 19A.

Step 3: Select a Transformer Based on Inductance and Saturation Current Requirements

Set the primary inductance for the transformer above a minimum value to satisfy the minimum demagnetize and switch-on time requirements (Equation 26).

$$L_{PRI} \geq \frac{(V_{OUT}+V_F)\bullet R_{SENSE} \bullet t_{DEMAG(MIN)} \bullet N_{PS}}{V_{SENSE(MIN)}} \quad (25)$$

$$L_{PRI} \geq \frac{V_{IN(MAX)}\bullet R_{SENSE} \bullet t_{ON(MIN)}}{V_{SENSE(MIN)}} \quad (26)$$

$$V_{SENSE(MIN)} = 17mV(typ)$$

$$t_{DEMAG(MIN)} = 440ns$$

$$t_{ON(MIN)} = 200ns$$

For this application, the minimum primary inductance with a 2:1 transformer and a 0.005Ω sense resistor for an 19A current limit is decided by the minimum demagnetize time requirement to be 3.2µH.

Once the primary inductance is determined, calculate the maximum load switching frequency by Equation 28.

$$f_{SW} = \frac{1}{t_{ON}+t_{DEMAG}} = \frac{1}{\frac{L_{PRI}\bullet I_{LIM}}{V_{IN}} + \frac{L_{PRI}\bullet I_{LIM}}{N_{PS}\bullet(V_{OUT}+V_F)}} \quad (28)$$

The transformer also needs to be rated for the correct saturation current level across line and load conditions. A saturation current rating larger than 19A is necessary to work in this application. The 10393-T174-VER3 from Sumida is chosen as the flyback transformer.

Step 4: Select a MOSFET Switch

The selected 2:1 transformer requires a nominal 60V rating on the MOSFET switch, assuming no leakage inductance. However, even a small amount of leakage inductance may cause the drain to ring to double the anticipated voltage, and generally this needs to be verified in the final design. At currents below 19A, it is easy to find a MOSFET with sufficiently low $R_{DS(ON)}$ to have little influence on the full load efficiency while at the same time having low enough Q_G to minimize gate driver dissipation at lighter loads. Also, while considering the efficiency gains and losses with a given MOSFET, it is important to realize that a trade-off in $R_{DS(ON)}$ for $V_{DS(MAX)}$ may backfire if a snubber needs to be added to the circuit to meet the voltage requirements and dissipates more energy than the difference in switch resistance. For that reason, an ON Semi FDMS86183 is selected to give lots of margin with its 100V rating. The RMS current in the MOSFET can be squared and multiplied by the $R_{DS(ON)}$ to calculate losses and the current required to drive the MOSFET at frequency can be determined by Equation 29.

$$I_{MOSFET(RMS)} = \sqrt{I_{LIM}{}^2 \bullet D/3} \quad (29)$$

$$I_{GATE} = f_{SW} \bullet Q_G \quad (30)$$

$$P_{GATE} = I_{GATE} \bullet (V_{IN} - 8V) \quad (31)$$

In this application, the MOSFET RMS current at maximum load is about 8.5A, which multiplied by the 0.011Ω $R_{DS(ON)}$ is 0.8W, or on the order of 2% loss in efficiency.

Step 5: Select the Output Diode

The output diode reverse voltage, as calculated earlier, is the first important specification for the output diode. As with the MOSFET, choosing a diode with enough margin should preclude the use of a snubber. The second criterion is the power requirement of the diode, which is more difficult to correctly ascertain. Some manufacturers give direct data about power dissipation versus duty cycle, which can be used with the data from the table. To avoid using a snubber, select a diode with a 60V reverse-bias capability and minimal forward drop. In this case, the On Semi NRVB860MFS. In this application, where maximizing efficiency is the goal, minimizing the maximum voltage requirement on V_{IN} may allow the use of a diode with a lower reverse bias rating and a lower forward drop, which could further increase efficiency.

Alternatively, if no efficient diode is available for a particular reverse bias rating, it may be more beneficial to increase the windings ratio until a diode with low forward drop can be selected and then re-evaluate whether the solution with higher RMS diode current is beneficial.

Step 6: Select the Output Capacitor

Choose the output capacitor to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Equation 32 calculates the output voltage ripple:

$$\Delta V_{OUT} = \frac{L_{PRI}\bullet I_{LIM}{}^2}{2\bullet C_{OUT}\bullet V_{OUT}} \quad (32)$$

Step 7: Add Snubber Circuitry as Necessary

With the primary components selected, construct the application to evaluate ringing at the drain of the MOSFET switch. A (RC + DZ) snubber is recommended for this application.

For the RC snubber, use the equations from the Leakage Inductance and Snubbers section, or an estimate of component values from using the published leakage inductance of the transformer and selecting a snubber capacitor ranging from 1 to 3 times larger than the published MOSFET output capacitance.

The maximum Zener breakdown voltage is set according to the maximum V_{IN} and maximum drain voltage of MOSFET (Equation 33).

$$V_{ZENER(MAX)} = V_{DS(MAX)} - V_{IN(MAX)} \quad (33)$$

Choose a diode that is fast and has sufficient reverse voltage breakdown.

Step 8: Select the R_{FB} Resistor

Use Equation 34 to calculate the starting values for R_{FB}.

$$R_{FB} = \frac{N_{PS} \bullet (V_{OUT} + V_F)}{100\mu A} \quad (34)$$

Depending on the tolerance of standard resistor values, the precise resistor value may not exist. As discussed in the Applications Information section, adjust the final R_{FB} value on the measured output voltage.

Step 9: Select the EN/UVLO Resistors

Determine the amount of hysteresis required and calculate the R1 resistor value using Equation 35.

$$V_{IN(HYS)} = 2.5\mu A \bullet R1 \quad (35)$$

Determine the UVLO thresholds and calculate the R2 resistor value using Equation 36.

$$V_{IN(UVLO^+)} = \frac{1.246V \bullet (R1+R2)}{R2} + 2.5\mu A \bullet R1 \quad (36)$$

Related Parts

Table 6. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT8300	100VIN Micropower Isolated Flyback Converter with 150V/260mA Switch	Low IQ Monolithic No-Opto Flybacks, 5-Lead TSOT-23
LT8301	42VIN Micropower Isolated Flyback Converter with 65V/1.2A Switch	Low IQ Monolithic No-Opto Flybacks, 5-Lead TSOT-23
LT8302	42VIN Micropower Isolated Flyback Converter with 65V/3.6A Switch	Low IQ Monolithic No-Opto Flybacks, 8-Lead SO-8E
LT8303	100VIN Micropower Isolated Flyback Converter with 150V/450mA Switch	Low IQ Monolithic No-Opto Flybacks, 5-Lead TSOT-23
LT8304	100VIN Micropower Isolated Flyback Converter with 150V/2A Switch	Low IQ Monolithic No-Opto Flybacks, 8-Lead SO-8E
LT8309	Secondary-Side Synchronous Rectifier Driver	4.5V ≤ V_{CC} ≤ 40V, Fast Turn-On and Turn-Off, 5-Lead TSOT-23
LT3748	100V Isolated Flyback Controller	5V ≤ V_{IN} ≤ 100V, No Opto Flyback, MSOP-16(12)

OUTLINE DIMENSIONS

Table 7. S6 Package 6-Lead Plastic TSOT-23

Thermal Resistance	
Junction-to-Ambient (θ_{JA})	192°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	51°C/W

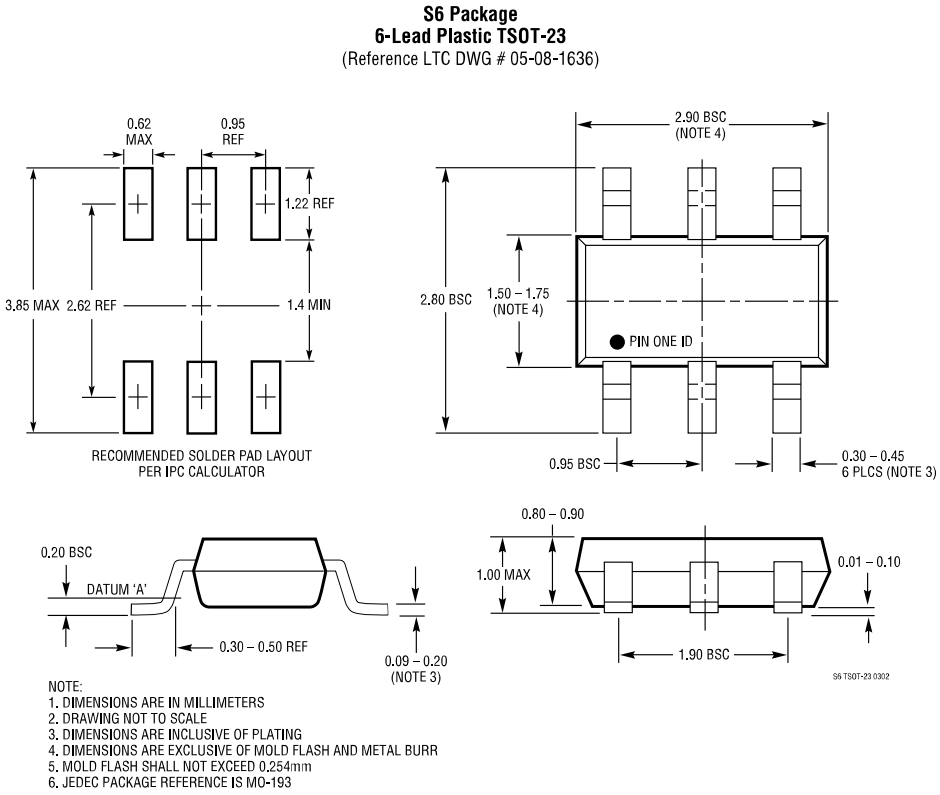

Figure 28. Package Drawing

TYPICAL APPLICATION CIRCUITS

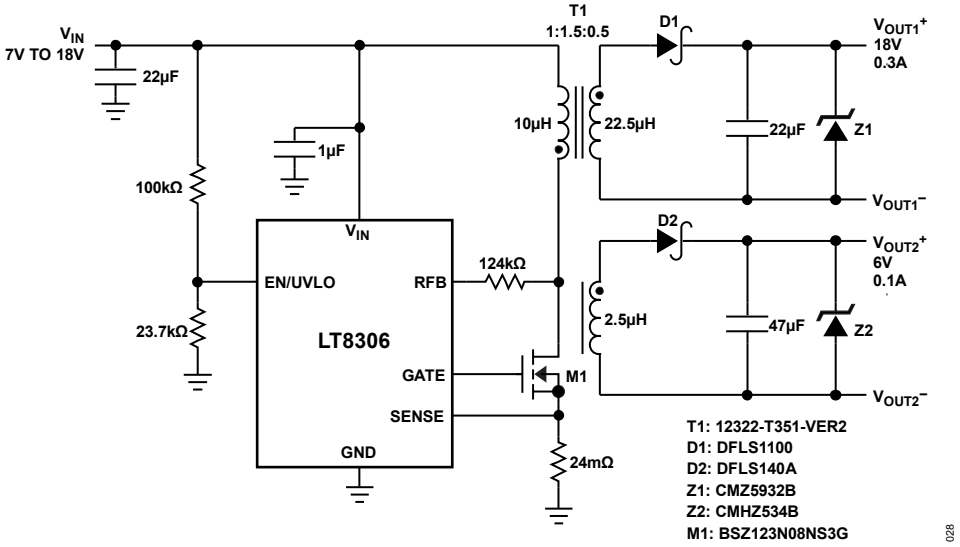

Figure 29. 7V to 18V Input,18V/0.3A and 6V/0.1A Output Isolated Flyback Converter

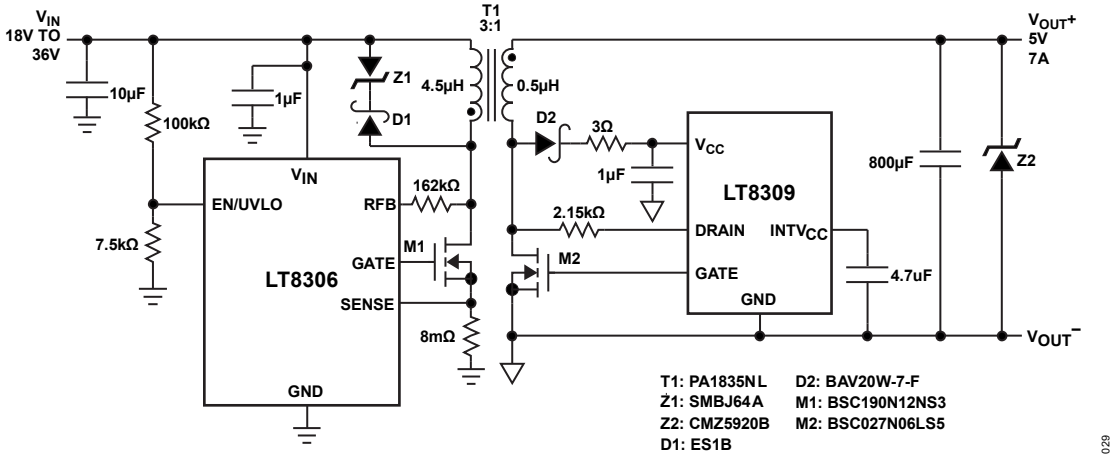

Figure 30. 18V to 36V Input, 5V/7A Output Isolated Flyback Converter

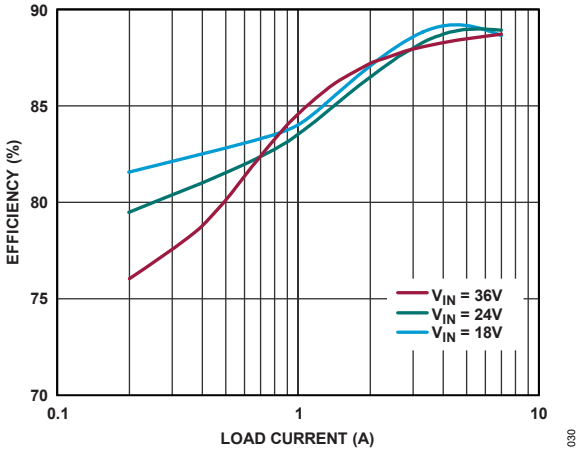

Figure 31. Efficiency vs. Load Current

ORDERING GUIDE

Table 8. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8306RS6#TRMPBF	LT8306RS6#TRPBF	LTHNM	6-Lead Plastic TSOT-23	−40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8306RS6#WTRMPBF	LT8306RS6#WTRPBF	LTHNM	6-Lead Plastic TSOT-23	−40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges.

*Identify the temperature grade by a label on the shipping container.

Tape and reel specifications: Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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