# Floating, High-Voltage Active Rectifier Controller

## FEATURES

- **Replaces Rectifying Diodes with N-Channel MOSFETs in Rectifier Applications**
- **Maximizes Power Efficiency, Eliminates Thermal Design Problems**
- **Low 25mV Forward Voltage Drop**
- **Wide Operating Voltage Range: 9V to >500V**
- **Wide Operating Frequency Range: DC to 100kHz**
- Regulated 12V GATE Drive for External N-Channel MOSFET Enhancement
- *8-Lead MSOP* and *8-Lead, 3mm x 3mm, Side Wettable DFN* Packages

## APPLICATIONS

- Single-Phase, 3-Phase, and 6-Phase Bridge Rectifiers
- Automotive Alternator Bridge Rectifiers
- Off-Line Active Bridge Rectifier
- 3-Phase Aircraft Power
- High-Voltage DC Diode-OR with Reverse Blocking

## DESCRIPTION

The LT4322 is a floating active rectifier controller that drives an external N-Channel MOSFET to replace a rectifier diode. It is designed primarily for AC applications and operates with input supply frequencies ranging from DC to 100kHz. On each cycle of the input AC waveform, an external N-Channel MOSFET gate is enhanced to provide the equivalent of a low diode forward voltage drop of 25mV. The resulting reduction in power dissipation eliminates thermal design problems and costly heat sinks, greatly reducing PC board area.

The addition of a high-voltage depletion N-Channel MOSFET enables operation at very high output voltages, limited only by the voltage ratings of two external MOSFETs. In AC applications, an integrated LDO provides the required gate drive voltage to turn the external MOSFET fully on. Fast, high-current gate drivers minimize reverse current transients at high input frequencies.

## TYPICAL APPLICATION

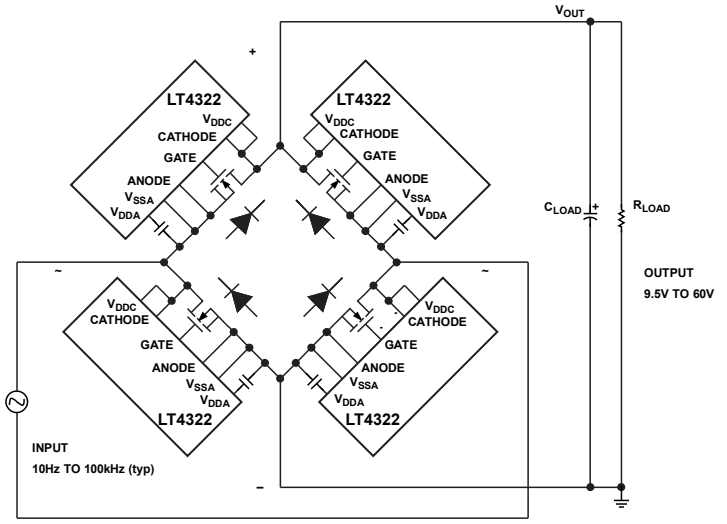


*Figure 1. 10Hz to 100kHz, 9.5V to 60V Full-Bridge Application*

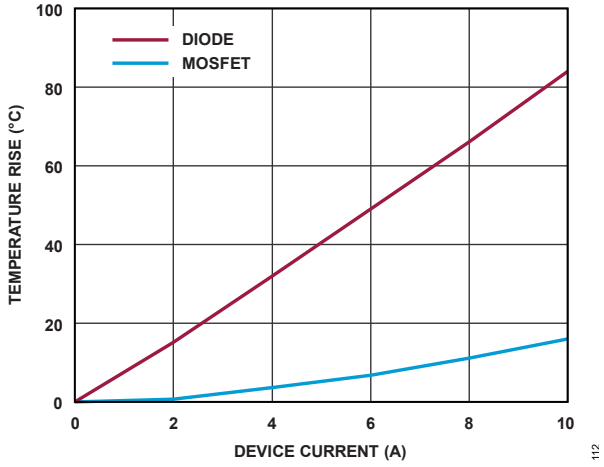


*Figure 2. Temperature Rise vs. Device Current*


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# REVISION HISTORY

**02/2023 - Rev. 0: Initial Release**

# SPECIFICATIONS

**Table 1. Electrical Characteristics**

($T_J$ = -40°C to +150°C for the minimum and maximum values. $T_{JA}$ = 25°C for the typical values. $V_{CATHODE}$ = $V_{VDDC}$ = $V_{VDDA}$ = 12V, $V_{VSSA}$ = $V_{ANODE}$ = 0V unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{DDC}$ Input Supply Operating Voltage Range ($V_{DDC}$ to $V_{SSA}$) [2] [3] | $V_{VDDC}$ | | 9.5 | 12 | 60 | V |
| $V_{DDA}$ Operating Voltage Range [4] | $V_{VDDA}$ | | 9 | 12 | 14 | V |
| Input Supply Undervoltage Lockout | $V_{VDDA(UVL)}$ | $V_{DDC}$ Rising; measured at $V_{DDA}$ | | 4.4 | | V |
| $V_{DDA}$ Regulation Voltage | $V_{VDDA}$ | $V_{DDC}$ = 24V, $C_{VDDA}$ = 1µF | 11 | 12.35 | 14 | V |
| $V_{DDA}$ Regulation Hysteresis Voltage | $V_{VDDA, HYST}$ | $V_{DDC}$ = 24V, $C_{VDDA}$ = 1µF | | -0.6 | | V |
| $V_{DDA}$ Drop-Out Voltage, ($V_{DDC}$ – $V_{DDA}$) | $V_{DO}$ | $V_{DDC}$ = CATHODE = 11V | | 120 | 400 | mV |
| $V_{DDA}$ Input Supply Current | $I_{VDDA(IN)}$ | Forward Bias, CATHODE = $V_{DDC}$ = -100mV | | 2.2 | 4.4 | mA |
| | | Reverse Bias, CATHODE = $V_{DDC}$ = 2V | | 1.2 | 2.4 | |
| $V_{DDA}$ Output Start-up Current | $I_{START}$ | $V_{DDA}$ = 0V, $V_{DDC}$ = 24V | -3 | -12 | -50 | mA |
| $V_{DDA}$ Output Refresh Current | $I_{GULP}$ | $V_{DDA}$ = 10V, $V_{DDC}$ = 24V | -10 | -40 | -85 | mA |
| CATHODE Input Bias Current | $I_{CATHODE}$ | Forward Bias, CATHODE = -25mV | 0 | -3 | -10 | µA |
| | | Reverse Bias, CATHODE = 60V | 5 | 20 | 50 | |
| ANODE Input Bias Current | $I_{ANODE}$ | CATHODE = -25mV | 0 | -3 | -10 | µA |
| ANODE–CATHODE Regulation Voltage | $\Delta V_{SD}$ | GATE = 4V | 15 | 25 | 35 | mV |
| GATE Drive Output High Voltage (GATE-ANODE) | $\Delta V_{GATE(H)}$ | CATHODE = -0.2V, $I_{GATE}$ = -1mA | 11.5 | 11.88 | 14 | V |

($T_J$ = -40°C to +150°C for the minimum and maximum values. $T_{JA}$ = 25°C for the typical values. $V_{CATHODE}$ = $V_{VDDC}$ = $V_{VDDA}$ = 12V, $V_{VSSA}$ = $V_{ANODE}$ = 0V unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| GATE Drive Output Low Voltage | $\Delta V_{GATE(L)}$ | CATHODE = 12V, $I_{GATE}$ = 1mA | | 5 | 50 | mV |
| Propagation Delay, CATHODE to GATE Rising to 4V | $t_{D,RISE}$ | CATHODE = Step 1.5V to -0.2V, $C_{GATE}$ = 10nF | | 550 | 1000 | ns |
| | | CATHODE = Step 1.5V to -0.2V, $C_{GATE}$ = 100nF | | 870 | 1500 | |
| GATE Rise Time, 1V to 4V | $t_{RISE}$ | CATHODE = Step 1.5V to -0.2V, $C_{GATE}$ = 10nF | | 370 | 650 | ns |
| | | CATHODE = Step 1.5V to -0.2V, $C_{GATE}$ = 100nF | | 550 | 900 | |
| Propagation Delay, CATHODE to GATE Falling to 2V | $t_{D,FALL}$ | CATHODE = Step -0.1V to 0.1V, $C_{GATE}$ = 10nF | | 130 | 260 | ns |
| | | CATHODE = Step -0.1V to 0.1V, $C_{GATE}$ = 100nF | | 330 | 660 | |
| GATE Fall Time, 9V to 2V | $t_{FALL}$ | CATHODE = Step -0.1V to 0.1V, $C_{GATE}$ = 10nF | 10 | 45 | 100 | ns |
| | | CATHODE = Step -0.1V to 0.1V, $C_{GATE}$ = 100nF | 85 | 170 | 350 | |

[1] All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to $V_{SSA}$ unless otherwise specified. $V_{SSA}$ is the device ground and substrate.

[2] The maximum $V_{DDC}$ to $V_{SSA}$ operating voltage is 60V. Users can add an external high-voltage depletion N-Channel MOSFET to operate with input voltages above 60V. See the *Operation at Voltages Above 60V* section for more details.

[3] The minimum peak voltage of the $V_{DDC}$ input AC signal with respect to $V_{SSA}$ must ensure that the $V_{DDA}$ voltage always exceeds 9V. The minimum $V_{DDC}$ peak voltage will depend upon application circuit architecture, parasitic input inductance between the AC input supply and the $V_{DDC}$ pin, and $V_{DDA}$ hold-up capacitor value.

[4] A DC supply voltage can be used to power the $V_{DDA}$ pin directly. In that case, the $V_{DDC}$ pin must be connected to $V_{SSA}$.

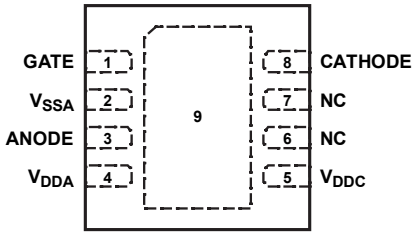
# ABSOLUTE MAXIMUM RATINGS

**Table 2. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| Supply Voltage $V_{DDC}$ | -2.0V to 60V |
| Output Voltage $V_{DDA}$ | -0.3V to 15V |
| Output Voltage GATE | -0.3V to ($V_{DDA}$ + 0.3)V |
| Input Voltage ANODE | -0.3V to 0.3V |
| Input Voltage CATHODE | -2.0V to 60V |
| Operating Ambient Temperature Range LTC4322R | -40°C to 150°C |
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (Soldering, 10 sec), MSOP | 300°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS




NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. EXPOSED PAD MAY BE LEFT OPEN OR CONNECTED TO DEVICE GROUND ($V_{SSA}$).

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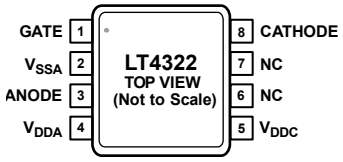
*Figure 3. DDM8 Package 8-Lead, 3mm × 3mm Plastic Side Wettable DFN. $T_{JMAX}$ = 150°C, $\theta_{JA}$ = 43°C/W. Exposed Pad (Pin 9) PCB Connection to $V_{SSA}$ is Optional*




NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

002

*Figure 4. MS8 Package 8-Lead, Plastic MSOP. $T_{JMAX}$ = 150°C, $\theta_{JA}$ = 163°C/W*

**Table 3. Pin Descriptions**

| PIN | NAME | DESCRIPTION |
|---|---|---|
| DDM Package Only | Exposed Pad | Exposed pad can be left open or connected to the device ground ($V_{SSA}$). |
| Pin 1 | GATE | GATE Drive Output. The LT4322 controls the gate of an external N-Channel MOSFET to regulate the ANODE-to-CATHODE voltage drop to 25mV. If a reverse ANODE-to-CATHODE voltage is detected, a fast pull-down circuit connects GATE to $V_{SSA}$ within 150ns, turning off the MOSFET. If the forward drop voltage exceeds 30mV, a fast pull-up circuit connects GATE to $V_{DDA}$ within 1µs, turning on the MOSFET hard. Connect to the gate of the external MOSFET. |
| Pin 2 | $V_{SSA}$ | Device Ground. This is the ground reference for the LT4322. Connect to the source of the external MOSFET. |
| Pin 3 | ANODE | External MOSFET Source Voltage Kelvin Sense Input. Connect to the source of the external MOSFET. |
| Pin 4 | $V_{DDA}$ | LDO Supply Voltage Output or Power Supply Input. The LT4322 is powered from the $V_{DDA}$ pin. The voltage on $V_{DDA}$ sets the maximum GATE drive voltage. When $V_{DDA}$ derives power from $V_{DDC}$, a 1µF or larger hold-up capacitor is required to maintain the $V_{DDA}$ voltage during the portion of the AC waveform when the $V_{DDC}$ voltage is lower than $V_{DDA}$. See the *VDDA Capacitor Selection* section for guidance in selecting the capacitor value. When powering $V_{DDA}$ directly from a DC power supply, ensure the supply voltage is |

| | | |
|---|---|---|
| | | always between 9V and 14V with respect to $V_{SSA}$ and connect a 1µF or larger ceramic bypass capacitor from $V_{DDA}$ to $V_{SSA}$. |
| Pin 5 | $V_{DDC}$ | Input Supply to LDO. This is the input supply voltage to the LDO. It replenishes the external $V_{DDA}$ hold-up capacitor when the $V_{DDC}$ voltage is higher than the $V_{DDA}$ voltage. Connect to the drain of the external MOSFET for $V_{DDC}$ to $V_{SSA}$ voltages less than or equal to 60V. For higher $V_{DDC}$ voltages, an external high-voltage depletion MOSFET is required. See the *Operation at Voltages Above 60V* section for details. If $V_{DDA}$ is powered directly with a DC power supply, connect $V_{DDC}$ to $V_{SSA}$. |
| Pin 8 | CATHODE | External MOSFET Drain Voltage Kelvin Sense Input. CATHODE is the sense pin connection to the CATHODE end of the ideal diode circuit. The voltage sensed at this pin with respect to ANODE is used to control the MOSFET gate for forward voltage regulation and reverse current turn-off. Connect to the drain of the N-Channel power MOSFET for CATHODE to $V_{SSA}$ voltages less than or equal to 60V. For higher CATHODE voltages, an external high-voltage MOSFET is required. See the *Operation at Voltages Above 60V* section for details. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

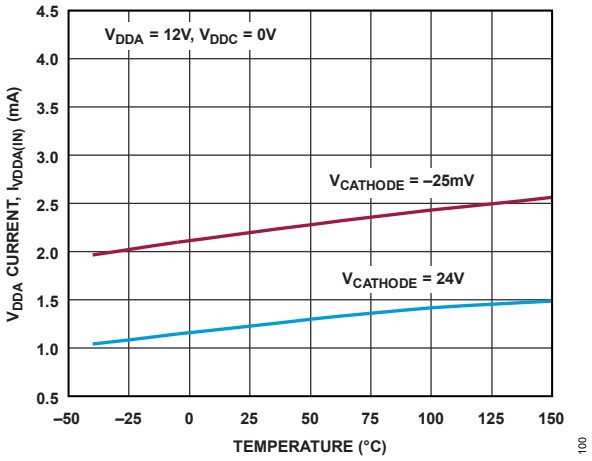



*Figure 5. $V_{DDA}$ Input Supply Current vs. Temperature*

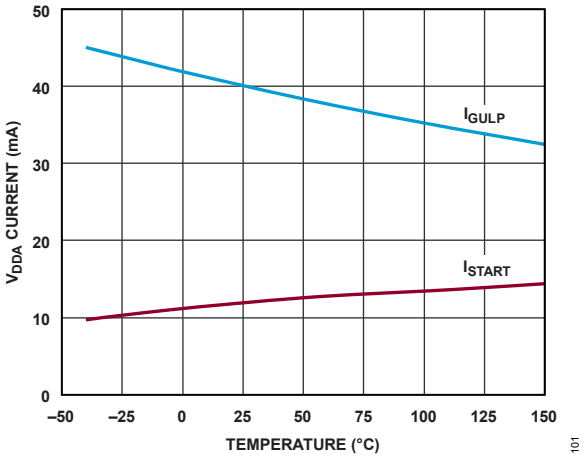



*Figure 6. $V_{DDA}$ LDO Start-Up and Gulp Current vs. Temperature*

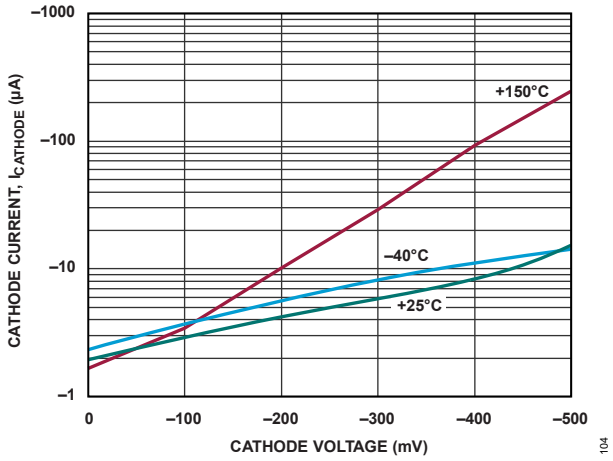



*Figure 7. CATHODE Current vs. Negative Voltage*

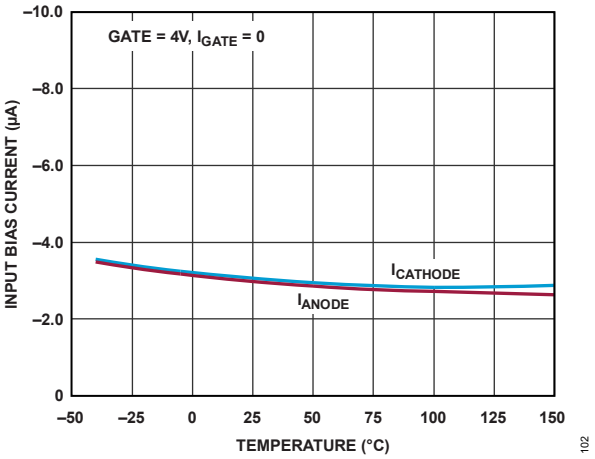



*Figure 8. Forward Regulation Input Bias Current vs. Temperature*

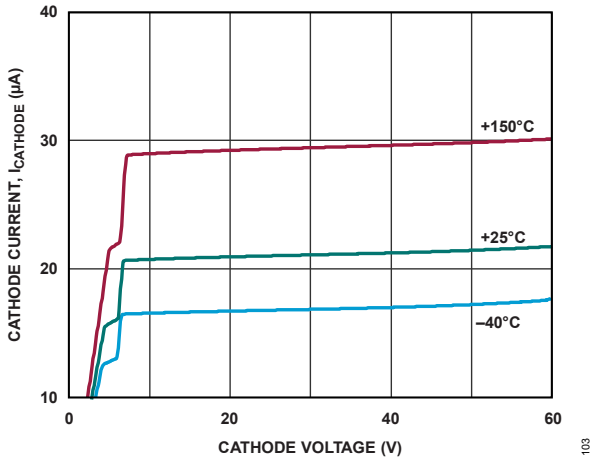



*Figure 9. CATHODE Current vs. Positive Voltage*

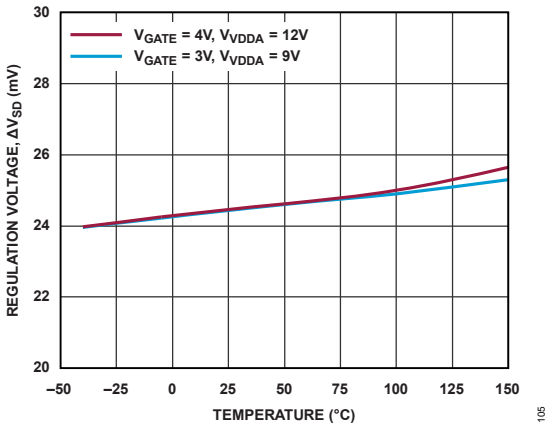



*Figure 10. ANODE–CATHODE Regulation Voltage vs. Temperature*

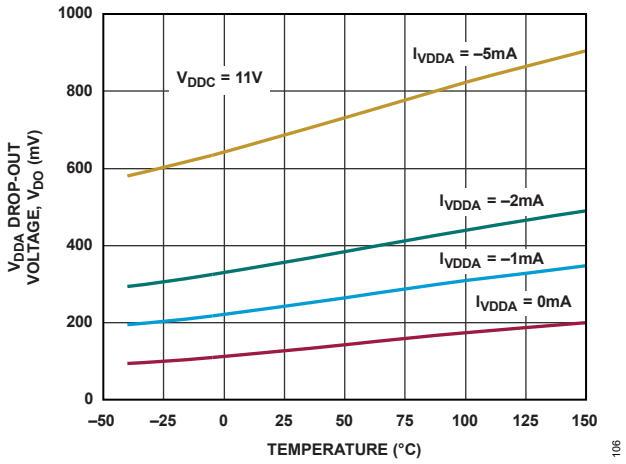



*Figure 11. $V_{DDA}$ Dropout Voltage vs. Temperature*

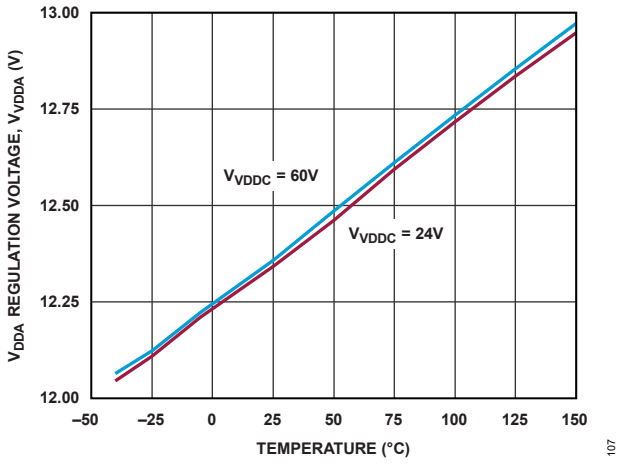



*Figure 12. $V_{DDA}$ Peak Regulation Voltage vs. Temperature*

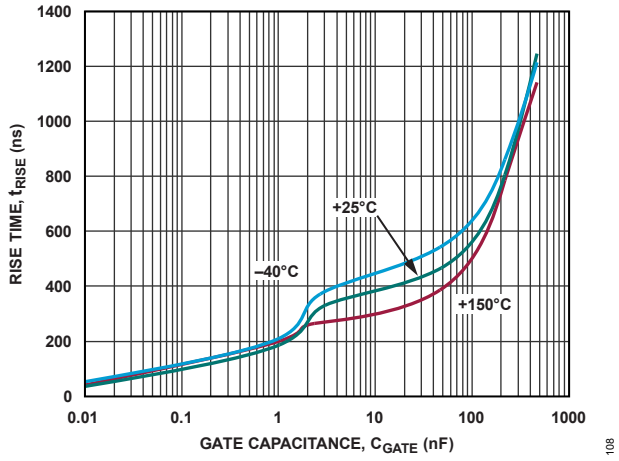



*Figure 13. GATE Rise Time vs. GATE Capacitance*

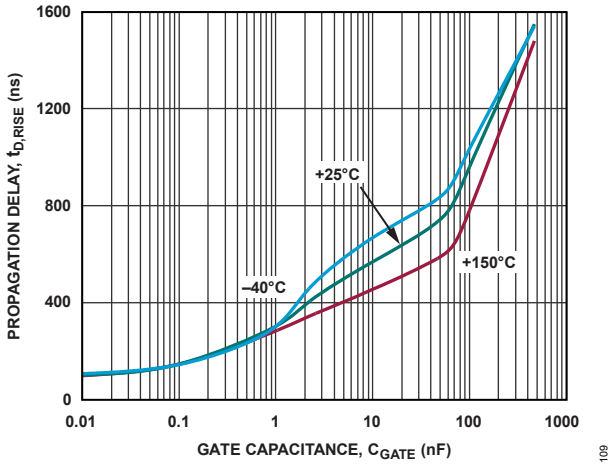



*Figure 14. GATE Rising Propagation Delay vs. GATE Capacitance*

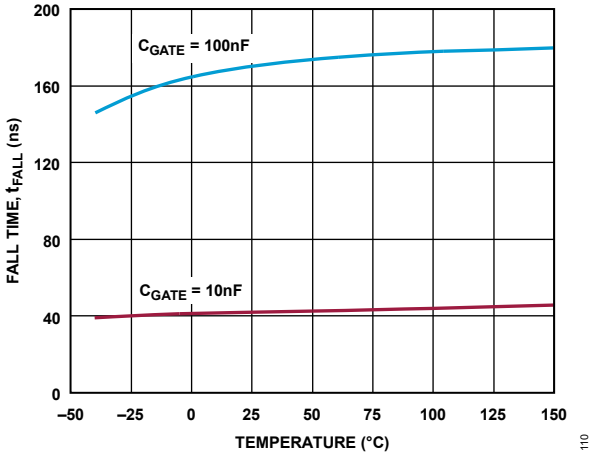



*Figure 15. GATE Fall Time vs. Temperature*

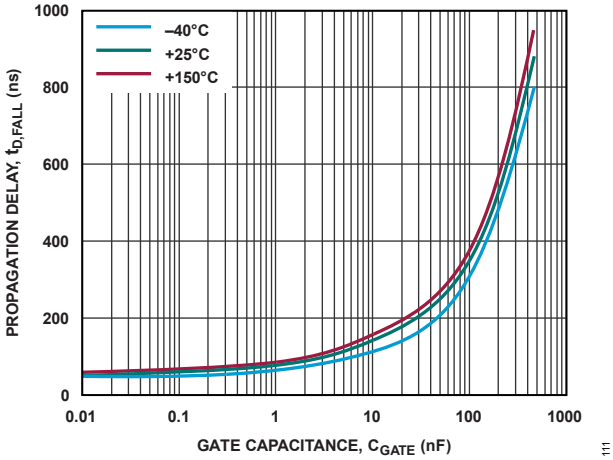



*Figure 16. GATE Falling Propagation Delay vs. GATE Capacitance*

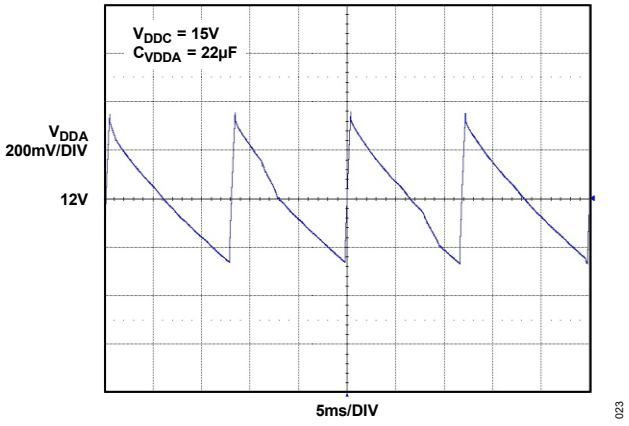



*Figure 17. $V_{DDA}$ Voltage Waveform*

# BLOCK DIAGRAM

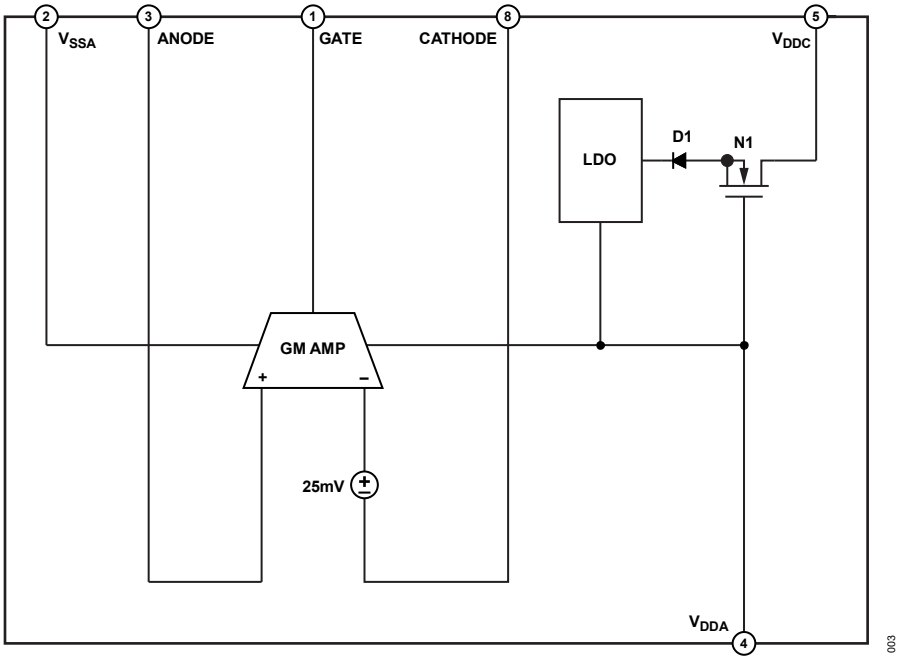



***Figure 18. Block Diagram***

# THEORY OF OPERATION

The LT4322 is a floating-ideal diode controller that operates from input power supply frequencies ranging from DC to 100kHz. Due to its floating architecture, the maximum operating voltage is limited only by the external MOSFETs in the application circuit. The operation is best understood by referring to the block diagram in *Figure 18*.

The LT4322 controls an external N-Channel MOSFET to form an ideal diode. The GM AMP senses the ANODE-to-CATHODE voltage and drives the gate of the MOSFET through the GATE pin to regulate the forward voltage to 25mV ($\Delta V_{SD}$). As the load current increases, the GATE voltage is driven higher to maintain a drop of 25mV. When the MOSFET gate is fully turned on for very large load currents, the forward drop rises linearly with the current according to $R_{DS(ON)}$ x $I_{LOAD}$. If the forward drop is less than 25mV, or if the ANODE-to-CATHODE voltage reverses, the amplifier drives the GATE voltage low to turn off the MOSFET.

During fast ANODE-to-CATHODE excursions, such as fast varying AC input signals where the GM AMP regulating loop is too slow, high-speed GATE drivers provide fast pull-up and pull-down currents capable of driving the external MOSFET on and off quickly. This rectifies the input signal similarly to a diode but with significantly less power dissipation.

## Powering the LT4322

The GM AMP and fast pull-up currents are powered from the $V_{DDA}$ pin. $V_{DDC}$ powers an internal LDO, whose output is $V_{DDA}$. The LT4322 draws power from $V_{DDC}$ and regulates 12V on $V_{DDA}$.

For AC applications, the LDO draws power from $V_{DDC}$ during the reverse mode of operation when the $V_{DDC}$ voltage exceeds the $V_{DDA}$ voltage. An external hold-up capacitor is required between $V_{DDA}$ and $V_{SSA}$ to power the LT4322 while in the forward mode of operation, where the $V_{DDC}$ voltage is very low.

For DC input supplies, $V_{DDC}$ must be driven from a DC supply voltage that is at least 9.5V higher than the ANODE/$V_{SSA}$ voltage. Alternatively, $V_{DDA}$ can also be driven directly from a DC power supply whose voltage ranges from 9V to 14V above $V_{SSA}$. In this case, the LDO is not used, and users must connect $V_{DDC}$ to $V_{SSA}$.

Internal undervoltage lockout (UVLO) circuitry drives the GATE pin to $V_{SSA}$ until $V_{DDA}$ has enough voltage to operate properly. During this time, there is still a conduction path from input to output via the body diode of the external MOSFET.

## Steady-State Operation

*Figure 19* shows the MOSFET gate and output voltage waveforms in steady-state operation for the full-bridge rectifier circuit shown in *Figure 20.* The input power supply waveform $V_{IN}$ is a $120V_{RMS}$, 60Hz sine wave. As $V_{IN}$ nears its peak voltage on positive half cycles, bottom side gate VBG1 and top side gate VTG1 are driven 12V above their respective $V_{SSA}$ voltages, turning on M1 and M2 and charging $V_{OUT}$ to the peak $V_{IN}$ voltage. On negative half-cycles, bottom-side gate VBG2 and top-side gate VTG2 are driven 12V above their respective $V_{SSA}$ voltages, turning on M3 and M4 and charging $V_{OUT}$ to the peak $V_{IN}$ voltage.

Power MOSFETs M1 to M4 conduct high current to the output with a much lower forward voltage drop than a Schottky diode, resulting in much higher efficiency and a lower temperature rise.

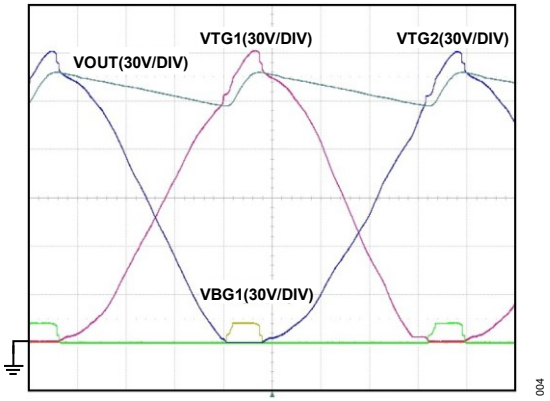



***Figure 19. Full-Bridge Waveforms in Steady State***

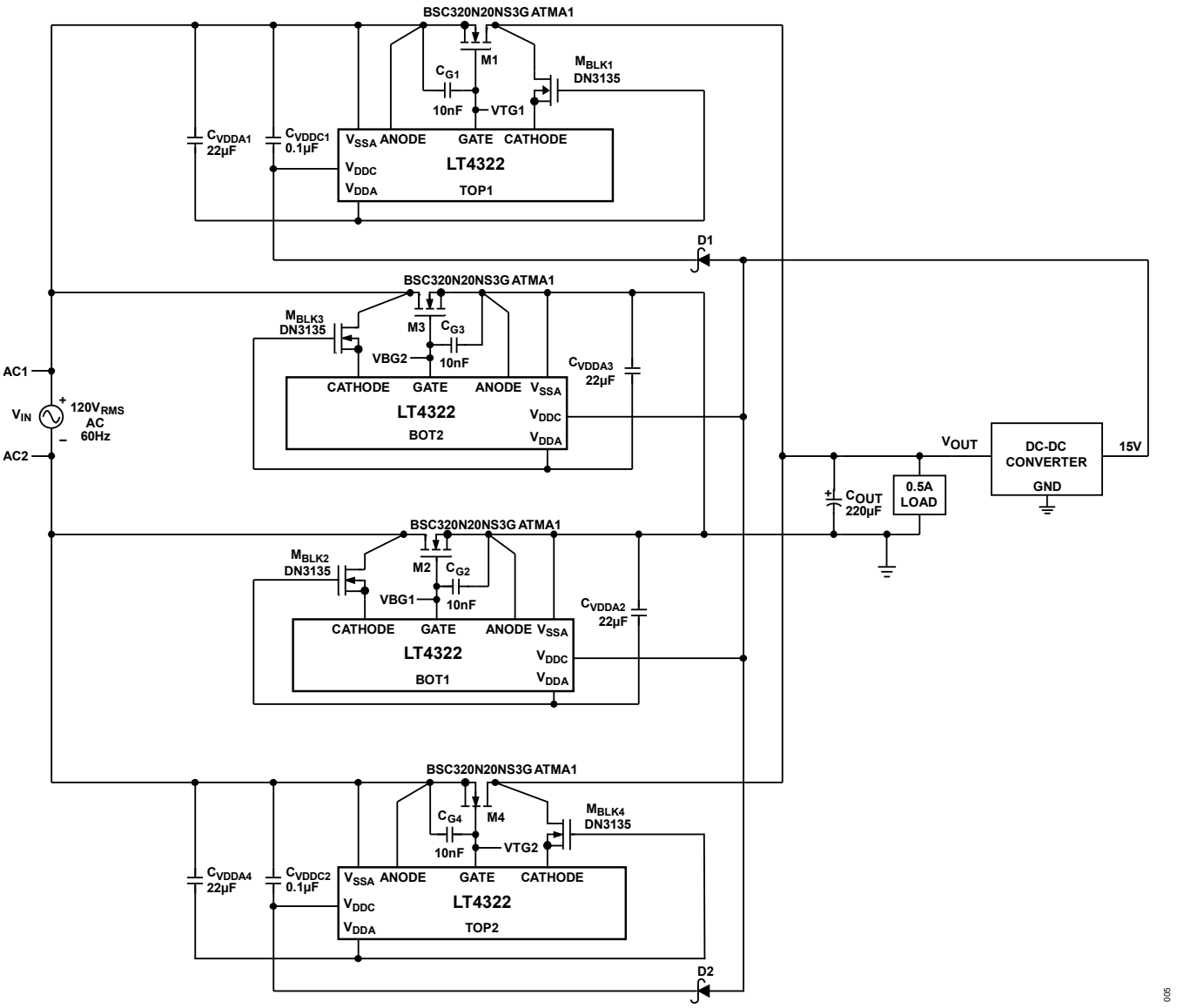



*Figure 20. Four-Diode, High-Voltage Full-Bridge Application, 120$V_{RMS}$, 60Hz*

## APPLICATIONS INFORMATION

Electronic systems that receive power from an AC power source often employ half-wave rectifier, full-wave rectifier, or full bridge circuits to convert an AC input current to a DC output current. High-availability systems employ parallel-connected DC power supplies or battery feeds to achieve redundancy and enhance system reliability. Schottky diodes are often used in these AC and DC applications. The chief disadvantage of Schottky and rectifier diodes is their significant forward voltage drop and resulting power and efficiency loss. The LT4322 solves these problems by using an N-Channel MOSFET as a low-loss pass element to emulate the behavior of a diode. *Figure 21* shows the LT4322 in a half-wave rectifier application.

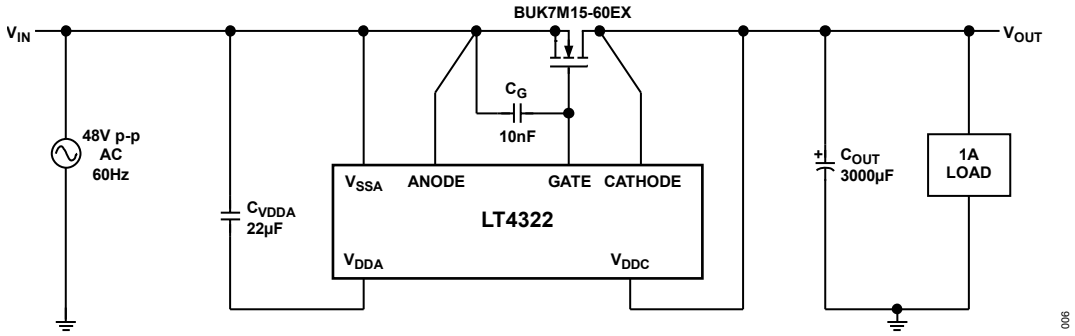



***Figure 21. LT4322 in a 48$V_{P-P}$, 60Hz, 1A Half-Wave Rectifier Application***

The LT4322 eliminates thermal design problems and costly heat sinks by maximizing available voltage and reducing power dissipation, which greatly improves efficiency and reduces PC board area. The LT4322 operates with input frequencies ranging from DC to 100kHz. Thanks to its floating architecture, the maximum operating voltage is limited only by the voltage ratings of the external MOSFETs in the particular application circuit where it is used. The following sections cover power-on, ideal diode operation, external component selection, a design example, and recommended PCB layout techniques.

## $V_{DDA}$ Capacitor Selection

In its primary applications, the LT4322 draws its input power from the $V_{DDC}$ pin and generates a 12V supply voltage between $V_{DDA}$ and $V_{SSA}$. For AC input supply voltages, the $V_{DDC}$ voltage is nearly zero during the forward bias phase of the AC cycle. The LT4322 draws its power from a reservoir capacitor, $C_{VDDA}$, during that time. Choose $C_{VDDA}$ as follows:

$$C_{VDDA}(\mu F) = 1{,}500 \times t \quad (1)$$

where t is the period of the AC input supply. Use capacitors with the appropriate voltage rating and temperature coefficient to ensure that the true capacitance matches the value in equation 1. In low-frequency applications having large MOSFET gate capacitance and/or high output current, use a 0.1µF ceramic capacitor in parallel with $C_{VDDA}$ for high-frequency bypassing. Place the 0.1µF capacitor as close to the $V_{DDA}$ and $V_{SSA}$ pins as possible. For frequencies greater than 200Hz where $C_{VDDA}$ will most likely be a ceramic capacitor, $C_{VDDA}$ is sufficient, and a parallel ceramic capacitor is not needed.

When powering $V_{DDC}$ with a DC input supply, connect a 1µF or larger capacitor between $V_{DDA}$ and $V_{SSA}$. When powering $V_{DDA}$ with a DC input supply, connect a 1µF or larger capacitor between $V_{DDA}$ and $V_{SSA}$ and connect $V_{DDC}$ to $V_{SSA}$.

## MOSFET Selection

The LT4322 drives N-Channel MOSFETs to conduct the load current. The important characteristics of the MOSFET are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, $BV_{DSS}$, the gate threshold voltage $V_{GS(TH)}$, the continuous body diode current rating $I_S$ and the single pulse avalanche energy rating $E_{DS,AL(R)}$.

The maximum allowable drain-source voltage, $BV_{DSS}$, must be higher than the maximum CATHODE-to-ANODE voltage seen in the application circuit. For half-wave rectifier applications, the full peak-to-peak AC input voltage appears across the MOSFET when the input voltage is at its minimum value. For full-wave rectifier applications, each of the four MOSFETs sees one-half of the peak-to-peak input voltage. An avalanche-rated MOSFET ensures robustness during momentary drain-to-source overvoltage conditions.

The MOSFET's on-resistance, $R_{DS(ON)}$, directly affects the forward voltage drop and power dissipation during heavy load. The desired forward voltage drop should be less than that of a diode for reduced power dissipation; 100mV is a good starting point. Given the average output load current $I_{AVG}$, choose a MOSFET for DC inputs which has:

$$R_{DS(ON)} < 100\ mV/I_{AVG} \quad (2)$$

For AC full-bridge rectifier applications, use:

$$R_{DS(ON)} < 100\ mV/(3 \times I_{AVG}) \quad (3)$$

The AC input calculation assumes the duration of the current conduction occupies 1/3 of the AC period.

For very high output current applications, users may connect several MOSFETs in parallel to reduce the overall $R_{DS(ON)}$. The LT4322's high-speed transconductance (GM AMP) amplifier is capable of driving up to 100nF MOSFET gate capacitance at frequencies up to 100kHz. At initial power-up, the application output capacitance is initially charged via the body diode of the power MOSFET until the LT4322 has enough supply voltage to properly control the MOSFET gate. Ensure the MOSFET has a sufficient continuous body diode current rating $I_S$ to handle the current at startup.

The LT4322's GATE drive ranges from 10V to 14V when powered from $V_{DDC}$ input supply voltages greater than or equal to 15V. When powered directly from $V_{DDA}$, the GATE drive voltage equals the $V_{DDA}$ voltage. $V_{GS(TH)}$ must be a minimum of 2V or higher. A gate threshold voltage lower than 2V is not recommended because too much time is needed to discharge the gate below the threshold and halt reverse current conduction when the input AC voltage falls below the CATHODE output voltage.

## GATE Capacitor Selection

The GM amplifier is optimally compensated with 10nF capacitance between the gate and source of the external power MOSFET. For applications using MOSFETs with $C_{ISS}$ less than 10nF and/or when voltage peaking is observed in the GATE waveform, adding a 10nF ceramic capacitor $C_{GATE}$ directly across the gate and source of the external power MOSFET can greatly improve the stability of the forward regulation voltage. This comes at the expense of the added charge needed to enhance the gate of the external MOSFET. For high output current and/or high frequency applications where the circuit is rarely in forward regulation, this capacitor can be omitted.

## Output Capacitor $C_{OUT}$ Selection

Capacitance $C_{OUT}$ is needed across the application output voltage and system ground to provide the output load current for the majority of the AC period. Downstream power needs and voltage ripple tolerance determine how much capacitance is required. $C_{OUT}$ in the hundreds to thousands of microfarads is common. A combination of electrolytic and ceramic capacitors is used to optimize capacitance ESR while minimizing cost. Add a 1µF ceramic capacitor from the output to the ground near the LT4322 if the bulk electrolytic capacitors are physically remote from the LT4322.

For full-wave rectifier applications, a good starting point is selecting $C_{OUT}$ such that:

$$C_{OUT} \geq I_{AVG}/(V_{RIPPLE} \times 2 \times Freq) \quad (4)$$

Where $I_{AVG}$ is the average output load current, $V_{RIPPLE}$ is the maximum tolerable output ripple voltage, and Freq is the frequency of the AC input source. For example, in a 60Hz, 24V application where the load current is 1A and the tolerable ripple is 15V, choose:

$$C_{OUT} \geq 1A/(15V \times 2 \times 60Hz) = 556\mu F \quad (5)$$

For half-wave rectifier applications, use:

$$C_{OUT} \geq I_{AVG}/(V_{RIPPLE} \times Freq) \quad (6)$$

Users must also ensure that the RMS current in the electrolytic capacitors does not exceed the maximum ripple current rating so that the capacitor's lifetime is not compromised. An electrolytic capacitor's ripple current rating is a function of RMS current, frequency, and ambient temperature. Consult the manufacturer's specifications and ensure

that the selected device is suited to operate within the required frequency, temperature, and load current of the application.

## Input Snubber

A small percentage of application circuits may suffer from undamped oscillations due to the parasitic input inductance and any input bypass capacitance $C_{IN}$. In those cases, utilize an RC snubber network, as shown in *Figure 22*, to prevent oscillations. Users must estimate their parasitic inductance $L_{IN}$ and choose a resistor $R_{SN}$ according to the following equation:

$$R_{SN} = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (7)$$

Choose $C_{SN}$ as follows:

$$C_{SN} = 2 \times \pi \times \sqrt{L_{IN} \times C_{IN}} / R_{SN} \quad (8)$$

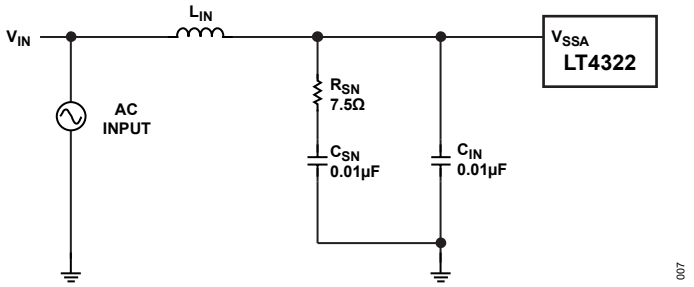



***Figure 22. Input Snubber Circuitry***

## Operation at Voltages Above 60V

An extra blocking device is necessary to protect the $V_{DDC}$ and/or CATHODE pins when the peak-to-peak AC input voltage exceeds 120V for full-wave rectifier and full-bridge applications. The blocking device is also needed when the peak-to-peak AC voltage exceeds 60V for half-wave rectifier applications and when the DC input voltage exceeds 60V for DC input applications. Depletion N-Channel MOSFET M2 in *Figure 23* extends the input operating voltage range to 600V. It safely clamps the $V_{DDC}$ and CATHODE voltages to about 2V higher than the $V_{DDA}$ voltage. M2 must be a depletion mode device whose $V_{GS(OFF)} \approx$ -2.5V and $I_{DSS} \geq$ 75mA to ensure the circuit starts up and regulates properly. Power MOSFET M1 must also be rated to handle the maximum input voltage. The DN3765 depletion MOSFET comes in a large package due to its 600V rating. Depletion MOSFETs rated for lower voltages (e.g., 350V) are available in smaller packages.

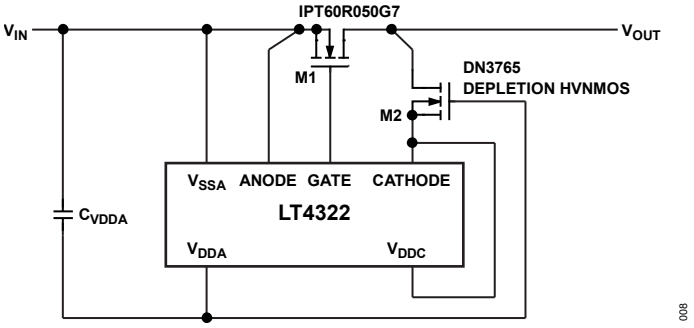



***Figure 23. M1 $BV_{DSS}$ Selection and Addition of Depletion Mode MOSFET, M2, Extends Operating Range to 600V***

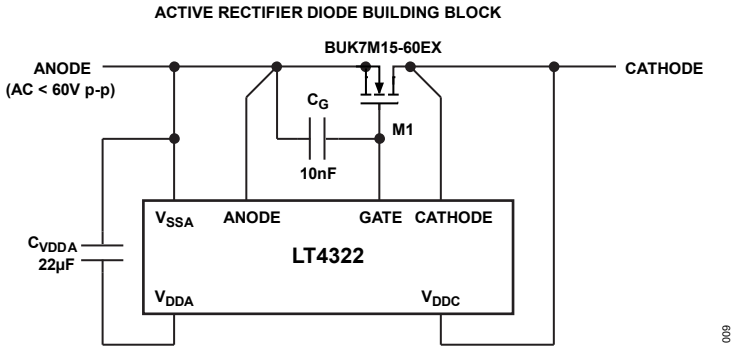



*Figure 24. LT4322 Active Rectifier Diode Building Block*

## Design Example

*Figure 24* shows an LT4322 building block circuit that replaces a Schottky or rectifier diode in AC rectification applications. This building block can be used to construct half-wave rectifiers, full-wave rectifiers, and full bridge rectifiers. The following example shows how to choose components for a 60Hz, $24V_{RMS}$ full-bridge application circuit with a 2A average output load current. The AC input is applied to the ANODE.

A $24V_{RMS}$ input waveform is typically 34V peak and 68V peak-to-peak. In a full-bridge application, each power MOSFET has a maximum drain-to-source voltage that is half of the peak-to-peak voltage, or 34V in this case. Choose a power MOSFET using equation (3).

$$R_{DS(ON)} < 100\ mV/(3 \times 2A) = 16.7m\Omega \qquad (9)$$

The BUK7M15-60E is a good choice for this application, with its 60V drain-to-source voltage rating and 13mΩ typical $R_{DS(ON)}$ at $V_{GS}$ = 10V. Additionally, its minimum threshold voltage $V_{GS(TH)}$ of 2.4V ensures that the LT4322 will be able to turn it off quickly to prevent reverse conduction when the ANODE voltage falls below the CATHODE voltage.

Because the BUK7M15-60E's $C_{ISS}$ is much lower than 10nF, a 10nF capacitor $C_G$ is connected between the gate and source of the power MOSFET for optimal compensation of the LT4322's transconductance amplifier.

Choose a hold-up cap for a 60Hz input waveform:

$$C_{VDDA}(\mu F) = 1{,}500 \times (1/60Hz) = 25\mu F \qquad (10)$$

Rounding to the nearest standard value capacitor, a 22µF, 25V electrolytic capacitor is chosen.

## PCB Layout Considerations

Special attention should be given to the PC board layout to ensure a stable and efficient application circuit. *Figure 25* shows a representative 2-layer PCB to outline some of the primary considerations. U1 is the LT4322, M1 is the power MOSFET, and M2 is the depletion MOSFET.

Connect the ANODE, $V_{SSA}$, and CATHODE as close as possible to the MOSFET source and drain pins. Use a Kelvin connection from the ANODE pin to the source of the external MOSFET. Lay out the ANODE and $V_{SSA}$ connections so that the $V_{SSA}$ currents are minimized in the ANODE connection. Keep the drain and source traces to the MOSFET wide and short to minimize parasitic resistance. Keep the trace from the LT4322 GATE pin to the MOSFET gate short and wide. This practice will reduce the chance of MOSFET parasitic oscillations. Locate the GATE trace near the ANODE side of the circuit, not the CATHODE side, in order to minimize coupling from the CATHODE connection to the GATE. Place the $C_{VDDA}$ as close as possible to the $V_{DDA}$ and $V_{SSA}$ pins. Use short, wide traces to connect $C_{VDDA}$ to $V_{DDA}$ and $V_{SSA}$.

For applications utilizing a 10nF $C_G$ capacitor, locate $C_G$ as close as possible to the power MOSFET. Place output bulk capacitors close to the drains and sources of the power MOSFETs. Use a large power plane to minimize the parasitic inductance in the CATHODE-to-ANODE circuit pathways of the LT4322s.

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check the creepage and clearance guidelines to determine if this is an issue. To increase the effective pin spacing between high voltage and ground pins, leave the exposed pad connection open. Use no-clean flux to minimize PCB contamination.

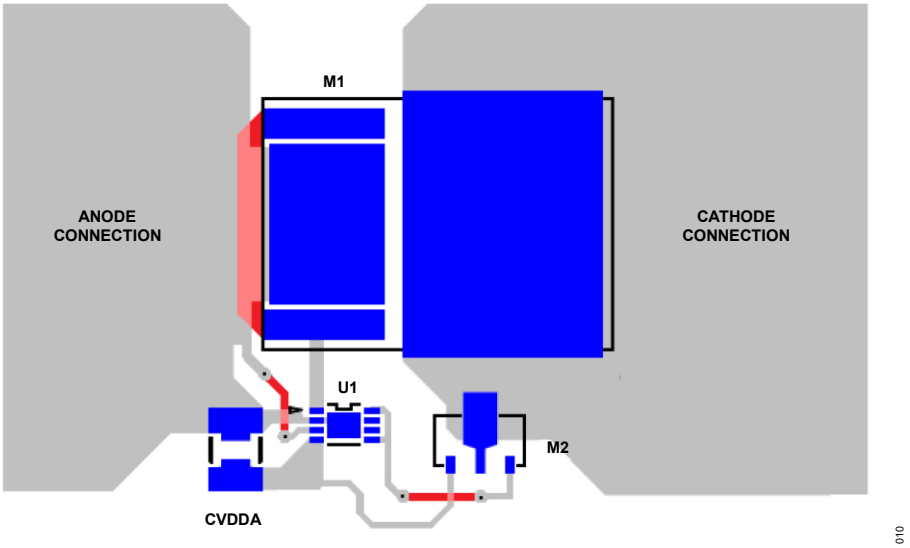



***Figure 25. Recommended PCB Layout***

## Reverse Recovery

The LT4322 responds very quickly to reverse bias conditions, minimizing reverse current and reverse charge. The waveforms in *Figure 26* illustrate the reverse recovery time. Initially, the LT4322 is driving the gate of the external power MOSFET to 12V. The current waveform indicates that 3A is flowing in the forward direction from ANODE to CATHODE. A controlled change in current is used to force reverse current through the power MOSFET at a rate of 100A/µs. In this example, the LT4322 MOSFET gate is fully turned off 50ns after the reverse current is detected, resulting in a peak reverse current of -3A. The LT4322 turns off even large MOSFETs within 300ns of a sudden reverse bias condition.

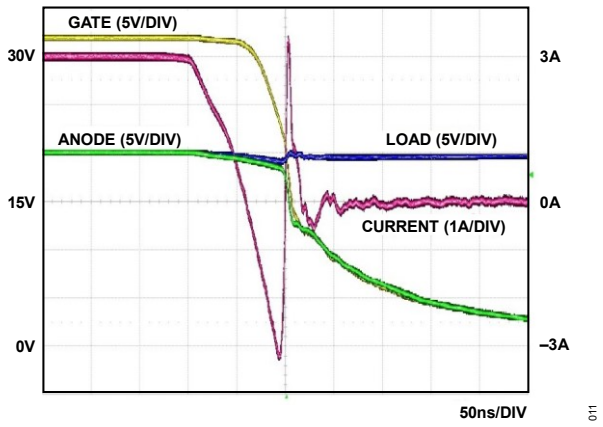



***Figure 26. Reverse Recovery Waveforms***

## Capacitively Loaded Full-Bridge Applications and $V_{DDA}$ Refresh Currents

In the capacitively loaded full-bridge application circuit shown in *Figure 34*, the positive and negative terminals of the AC input supply are high impedance with respect to $V_{OUT}$ and load ground at various points of the AC cycle. When an LT4322 draws current from its $V_{DDC}$ pin to refresh its $V_{DDA}$ reservoir capacitor, the AC input supply terminal voltages can jump several Volts with respect to ground to provide a return path for the refresh current. The waveforms in *Figure 27* illustrate this behavior. Note that the AC input supply differential voltage (AC1–AC2) remains smooth and continuous despite the AC1 and AC2 voltages jumping with respect to the load ground.

To prevent this behavior, power each LT4322 from a circuit that is always low impedance during the time it is refreshing the $V_{DDA}$ capacitor. *Figure 20* in the Operation section shows one such circuit. That circuit is redrawn in *Figure 28*, with only LT4322 TOP1 and LT4322 TOP2 shown for simplicity. A DC-DC converter generates a 15V supply with respect to ground to power the $V_{DDC}$ pins of LT4322 BOT1 and LT4322 BOT2 (not shown). For LT4322 TOP1 and LT4322 TOP2, using a Schottky diode with the 15V supply forms a charge pump circuit with the AC input supply terminal connected to $V_{SSA}$. The charge pump generates a $V_{DDC}$ voltage that is 15V relative to $V_{SSA}$.

When the AC input nears its peak positive voltage on each AC cycle, LT4322 TOP1 turns on M1 to charge $V_{OUT}$. Turning on M1 also completes a low-impedance circuit that causes the 15V supply to replenish LT4322 TOP2's $V_{DDC}$ and $V_{DDA}$ voltages. Likewise, when the AC input nears its peak negative voltage on each AC cycle, LT4322 TOP2 turns on M2 to charge $V_{OUT}$. Turning on M2 also completes a low-impedance circuit that causes the 15V supply to replenish LT4322 TOP1's $V_{DDC}$ and $V_{DDA}$ voltages. Capacitors $C_{VDDC1}$ and $C_{VDDC2}$ prevent the $V_{DDC}$ voltages from overcharging due to leakage during the remainder of the AC input cycle. Using a high-efficiency DC-DC converter to power $V_{DDC}$ to 15V improves overall efficiency by minimizing the power losses in the LT4322, and associated depletion MOSFETs, if present.

*Figure 29* shows the resulting waveforms when the LT4322s are powered in this manner. Note that there are no voltage steps in the AC1 and AC2 waveforms.

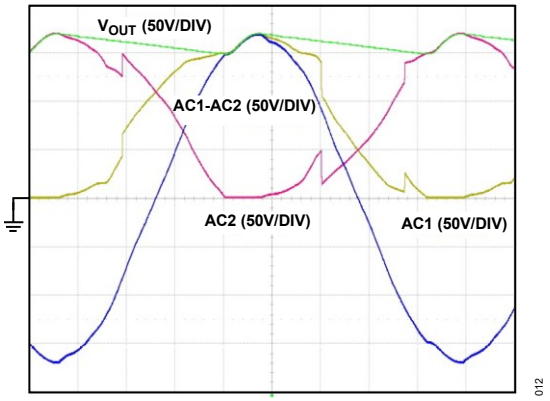



***Figure 27. Full Bridge AC Input Waveforms (AC1, AC2) Shows Common-Mode Voltage Steps due to $V_{DDA}$ Refresh Current***

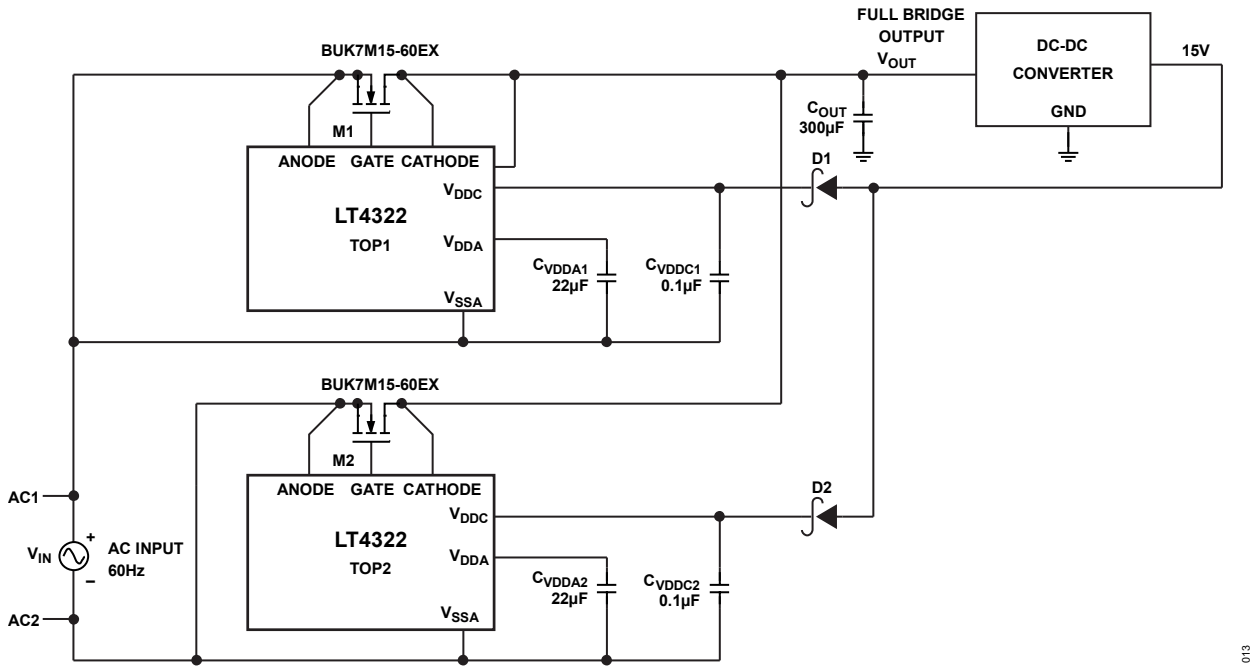



***Figure 28. $V_{DDC}$ Power Scheme Synchronizes Refresh Current and Improves $I_{CC}$ Power Dissipation in Full-Bridge Applications***

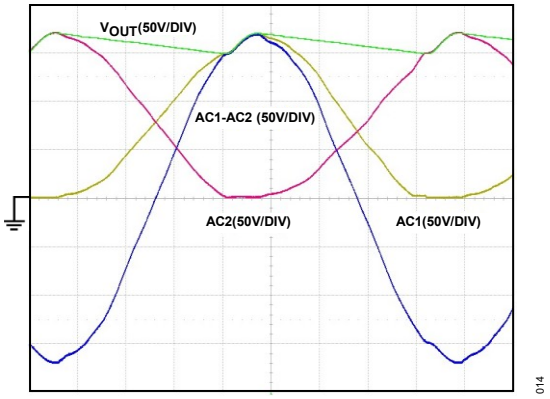



***Figure 29. Full Bridge AC Input Waveforms (AC1, AC2) Shows Improved Common-Mode Voltage due to Synchronizing $V_{DDA}$ Refresh Current***

## DC Diode-OR Application

*Figure 30* shows two LT4322s in a DC diode-OR application. The application prioritizes the input supply having the higher voltage and generates a low-loss path from that input to $V_{OUT}$ while blocking the lower voltage input from $V_{OUT}$.

Because of the DC nature of this application, the $V_{DDC}$ pin rarely exceeds 12V relative to $V_{SSA}$. Since this is needed to refresh the voltage on the capacitor connected to the $V_{DDA}$, the LT4322 does not power up or stay powered. To power the LT4322s, a floating supply with a negative reference tied to $V_{OUT}$ is needed. A good choice for this is a flyback converter, as shown in *Figure 30*.

*Figure 30* shows that the lower voltage input supply must be capable of sinking 2mA average quiescent current from the LT4322 $V_{SSA}$ pin. If input supplies are not capable of sinking this current, use a two-output flyback converter and power each LT4322's $V_{DDC}$ pin from its own dedicated supply voltage, as shown in *Figure 31*.

## Very High Input Reverse Voltage Blocking

The LT4322 can withstand reverse battery voltages on its $V_{SSA}$ input due to its floating architecture, as long as the CATHODE and $V_{DDC}$ pin voltages never exceed 60V with respect to $V_{SSA}$. For example, in *Figure 31*, the $V_{IN1}$ and $V_{IN2}$ inputs can be safely connected to reverse voltages as high as ($V_{OUT}$ – 60V). The use of a high-voltage depletion MOSFET to protect CATHODE, as shown in *Figure 23*, along with an appropriately rated power MOSFET, extends the maximum tolerable reverse voltage rating to the $BV_{DSS}$ ratings of the MOSFETs. This feature is especially useful in high-voltage DC diode-OR applications; if a high-voltage battery is plugged in backwards, no damage is done to the system, and the diode-OR output voltage is not perturbed.

# TYPICAL APPLICATIONS

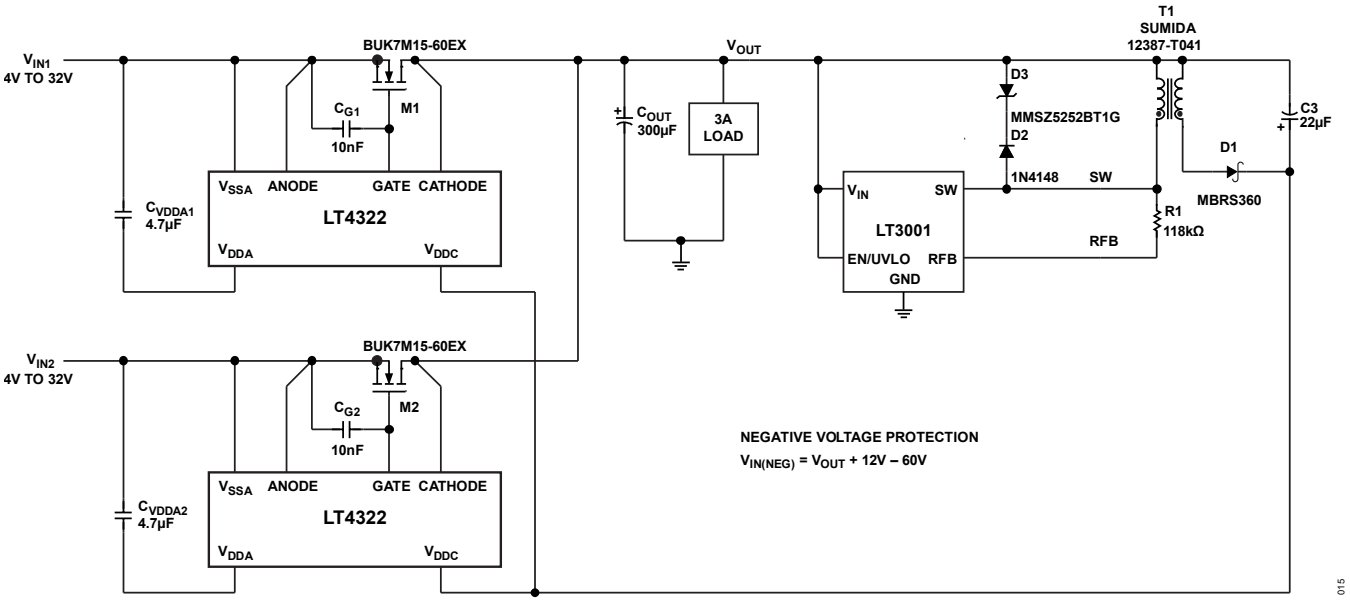



***Figure 30. DC Diode-OR Application Circuit: Flyback Circuitry Provides Refresh Power to Floating-Ideal Diode Architecture***

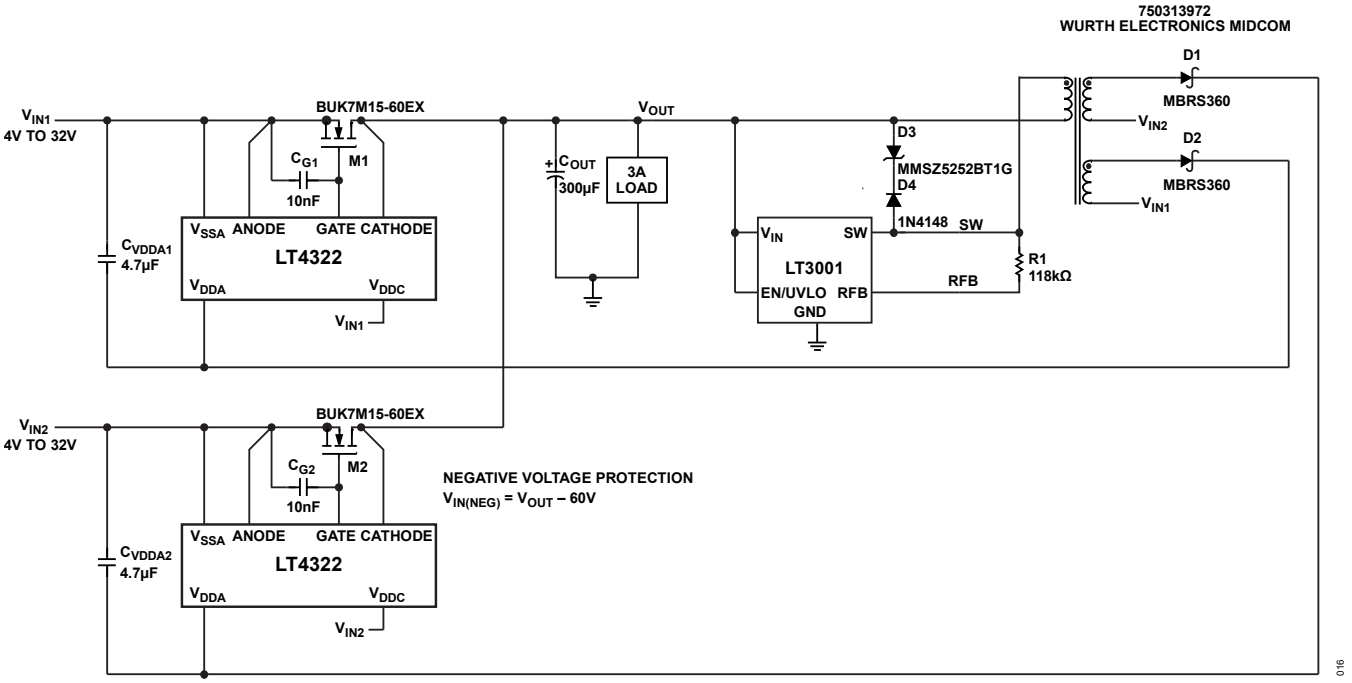



*Figure 31. DC Diode-OR Application Circuit for Battery Applications where ICC Generated Reverse Current is Problematic. Dual Output Flyback Converter Provides Power for Each Input Without Generating Reverse Current into $V_{IN1}$ and $V_{IN2}$.*

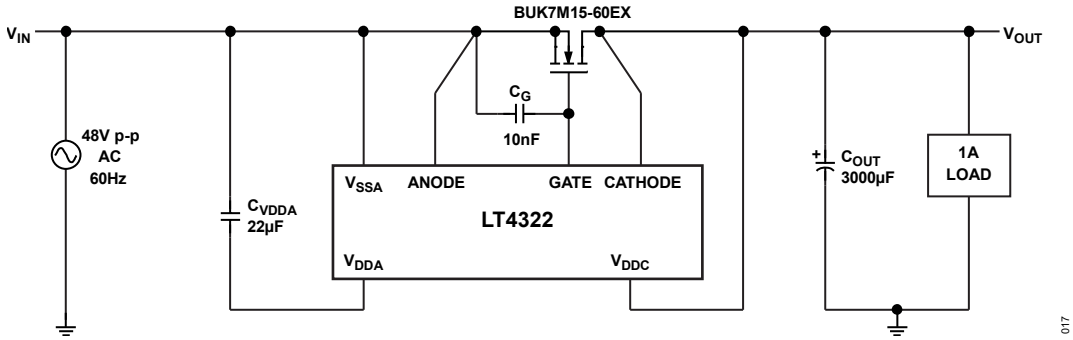



*Figure 32. Single-Diode, Half-Wave Rectifier Application Circuit, $48V_{P-P}$, 60Hz, 1A*

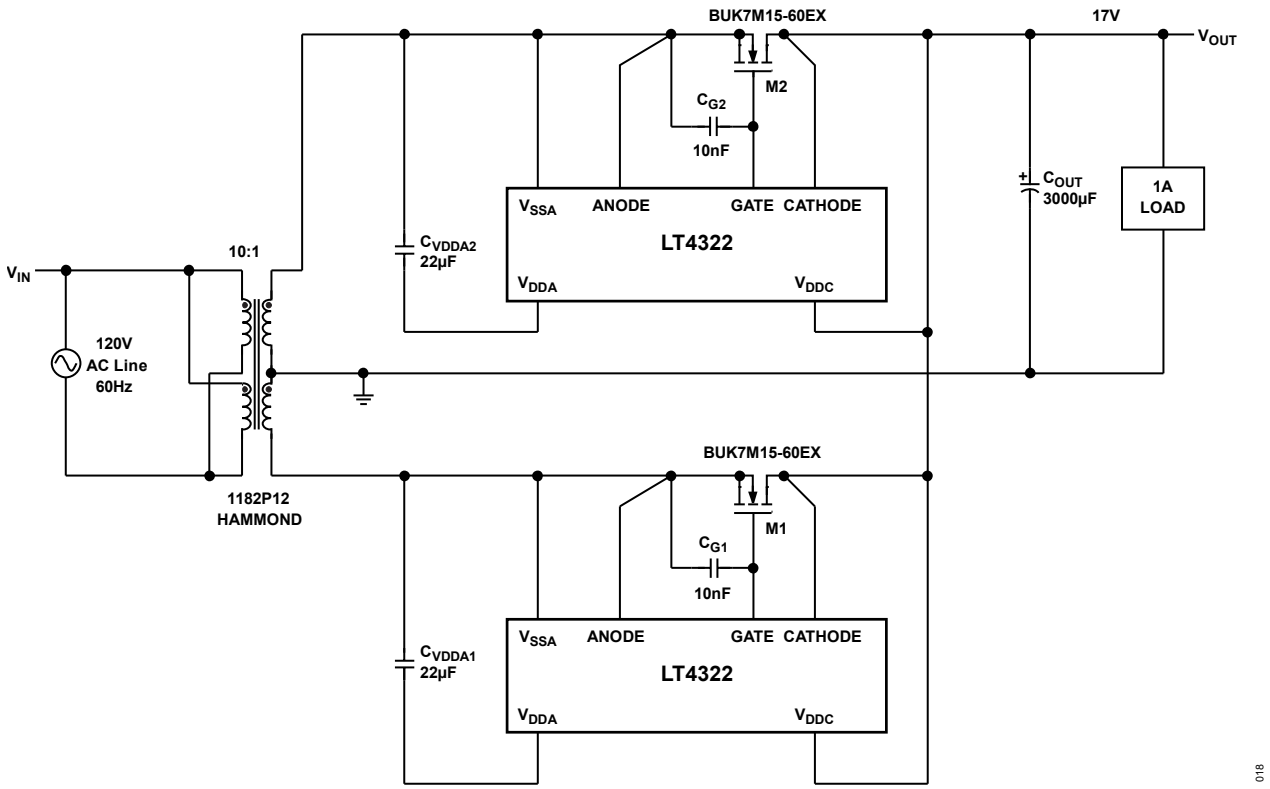



*Figure 33. Two Diode, Full-Wave Rectifier with Center-Tapped Transformer, 120V, 60Hz Line Input, 17V DC Output*

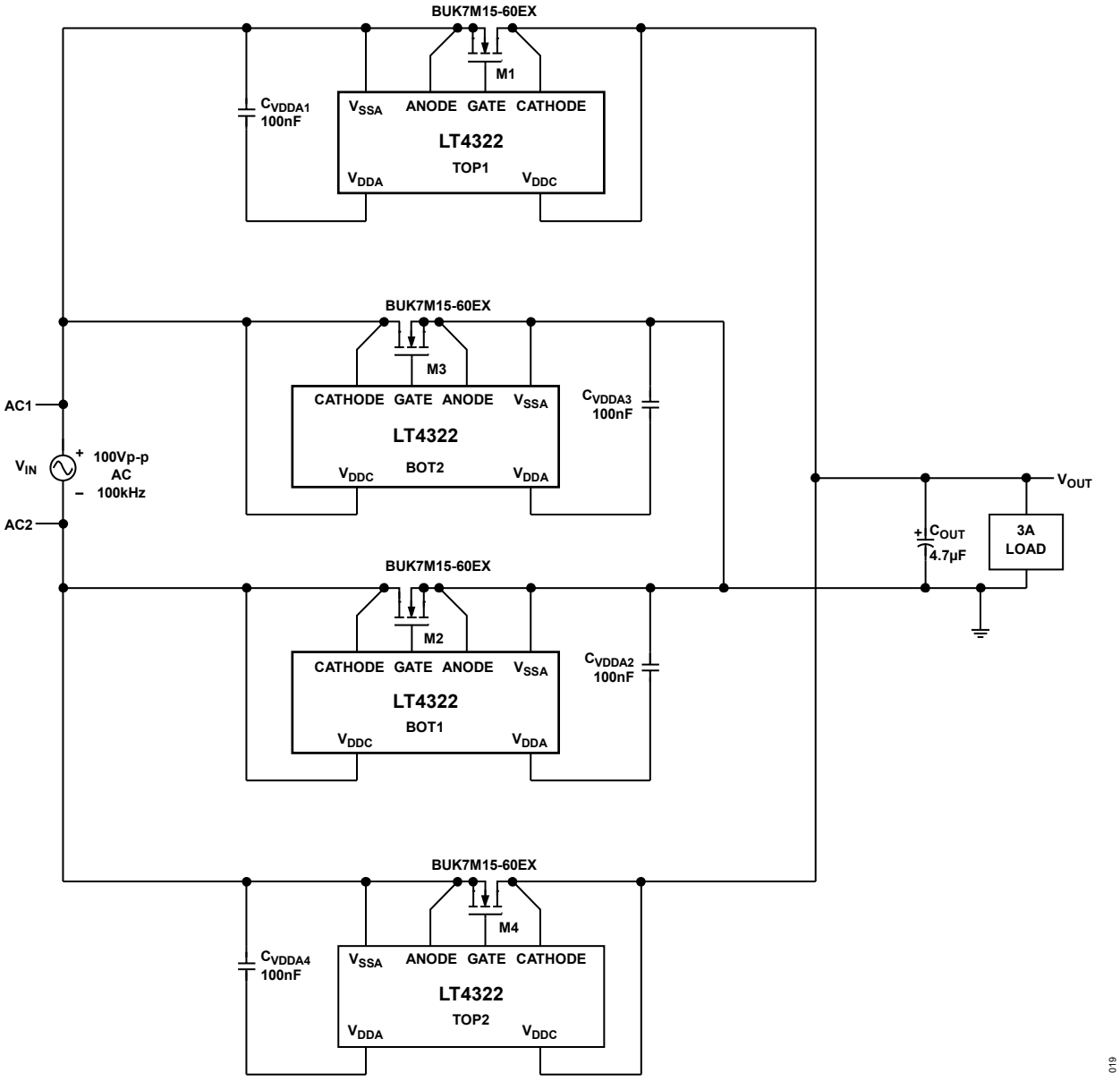



*Figure 34. High-Speed Four-Diode Full-Bridge Application Circuit, 100$V_{P-P}$, 100kHz, 3A*

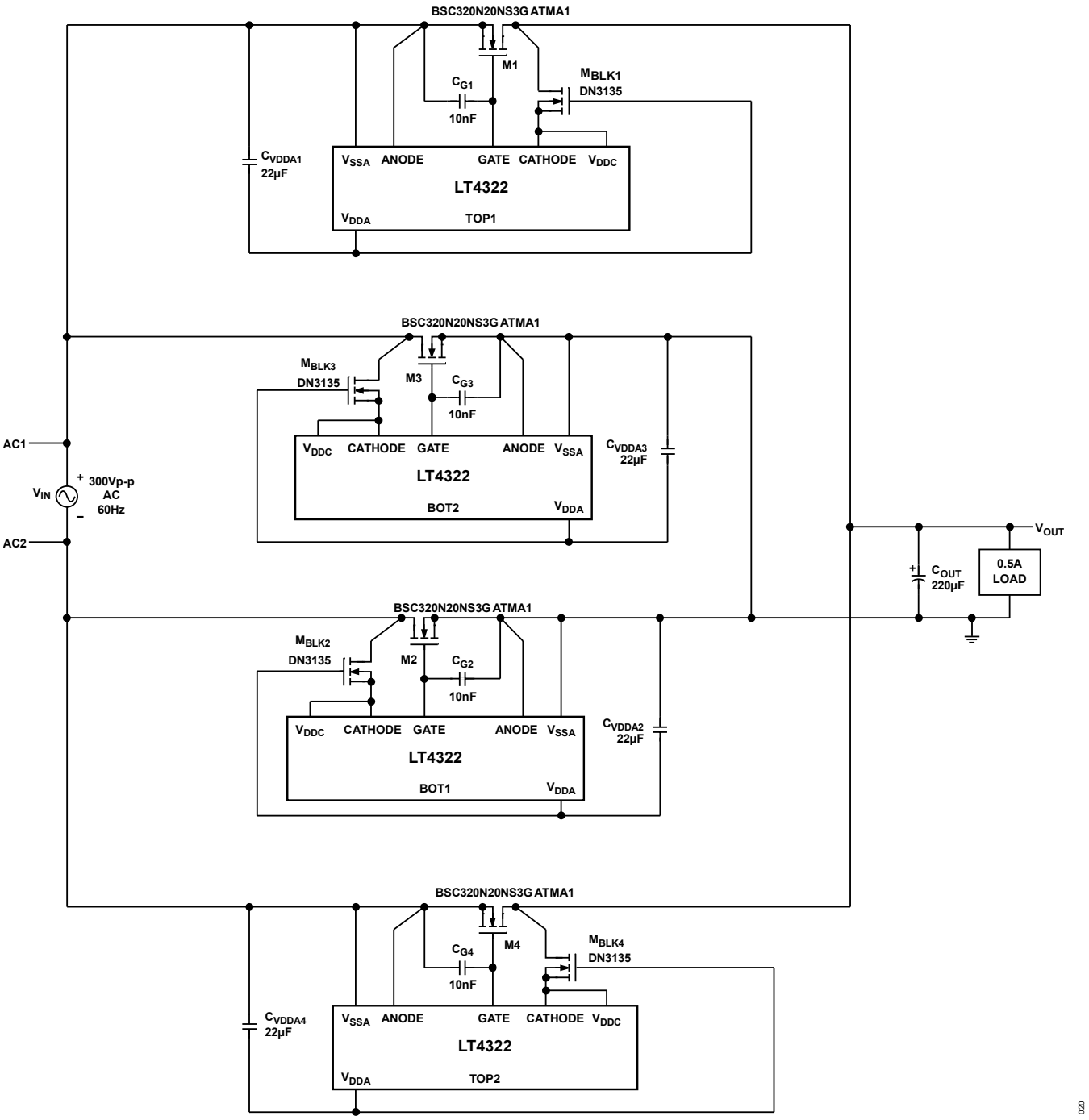



*Figure 35. High-Voltage Four-Diode Full-Bridge Application Circuit, 300$V_{P-P}$, 60Hz, 0.5A*

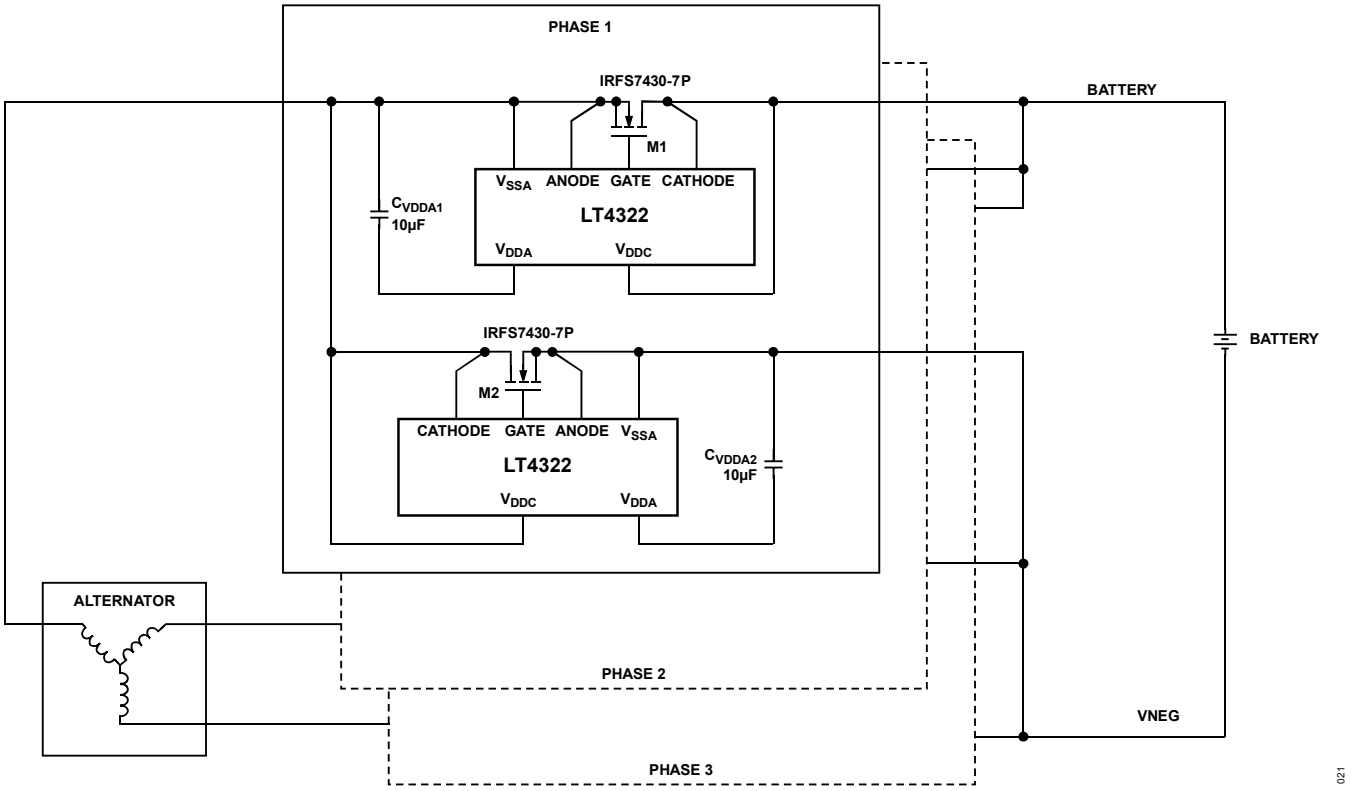
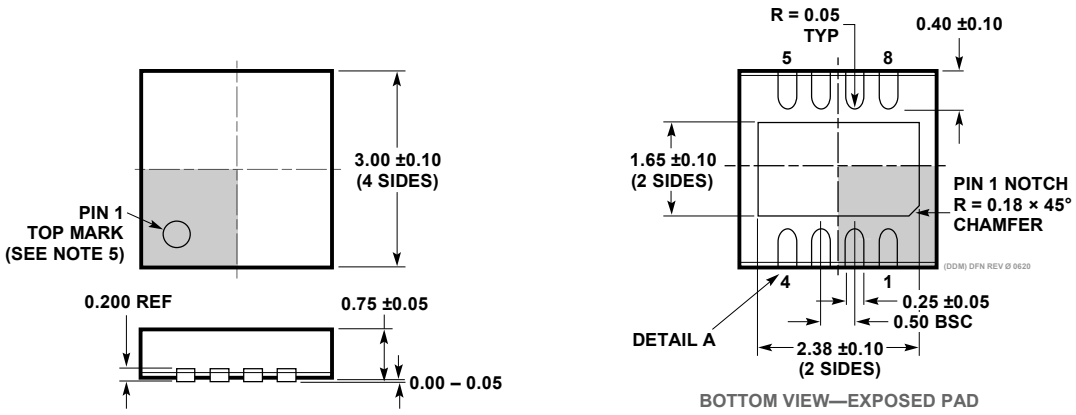


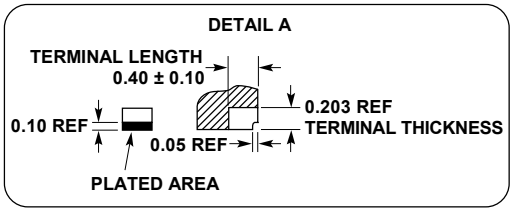

*Figure 36. Six LT4322's in a 3-Phase Alternator Application*

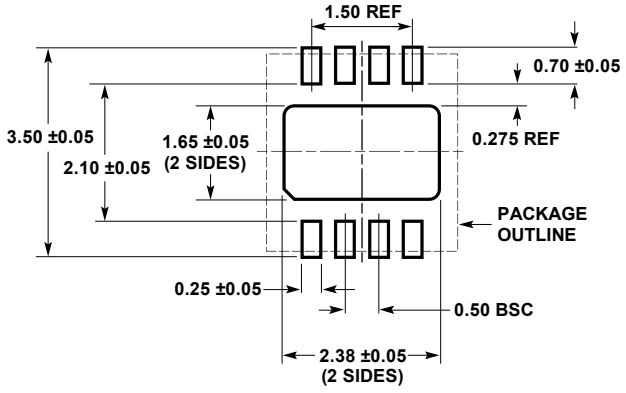
# OUTLINE DIMENSIONS

**DDM Package**
**8-Lead Plastic Side Wettable DFN (3mm × 3mm)**
**(Reference LTC DWG # 05-08-7009 Rev Ø)**




NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

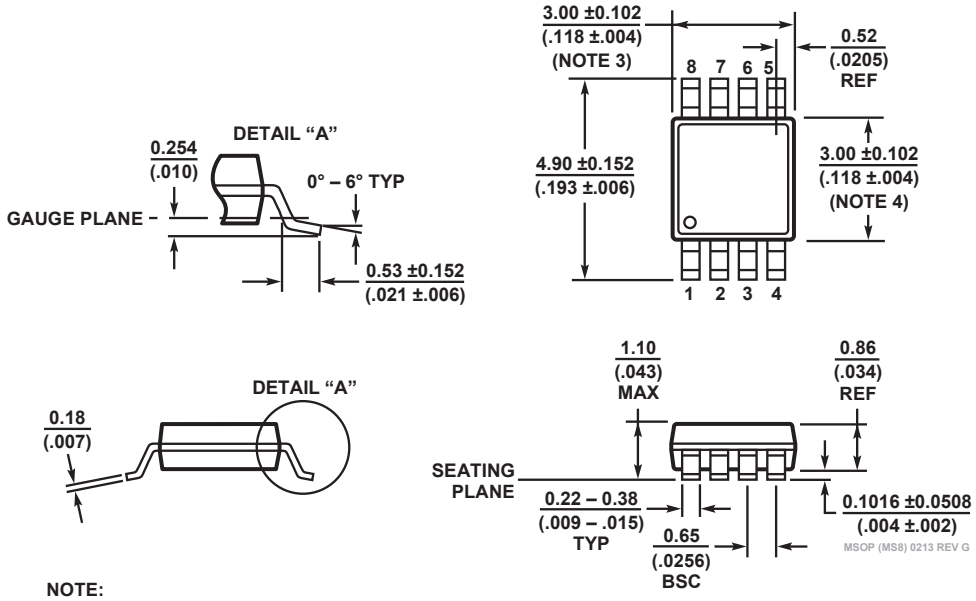



05-08-7009

*Figure 37. 8-Lead, 3mm x 3mm, Side Wettable DFN*

**MS8 Package**
**8-Lead Plastic MSOP**
**(Reference LTC DWG # 05-08-1660 Rev G)**




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

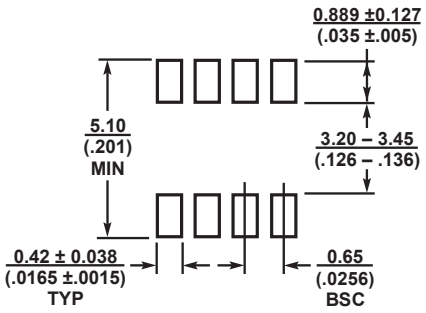



***Figure 38. 8-Lead MSOP***

# ORDERING GUIDE

**Table 4. Ordering Guide**

| TUBE | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT4322RDDM#PBF | LT4322RDDM#TRPBF | LHPK | 8-Lead, (3mm × 3mm) Plastic DFN | –40°C to 150°C |
| LT4322RMS8#PBF | LT4322RMS8#TRPBF | LTHPM | 8-Lead, Plastic MSOP | –40°C to 150°C |

For more information on tape and reel specifications, go to: *http://www.adi.com/tapeandreel/*

# RELATED PARTS

**Table 5. Related Parts**

| Part Number | Description | Comments |
|---|---|---|
| *LT4320/LT4320 -1* | Ideal Diode Bridge Controller | Controls N-Channel MOSFETs, 9V to 72V Operation, DC to 600Hz |
| *LTC4353* | Dual Low Voltage Ideal Diode Controller | Controls Two N-Channel MOSFETs, 0V to 18V Operation |
| *LTC4355* | Positive Voltage Diode-OR Controller and Monitor | Controls Two N-Channel MOSFETs, 0.4µs Turn-Off, 80V Operation |
| *LTC4357* | Positive High Voltage Ideal Diode Controller | Controls Single N-Channel MOSFET, 0.5µs Turn-Off, 80V Operation |
| *LTC4358* | 5A Ideal Diode | Internal N-Channel MOSFET, 9V to 26.5V Operation |
| *LTC4359* | Ideal Diode Controller with Reverse Input Protection | Controls N-Channel MOSFET, 4V to 80V Operation, –40V Reverse Input |
| *LTC4364* | Surge Stopper with Ideal Diode | 4V to 80V Operation, –40V Reverse Input, –20V Reverse Output |
| *LTC4371* | Dual Negative Voltage Ideal Diode-OR Controller and Monitor | Controls Two MOSFETs, 220ns Turn-Off, Withstands > ±300V Transients |
| *LTC4376* | 7A Ideal Diode Controller with Reverse Input Protection | Internal N-Channel MOSFET, 4V to 40V Operation, –40V Reverse Input |
| *LT8672* | Active Rectifier Controller with Reverse Protection | 3V to 40V Operation, -40V Reverse Input, Rectifies $6V_{P-P}$ to 50kHz, $2V_{P-P}$ to 100kHz, 20µA Operating Current, 3.5µA Shutdown Current |

# EVALUATION BOARDS

**Table 6. Evaluation Boards**

| Model | Description |
|---|---|
| DC3117A | Half-Wave Active Rectifier Evaluation Board |
| DC3137A | Full-Wave Active Rectifier Evaluation Board |

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

DC3117A DC3137A LT4322RDDM#PBF LT4322RDDM#TRPBF LT4322RMS8#PBF LT4322RMS8#TRPBF