

## Evaluating the ADGS2414D 0.56 $\Omega$ On Resistance High Density Octal SPST Switch

### FEATURES

- ▶ SPI with error detection
  - ▶ Includes CRC, invalid read and write addresses, and SCLK count error detection
- ▶ Analog supply voltages
  - ▶ Dual supply:  $\pm 4.5$  V to  $\pm 16.5$  V
  - ▶ Single supply: 5 V to 20 V
- ▶ PC control in conjunction with the evaluation software
- ▶ [EVAL-SDP-CB1Z \(SDP-B\)](#) system demonstration platform

### EVALUATION BOARD KIT CONTENTS

- ▶ EV-ADGS2414DSDZ evaluation board

### DOCUMENTS NEEDED

- ▶ [ADGS2414D](#) data sheet

### EQUIPMENT NEEDED

- ▶ [EVAL-SDP-CB1Z \(SDP-B\)](#) controller board
- ▶ DC voltage source
  - ▶  $\pm 16.5$  V (dual supply)
  - ▶ 20 V (single supply)
- ▶ Optional 3.3 V digital logic supply
- ▶ Analog signal source
- ▶ Method to measure voltage, such as a digital multimeter (DMM)

### SOFTWARE NEEDED

- ▶ [ACE](#) software with EV-ADGS2414DSDZ plugin

### GENERAL DESCRIPTION

The EV-ADGS2414DSDZ is the evaluation board for the ADGS2414D. The ADGS2414D is an octal SPST switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read and write address detection, and SCLK count error detection. The ADGS2414D also supports burst mode, which decreases the time between SPI commands.

[Figure 1](#) shows the EV-ADGS2414DSDZ in a typical evaluation setup. The EV-ADGS2414DSDZ is controlled by the system demonstration platform (SDP) [EVAL-SDP-CB1Z \(SDP-B\)](#), which connects to a PC via a USB port. The ADGS2414D is in the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides users with a defined digital logic-supply voltage, if required. Alternatively, the digital logic-supply voltage can be supplied from the [SDP-B](#). The [EVAL-SDP-CB1Z \(SDP-B\)](#) controller board is available to order on the Analog Devices, Inc., website.

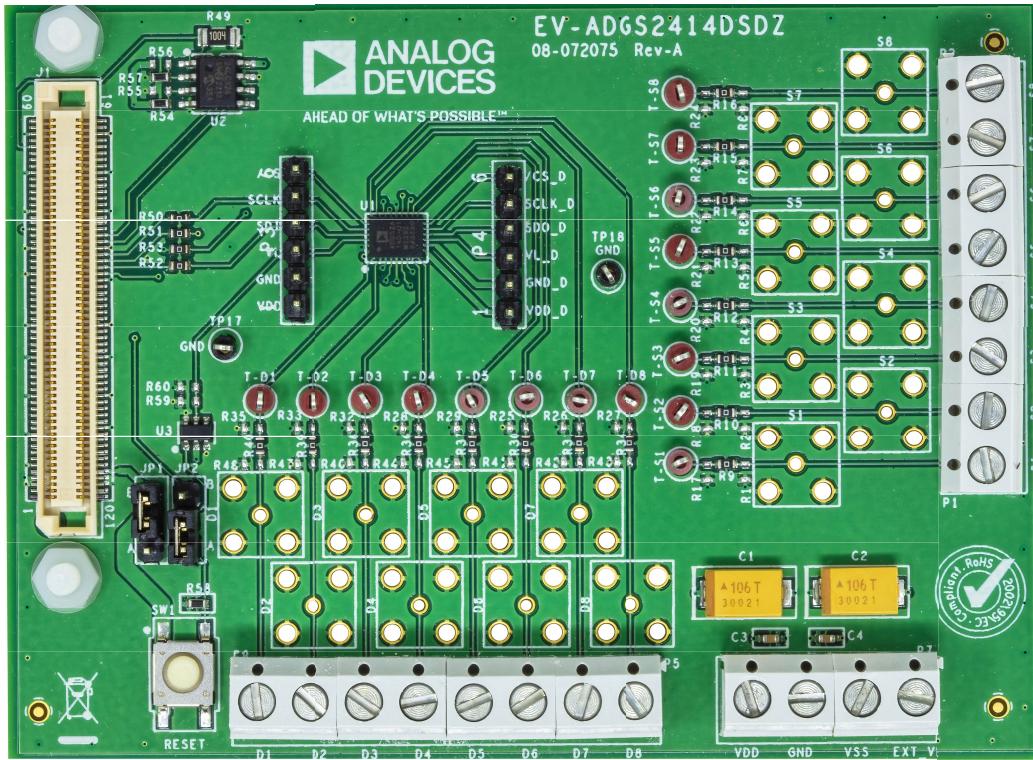
For full details on the ADGS2414D, refer to the ADGS2414D data sheet, which should be consulted in conjunction with this user guide when using the EV-ADGS2414DSDZ.

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**REVISION HISTORY****12/2023—Revision 0: Initial Version**

## EVALUATION BOARD PHOTOGRAPH



**Figure 1. EV-ADGS2414DSDZ Evaluation Board Photograph**

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## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

The P7 connector provides access to the supply pins of the ADGS2414D.  $V_{DD}$ , GND, and  $V_{SS}$  on P7 link to the appropriate pins on the ADGS2414D. For dual-supply voltages, the EV-ADGS2414DSDZ can be powered from  $\pm 4.5$  V to  $\pm 16.5$  V. For single-supply voltages, the GND and  $V_{SS}$  terminals must be connected together and can power the EV-ADGS2414DSDZ with 5 V to 20 V. Additionally, 3.3 V is supplied to the  $\overline{\text{RESET}}/V_L$  pins of the ADGS2414D by the **SDP-B** controller board when the JP1 link is in Position B. When controlling the ADGS2414D by a method other than the **SDP-B** controller board, supply between 2.7 V and 5.5 V to the  $\overline{\text{RESET}}/V_L$  pins of the ADGS2414D via the EXT\_VL screw terminal input on P7. Ensure JP1 is in Position A.

### INPUT SIGNALS

The P1, P2, P5, and P6 screw connectors connect to both the source and drain pins of the ADGS2414D. Additional subminiature version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain sides of the EV-ADGS2414DSDZ includes two sets of 0603 pads that can place a load on the signal path to the ground. A  $0\ \Omega$  resistor is placed in the signal path and can be replaced with a user-defined value. The resistor and the 0603 pads create a simple RC filter.

### LINK OPTIONS

Ensure that the link options provided on the EV-ADGS2414DSDZ are set for the required operating conditions before using the evaluation board. **Table 1** details the positions of the links to control the evaluation board via the **SDP-B** controller board using a PC and external power supplies. The functions of these link options are detailed in **Table 2**.

When using the **SDP-B** controller board in conjunction with the EV-ADGS2414DSDZ, place JP1 in Position B to avoid damage to the **SDP-B**.

**Table 1. Link Options for SDP-B Control (Default)**

Link Number	Option
JP1	B
JP2	B

### ROUTE THROUGH PINS FOR DAISY CHAINS

The P3 and P4 headers allow access to the route through pins of the ADGS2414D. Use the P3 and P4 headers to daisy-chain multiple EV-ADGS2414DSDZ devices together. To daisy-chain the EV-ADGS2414DSDZ devices, connect  $\overline{CS}_D$ ,  $SCLK_D$ , and  $SDO_D$  on P4 of one EV-ADGS2414DSDZ to  $\overline{CS}$ ,  $SCLK$ , and  $SDI$  on P3 of the next EV-ADGS2414DSDZ.  $V_L$ , GND, and  $V_{DD}$  can also be shared between these evaluation boards via the P3 and P4 headers. However, because  $V_{SS}$  is only accessible from P7, connect  $V_{SS}$  to each daisy-chained EV-ADGS2414DSDZ.

**Table 2. Link Functions**

Link Number	Function
JP1	The JP1 link selects the source of the $V_L$ voltage supplied to the ADGS2414D. Position A selects EXT_VL from P7. Position B selects 3.3 V from the <b>SDP-B</b> controller board.
JP2	The JP2 link selects how a hardware reset is performed. Position A indicates the SW1 push-button performs a hardware reset. Position B indicates the <b>SDP-B</b> controller board performs a hardware reset.

## EVALUATION BOARD SOFTWARE

### INSTALLING THE SOFTWARE

The EV-ADGS2414DSDZ uses the Analog Devices [Analysis, Control, Evaluation \(ACE\)](#) software. [ACE](#) is a desktop software application that allows users to evaluate and control multiple evaluation systems.

The [ACE](#) installer installs the necessary SDP drivers and .NET Framework 4 by default. Install [ACE](#) before connecting to the [SDP-B](#) controller board. The full instructions on how to install and use the [ACE](#) software can be found on the Analog Devices website at [www.analog.com/ace](http://www.analog.com/ace).

After [ACE](#) is installed, the EV-ADGS2414DSDZ plugin appears when opening the application.

### INITIAL SET UP

To set up the EV-ADGS2414DSDZ, complete the following steps:

1. Connect the EV-ADGS2414DSDZ to the [SDP-B](#) controller board via the 120-pin connector.
2. Connect the [SDP-B](#) controller board to the computer using the USB cable provided with the [SDP-B](#).
3. Power the EV-ADGS2414DSDZ as described in the [Power Supplies](#) section.
4. Run the [ACE](#) application. The EV-ADGS2414DSDZ plugin appears in the [Attached Hardware](#) section of the [Start](#) tab.
5. Double click the **ADGS2414D Board** evaluation board plugin to open the ADGS2414D chip view, as shown in [Figure 2](#).

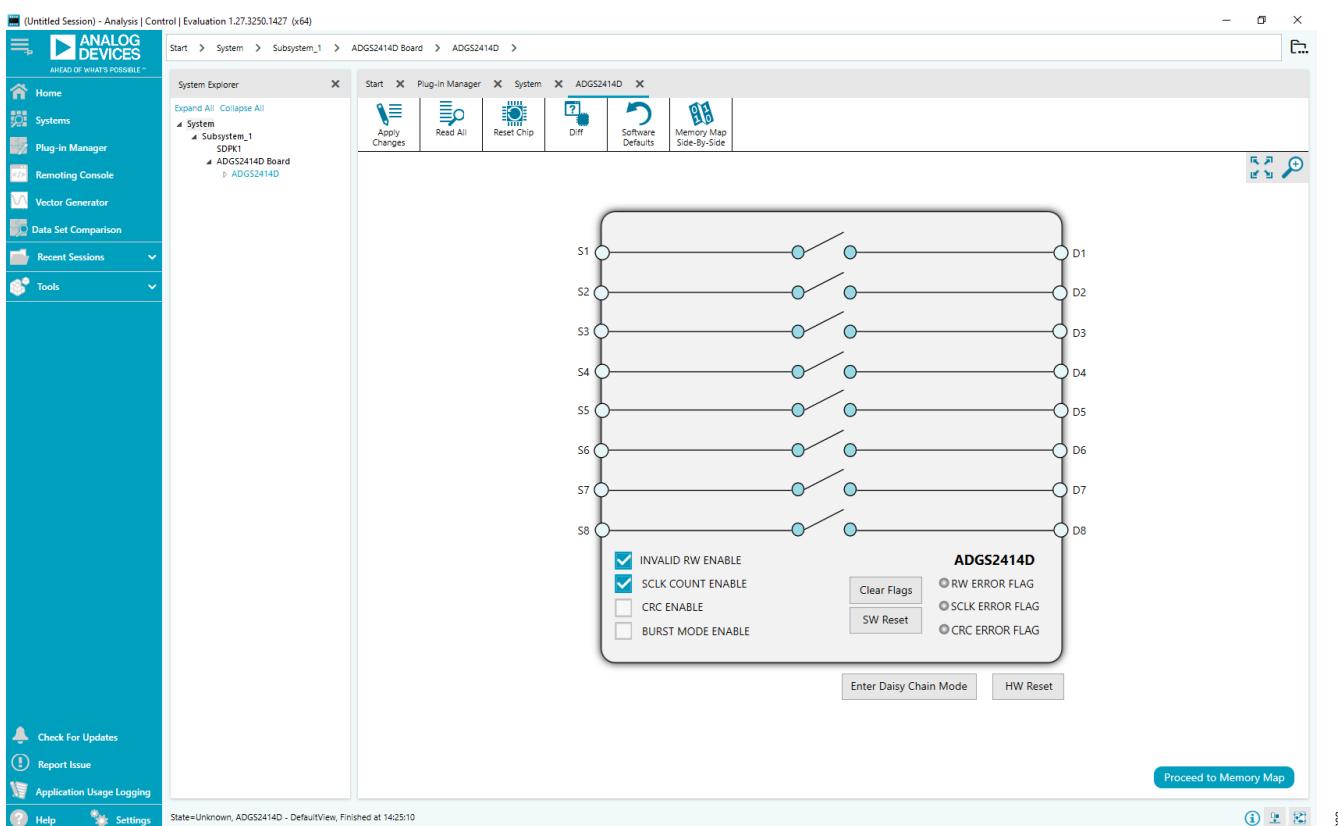


Figure 2. Chip View for the ADGS2414D

## BLOCK DIAGRAM AND DESCRIPTION

The ADGS2414D chip view is similar to the functional block diagram shown in the ADGS2414D data sheet. Therefore, it is simple to correlate the functions on the EV-ADGS2414DSDZ with the descriptions in the data sheet. Refer to the ADGS2414D data sheet for a full description of each block, register, and setting.

Some of the blocks and their functions are described in this section as they pertain to the EV-ADGS2414DSDZ. Figure 3 shows the full screen block diagram (with labels), and Table 3 describes the functionality of each labeled block.

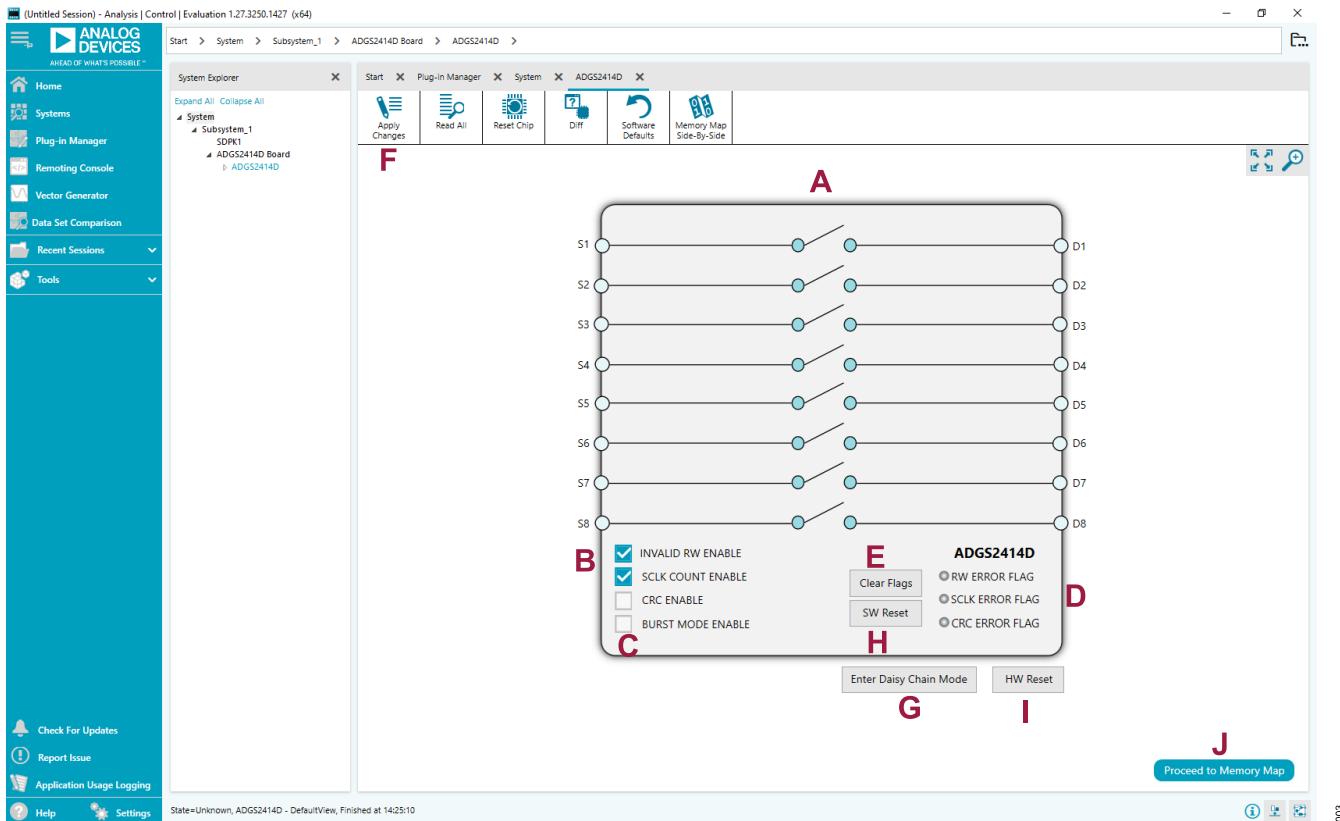


Figure 3. Chip View for the ADGS2414D with Labeled Block Diagram

Table 3. Block Diagram Functions

Label	Function
A	The eight switches configure SW1 to SW8 as open or closed. Click the switch to configure it.
B	<b>INVALID RW ENABLE</b> , <b>SCLK COUNT ENABLE</b> , and <b>CRC ENABLE</b> . Select or clear these check boxes to enable or disable the error detection features on the SPI.
C	<b>BURST MODE ENABLE</b> . Select or clear this check box to enable or disable burst mode.
D	<b>RW ERROR FLAG</b> , <b>SCLK ERROR FLAG</b> , and <b>CRC ERROR FLAG</b> . These indicators illuminate red if flags assert in the error flags register.
E	<b>Clear Flags</b> . Click this button to clear the error flags register.
F	<b>Apply Changes</b> . Click this button to apply all modified values to the devices.
G	<b>Enter Daisy Chain Mode</b> . Click this button to put all evaluation boards that are connected in a daisy-chain configuration into daisy-chain mode.
H	<b>SW Reset</b> . Click this button to perform a software reset on the ADGS2414D.
I	<b>HW Reset</b> . Click this button to perform a hardware reset on the ADGS2414D. JP2 must be set to Position B.
J	<b>Proceed to Memory Map</b> . Click this button to access the <b>ADGS2414D Memory Map</b> view.

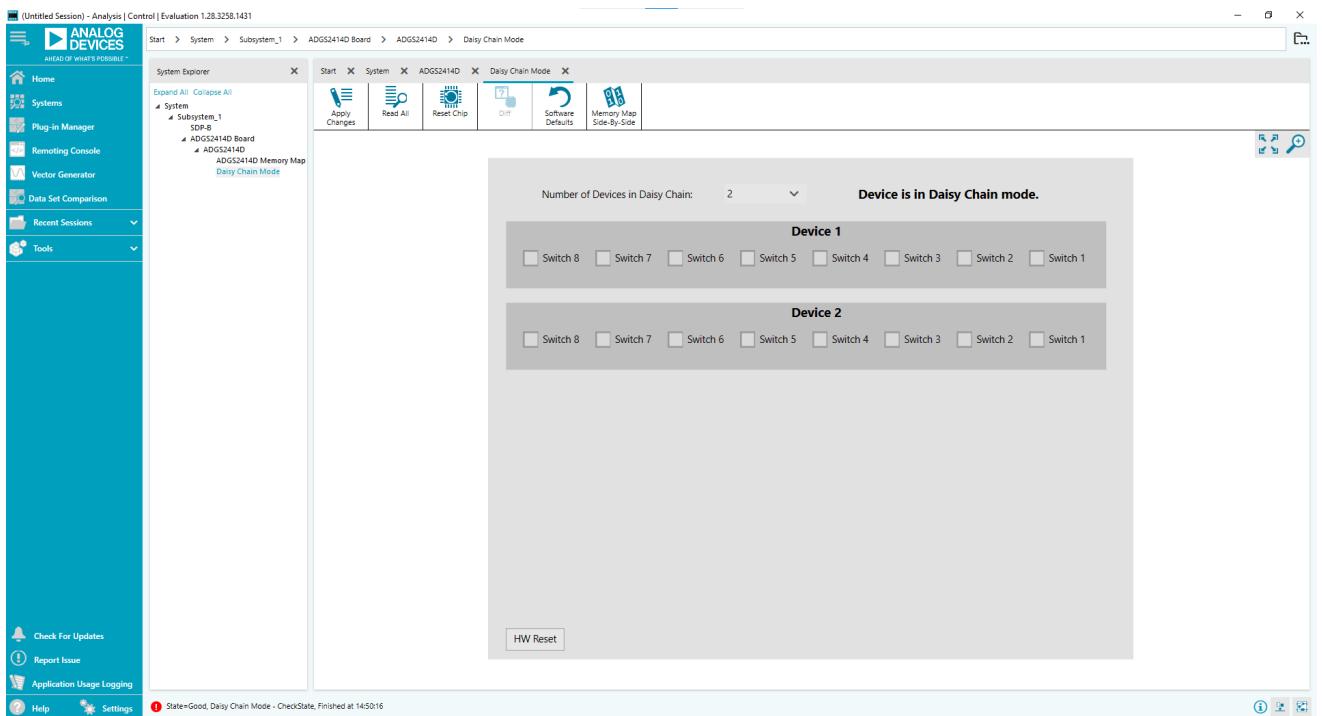
## BLOCK DIAGRAM AND DESCRIPTION

### DAISY-CHAIN MODE

It is possible to daisy-chain multiple ADGS2414D devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The route of digital signals and supplies through the ADGS2414D allows an increase in channel density when using the device in daisy-chain mode. Integrated passive components eliminate the need for external passive components.

Click **Enter Daisy Chain Mode** to open the **Daisy Chain Mode** view, as shown in [Figure 4](#). Select the number of boards that are

connected in the daisy chain from the **Number of Devices in Daisy Chain** dropdown box. Select the checkboxes of the switches that are to be turned on. Click **Apply Changes** to write these values to the devices in the daisy chain. To exit daisy-chain mode, perform a hardware reset. To perform a hardware reset, click the **HW Reset** button in the **Daisy Chain Mode** view (JP2 must be set to Position B), or press the physical hardware reset button on the EV-ADGS2414DSDZ.



*Figure 4. Daisy Chain Mode View*

## BLOCK DIAGRAM AND DESCRIPTION

### MEMORY MAP

All registers are fully accessible from the **ADGS2414D Memory Map** view. To access the **ADGS2414D Memory Map** view, click **Proceed to Memory Map**. The **ADGS2414D Memory Map** view allows registers to be edited at a bit level (see [Figure 5](#) and [Figure 6](#)). The shaded bits are read-only bits and cannot be accessed in **ACE**.

All other bits are toggled. The bold bits or registers are modified values that have not been transferred to the evaluation board. Click **Apply Changes** to transfer the data to the EV-ADGS2414DSDZ.

All changes made in the **ADGS2414D Memory Map** view correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled on the block diagram.

Registers		Address (Hex)	Name	Data (Hex)	Data (Binary)							
+	-				0 0 0 0 0 0 0 0 0 0 0 0							
+	0001	* SW_DATA		00	0	0	0	0	0	0	0	0
+	0002	ERR_CONFIG		06	0	0	0	0	0	1	1	0
+	0003	* ERR_FLAGS		00	0	0	0	0	0	0	0	0
+	0005	BURST_EN		00	0	0	0	0	0	0	0	0

*Figure 5. ADGS2414D Memory Map View*

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Registers		Address (Hex)	Name	Data (Hex)	Data (Binary)							
+	-				0 0 0 0 0 0 0 0 0 0 0 1							
+	0001	* SW_DATA		01	0	0	0	0	0	0	0	1
+	0002	ERR_CONFIG		06	0	0	0	0	0	1	1	0
+	0003	* ERR_FLAGS		00	0	0	0	0	0	0	0	0
+	0005	BURST_EN		00	0	0	0	0	0	0	0	0

*Figure 6. ADGS2414D Memory Map View with Unapplied Changes in the SW\_DATA Register*

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## EVALUATION BOARD SCHEMATICS AND ARTWORK

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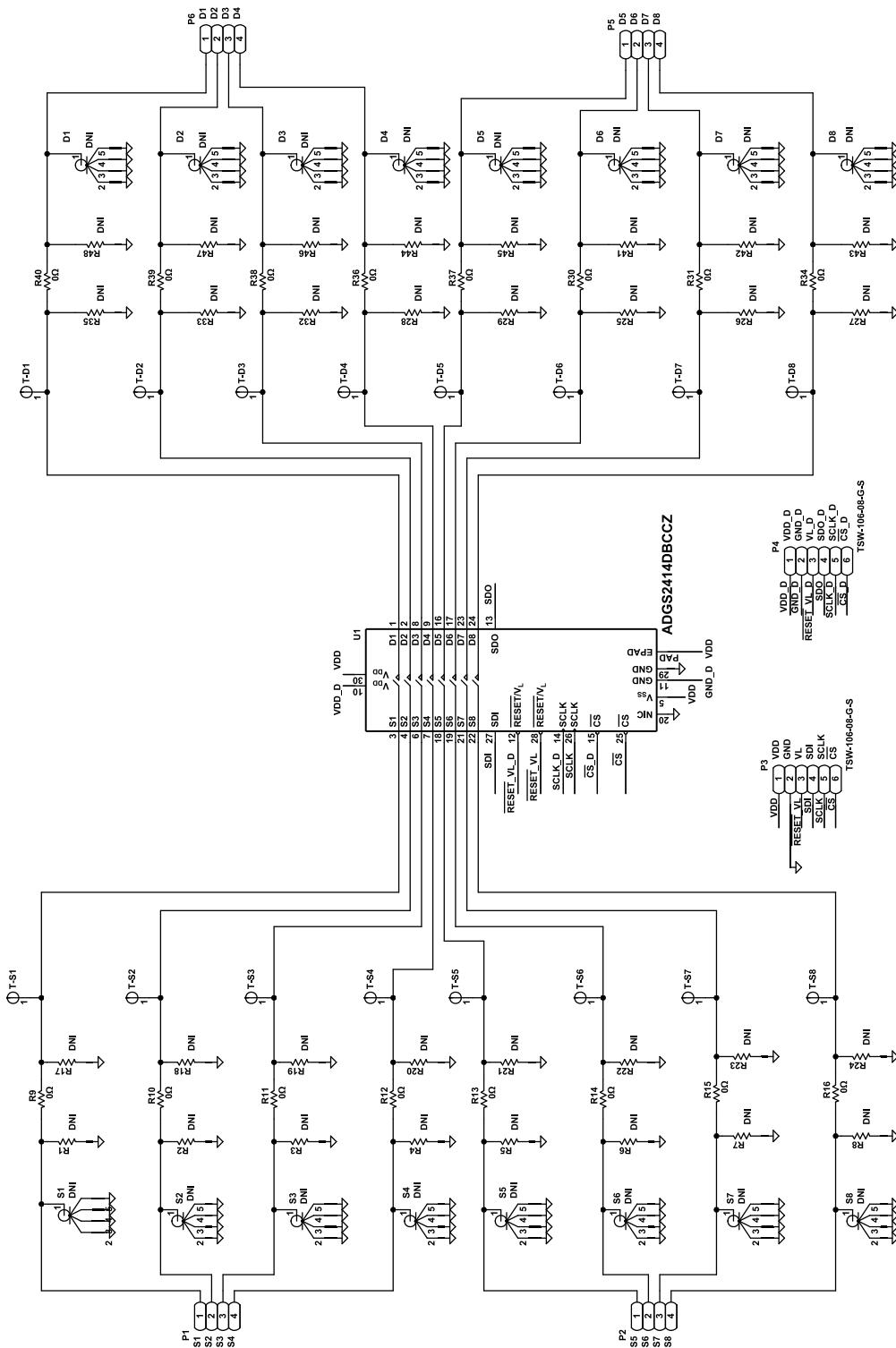
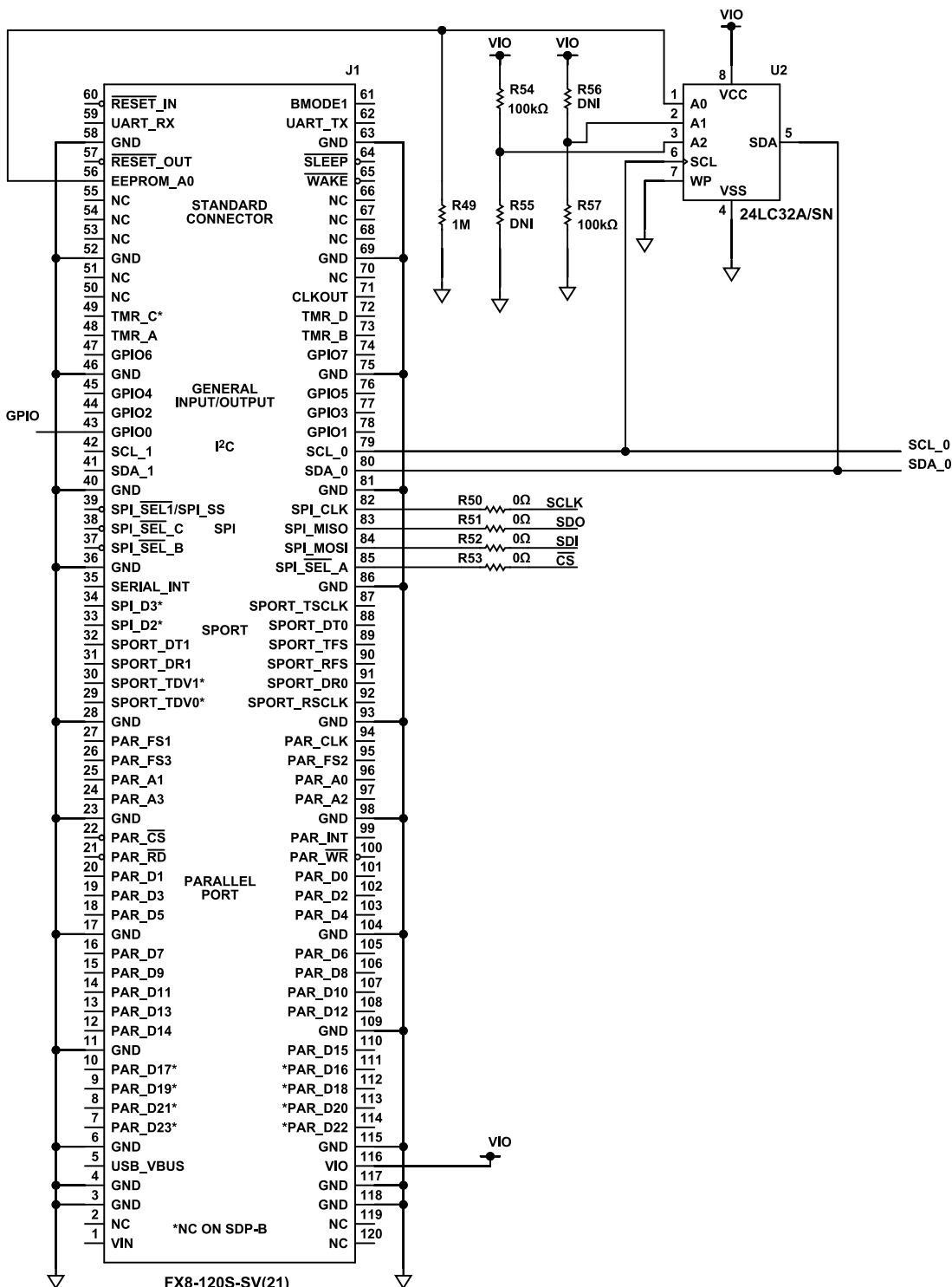


Figure 7. EV-ADGS2414DSDZ Schematic 1

## EVALUATION BOARD SCHEMATICS AND ARTWORK



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Figure 8. EV-ADGS2414D Schematic 2

## EVALUATION BOARD SCHEMATICS AND ARTWORK

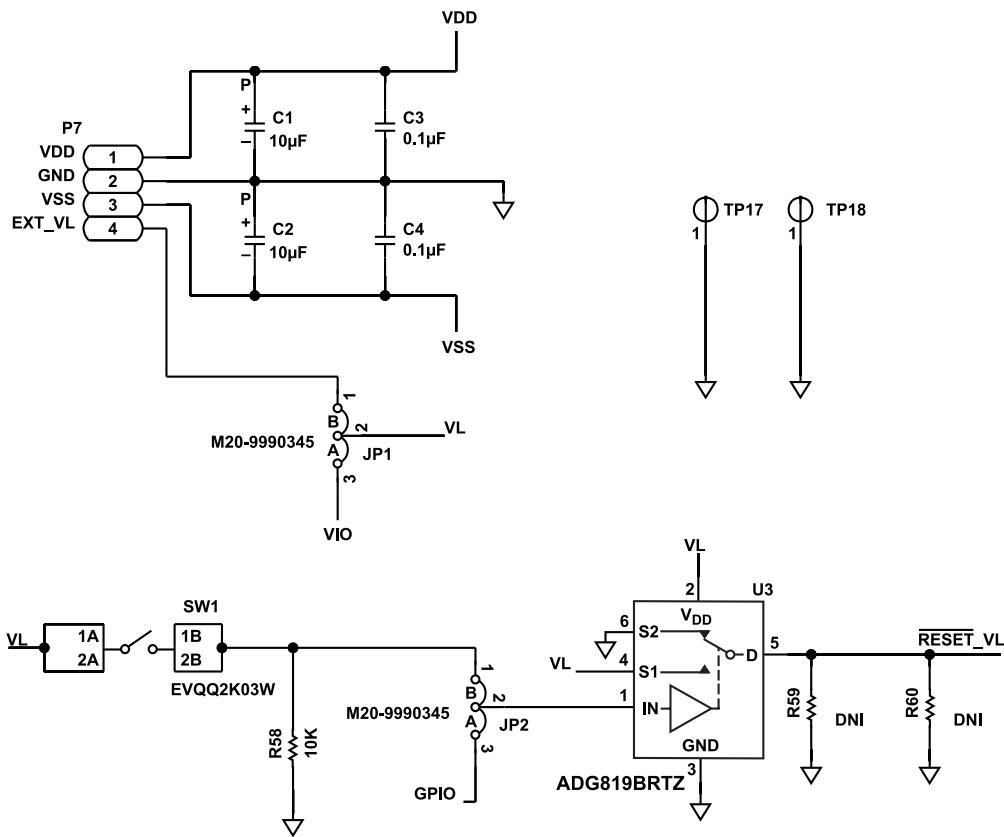
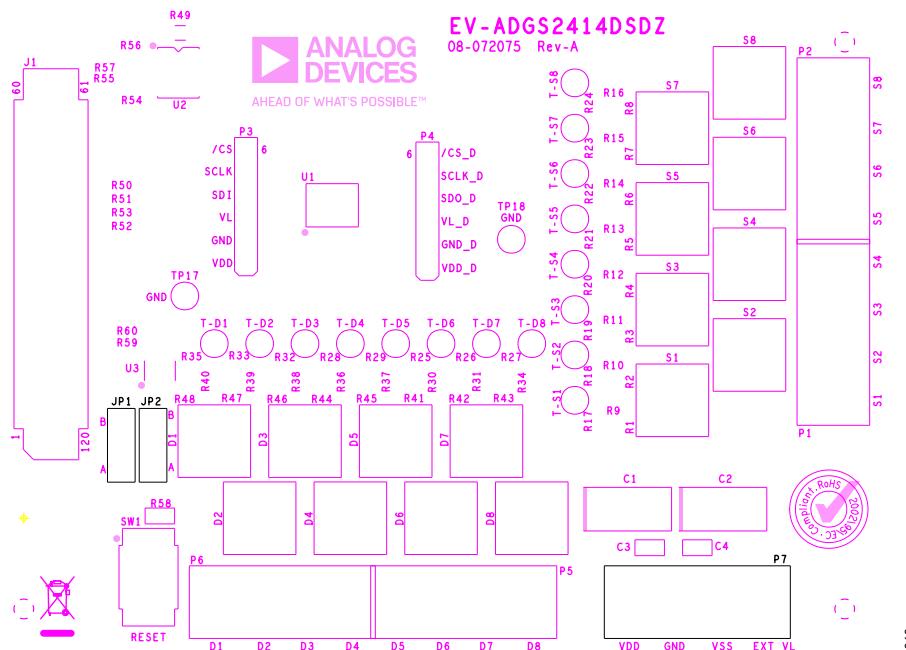


Figure 9. EV-ADGS2414DSDZ Schematic 3

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**Figure 10. EV-ADGS2414DSDZ Silkscreen**

## EVALUATION BOARD SCHEMATICS AND ARTWORK

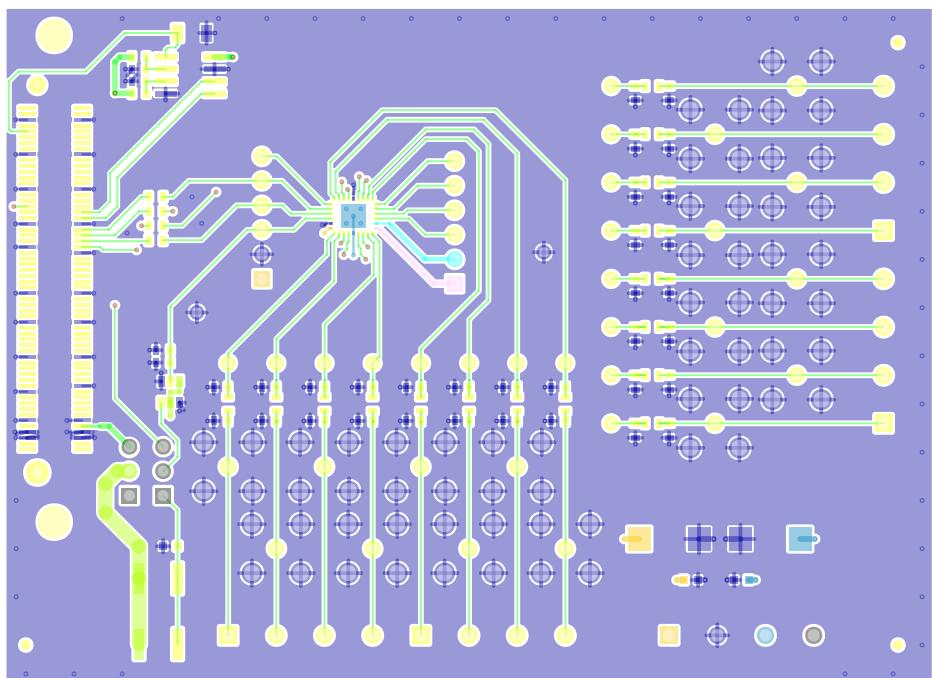


Figure 11. EV-ADGS2414DSDZ Top Layer

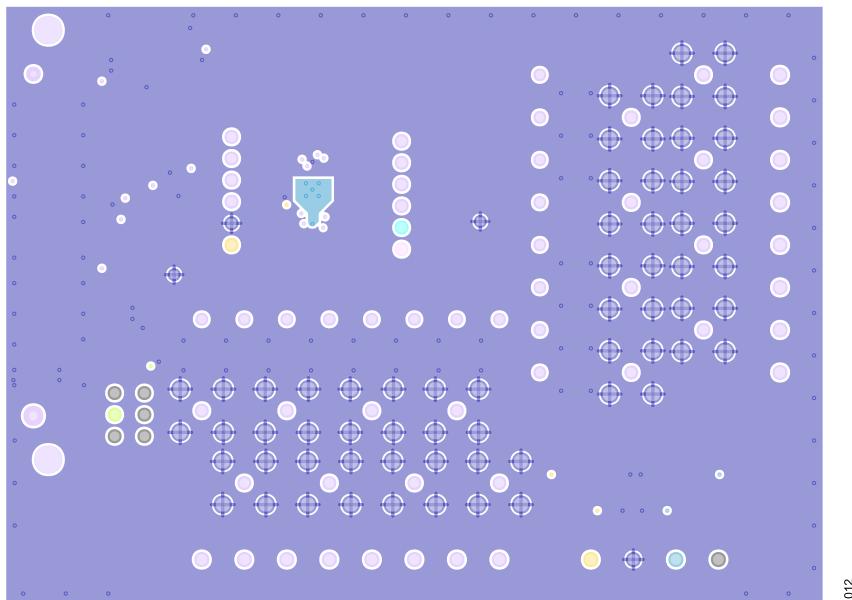
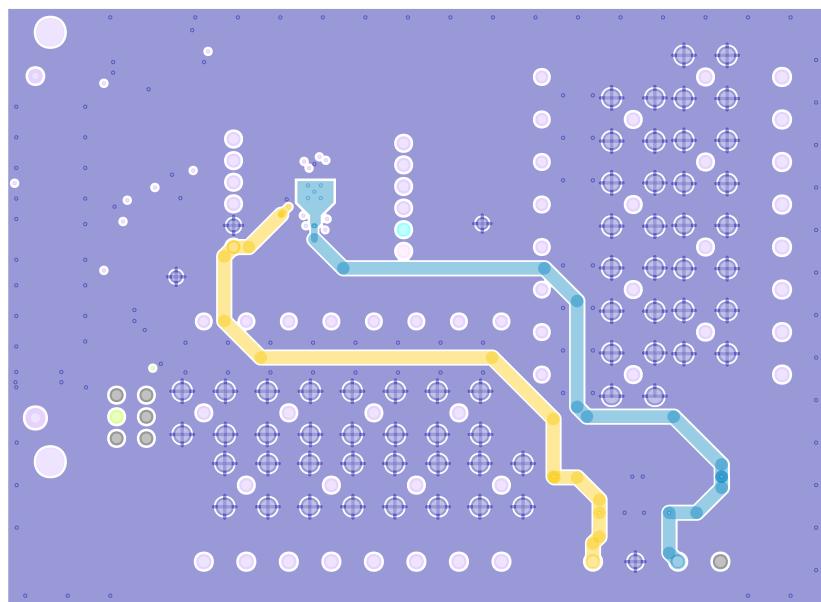


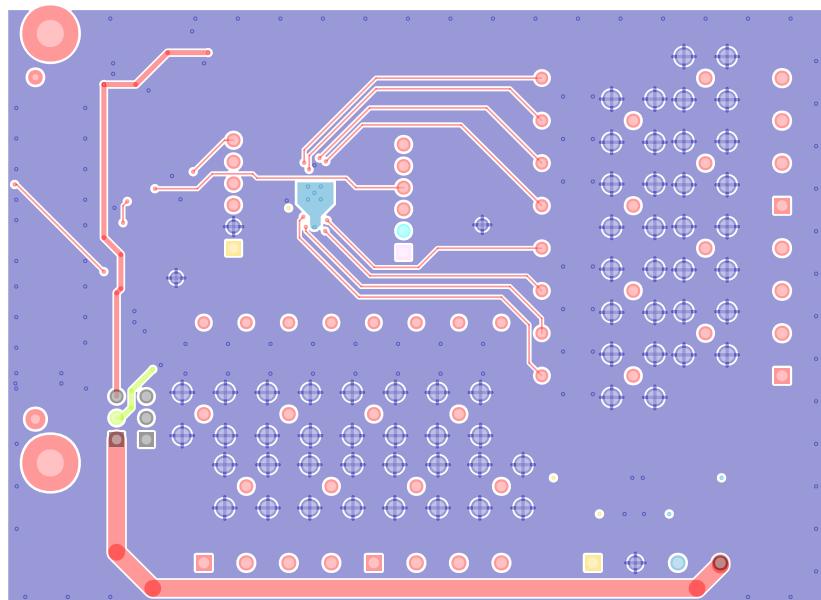
Figure 12. EV-ADGS2414DSDZ Layer 2

## EVALUATION BOARD SCHEMATICS AND ARTWORK



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Figure 13. EV-ADGS2414DSDZ Layer 3



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Figure 14. EV-ADGS2414DSDZ Bottom Layer

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 4. Bill of Materials for EV-ADGS2414DSDZ

Reference Designator	Description
C1, C2	50 V tantalum capacitor, 10 $\mu$ F, D size
C3, C4	50 V, X7R, multilayer ceramic capacitor, 0.1 $\mu$ F, 0603
D1 to D8	Not placed
S1 to S8	Not placed
T-D1 to T-D8, T-S1 to T-S8	Red test point
TP17, TP18	Black test point
P1, P2, P5 to P7	4-pin terminal block, 5 mm pitch
P3, P4	Through hole, header, 4 x 2, 2.54 mm
J1	120-way connector, 0.6 mm pitch
JP1, JP2	3-pin single inline (SIL) header and shorting link
R1 to R8, R17 to R29, R32, R33, R35, R41 to R48, R55, R56, R59, R60	Not placed
R9 to R16, R30, R31, R34, R36 to R40, R50 to R53	Resistor, 0 $\Omega$ , 0603, 1%
R58	Resistor, 10 k $\Omega$ , 0.063 W, 1%, 0603
R49	Resistor, 1 M $\Omega$ , 0.25 W, 1%, 1206
R54, R57	Resistor, 100 k $\Omega$ , 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push-button switch
U1	ADGS2414D, SPI controlled, octal SPST switch
U2	32 k $\Omega$ , I <sup>2</sup> C serial electronically erasable programmable read only memory (EEPROM)
U3	<a href="#">ADG819</a> , 1.8 V to 5.5 V, 2:1 multiplexer and SPDT switch

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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