

Evaluating the ADG1634L 4.7 Ω R_{ON} , Quad SPDT Switch with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- ▶ Single inline headers provide flexibility for the field programmable gate array (FPGA) or microcontroller 1.2 V or 1.8V logic input signals
- ▶ SMD pin resistor or capacitor sockets available for the addition of passive components
- ▶ SMB connector sockets provide flexibility for the input and output signals

EVALUATION KIT CONTENTS

- ▶ EVAL-ADG1634LEBZ evaluation board

DOCUMENTS NEEDED

- ▶ [ADG1634L](#) data sheet
- ▶ EVAL-ADG1634LEBZ user guide

EQUIPMENT NEEDED

- ▶ DC voltage source (V_{DD}/V_{SS})
 - ▶ ± 5 V for dual supply
- ▶ Optional digital logic supply (V_L)
 - ▶ 1.1 V to 1.3 V for 1.2 V logic
 - ▶ 1.65 V to 1.95 V for 1.8 V logic
- ▶ Analog signal source
- ▶ Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG1634LEBZ is the evaluation board for the ADG1634L. The ADG1634L contains four independent single-pole, double-throw (SPDT) switches. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

An external V_L supply pin provides logic control flexibility for lower logic controls. The ADG1634L is both 1.2 V and 1.8 V JEDEC standard compliant.

[Figure 1](#) shows the EVAL-ADG1634LEBZ in a typical evaluation setup. The EVAL-ADG1634LEBZ is located in the center of the evaluation board. Eight test points are included to connect to each of the source pins. Subminiature Version B (SMB) sockets are included for the drain inputs. Three screw terminals power the device. A 5-pin header is provided for user defined digital voltage, if required.

Full specifications on the ADG1634L are available in the ADG1634L data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the EVAL-ADG1634LEBZ.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

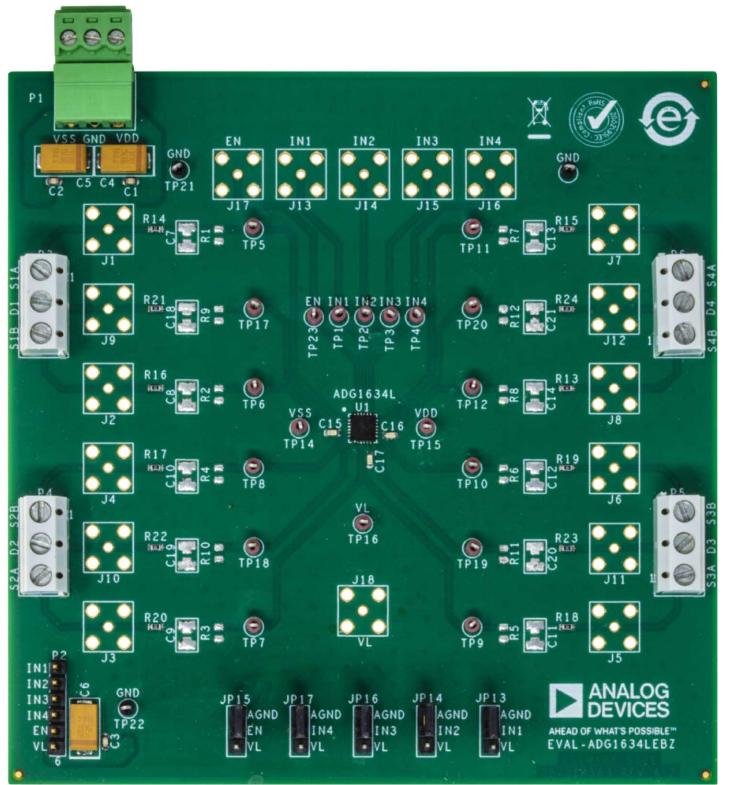


Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLY

Connector P1 provides access to the supply pins on the [ADG1634L](#). VDD, GND, and VSS on P1 link to the appropriate pins on the ADG1634L. For dual-supply voltages, the EVAL-ADG1634LEBZ can be powered at ± 5 V. For single-supply voltages, the GND and VSS terminals must be connected and power the EVAL-ADG1634LEBZ with 5 V or 12 V. Additionally, 1.1 V to 1.95 V is supplied to the V_L pin of the ADG1634L.

LINK HEADERS

A number of link options are provided on the EVAL-ADG1634LEBZ that must be set for the required operating conditions before using. [Table 1](#) shows the summary of the link headers and how they are used on the EVAL-ADG1634LEBZ. The functions of these link options are described in detail in [Table 2](#).

Table 1. Link Header Descriptions

Link	Position	Description
JP13 to JP17	A	V_L
	B	GND

Table 2. Link Header Functions

Link	Function
JP13 to JP17	This link selects the source of the IN_x voltage supplied to the ADG1634L. Position A selects V_L from P2. Position B selects 0 V or GND.

SMB CONNECTORS

The parallel interface of the ADG1634L is controlled manually using the link headers of JP13 to JP17, or it can be accessed using the SMB connectors, IN1 to IN4. To use the SMB connectors, remove the JP13 to JP17 link headers.

INPUT SIGNALS

Four screw connectors, P3, P4, P5, and P6, are provided to connect to both the source and drain pins of the ADG1634L. Additional SMB connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground. A $0\ \Omega$ resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple RC filter.

EVALUATION BOARD SCHEMATIC AND ARTWORK

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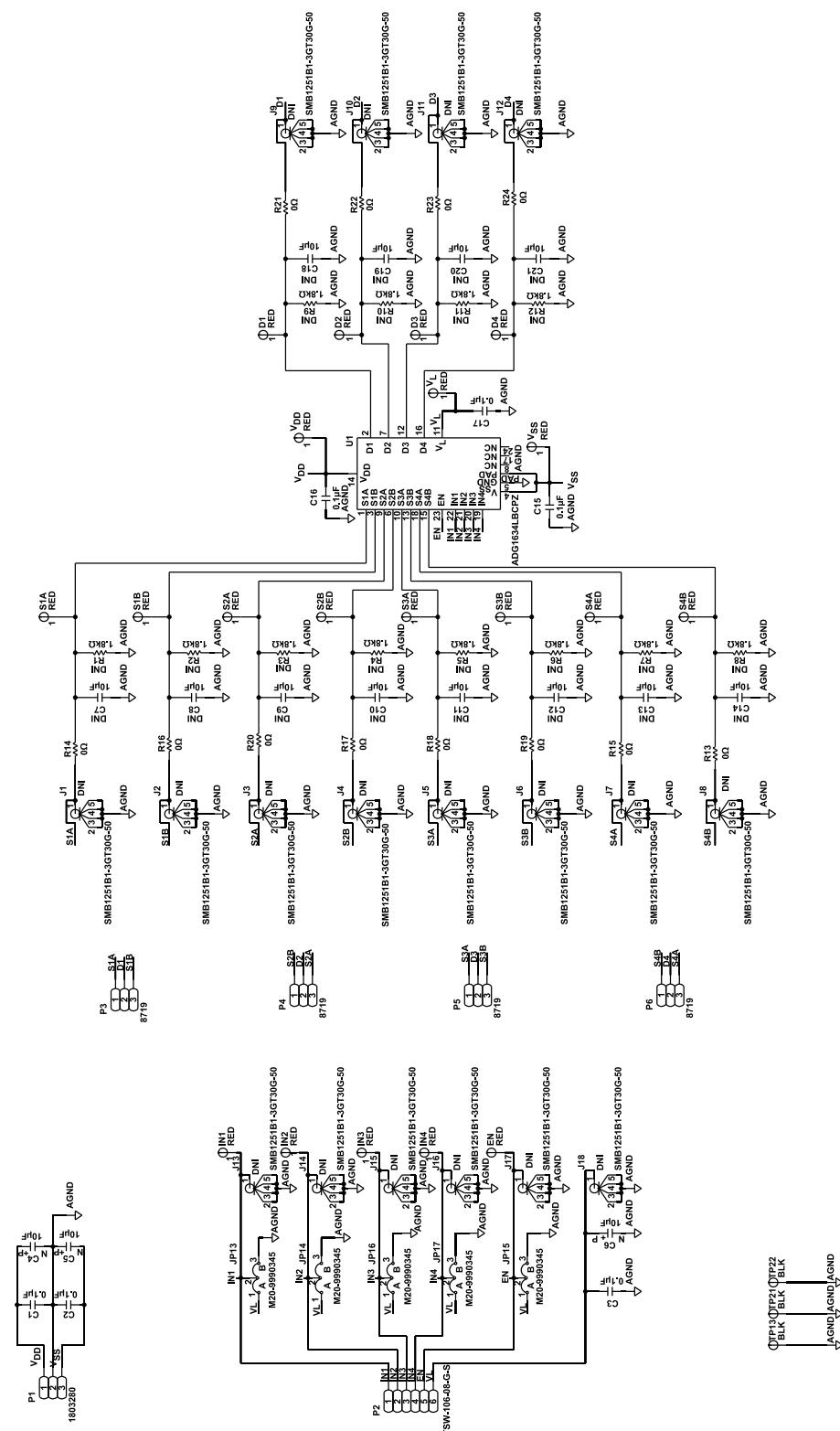
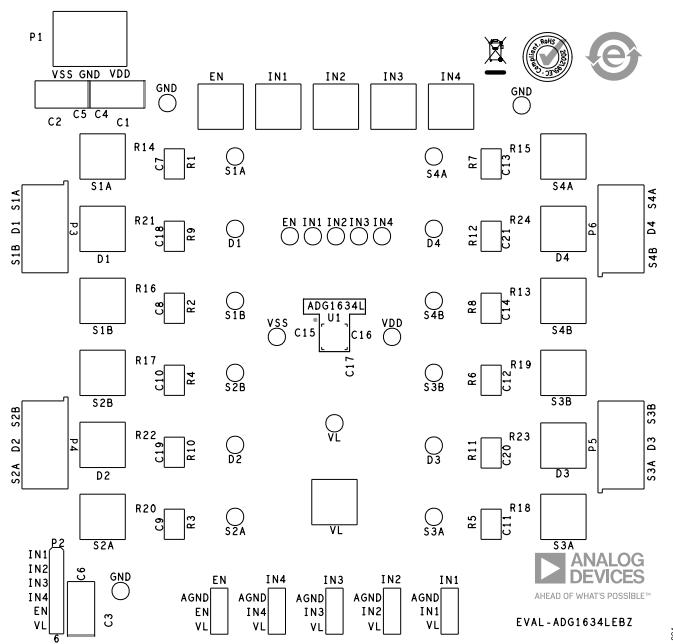


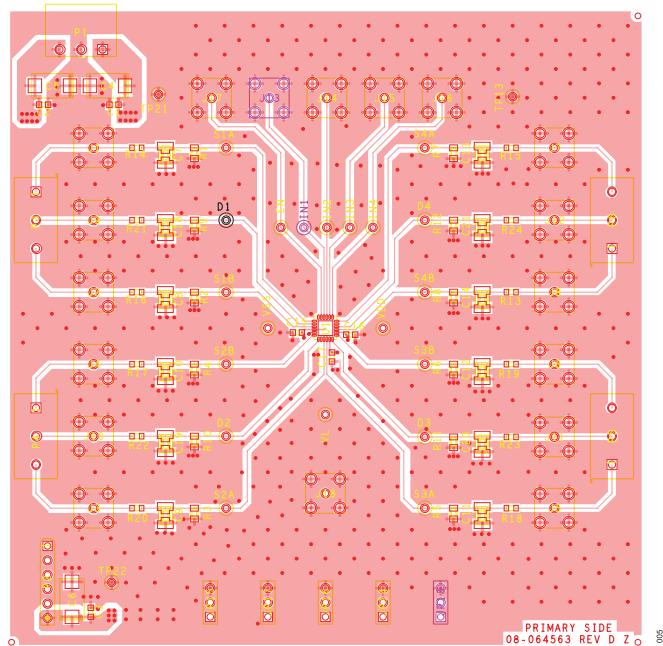
Figure 2. EVAL-ADG1634LEBZ Evaluation Board Schematic, Part 1

EVALUATION BOARD SCHEMATIC AND ARTWORK



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Figure 3. EVAL-ADG1634LEBZ Silkscreen



005

Figure 4. EVAL-ADG1634LEBZ Top Layer

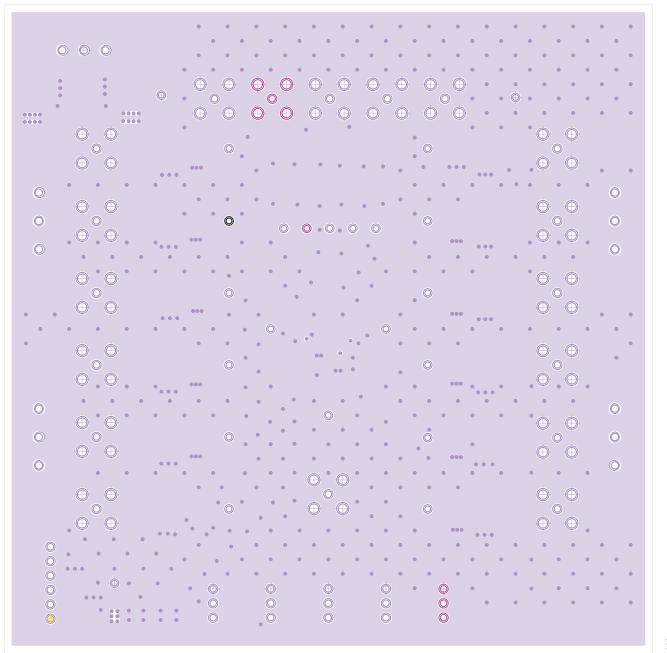
EVALUATION BOARD SCHEMATIC AND ARTWORK

Figure 5. EVAL-ADG1634LEBZ Layer 2

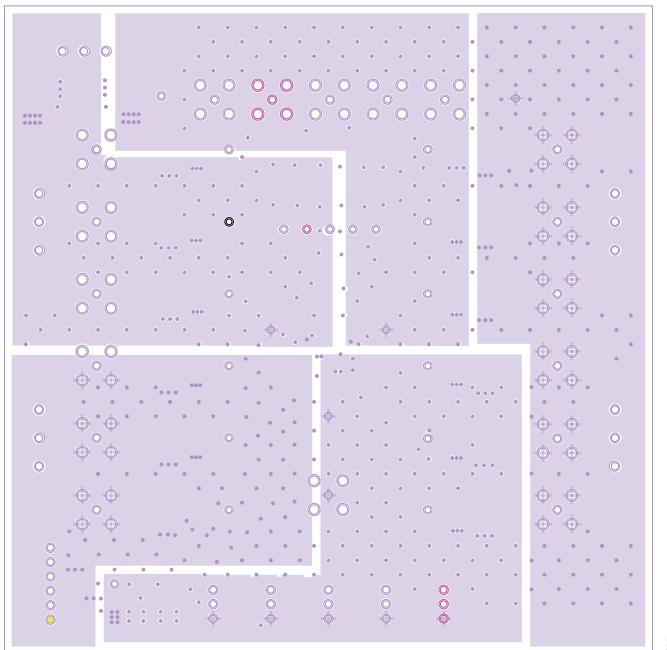


Figure 6. EVAL-ADG1634LEBZ Layer 3

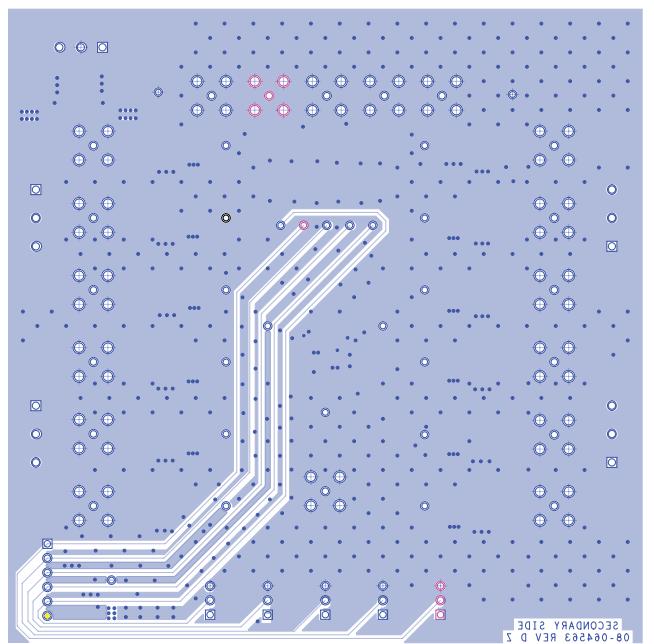
EVALUATION BOARD SCHEMATIC AND ARTWORK

Figure 7. EVAL-ADG1634LEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Manufacturer	Part Number
C1 to C3	50 V tantalum capacitors, 10 μ F, D size	Kemet	T491D106K050AT
C4 to C6, C15 to C17	50 V, X7R multilayer ceramic capacitors, 0.1 μ F, 0603	Vishay	VJ0603Y104KXAAC31X
C7 to C14, C18 to C21	Not placed	Not applicable	Not applicable
R1 to R12	Not placed	Not applicable	Not applicable
R13 to R24	Resistors, 0 Ω , 0603, 1%	Yageo	RC0603JR-070RL
J1 to J18	50 Ω , SMB sockets, not placed	Amphenol	SMB1251B1-3GT30G-50
T1 to T12, TP14 to TP20, TP23	Red test points	Vero Technologies	20-313137
TP13, TP21 to TP22	Black test points	Vero Technologies	20-2137
P1	Header, right angle, 3.81 mm with plug	Phoenix Contact	1803280
P2	Through hole header, 6-position	Samtec	TSW-106-08-G-S
P3 to P6	2-pin terminal blocks, 5 mm	Keystone Electronics	8719
JP13 to JP17	3-pin single inline headers and shorting links	Harwin	M20-9990345
U1	ADG1634L, 4.7 Ω R_{ON} , quad SPDT switch with 1.2 V and 1.8 V JEDEC logic compliance	Analog Devices Inc.	ADG1634L



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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