Evaluating the ADG1206L/ADG1207L, Low Capacitance, 16- and 8-Channel iCMOS Multiplexers with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- Single inline headers provide flexibility for the field programmable gate array (FPGA) or microcontroller 1.2 V or 1.8 V logic input signals
- SMD pin resistor or capacitor sockets available for the addition of passive components
- SMB connector sockets provide flexibility for the input and output signals

EVALUATION KIT CONTENTS

- EVAL-ADG1206LEBZ evaluation board
- EVAL-ADG1207LEBZ evaluation board

DOCUMENTS NEEDED

- ADG1206L/ADG1207L data sheet
- EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ user guide

EQUIPMENT NEEDED

- DC voltage source (V_{DD}/V_{SS})
  - ±15 V for dual supply
- Optional digital logic supply (V_L)
  - 1.1 V to 1.3 V for 1.2 V logic
  - 1.65 V to 1.95 V for 1.8 V logic
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ are the evaluation boards for the ADG1206L/ADG1207L. The ADG1206L/ADG1207L contain sixteen single channels and eight differential channels, respectively. The ADG1206L switches one of sixteen inputs to a common output, as determined by 4-bit binary address lines A0, A1, A2, and A3. The ADG1207L switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines, A0, A1, and A2. The enable pin (EN) on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

An external V_L supply pin provides logic control flexibility for lower logic controls. The ADG1206L/ADG1207L is both 1.2 V and 1.8 V JEDEC standard compliant.

Figure 1 and Figure 2 show the EVAL-ADG1206LEBZ and EVAL-ADG1207LEBZ in a typical evaluation setup. The ADG1206L/ADG1207L is placed in the center of the evaluation board, and wire screw terminals are provided to connect to each source and drain pin. Three screw terminals are used to power the device and an external pin provides users with a defined digital logic supply voltage. Alternatively, the digital logic supply voltage can be supplied from 5-pin and 6-pin headers.

Full specifications on the ADG1206L/ADG1207L are available in the ADG1206L/ADG1207L data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ.

TABLE OF CONTENTS

REVISION HISTORY

1/2023—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

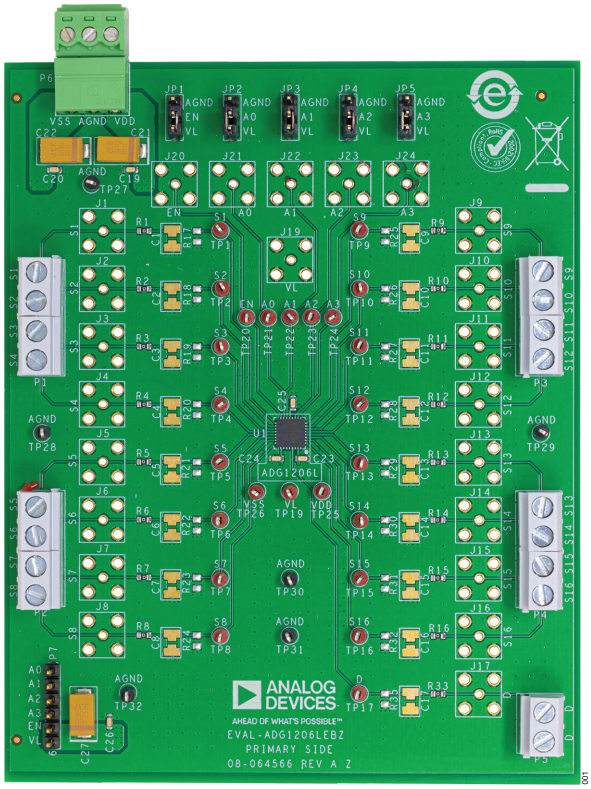

Figure 1. EVAL-ADG1206LEBZ

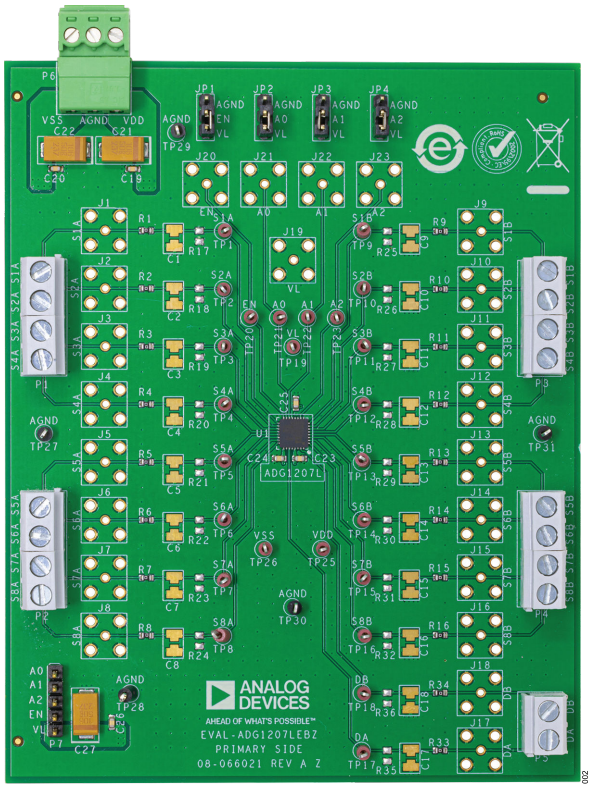

Figure 2. EVAL-ADG1207LEBZ

EVALUATION BOARD HARDWARE

POWER SUPPLY

Connector P6 provides access to the supply pins of the ADG1206L/ADG1207L. V_{DD}, GND, and V_{SS} on the P6 terminal block link to the appropriate pins on the ADG1206L/ADG1207L. For dual-supply voltages, the EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ can be powered at ±15 V. For single-supply voltages, the GND and V_{SS} terminals must be connected and power the EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ with 12 V. Additionally, 1.1 V to 1.95 V is supplied to the V_L pin of the ADG1206L/ADG1207L.

LINK HEADERS

The EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ provide several link options that must be set at the required operating conditions before use.

Table 1 describes the positioning of the links necessary for controlling the EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ via link headers. The functions of these link options are described in detail in Table 2.

Table 1. Link Header Descriptions

Link	Position	Description
JP1 to JP5 (ADG1206L)	A	V_L
JP1 to JP4 (ADG1207L)	A	V_L
	B	GND

Table 2. Link Header Functions

Link	Function
JP1 to JP5 (ADG1206L)	This link selects the source of the Ax voltage supplied to the ADG1206L.
JP1 to JP4 (ADG1207L)	This link selects the source of the Ax voltage supplied to the ADG1207L.
	Position A selects V_L from P7.
	Position B selects 0 V or GND.

SMB CONNECTORS

The parallel interface of the ADG1206L/ADG1207L is controlled manually using the link headers of JP1 to JP5 (EVAL-ADG1206LEBZ), JP1 to JP4 (EVAL-ADG1207LEBZ), or it can be accessed using the SMB connectors, J20 to J24 (EVAL-ADG1206LEBZ) and J20 to J23 (EVAL-ADG1207LEBZ). To use the SMB connectors, remove the link headers of JP1 to JP5 (EVAL-ADG1206LEBZ) and JP1 to JP4 (EVAL-ADG1207LEBZ).

INPUT SIGNALS

Provided in the EVAL-ADG1206LEBZ/EVAL-ADG1207LEBZ are screw connectors P1, P2, P3, P4, and P5 to connect to both the source and drain pins of the ADG1206L/ADG1207L. Additional SMB connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user-defined value. The resistor combined with the 0603 pads can create a simple RC filter.

EVALUATION BOARD SCHEMATICS AND ARTWORK

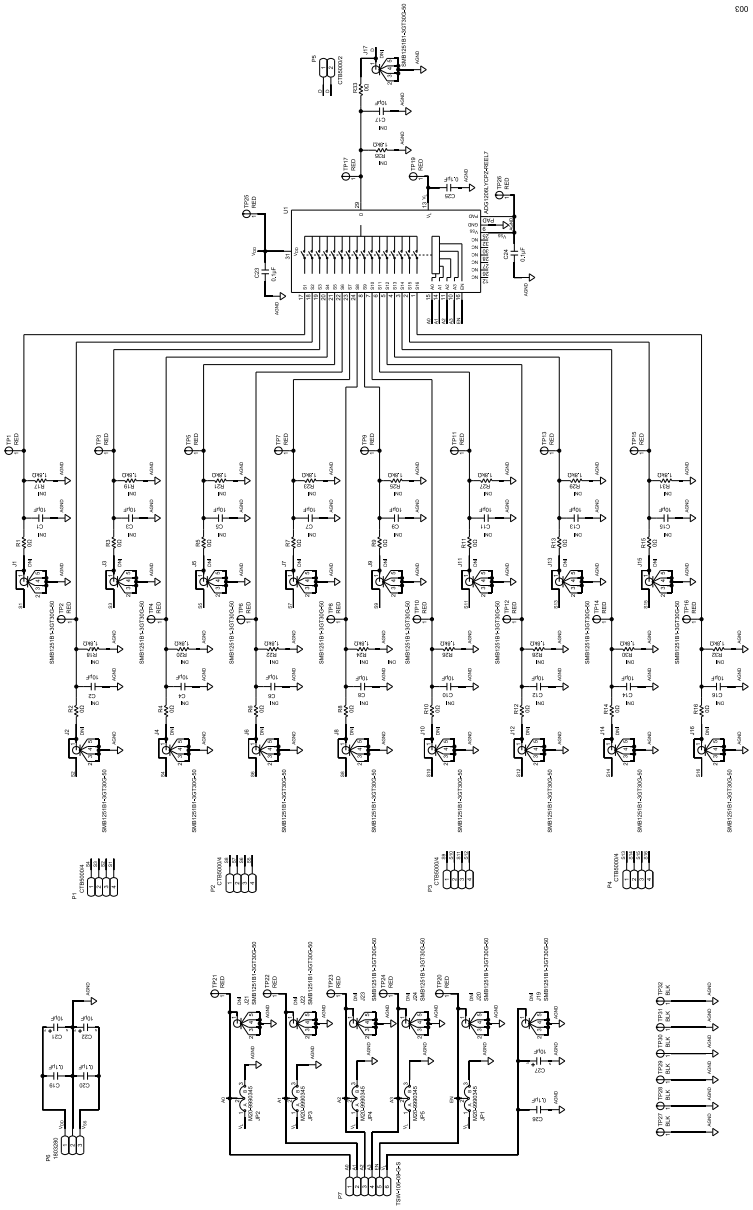

Figure 3. EVAL-ADG1206LEBZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

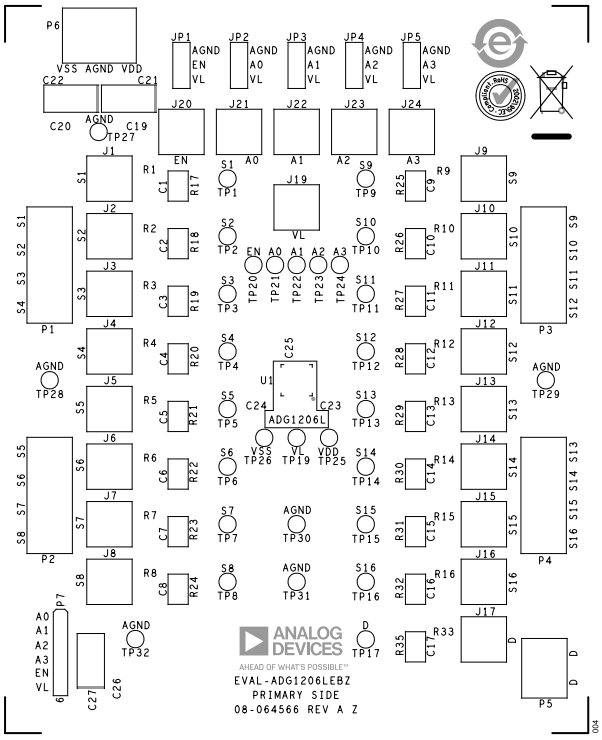

Figure 4. EVAL-ADG1206LEBZ Silkscreen

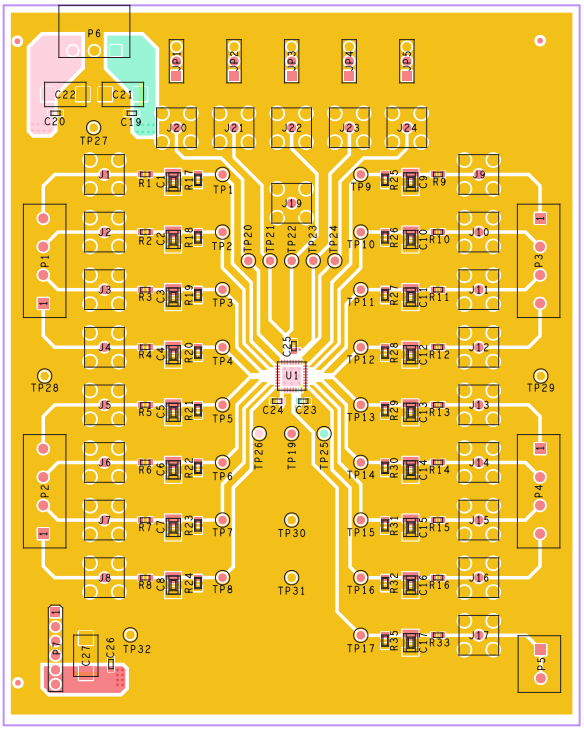

Figure 5. EVAL-ADG1206LEBZ Top Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

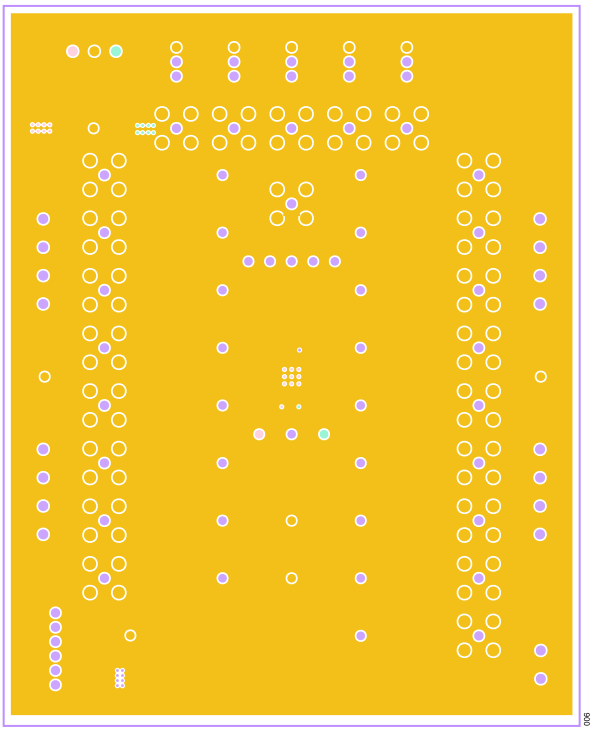

Figure 6. EVAL-ADG1206LEBZ Layer 2

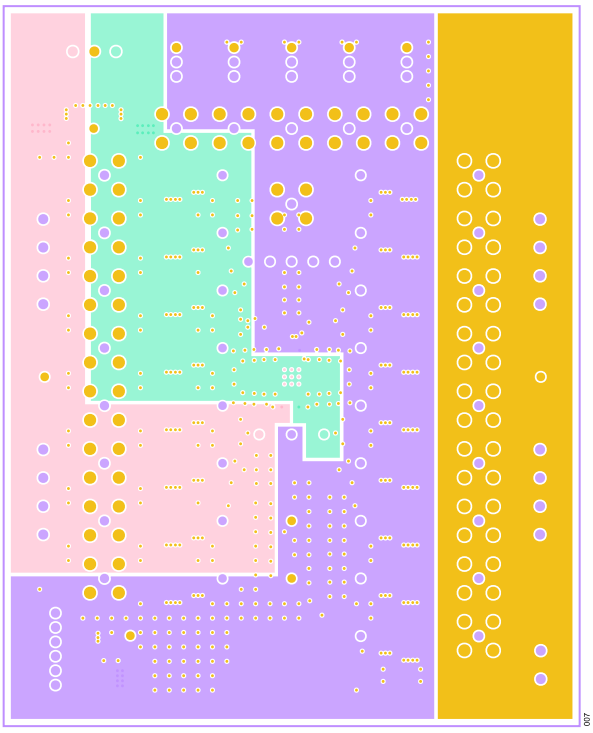

Figure 7. EVAL-ADG1206LEBZ Layer 3

EVALUATION BOARD SCHEMATICS AND ARTWORK

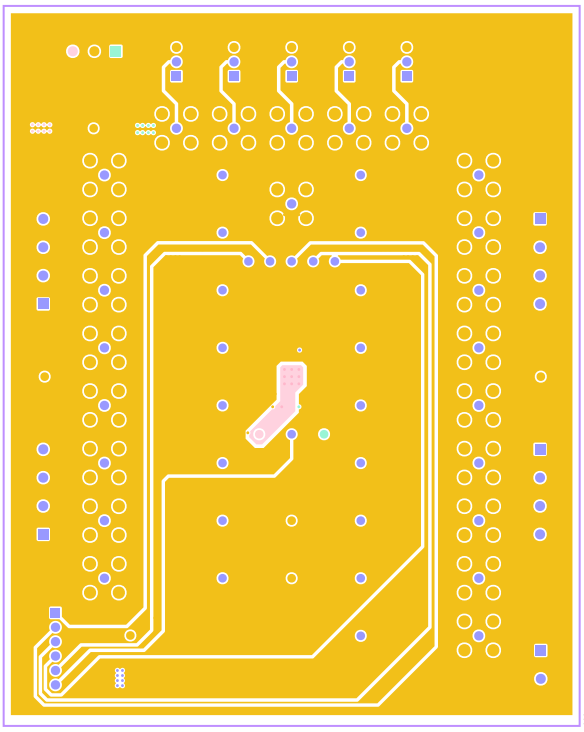

Figure 8. EVAL-ADG1206LEBZ Bottom Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

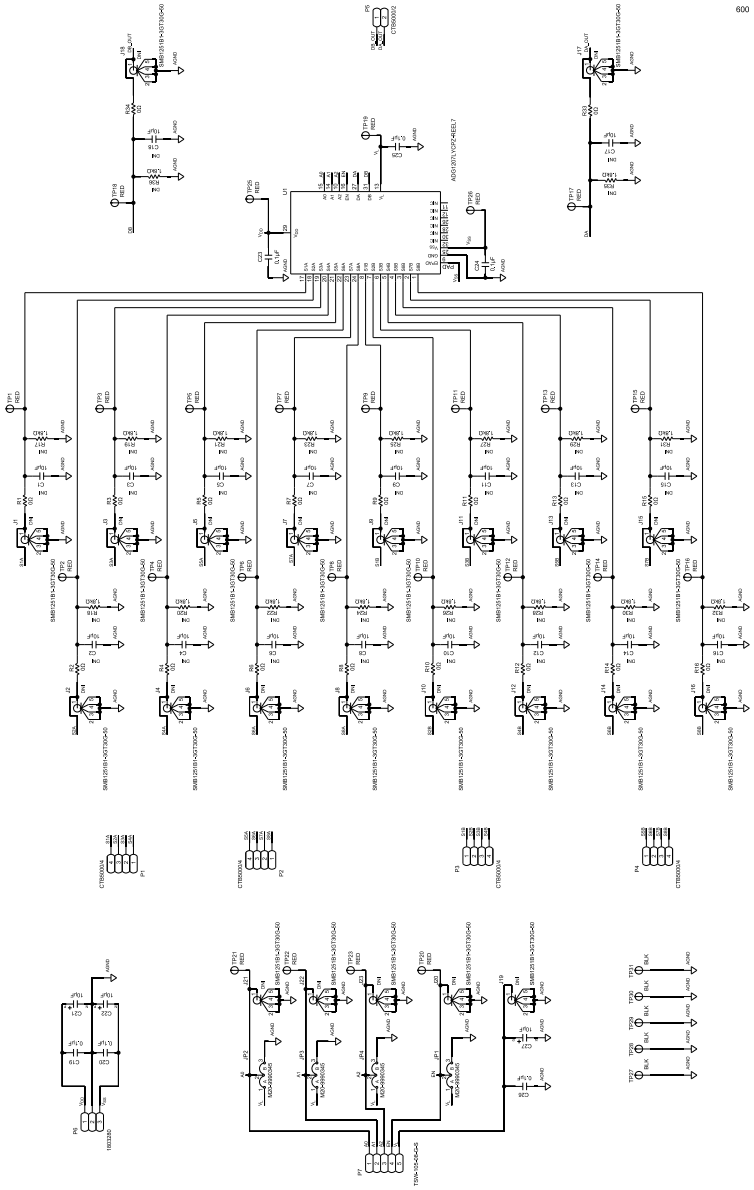

Figure 9. EVAL-ADG1207LEBZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

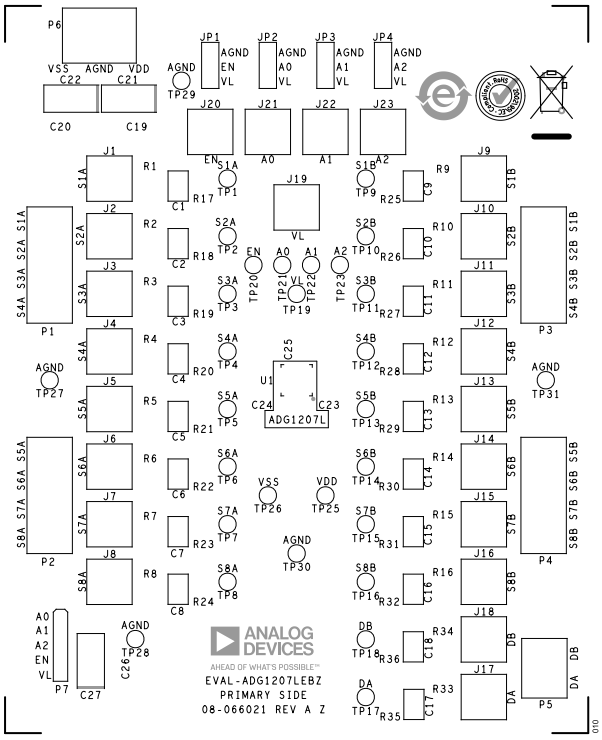

Figure 10. EVAL-ADG1207LEBZ Silkscreen

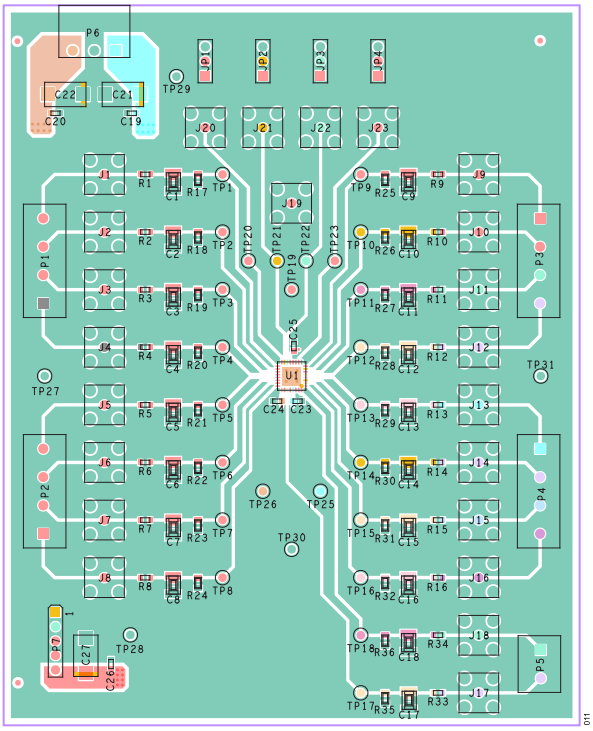

Figure 11. EVAL-ADG1207LEBZ Top Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

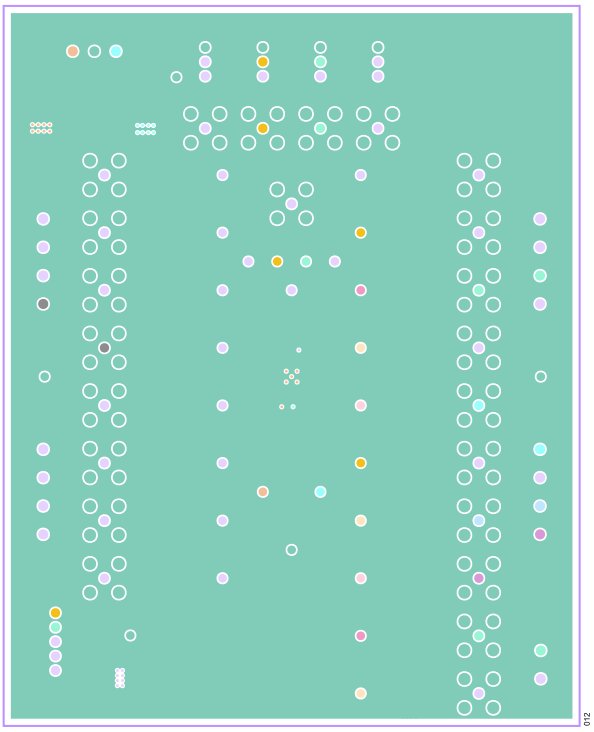

Figure 12. EVAL-ADG1207LEBZ Layer 2

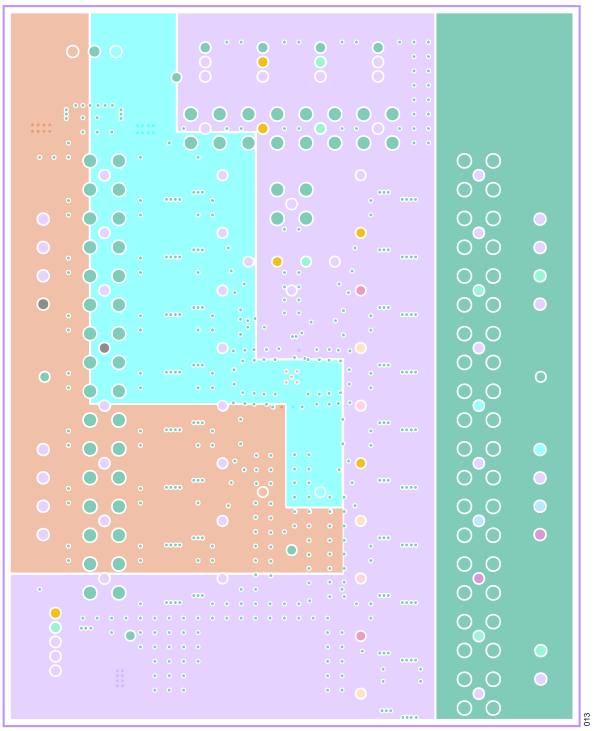

Figure 13. EVAL-ADG1207LEBZ Layer 3

EVALUATION BOARD SCHEMATICS AND ARTWORK

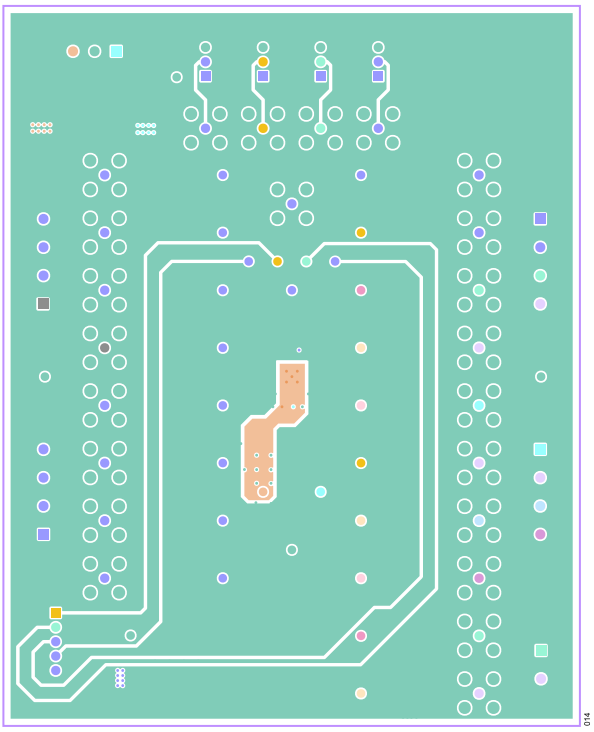

Figure 14. EVAL-ADG1207LEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Manufacturer	Part Number
C21, C22 to C27	50 V tantalum capacitors, 10 µF, D size	Kemet	T491D106K050AT
C19, C20, C23 to C26	50 V, X7R multilayer ceramic capacitors, 0.1 µF, 0603	Vishay	VJ0603Y104KXAAC31X
C1 to C18	Not placed	Not applicable	Not applicable
R17 to R32, R35, R36	Not placed	Not applicable	Not applicable
R1 to R16, R33, R34	Resistors, 0 Ω, 0603, 1%	Vishay	CRCW06030000Z0EA
J1 to J24	50 Ω, SMB sockets, not placed	Amphenol	SMB1251B1-3GT30G-50
S1A to S8A, S1B to S8B, S1 to S16, DA, DB, D, A0 to A3, V_{DD}, V_{SS}, V_L	Red test points	Vero Technologies	20-313137
AGND1 to AGND5	Black test points	Vero Technologies	20-2137
P1 to P4	4-pin terminal block, 5 mm	Camdenboss Ltd.	CTB5000/4
P5	2-pin terminal block, 5 mm	Camdenboss Ltd.	CTB5000/2
P6	3-pin terminal block, 5 mm	Phoenix Contact	1803280
P7	Header RA, 3.81 mm	Samtec	TSW-106-08-G-S
JP1 to JP5	3-pin single inline (SIL) header and shorting link	Harwin	M20-9990345
U1	ADG1206L/ADG1207L, low capacitance, 16-channel and 8-channel iCMOS multiplexers with 1.2 V and 1.8 V JEDEC logic compliance	Analog Devices Inc.	ADG1206L/ADG1207L

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

EVAL-ADG1206LEBZ