

LTC3310

3.3V to 1.2V at 10A, 2MHz Automotive Low EMI
Buck Regulator in a 1.17cm² Solution**DESCRIPTION**

Demonstration circuit 3042A features the LTC[®]3310, 10A, Low Voltage Synchronous Step-Down Silent Switcher[®] operating as a 2MHz, 2.25V to 5.5V input, 1.2V/10A output buck regulator. The LTC3310 supports output voltages from 0.5V to V_{IN} with operating frequencies from 500kHz up to 5MHz. The LTC3310 is a compact, ultralow emission, high efficiency, and high speed synchronous monolithic step-down switching regulator. The Silent Switcher technology optimizes the fast-current loops and makes it easier to minimize EMI/EMC emissions. Fast minimum on-time of 35ns enables high V_{IN} to low V_{OUT} conversion at high frequency.

DC3042A is set up to run in forced continuous mode with a 2MHz switching frequency but can be configured to pulse-skipping mode and different switching frequencies. Connecting RT to V_{IN} sets the MODE/SYNC pin as an input and allows the LTC3310 to sync from an external clock. Connecting the MODE/SYNC pin to V_{IN} sets the mode to forced continuous mode and connecting the MODE/SYNC pin to GND sets the mode to pulse-skipping mode. The Efficiency vs Load graph (Figure 3) shows the efficiency

and power loss of the circuit with a 3.3V input in forced continuous mode operation.

The DC3042A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the V_{IN} EMI terminal. The EMI performance of the board is shown in the EMI Test Results section. The red lines in the EMI performance in Figures 3 to 6 illustrate the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3310 data sheet gives a complete description of the device, operation and application information. The data sheet must be read in conjunction with this demo manual. The LTC3310 is assembled in a 3mm × 3mm LQFN package with exposed pads for low thermal resistance. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet Low EMI PCB Layout section.

Design files for this circuit board are available.

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PERFORMANCE SUMMARYSpecifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	DC3042A Input Voltage Range		2.25		5.5	V
V_{OUT}	DC3042A Output Voltage Range		1.183	1.200	1.217	V
I_{OUT}	DC3042A Output Current				10	A
f_{SW}	Switching Frequency		1.8		2.2	MHz
EFF	Efficiency	$V_{IN} = 3.3\text{V}$, $I_{OUT} = 5\text{A}$		91		%

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BOARD PHOTO

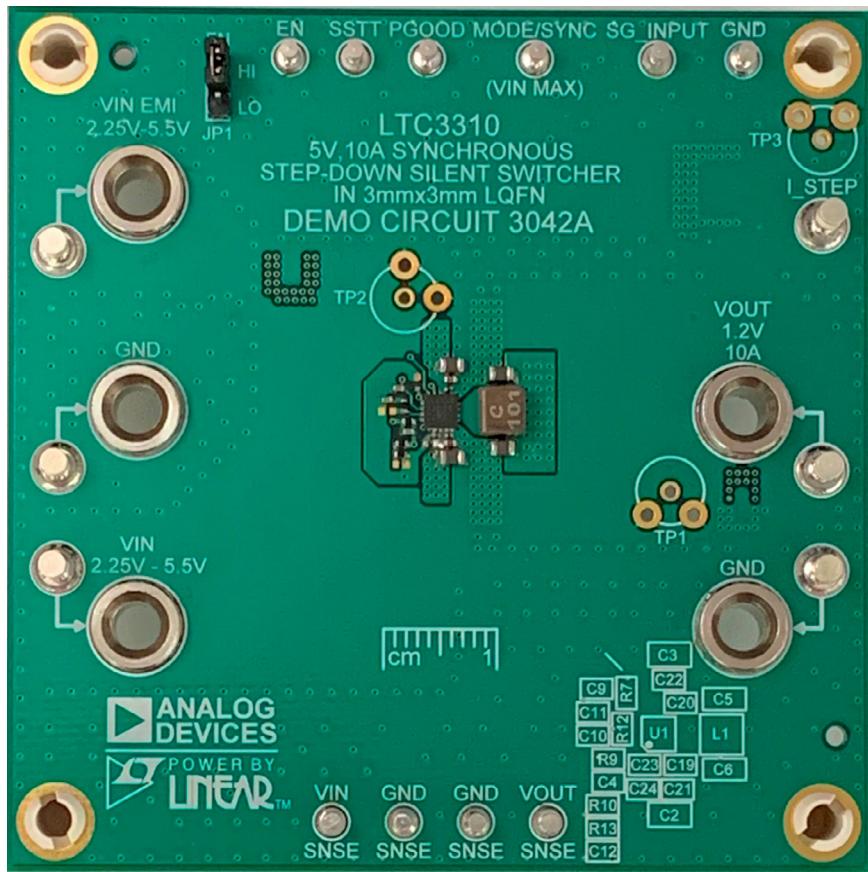


Figure 1. DC3042A Demo Board

TYPICAL PERFORMANCE CHARACTERISTICS

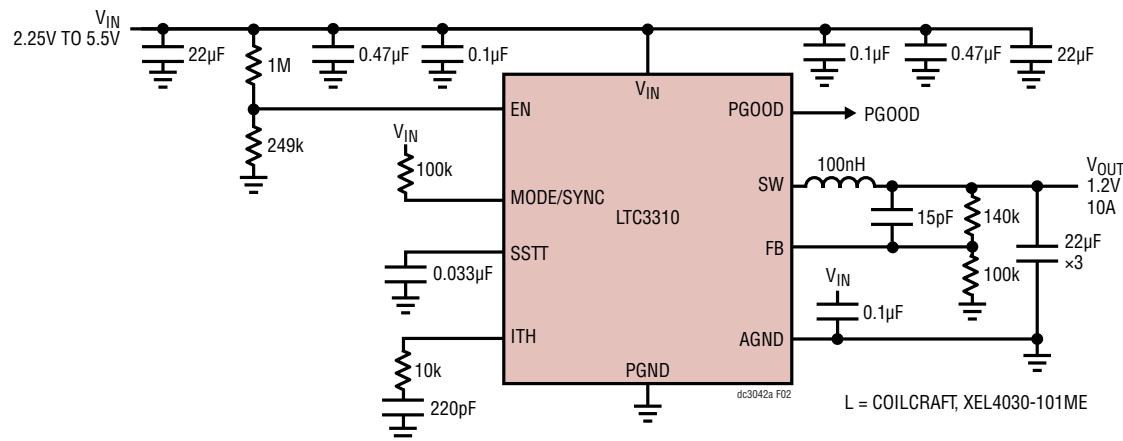


Figure 2. 1.2V 10A Step-Down Converter

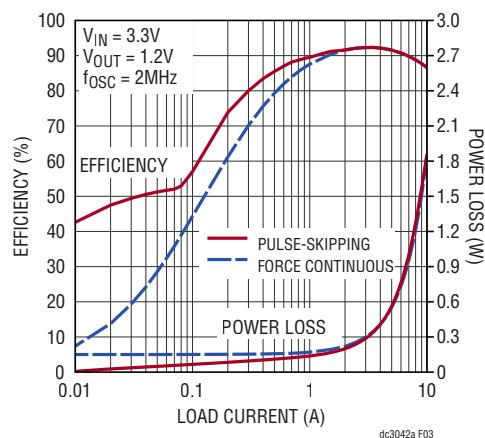


Figure 3. Efficiency vs Load Current

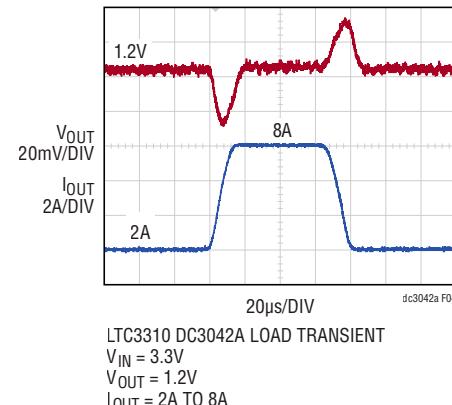
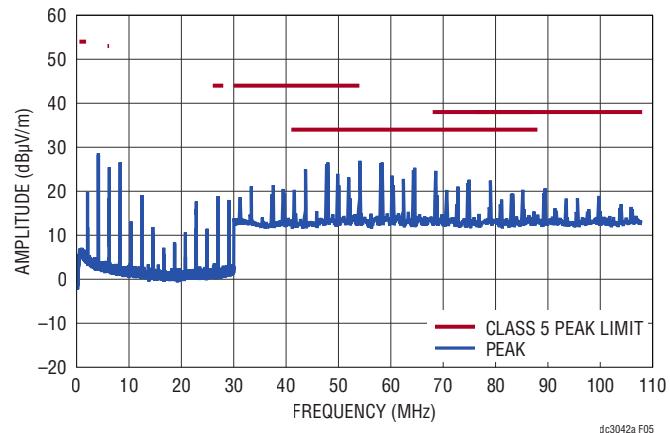


Figure 4. Load Step Response

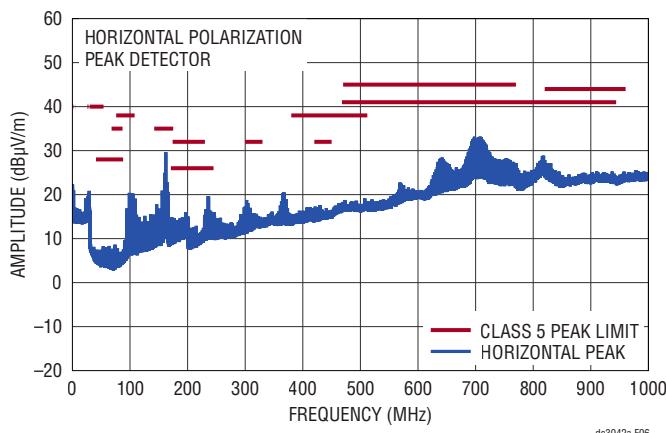
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EMI TEST RESULTS



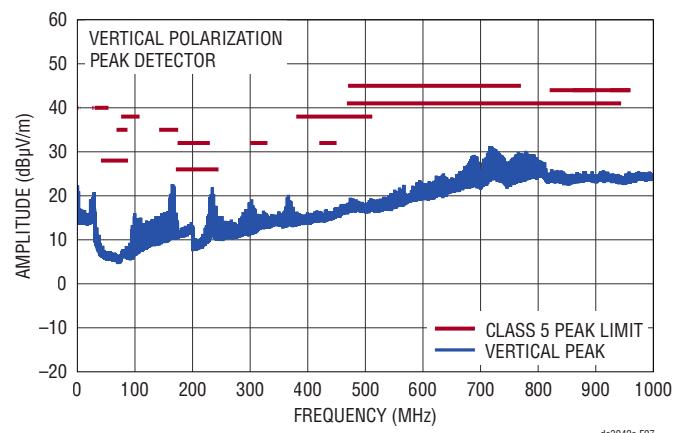
DC3042A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 1.2V OUTPUT AT 8A, $f_{SW} = 2\text{MHz}$

Figure 5. CISPR25 Conducted Emission Test with Class 5 Peak Limits (Voltage Method)



DC3042A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 1.2V OUTPUT AT 8A, $f_{SW} = 2\text{MHz}$

Figure 6. CISPR25 Conducted Emission Test with Class 5 Peak Limits (Horizontal)



DC3042A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 1.2V OUTPUT AT 8A, $f_{SW} = 2\text{MHz}$

Figure 7. CISPR25 Conducted Emission Test with Class 5 Peak Limits (Vertical)

QUICK START PROCEDURE

Refer to Figure 8 for the proper measurement equipment setup and follow the procedure below.

NOTE: For accurate V_{IN} , V_{OUT} and efficiency measurements, measure V_{IN} at the V_{IN} SNS and GND SNS turrets, and measure V_{OUT} at the V_{OUT} SNS and GND SNS turrets as illustrated as VM1 and VM2 in Figure 8. When measuring the input or output ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output turrets or to TP1 as shown in Figure 9.

1. Set the JP1 jumper to the high position.
2. With power off, connect the input power supply to V_{IN} and GND. If the input EMI filter is desired, connect the input power supply to V_{IN} EMI and GND.
3. Set power supply PS1 current limit to 10A. Set the electronic load LD1 to CC mode and 0A current. Slowly increase PS1 to 1.0V. If PS1 output current reads less than 20mA, increase PS1 to 3.3V. Verify that VM1 reads 3.3V and VM2 reads 1.2V. Check VM1, VM2, VM3, PS1 output current and LD1 input current. Connect an oscilloscope voltage probe as shown in Figure 9. Set channel to AC-coupled, voltage scale to 20mV and time base to 10 μ s. Check V_{OUT} ripple voltage. Verify that PGOOD voltage is above 3V.
4. Increase the load by 1A intervals up to 10A and observe the voltage output regulation, ripple voltage, and the voltage on the SSTT turret. Calculate die temperature using Equation 1.

$$T_J \text{ (}^{\circ}\text{C}\text{)} = \frac{V_{SSTT}}{4\text{mV}} - 273 \quad (1)$$

6. If pulse-skipping mode is desired, set PS1 to 0V. Install a 0 Ω resistor in the R6 location or short the MODE/SYNC turret to GND. Repeat Steps 1 through 4. In Step 4, observe that the switching waveform is now in pulse-skipping mode at low current.
7. **Optional:** To change the frequency, remove R4 and R6, if installed. Install the desired R_T resistor in the R7 location. Note that the MODE/SYNC pin should have high impedance to GND and V_{IN} . Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output. Refer to the LTC3310 data sheet and LTpowerCAD® for more information on choosing the required components.
8. To test the transient response with a base load, add the desired resistor to produce a minimum load between V_{OUT} and I_{STEP} turrets (RL shown on Figure 8). Note that the total load resistance will be RL plus R14 (100m Ω). Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.
9. Measure the I_{STEP} voltage to observe the current, $V_{I_{STEP}}/100\text{m}\Omega$. Adjust the amplitude of the pulse to provide the desired transient. Connect signal generator SG1 between SG_INPUT and GND turrets. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Figure 4 shows a load step from 2A to 8A. Refer to Equations 2 and 3.

$$I_{OUT} = \frac{V_{I_{STEP}}}{100\text{m}\Omega} \quad (2)$$

$$V_{SG} = V_{SG_INPUT} - V_{I_{STEP}} \quad (3)$$

11. When done, turn off SG1, PS1 and Load. Remove all the connections to the demo board.

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QUICK START PROCEDURE

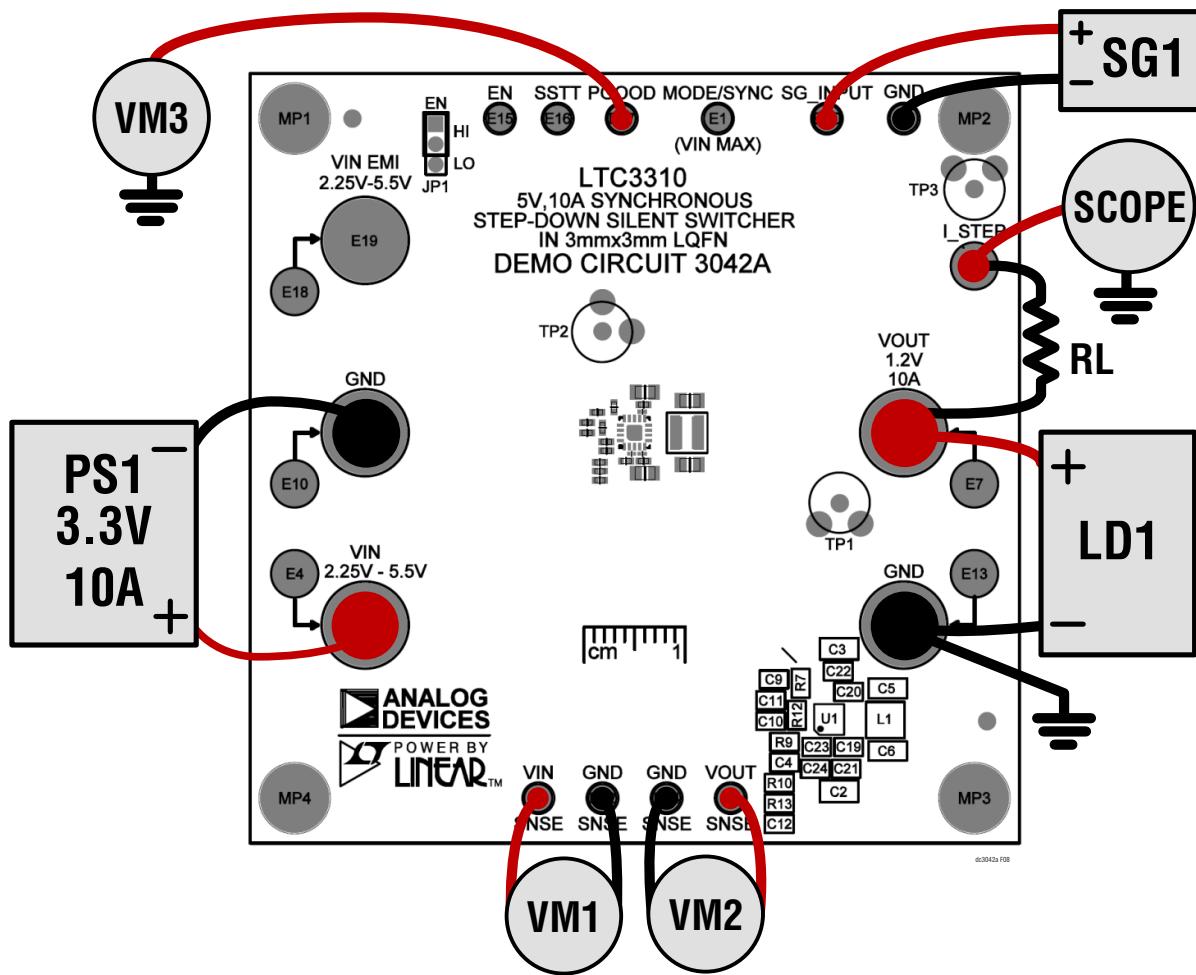


Figure 8. Test Setup for DC3042A

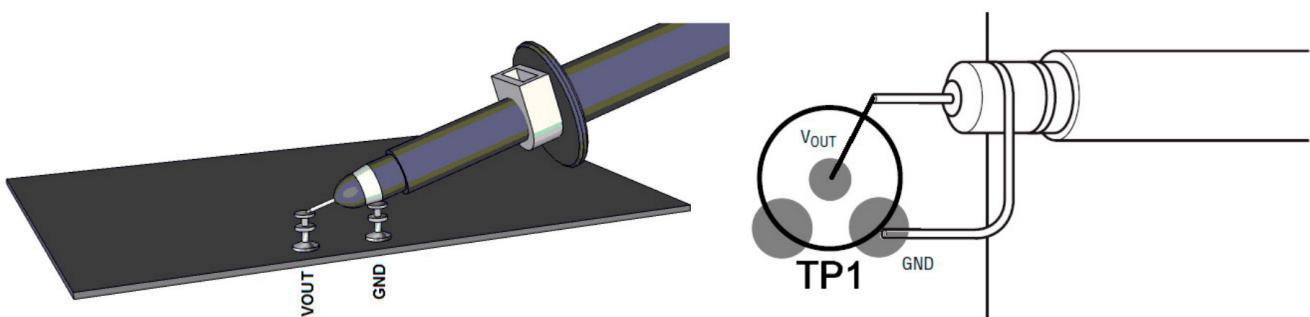


Figure 9. Technique for Measuring Output Ripple and Step Response

THEORY OF OPERATION

Introduction to the DC3042A

The DC3042A demonstration circuit features the LTC3310, a low voltage synchronous step-down Silent Switcher. The LTC3310 is a monolithic, constant-frequency, current mode step-down DC/DC converter. An oscillator, with frequency set by a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current, at which the top switch turns off, is controlled by the voltage on the internal ITH node. The error amplifier servos the ITH node by comparing the voltage on the V_{FB} pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous bottom power switch turns on until the next clock cycle begins. In pulse-skipping mode, the bottom switch also turns off when inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

If the EN pin is low, the LTC3310 is in shutdown and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

The MODE/SYNC pin synchronizes the switching frequency to an external clock. It can be a clock output for multi-phase operation. It also sets the PWM mode. The PWM modes of operation are either pulse-skipping or forced continuous mode. See the LTC3310 data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of V_{OUT} to V_{IN} and the available inductor values. The maximum allowable operating frequency may be calculated using Equation 4.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot T_{ON(MIN)}} \quad (4)$$

Select an operating switching frequency below f_{SW}(MAX). Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3310 operating load, 10A. Use Equations 5 and 6 to calculate the inductor value to obtain a 30% (3A) inductor ripple for the operating frequency.

$$L \geq \frac{V_{OUT}}{3A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \geq 0.5 \quad (5)$$

$$L \geq \frac{0.25V_{OUT}}{3A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \geq 0.5 \quad (6)$$

When determining the compensation components, C4, C10, C11 and R12, controlling the loop stability and transient response are the two main considerations. The LTC3310 has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces required output capacitance to meet the desired transient voltage range. The mid-band gain of the loop increases with R12 and the bandwidth of the loop increases with decreasing C11. C4 along with R9 provides a phase lead which will improve the phase margin. C10 along with R12 provides a high frequency pole to reduce the high frequency gain.

Loop stability is generally measured using the Bode Plot method of plotting loop gain in dB and phase shift in degrees. The 0dB crossover frequency should be less the 1/6 of the operating frequency to reduce the effects of added phase shift of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

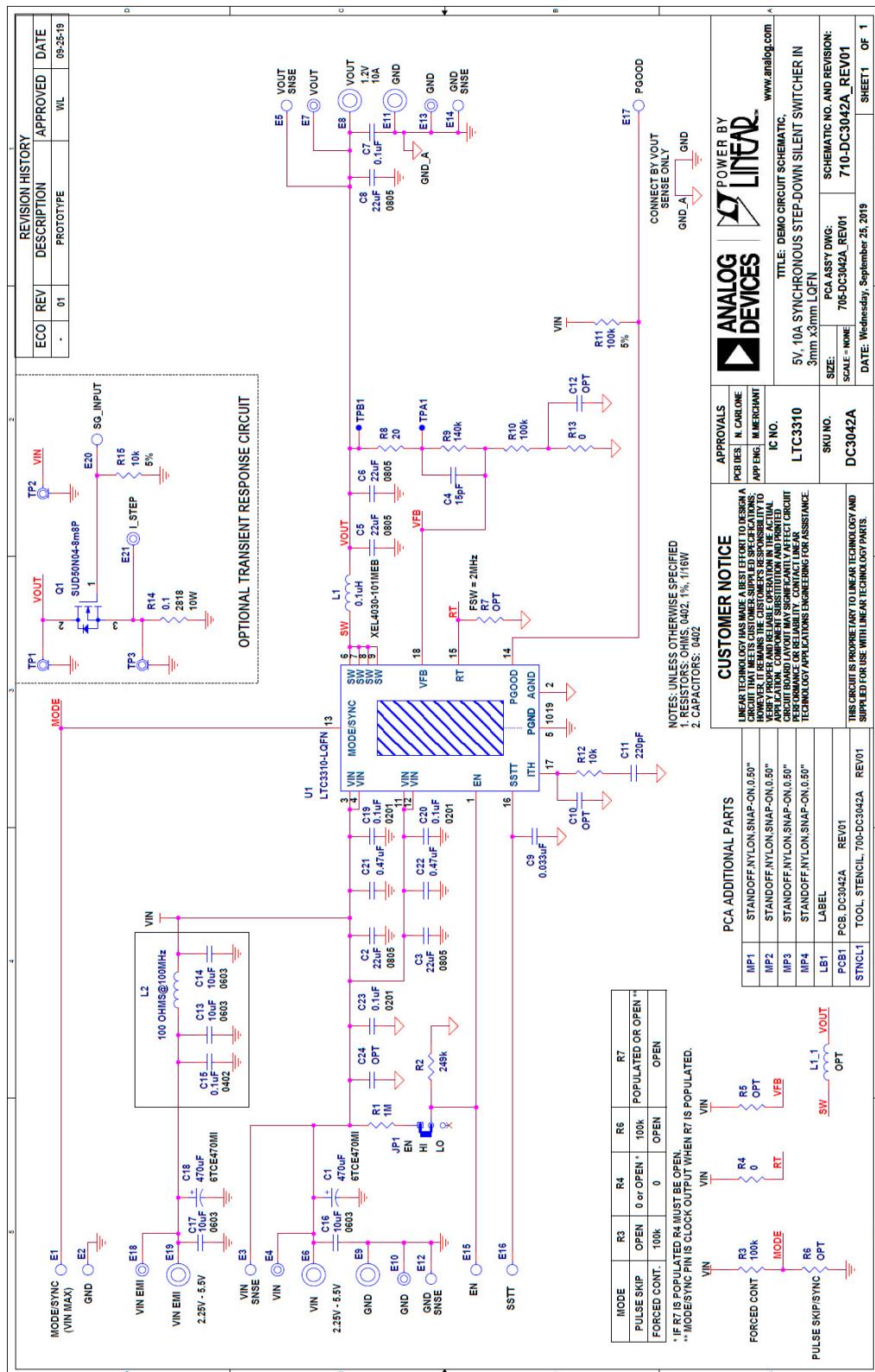
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PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	4	C2, C3, C5, C6	CAP, 22µF, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
2	1	C4	CAP, 15pF, COG/NPO, 50V, 5%, 0402	KEMET, C0402C150J5GAC7867
3	1	C9	CAP, 0.033µF, X7R, 25V, 10%, 0402	KEMET, C0402C333K3RACTU
4	1	C11	CAP, 220pF, X7R, 50V, 10%, 0402	YAGEO, CC0402KRX7R9BB221
5	2	C13, C14	CAP, 10µF, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
6	3	C19, C20, C23	CAP, 0.1µF, X7S, 16V, 10%, 0201	MURATA, GRM033C71C104KE14D
7	2	C21, C22	CAP, 0.47µF, X7S, 10V, 10%, 0402, AEC-Q200	MURATA, GCM155C71A474KE36D
8	1	L1	IND., 0.10µH 20% SHEILDDED POWER INDUCTOR	COILCRAFT, XEL4030-101MEC
9	1	R9	RES., 140k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402140KFKED
10	1	R10	RES., 100k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KFKED
11	1	R12	RES., 10k, 1%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2RKF1002X
12	1	U1	IC, LOW VOLTAGE SYN. STEP-DOWN REG., LQFN-18, 10A	ANALOG DEVICES, LTC3310HV#PBF
Additional Demo Board Circuit Components				
1	2	C1, C18	CAP, 470µF, TANT POLY, 6.3V, 20%, 2917	PANASONIC, 2501-2-00-80-00-00-07-0
2	2	C7, C15	CAP, 0.1µF, X7R, 50V, 10%, 0402, AEC-Q200	MURATA, GCM155R71H104KE02D
3	1	C8	CAP, 22µF, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
4	2	C16, C17	CAP, 10µF, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
5	1	L2	IND., 100Ω @ 100MHz, FERRITE BEAD, 25%, 8A, 6mΩ, 1812	WURTH ELEKTRONIK, 74279226101
6	1	Q1	XSTR., MOSFET, N-CH, 40V, 14A, TO-252 (DPAK)	VISHAY, SUD50N04-8M8P-4GE3
7	1	R1	RES., 1MΩ, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M00FKED
8	1	R2	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402249KFKED
9	2	R3, R11	RES., 100k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KJNED
10	2	R4, R13	RES., 0Ω, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04020000Z0ED
11	1	R8	RES., 20Ω, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040220R0FKED
12	1	R14	RES. 0.1Ω, 1%, 10W, 2818	VISHAY DALE, WSHP2818R1000FEA
13	1	R15	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0JNED
Hardware: For Demo Board Only				
1	10	E1-E3, E5, E12, E14-E17, E20	TEST POINT, TURRET, 0.064", MTG. HOLE	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E10, E13, E18, E21	CAP, 0.1µF, X7R, 50V, 10%, 0402, AEC-Q200	MURATA, GCM155R71H104KE02D
3	5	E6, E8, E9, E11, E19	CONN., BANANA JACK, FEMALE, THT, NONINSULATED, SWAGE	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1x3, 2mm, VERT, STR, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	KEYSTONE, 8833
6	1	XJP1	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

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SCHEMATIC DIAGRAM



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ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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