5.7 kV RMS Digital Isolators for Isolated USB 2.0 High, Full, and Low Speed

FEATURES

- USB 2.0 signaling with automatic detection of low, full, and high speed connections
  - 1.5 Mbps, 12 Mbps, and 480 Mbps data rates
- Bidirectional USB isolator for upstream or downstream ports
  - Redriving and high speed data retiming for input jitter removal and an open eye
  - Flexible clock input options
- 4.5 V to 5.5 V V_{BUSx} or 3 V to 3.6 V operation on each side
  - 21 mA typical idle, low or full speed mode supply current
  - 48 mA typical idle, high speed mode supply current
- Ultra low power standby in USB 2.0 suspend (L2) or disconnect
  - 1.7 mA typical low power standby, upstream supply current
  - 20 µA typical low power standby, downstream supply current
- ±8000 V IEC 61000-4-2 ESD protection across the isolation barrier
- Passed CISPR32/EN55032 Class B emissions
- High common-mode transient immunity: 50 kV/µs typical
- Safety and regulatory approvals (pending)
  - UL (pending): 5700 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
    - IEC 62368-1, IEC 61010-1 and IEC60601-1
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-11 (VDE V 0884-11):2017-01
    - V_{IORM} = 849 V_{PEAK}
- Operating temperature range: −55°C to +125°C
- 20-lead, wide-body, increased creepage SOIC_IC package with 8.3 mm creepage and clearance

APPLICATIONS

- USB peripheral, USB host, and USB hub isolation
- Electronic test and measurement equipment
- Medical devices and integrated PCs
- Industrial PCs and isolated USB ports for debug or upgrade
- USB isolator modules and USB cable isolators

FUNCTIONAL BLOCK DIAGRAMS

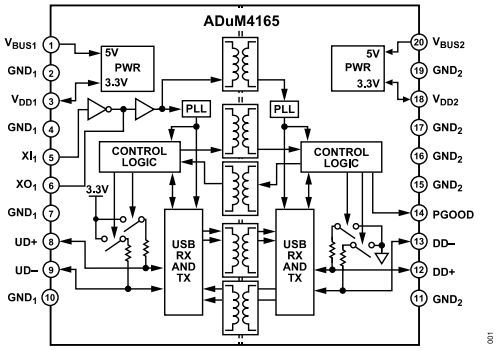

Figure 1. ADuM4165 Clock Input from Host Side

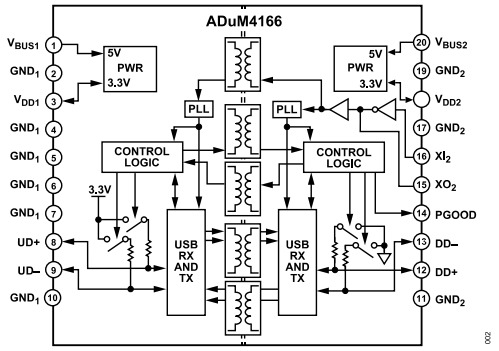

Figure 2. ADuM4166 Clock Input from Peripheral Side

GENERAL DESCRIPTION

The ADuM4165/ADuM4166[1] are USB 2.0 port isolators, utilizing Analog Devices, Inc., *i*Coupler® technology to dynamically support all USB 2.0 data rates; low (1.5 Mbps), full (12 Mbps), or high (480 Mbps), as required. The devices support host isolation with automatic speed negotiation as well as peripheral isolation.

High speed data is retimed for jitter reduction, requiring an external clock signal or crystal input. The ADuM4165 supports the clock or crystal input on the upstream side, and the ADuM4166 supports the clock or crystal input on the downstream side, offering two options to best suit the system design.

The low power standby mode for downstream (Side 2) supports applications with limited available power, such as battery-operated peripherals. The upstream (Side 1) standby current meets USB 2.0 requirements for suspended operation.

The isolators are specified over an extended industrial temperature range of −55°C to +125°C and are available in a 20-lead, wide-body, increased creepage SOIC_IC with 8.3 mm creepage and clearance.

[1] Protected by U.S. Patents 7,075,329; 8,432,182; 8,525,547; and 8,564,327. Other patents are pending.

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REVISION HISTORY

3/2022—Revision 0: Initial Version

SPECIFICATIONS

4.5 V ≤ V_{BUS1} ≤ 5.5 V, 4.5 V ≤ V_{BUS2} ≤ 5.5 V, 3.0 V ≤ V_{DD1} ≤ 3.6 V, and 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum and maximum specifications are applied over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V, unless otherwise noted. Each voltage is relative to its respective ground.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Supply Current						
Idle (V_{DD1}, V_{DD2}, V_{BUS1} or V_{BUS2})[1]						UD+, UD−, DD+, and DD− idle
Low or Full Speed Mode	$I_{DD1(LFI)}$, $I_{DD2(LFI)}$		21	27	mA	
High Speed Mode	$I_{DD1(HI)}$, $I_{DD2(HI)}$		48	60	mA	
Busy (V_{DD1}, V_{DD2}, V_{BUS1}, or V_{BUS2})[2]						
Low Speed Mode	$I_{DD1(L)}$, $I_{DD2(L)}$		29	45	mA	Input frequency (f_{IN}) = 750 kHz, load capacitance (C_L) = 450 pF
Full Speed Mode	$I_{DD1(F)}$, $I_{DD2(F)}$		31	45	mA	f_{IN} = 6 MHz, C_L = 50 pF
High Speed Mode	$I_{DD1(H)}$, $I_{DD2(H)}$		59	70	mA	f_{IN} = 240 MHz, C_L = 10 pF
Low Power Standby						USB suspended or disconnected
Upstream (V_{DD1} or V_{BUS1})	$I_{DD1(S)}$		1.7	2.5	mA	Side 2 not powered
			1.7		mA	Side 2 powered (average)
Downstream (V_{DD2} and V_{BUS2})	$I_{DD2(S)}$		20	40	µA	V_{BUS2} = V_{DD2} = 3 V to 3.6 V, Side 1 not powered
			40	100	µA	V_{BUS2} = 4.5 V to 5.5 V, Side 1 not powered
			40		µA	Side 1 powered (average)
V_{DD2} Maximum Voltage Until After Side 1 Start-Up	V_{START}			3.5	V	See the PGOOD, Clock, and Power Sequencing section
Side 1 Start-Up Time	t_{START}		3		ms	Time after V_{DD1} rises above V_{UVLO3+}[3] before V_{DD2} can be >3.5 V, see the PGOOD, Clock, and Power Sequencing section
V_{BUS1} or V_{BUS2} Undervoltage Lockout (UVLO)						
UVLO Threshold, V_{BUS1} or V_{BUS2} Rising	V_{UVLO5+}	3.5	4.16	4.35	V	
UVLO Threshold, V_{BUS1} or V_{BUS2} Falling	V_{UVLO5-}	3.0	3.77	3.95	V	
V_{BUS1} or V_{BUS2} UVLO Hysteresis	$V_{UVLO5HST}$		0.44		V	
V_{DD1} or V_{DD2} Undervoltage Lockout						
UVLO Threshold, V_{DD1} or V_{DD2} Rising	V_{UVLO3+}	2.4	2.77	2.95	V	
UVLO Threshold, V_{DD1} or V_{DD2} Falling	V_{UVLO3-}	2.2	2.60	2.90	V	
V_{DD1} or V_{DD2} UVLO Hysteresis	$V_{UVLO3HST}$		0.18		V	
LOGIC INPUTS						
Input Current	I_{IN}					0 V ≤ input voltage (V_{IN}) ≤ 3.6 V
UD+ and UD−		−20	+0.1	+20	µA	
DD+ and DD−		−250	+0.1	+250	µA	
XI_1 and XI_2		−30	+0.1	+30	µA	
Single-Ended Inputs						
Input Logic High Threshold	V_{IH}	2.0			V	
Input Logic Low Threshold	V_{IL}			0.8	V	
Input Hysteresis	V_{HYS}		0.4		V	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
High Speed Input Differential Threshold[4]	V_{TH}		0.09		V	|(DD+) – (DD−)| or |(UD+) – (UD−)|
Low and Full Speed Differential Input Sensitivity[4]	V_{DI}	0.2			V	|(DD+) – (DD−)| or |(UD+) – (UD−)|
OUTPUTS (DRIVERS)						
Low or Full Speed Output Voltages						UD+, UD−, DD+, and DD−
Logic High	V_{OH}	0.8 V_{DDx}		3.6	V	Load resistance (R_L) = 15 kΩ, load voltage (V_L) = 0 V
Logic Low	V_{OL}	0		0.3	V	R_L = 1.5 kΩ, V_L = 3.6 V
Transceiver Capacitance[4]	C_{IN}		14		pF	$C_{IN, UD+}$ or $C_{IN, UD-}$ (UD+ or UD− to GND_1), $C_{IN, DD+}$ or $C_{IN, DD-}$ (DD+ or DD− to GND_2), f_{IN} = 6 MHz
			19		pF	$C_{IN, UD+}$, $C_{IN, UD-}$, $C_{IN, DD+}$ or $C_{IN, DD-}$, f_{IN} = 240 MHz
Capacitance Matching[4]			1		%	$\|1 - C_{IN, UD+}/C_{IN, UD-}\|$
			3		%	$\|1- C_{IN, DD+}/C_{IN, DD-}\|$
Full Speed Driver Impedance	Z_{OUTH}	40.5	45	49.5	Ω	
Impedance Matching			10		%	UD+ and UD− or DD+ and DD−
COMMON-MODE TRANSIENT IMMUNITY[4]						Common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V[5]
At Logic High Output[6]	$\|CMTI_H\|$	40	50		kV/µs	$V_{IN} = V_{DD1}$ for UD+ or UD− (other input = 0 V), $V_{IN} = V_{DD2}$ for DD+ or DD− (other input = 0 V)
At Logic Low Output[7]	$\|CMTI_L\|$	40	50		kV/µs	UD+ and UD− = 0 V, or DD+ and DD− = 0 V

1 Measured when the device is powered, connected to a USB host, and connected to a USB peripheral using the specified communication speed. However, the USB is idle without being suspended, meaning there has been no USB activity for a frame interval (1 ms for low or full speed, or 0.125 ms for high speed), but short keep alive packets may be occurring within each frame to keep the USB from suspending.

2 The busy USB supply current values are for the device running at a fixed continuous data rate at 50% duty cycle, alternating J and K states. Supply current values are specified with a USB-compliant load present.

3 V_{UVLO3+} is the UVLO threshold, V_{DD1} or V_{DD2} rising.

4 These specifications are guaranteed by design and characterization.

5 CMTI is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. V_{CM} is the common-mode potential difference between Side 1 and Side 2. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

6 Output voltage for UD+ or UD− > 0.8 V_{DD1} (other output ≤ 0.3 V), and output voltage for DD+ or DD− > 0.8 V_{DD2} (other output ≤ 0.3 V).

7 UD+ and UD− ≤ 0.3 V or DD+ and DD− ≤ 0.3 V.

SPECIFICATIONS

TIMING SPECIFICATIONS

4.5 V ≤ V_{BUS1} ≤ 5.5 V, 4.5 V ≤ V_{BUS2} ≤ 5.5 V, 3.0 V ≤ V_{DD1} ≤ 3.6 V, and 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum and maximum specifications were applied over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V, unless otherwise noted. Each voltage is relative to its respective ground.

Table 2.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
USB INPUT AND OUTPUT PINS LOW SPEED MODE						UD+, UD−, DD+, and DD− and C_L = 450 pF
Data Rate			1.5		Mbps	
Propagation Delay[2]	t_{PHLL}, t_{PLHL}	300	500	600	ns	T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V
		300	500	650	ns	
Output Rise and Fall Time (10% to 90%)	t_{RL}/t_{FL}	75		300	ns	T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V
		75		350	ns	
Differential Jitter						
Next Transition	$\|t_{LJN}\|$		5		ns	
Paired J to K Transition	$\|t_{LJPJK}\|$		2		ns	
Paired K to J Transition	$\|t_{LJPKJ}\|$		3		ns	
USB INPUT AND OUTPUT PINS FULL SPEED MODE						UD+, UD−, DD+, and DD−, and C_L = 50 pF
Data Rate			12		Mbps	
Propagation Delay[2]	t_{PHLF}, t_{PLHF}	70	110	140	ns	
Output Rise/Fall Time (10% to 90%)	t_{RF}/t_{FF}	4		20	ns	T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V
		4		32	ns	
Differential Jitter						
Next Transition	$\|t_{FJN}\|$		450		ps	
Paired J to K Transition	$\|t_{FJPJK}\|$		300		ps	
Paired K to J Transition	$\|t_{FJPKJ}\|$		500		ps	
USB INPUT AND OUTPUT PINS HIGH SPEED MODE						UD+, UD−, DD+, and DD−, and C_L = 10 pF
Data Rate			480		Mbps	
Propagation Delay[3]	t_{PHLH}, t_{PLHH}	71	73	77	ns	
Output Rise and Fall Time (10% to 90%)	t_{RH}, t_{FH}	675			ps	
Differential Jitter (rms)						
Next Transition	$\|t_{HJN(R)}\|$		40		ps rms	
Paired J to K Transition	$\|t_{HJPJK(R)}\|$		11		ps rms	
Paired K to J Transition	$\|t_{HJPKJ(R)}\|$		14		ps rms	
Differential Jitter (peak)						
Next Transition	$\|t_{HJN(P)}\|$		90		ps	
Paired J to K Transition	$\|t_{HJPJK(P)}\|$		30		ps	
Paired K to J Transition	$\|t_{HJPKJ(P)}\|$		40		ps	

[1] These specifications are guaranteed by design and characterization.

[2] Propagation delay of the low or full speed USB signals in either direction is measured from the 50% level of the input signal rising or falling edge to the 50% level of the rising or falling edge of the corresponding output signal. This delay is between one and two hub differential data delays as defined in USB 2.0 specification, Table 7-11 (T_{HDD1} and T_{LHDD} parameters).

[3] Propagation delay of the high speed USB signals in either direction is measured from the 50% level of the input signal rising or falling edge to the 50% level of the rising or falling edge of the corresponding output signal. This delay is specified to be less than one hub data delay (without cable) as defined in USB 2.0 specification, Table 7-11 (T_{HSHDD} parameter).

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5.7	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	Voltage (input to output) (V_{I-O}) = 500 V dc
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Frequency = 1 MHz

[1] Device is considered a 2-terminal device; Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.

REGULATORY INFORMATION

See Table 10 for details regarding the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

Regulatory Agency	Standard Certification/Approval	File
UL (Pending)	To be recognized under UL 1577 Component Recognition Program[1] Single protection, 5700 V rms isolation voltage	E214100
CSA (Pending)[2]	To be approved under CSA Component Acceptance Notice 5A CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition Basic insulation at 830 V rms Reinforced insulation at 415 V rms CSA 61010-1-12+A1 and IEC 61010-1 third edition Basic insulation at 600 V rms Reinforced insulation at 300 V rms CSA 60601-1:14 and IEC60601-1 third edition, A1	205078
VDE (Pending)	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[3] Reinforced insulation, V_{IORM} = 849 V_{PEAK}, V_{IOSM} = 10000 V_{PEAK}	2471900-4880-0001
CQC (Pending)	To be certified according to GB4943.1-2011 per CQC11-471543-2015 Basic insulation at 820 V rms (1159 V_{PEAK}) Reinforced insulation at 410 V rms (578 V_{PEAK})	Pending

[1] In accordance with UL 1577, each ADuM4165/ADuM4166 is proof tested by applying an insulation test voltage ≥6840 V rms for 1 sec.

[2] Working voltages are quoted for Pollution Degree 2, Material Group III. ADuM4165/ADuM4166 case material has been evaluated by CSA as Material Group I.

[3] In accordance with DIN V VDE V 0884-11, each ADuM4165/ADuM4166 is proof tested by applying an insulation test voltage ≥1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

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DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 6.

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1274	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1019	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Surge Isolation Voltage				
Reinforced	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.5	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-11.

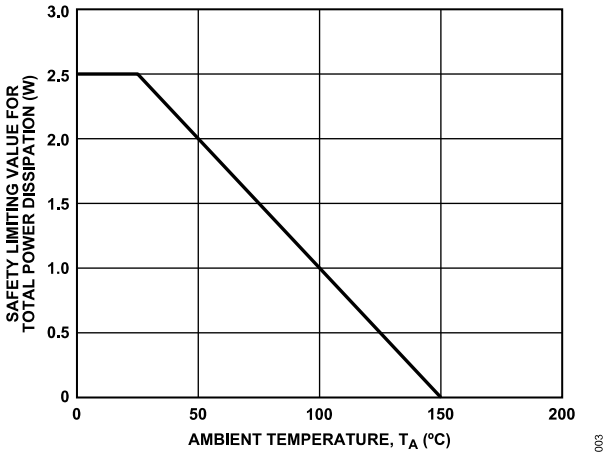


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Rating
Operating Temperature	T_A	−55°C to +125°C
Supply Voltages	V_{BUS1}, V_{BUS2}	3.0 V to 5.5 V
	V_{DD1}, V_{DD2}	3.0 V to 3.6 V

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply (V_{BUS1}, V_{DD1}) to GND_1	−0.5 V to +6.5 V
Supply (V_{BUS2}, V_{DD2}) to GND_2	−0.5 V to +6.5 V
Upstream Input Voltage (UD−, UD+, XI_1, and XO_1) to GND_1	−0.5 V to V_{DD1} + 0.5 V
Downstream Input Voltage (DD−, DD+, XI_2, XO_2, and PGOOD) to GND_2	−0.5 V to V_{DD2} + 0.5 V
Common-Mode Transients[1]	−100 kV/µs to +100 kV/µs
Temperature	
Operating Range	−55°C to +125°C
Storage Range	−65°C to +150°C
Junction (T_J Maximum)	150°C
Power Dissipation[2]	(T_J maximum − T_A)/θ_{JA}

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

[2] See Figure 3 for the maximum power dissipation for various temperatures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. Ψ_{JT} is the junction to top thermal characterization parameter.

Table 9. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
RI-20-1	50	2.3	°C/W

[1] Test Condition 1: thermal impedance simulated with 4-layer standard JEDEC PCB.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	650 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	600 V rms	Reinforced insulation rating per IEC60747-17. Accumulative FROL ≤ 1 ppm at 26 years.
Unipolar Waveform		
Basic Insulation	1838 V_{PEAK}	Rating limited by AC bipolar waveform accumulative FROL ≤ 1000 ppm at 20 years.
Reinforced Insulation	1355 V_{PEAK}	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	1660 V dc	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Reinforced Insulation	830 V dc	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADuM4165/ADuM4166

Table 11. ADuM4165/ADuM4166, 20-Lead SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4000	3A
IEC[2]	±8000 (contact discharge)	Level 4

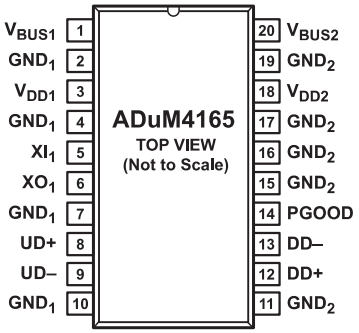
[1] All pins to respective GNDx, 1.5 kΩ, 100 pF.

[2] GND_1 to GND_2 or GND_2 to GND_1 across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES:
1. PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO SIDE 1 PCB GROUND IS RECOMMENDED.
2. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO SIDE 2 PCB GROUND IS RECOMMENDED.

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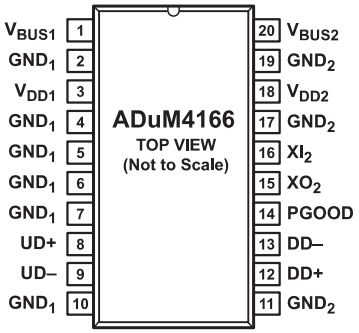
Figure 4. ADuM4165 Pin Configuration

Table 12. ADuM4165 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{BUS1}	Optional 5 V Power Supply/Low Dropout (LDO) Input for Side 1. Connect V_{BUS1} to 4.5 V to 5.5 V and bypass to GND_1 using a 0.1 µF capacitor to power Side 1 from a 5 V supply (an integrated LDO regulator generates the 3.3 V required internally). Alternatively, if powering Isolator Side 1 directly from an external 3.3 V power supply, connect both V_{BUS1} and V_{DD1} together to 3.3 V. (Bypass to GND_1 is still required.)
2, 10	GND_1	Ground, Side 1. Ground reference for Isolator Side 1, connect to Side 1 PCB ground.
3	V_{DD1}	3.3 V Power Supply/LDO Output for Side 1. Bypass to GND_1 with a required capacitor value of 0.1 µF for correct operation of the internal 3.3 V regulator (used when connecting 5 V to V_{BUS1}). Alternatively, if powering Isolator Side 1 directly from an external 3.3 V power supply, connect both V_{BUS1} and V_{DD1} together to 3.3 V. (Bypass to GND_1 is still required.)
4, 7	GND_1	Ground, Side 1. These pins must be connected to Side 1 PCB ground for proper operation. These pins are not suitable for connection of bypass capacitance.
5	XI_1	Crystal Input or External Clock Input, Isolator Side 1.
6	XO_1	Crystal Output Driver, Isolator Side 1.
8	UD+	USB D+ Signal, Upstream (Isolator Side 1).
9	UD−	USB D− Signal, Upstream (Isolator Side 1).
11, 19	GND_2	Ground 2. Ground reference for Isolator Side 2, connect to Side 2 PCB ground.
12	DD+	USB D+ Signal, Downstream (Isolator Side 2).
13	DD−	USB D− Signal, Downstream (Isolator Side 2).
14	PGOOD	Power Good. High output indicates that the voltages at V_{BUS1}/V_{DD1} and V_{BUS2}/V_{DD2} are greater than UVLO thresholds, and low output indicates V_{BUS1}/V_{DD1} or V_{BUS2}/V_{DD2} are less than UVLO thresholds. When PGOOD is low, Side 2 reverts to low power standby mode.
15, 16, 17	GND_2	Ground 2. These pins must be connected to Side 2 PCB ground for proper operation. These pins are not suitable for connection of bypass capacitance.
18	V_{DD2}	3.3 V Power Supply/LDO Output for Side 2. Bypass to GND_2 with a required capacitor value of 0.1 µF for correct operation of the internal 3.3 V regulator (used when connecting 5 V to V_{BUS2}). Alternatively, if powering Isolator Side 2 directly from an external 3.3 V power supply, connect both V_{BUS2} and V_{DD2} together to 3.3 V. (Bypass to GND_2 is still required.)
20	V_{BUS2}	Optional 5 V Power Supply/LDO Input for Side 2. Connect V_{BUS2} to 4.5 V to 5.5 V and bypass to GND_2 using a 0.1 µF capacitor to power Side 2 from a 5 V supply (an integrated LDO regulator generates the 3.3 V required internally). Alternatively, if powering Isolator Side 2 directly from an external 3.3 V power supply, connect both V_{BUS2} and V_{DD2} together to 3.3 V. (Bypass to GND_2 is still required.)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES:
1. PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO SIDE 1 PCB GROUND IS RECOMMENDED.
2. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO SIDE 2 PCB GROUND IS RECOMMENDED.

005

Figure 5. ADuM4166 Pin Configuration

Table 13. ADuM4166 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{BUS1}	Optional 5 V Power Supply/LDO Input for Side 1. Connect V_{BUS1} to 4.5 V to 5.5 V and bypass to GND_1 using a 0.1 µF capacitor to power Side 1 from a 5 V supply (an integrated LDO regulator generates the 3.3 V required internally). Alternatively, if powering Isolator Side 1 directly from an external 3.3 V power supply, connect both V_{BUS1} and V_{DD1} together to 3.3 V. (Bypass to GND_1 is still required.)
2, 10	GND_1	Ground, Side 1. Ground reference for Isolator Side 1, connect to Side 1 PCB ground.
3	V_{DD1}	3.3 V Power Supply/LDO Output for Side 1. Bypass to GND_1 with a required capacitor value of 0.1 µF for correct operation of internal 3.3 V regulator (used when connecting 5 V to V_{BUS1}). Alternatively, if powering Isolator Side 1 directly from an external 3.3 V power supply, connect both V_{BUS1} and V_{DD1} together to 3.3 V. (Bypass to GND_1 is still required.)
4, 5, 6, 7	GND_1	Ground, Side 1. These pins must be connected to Side 1 PCB ground for proper operation. These pins are not suitable for connection of bypass capacitance.
8	UD+	USB D+ Signal, Upstream (Isolator Side 1).
9	UD−	USB D− Signal, Upstream (Isolator Side 1).
11, 19	GND_2	Ground 2. Ground reference for isolator side 2, connect to side 2 PCB ground.
12	DD+	USB D+ Signal, Downstream (Isolator Side 2).
13	DD−	USB D− Signal, Downstream (Isolator Side 2).
14	PGOOD	Power Good. High output indicates that the voltages at V_{BUS1}/V_{DD1} and V_{BUS2}/V_{DD2} are greater than UVLO thresholds, and low output indicates V_{BUS1}/V_{DD1} or V_{BUS2}/V_{DD2} are less than UVLO thresholds. When PGOOD is low, Side 2 reverts to low power standby mode.
15	XO_2	Crystal Output Driver, Isolator Side 2.
16	XI_2	Crystal Input or External Clock Input, Isolator Side 2.
17	GND_2	Ground 2. This pin must be connected to Side 2 PCB ground for proper operation. This pin is not suitable for connection of bypass capacitance.
18	V_{DD2}	3.3 V Power Supply/LDO Output for Side 2. Bypass to GND_2 with a required capacitor value of 0.1 µF for correct operation of internal 3.3 V regulator (used when connecting 5 V to V_{BUS2}). Alternatively, if powering Isolator Side 2 directly from an external 3.3 V power supply, connect both V_{BUS2} and V_{DD2} together to 3.3 V. (Bypass to GND_2 is still required).
20	V_{BUS2}	Optional 5 V Power Supply/LDO Input for Side 2. Connect V_{BUS2} to 4.5 V to 5.5 V and bypass to GND_2 using a 0.1 µF capacitor to power Side 2 from a 5 V supply (an integrated LDO regulator generates the 3.3 V required internally). Alternatively, if powering Isolator Side 2 directly from an external 3.3 V power supply, connect both V_{BUS2} and V_{DD2} together to 3.3 V. (Bypass to GND_2 is still required).

TRUTH TABLES

Table 14. USB Signals, All Modes

State	UD+	UD−	DD+	DD−
Downstream Disconnected	*Low (host pull-down)*	*Low (host pull-down)*	Low (15 kΩ pull-down)	Low (15 kΩ pull-down)
No Host or Peripheral	*High-Z*	*High-Z*	Low (15 kΩ pull-down)	Low (15 kΩ pull-down)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 15. USB Signals, High Speed

State	UD+	UD−	DD+	DD−
Idle and Reset	Low[1]	Low[1]	Low[1]	Low[1]
Initiate Suspend (<3.125 ms)	Low (host pull-down)[2]	Low (host pull-down)[2]	Low (15 kΩ pull-down)[2]	Low (15 kΩ pull-down)[2]
Suspend (>3.125 ms)	High (1.5 kΩ pull-pp)[3]	Low (host pull-down)	High (peripheral pull-up)[3]	Low (15 kΩ pull-down)
Upstream Disconnected	High (1.5 kΩ pull-up)	High-Z	High (peripheral pull-up) [4]	Low (15 kΩ pull-pown)
J to Downstream	~0.4 V due to host[1]	Low[1]	~0.4 V per UD+[1]	Low[1]
J to Upstream	~0.4 V per DD+[1]	Low[1]	~0.4 V due to peripheral[1]	Low[1]
K to Downstream	Low[1]	*~0.4 V due to Host*[1]	Low[1]	~0.4 V per UD–[1]
K to Upstream	Low[1]	~0.4 V per DD–[1]	Low[1]	~0.4 V due to peripheral[1]

[1] After high speed handshake, host and peripheral terminate to local GND with 45 Ω. The isolator also terminates UD+, UD–, DD+, and DD– to local GND with its own 45 Ω resistors. During high speed transmission, the host or peripheral and the isolator drive 17.8 mA on the appropriate D+ or D– signals, giving a voltage of ~0.4 V across the parallel 45 Ω terminations.

[2] UD+ and UD– are pulled down by the host reverting to full speed termination (connecting 15 kΩ to GND). High speed 45 Ω termination remains connected to DD+ and DD– by the peripheral, and internally by the isolator on UD+ and UD– until the peripheral switches to suspend. Upon entry to suspend, 45 Ω terminations are disconnected, and 1.5 kΩ pull-ups are connected to DD+ (by the peripheral) and UD+ (by the isolator).

[3] UD+ also has an external 15 kΩ pull-down connected by the host; a corresponding internal 15 kΩ pull-down is connected by the isolator to DD+. DD+ is high due to external 1.5 kΩ pull-up connected by the peripheral, corresponding internal 1.5 kΩ pull-up is connected on UD+, setting the UD+ pin state high.

[4] A 15 kΩ pull-down is connected on DD+.

Table 16. USB Signals, Full Speed

State	UD+[1]	UD−	DD+[1, 2]	DD–[2]
Idle and Reset	High (pull-up)	Low (host pull-down)	High (peripheral pull-up)	Low (pull-pown)
Upstream Disconnected	High (pull-up)	High-Z	High (peripheral pull-up)	Low (pull-pown)
J to Downstream	High (host)	Low (host)	High (driven per UD+)	Low (driven per UD−)
J to Upstream	High (driven per DD+)	Low (driven per DD–)	High (peripheral)	Low (peripheral)
K to Downstream	Low (host)	High (host)	Low (driven per UD+)	High (driven per UD–)
K to Upstream	Low (driven per DD+)	High (driven per DD–)	Low (peripheral)	High (peripheral)
SE0 to Downstream	Low (host)	Low (host)	Low (driven per UD+)	Low (driven per UD–)
SE0 to Upstream	Low (driven per DD+)	Low (driven per DD–)	Low (peripheral)	Low (peripheral)

[1] A 1.5 kΩ pull-up is connected on UD+ by the isolator, per peripheral 1.5 kΩ pull-up on DD+.

[2] A 15 kΩ pull-down is connected on DD+ and DD− by the isolator.

Table 17. USB Signals, Low Speed

State	UD+	UD−[1]	DD+[2]	DD–[1, 2]
Idle and Reset	Low (host pull-down)	High (pull-up)	Low (pull-down)	High (peripheral pull-up)
Upstream Disconnected	High-Z	High (pull-up)	Low (pull-down)	High (peripheral pull-up)
J to Downstream	Low (host)	High (host)	Low (driven per UD+)	High (driven per UD–)
J to Upstream	Low (driven per DD+)	High (driven per DD–)	Low (peripheral)	High (peripheral)
K to Downstream	High (host)	Low (host)	High (driven per UD+)	Low (driven per UD–)
K to Upstream	High (driven per DD+)	Low (driven per DD–)	High (peripheral)	Low (peripheral)
SE0 to Downstream	Low (host)	Low (host)	Low (driven per UD+)	Low (driven per UD−)
SE0 to Upstream	Low (driven per DD+)	Low (driven per DD−)	Low (peripheral)	Low (peripheral)

[1] A 1.5 kΩ pull-up connected on UD– by the isolator, per peripheral 1.5 kΩ pull-up on DD–.

[2] A 15 kΩ pull-down connected on DD+ and DD– by the isolator.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 18. Control Signals and Power (Positive Logic)

V_{BUS1} (V)	V_{DD1} (V)	V_{BUS2} (V)	V_{DD2} (V)	PGOOD	UD+/UD–	DD+/DD–
5 or 3.3	3.3	5 or 3.3	3.3	High	Per normal operation	Per normal operation
0	0	5 or 3.3	3.3	Low	High-Z	Low (15 kΩ pull-down)
5 or 3.3	3.3	0	0	High-Z	High-Z (no host) or low (host pull-ups)	High-Z
0	0	0	0	High-Z	High-Z	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

V_{BUS1} = V_{DD1} = 3.3 V, V_{BUS2} = V_{DD2} = 3.3 V, and T_A = 25°C unless otherwise noted.

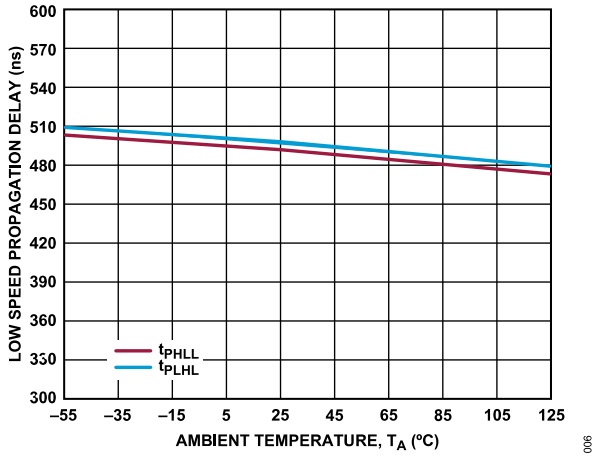


Figure 6. Low Speed Propagation Delay vs. Ambient Temperature, T_A

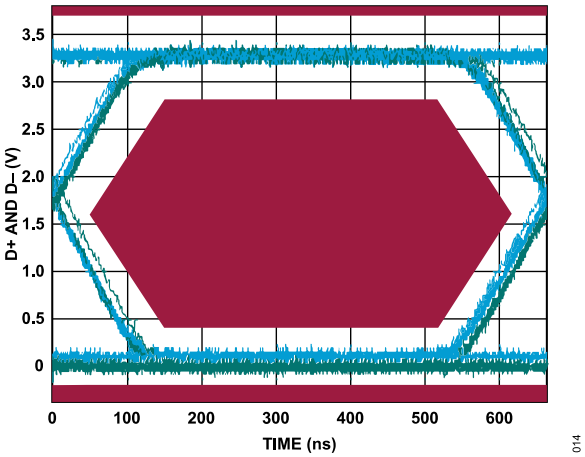


Figure 9. Low Speed Eye Diagram (Downstream Shown)

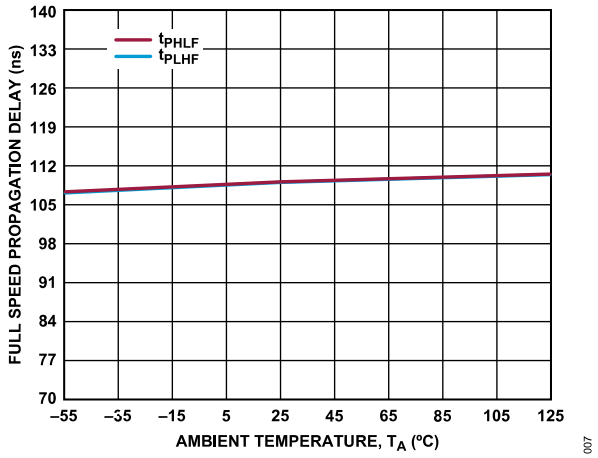


Figure 7. Full Speed Propagation Delay vs. Ambient Temperature, T_A

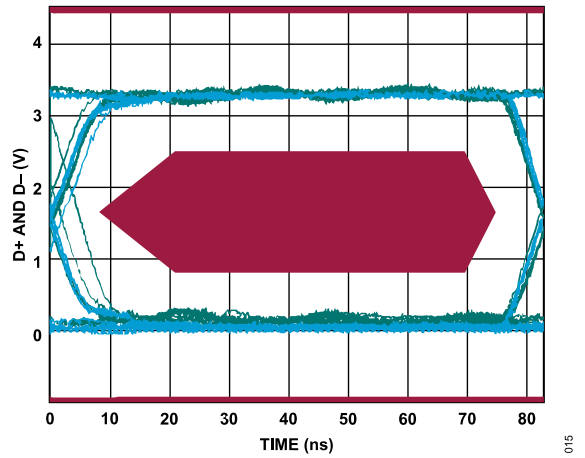


Figure 10. Full Speed Eye Diagram (Downstream Shown)

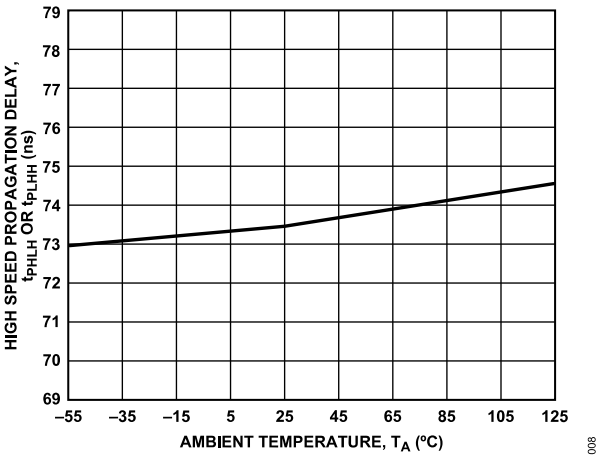


Figure 8. High Speed Propagation Delay, t_{PHLH} or t_{PLHH} vs. Ambient Temperature, T_A

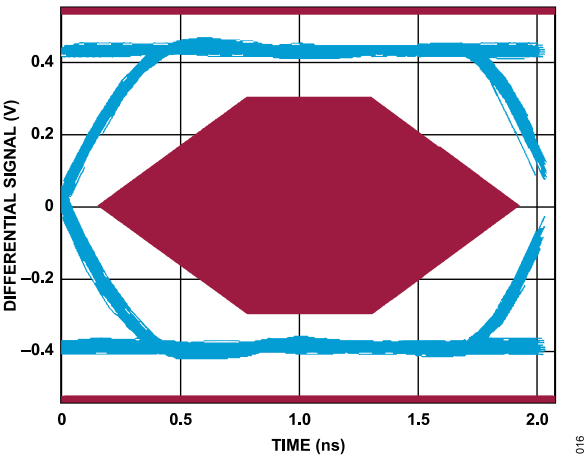


Figure 11. High Speed Eye Diagram (Downstream Shown)

TYPICAL PERFORMANCE CHARACTERISTICS

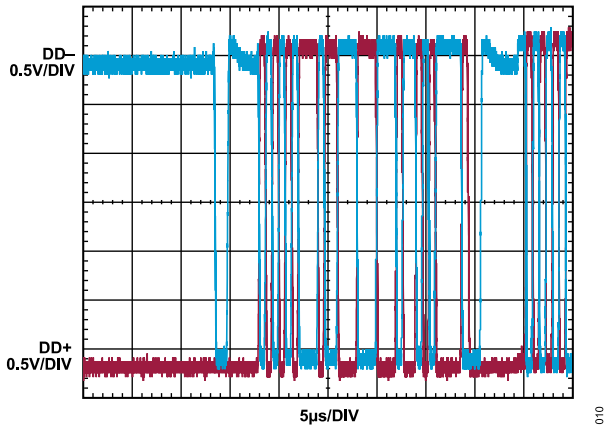


Figure 12. Low Speed Data (Downstream, DD+ and DD−)

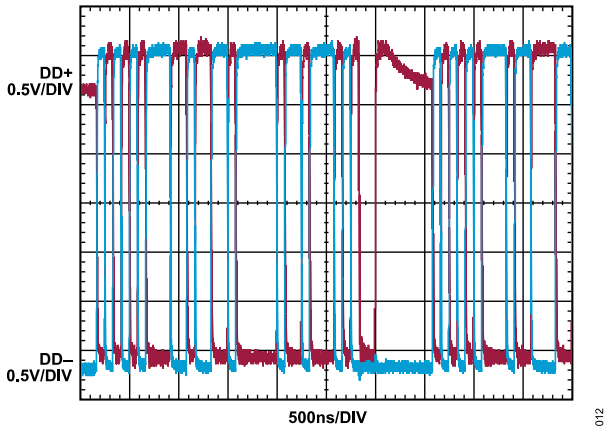


Figure 13. Full Speed Data (Downstream, DD+ and DD−)

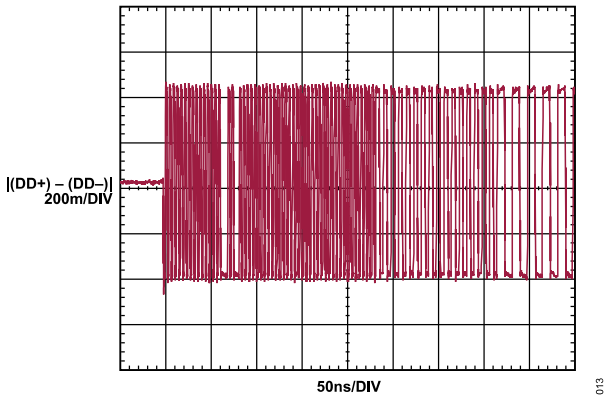


Figure 14. High Speed Data (Downstream)

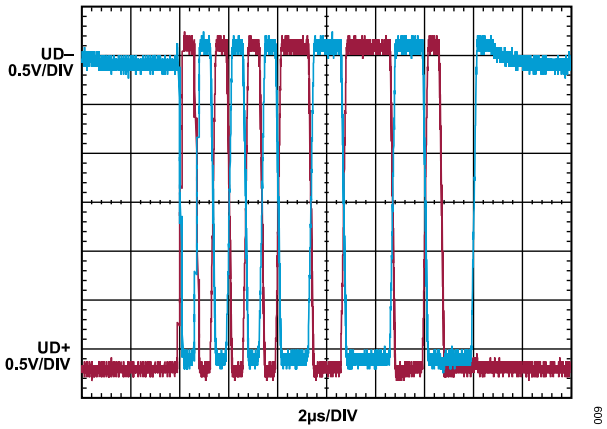


Figure 15. Low Speed Data (Upstream, UD+ and UD−)

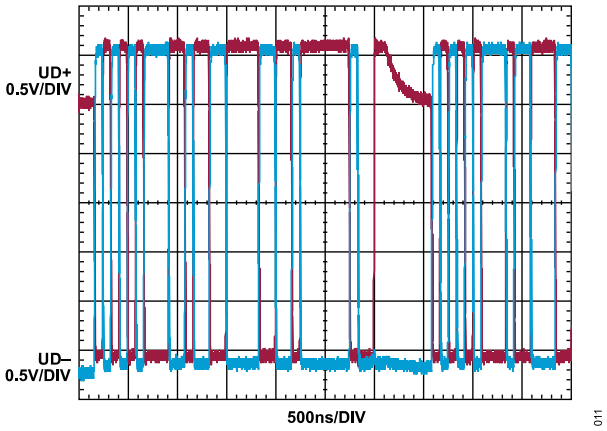


Figure 16. Full Speed Data (Upstream, UD+ and UD−)

TERMINOLOGY

Bus

The universal serial bus (USB) connects up to 127 devices via the D+ and D− signals in a star type topology with a hierarchy comprising multiple tiers (up to 6).

Upstream and Downstream

Upstream and downstream refer to the directions of the data flow on the bus. Upstream means toward the higher tiers of the USB device hierarchy (closer to the USB host atop the hierarchy), and downstream means toward the lower tiers of the USB device hierarchy (farther from the host). ADuM4165/ADuM4166 include an upstream facing port (UFP) and a downstream facing port (DFP) to allow insertion into an existing connection between a DFP (connecting to UD+ and UD–) and a UFP (connecting to DD+ and DD–).

Hub

A hub is a USB device that provides additional connections to the USB, including at least one DFP. Typically, a standalone hub has a UFP that connects to the DFP of another device, and multiple DFPs of its own to expand the number of devices that can be connected to the USB. The combination of a single upstream connection to multiple downstream connections creates a star topology. Each additional hub connecting its UFP to another DFP of a hub adds a tier in the USB hierarchy. The ADuM4165/ADuM4166 add between one and two hub plus cable delays, and accordingly, for a device integrating the isolator into a UFP or a DFP, two fewer tiers can be added to the hierarchy for that isolated USB port.

Host

A host is a USB device that includes the USB host controller and a hub (termed the root hub) containing at least one DFP, for example a PC or laptop that typically allows connection of a large variety of other USB devices.

Peripheral

A peripheral is a USB device with a UFP that can communicate with a USB host. Examples are portable devices offering access to records (mass storage and data logs), a configuration (debug port), a data stream (camera and measurements), or inputs (mouse and keyboard). Portable devices and specific purpose equipment that rely on a UFP for connection to a PC or a laptop for configuration can also include a separate USB host and associated DFP, which independently of the UFP, allows connection of a mouse, a keyboard, mass storage, or daughter modules.

Enumeration

Enumeration is the initial communication when a USB peripheral connects to the bus and identifies itself to the host, including its intended USB communication speed.

Low Speed

Low speed is the operation of USB communication at 1.5 Mbps, with voltage mode drivers to switch two signals, D+ and D−, to low and high voltage levels near 0 V and 3.3 V, respectively. During enumeration, a peripheral requests low speed communication by connecting a 1.5 kΩ pull-up to D−.

Full Speed

Full speed is the operation of USB communication at 12 Mbps, with voltage mode drivers for low speed to switch two signals, D+ and D−, but with shorter rise times, fall times, and unit intervals. During enumeration, a peripheral requests full speed communication by connecting a 1.5 kΩ pull-up to D+.

High Speed

High speed is operation of USB communication at 480 Mbps, with current mode drivers and 45 Ω to ground terminations for the D+ and D− signals, giving low and high voltage levels of approximately 0 V and 0.4 V, respectively.

During enumeration, a high speed capable peripheral initially presents as full speed (1.5 kΩ connected to D+). However, when the host resets the USB in preparation for communication, the peripheral drives current into the D− signal for high speed communication (the K state). Because the host is driving a single-ended zero into the D+ and D− signals (connecting both via 45 Ω to ground), this results in a low voltage on the D− signal of ~0.8 V. This particular chirp K signal is ignored by a full speed host. However, a high speed host can detect the chirp and initiate a handshake sequence to enter high speed mode with the peripheral, sending KJ pairs. After at least three KJ pairs, the peripheral completes the handshake by applying its 45 Ω, high speed termination resistors. Refer to Automatic Data Transfer and Modes for an example handshake through ADuM4165/ADuM4166, with the isolator ensuring both the host and the peripheral can negotiate this seamlessly. The isolator connects its own internal terminations on UD+ and UD− (45 Ω to GND_1) or DD+ and DD− (45 Ω to GND_2) at appropriate times during the handshake sequence to match behavior of host and peripheral.

End of Packet (EOP)

For low and full speed, EOP is indicated by a SE0 state at the end of a data packet, before the USB becomes idle (J state). For high speed, the SE0 state is present during idle conditions due to the 45 Ω to ground connections already present on the D+ and D– signals at both ends of the USB connection to provide high speed termination. Therefore, EOP is instead indicated by transmission of the Byte 0111 1111, distinguished by a bit stuffing error of >6 bits in a row with 1.

J State

In the J state, the D+ and D− signals are driven high or low to match the pull-up resistor applied by the peripheral. Therefore, for

TERMINOLOGY

low speed, D− is high and D+ is low, whereas for full speed, D+ is high and D− is low. Similarly for high speed (initially pull-up on D+ per full speed), the J state corresponds to a positive differential voltage (the voltage on D+ is greater than the voltage on D−, $V_{D+} > V_{D-}$). Refer to the Truth Tables section for additional information.

K State

The K state is opposite of the J state. For low speed, D+ is high, and D− is low, whereas for full speed, D− is high and D+ is low. Similarly for high speed, the K state corresponds to a negative differential voltage ($V_{D+} < V_{D-}$). Refer to the Truth Tables section for additional information.

SE0 State

In the SE0 state, both D+ and D− are driven low (regardless of any pull-up on D+ or D−). During low and full speed USB signaling, the SE0 state is used to signal EOP or reset. During high speed signaling, the SE0 state occurs between data packets and results from both the host and peripheral having 45 Ω connected from D+ to ground and from D− to ground. These 45 Ω connections provide differential termination of 90 Ω at both ends of the USB connection.

SE1 State

The SE1 state is an illegal bus state where the D+ and D− signals are both high. If this state is somehow applied to one side of ADuM4165/ADuM4166, the isolator does not propagate this error state in either direction.

Idle

In the idle state, no data is transmitted. For low and full speed, the D+ and D− signals are per the applied pull-up resistor or pulled low (D− high and D+ low for low speed, and D+ high and D− low for full speed). For high speed, no differential voltage is transmitted. However, 45 Ω to ground terminations are still present at D+ and D−, giving the SE0 state voltage conditions. Refer to the Truth Tables section for additional information.

L1 Suspend

L1 suspend is an additional sleep low power mode defined by the USB 2.0 link power management engineering change notice (ECN). This mode allows shorter entries and resume intervals than the original USB 2.0 suspend, although the maximum power consumption can be higher. L1 suspend must be entered via a handshaking packet exchange between the host and an L1 capable device, which includes negotiation of the L1 entry and exit intervals. This mode is not supported by all hosts or devices. In addition, L1 suspend is not supported by the ADuM4165/ADuM4166 because the handshake packets are not detected or interpreted by the isolator.

L2 Suspend

This mode is the standard suspend mode defined in the base USB 2.0 specification and called L2 suspend in the link power management ECN. This mode offers the lowest power consumption and is supported by the ADuM4165/ADuM4166. To initiate L2 suspend, the host stops USB data traffic on a USB segment for at least 3 ms, and connected devices detect the sustained period of idle bus.

THEORY OF OPERATION

The ADuM4165/ADuM4166 comprise galvanic isolation implemented with Analog Devices, Inc., *i*Coupler® technology enhanced for up to 480 Mbps operation, combined with USB 2.0 signal retransmission (including retiming). To repeat USB 2.0 signals bidirectionally, the isolators include both low, full, and high speed USB transmitters and receivers, and integrated phase-locked loops (PLLs) for retiming and internal synchronization. The isolators also include control logic to automatically control direction, speed, pull-ups, or pull-downs or to enter a low power suspend mode with much lower power consumption than required by the USB 2.0 standard.

AUTOMATIC DATA TRANSFER AND MODES

The ADuM4165/ADuM4166 realize the complex task of seamlessly isolating the bidirectional USB D+ and D− signals, without requiring access to external USB controllers or transceivers control signals. Isolation without interfering with USB communication is achieved with the control logic in the isolator. This control logic monitors activity on both the upstream and downstream D+ and D− waveforms and automatically determines what actions to perform, including the appropriate control of the USB transceivers integrated within the isolator, without requiring user intervention. The isolator reconstructs the signal on the output while retaining precise timing and not passing invalid SE1 states.

In addition, the isolator detects enumeration signals that set the data transfer speed to low, full, or high speed. An example of the ADuM4165/ADuM4166 allowing negotiation into high speed mode between the host and the peripheral is shown in Figure 17. After a low, full, or high speed USB connection is established, activity at a D+ or D− input sets the direction for the data transfer based on a transition from the idle state. When data direction is established, data transfer continues until either an EOP or a sufficiently long idle state is encountered. At this point, the isolator disables the USB transmitters on what was the output side and monitors both sets of D+ and D− inputs for the next activity.

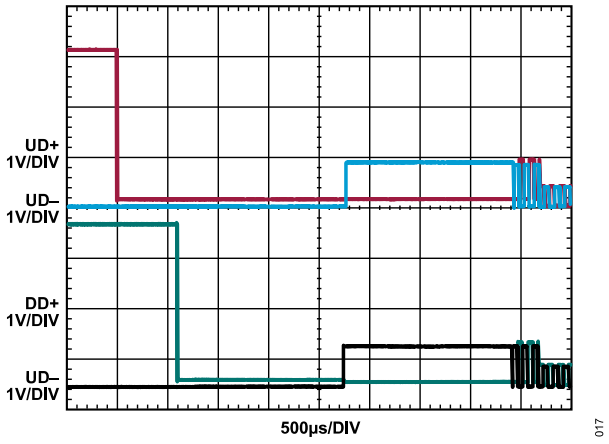


Figure 17. ADuM4166 High Speed Handshake

During data transfers, the input side of the isolator disables its USB transmitters while keeping its USB receiver active. The output side enables its USB transmitters and disables edge detection from its USB receiver. This automatic control of which side is enabled for data transmission allows the data to flow in one direction without erroneously feeding back. Logic is included to eliminate any artifacts due to different input thresholds of the differential and single-ended USB receivers. Either J, K, or SE0 transfer across the isolation barrier as one of the three valid states. The isolator output signal is a delayed copy of the input.

RETIMER AND OTHER FEATURES

In support of high speed mode, the isolator retimes the output data using an elastic buffer first in, first out (FIFO) that is clocked with a PLL locked to a precision 24 MHz reference clock applied to XI_1 or XI_2. This retiming minimizes jitter and skew in the USB output signal, providing a clean open eye that can potentially have fewer timing errors than the input signal. The XI_1 or XI_2 reference clock input is either an oscillation developed across an external crystal connected between XI_1 and XO_1 (or XI_2 and XO_2), or an external clock signal applied directly to XI_1 or XI_2. A copy of the internal PLL reference clock signal transfers through the isolation barrier. Therefore, only one clock input is required. The two versions offered for this isolator allow customers to choose where to input the clock: Side 1 for ADuM4165 or Side 2 for ADuM4166.

The retiming behavior via the elastic buffer is equivalent to that of a high speed repeater within a USB 2.0 hub, as described in USB 2.0, Chapter 7.1.14.2. As mentioned in USB 2.0, Chapter 7.1.10, such repeaters are allowed to drop up to 4 bits from the start of the synchronization field (SYNC) when repeating packets, where the packets consist of an initial SYNC pattern, followed by the packet payload and concluding with the EOP sequence. The isolator accordingly drops up to 4 bits from the start of the SYNC pattern as it copies the high speed packets from input to output as part of its elastic buffer function. All subsequent packet content is passed, including all the remaining SYNC bits, the packet payload, and the EOP. No bits are corrupted. The propagation delay conforms to USB 2.0 requirements for high speed repeaters. The isolator is equivalent to a USB 2.0 high speed repeater, in terms of data retiming, potential dropped SYNC bits, and propagation delay.

The isolator has a special low power mode to support low power peripherals. If either side of the isolator is not powered, either the host or the peripheral are disconnected or the USB is suspended, low power mode activates. During this mode, some circuits turn off to minimize power consumption, especially on Side 2 to help extend battery life in battery-operated devices. If new power connections are detected or USB activity is detected, low power mode automatically exits. The isolators comply overall with USB 2.0 requirements for suspend, resume, or remote resume situations, entering or exiting low power mode as appropriate with glitch-free transitions at D+/D–, correct resume signaling, and entry to suspend plus completion of resume within the required timing.

The isolators also provide a PGOOD output on Side 2 to indicate validity of Side 1 and Side 2 power supply voltages. PGOOD asserts when both sides have valid power supply voltages above

THEORY OF OPERATION

UVLO thresholds. PGOOD is no longer asserted if either side has an invalid supply voltage below UVLO thresholds.

ISOLATOR CHARACTERISTICS AND LOW POWER MODES

The ADuM4165/ADuM4166 combine enhanced Analog Devices, *i*Coupler channels for transmitting at 480 Mbps, high speed data rates with standard isolator channels for internal communication and synchronization. Current is steered into the input coils of the high speed channel, and the direction is switched to generate transitions on the receiving coil. This current steering technique minimizes parasitic coupling and emissions, with a trade-off of not switching off the current between edge transitions. Combining this technique with a high speed USB transceiver results in a total power consumption of approximately 50 mA per side during high speed data transfers, which is the maximum power consumption case for the isolator.

The USB isolator uses several power management techniques to reduce power consumption for each operating condition. Often in USB signaling, the D+ and D− signals only switch a small percentage of the time and are idle much more often. During the idle USB state, the isolator saves some power by turning off components that are only needed when there is active USB traffic. The isolator includes fast reacting and the higher power circuits required for high speed communications on the USB lines and across the isolation barrier. These components are turned off to save power when there is not active high speed communication, significantly reducing power for full speed or low speed connections, as well as high speed suspend mode.

If D+ and D− are idle for more than 3 ms, USB connections enter suspend mode. The isolator monitors for the suspended USB conditions, or if no peripheral is connected to Side 2 for more than 3 ms. When either is detected, the ADuM4165/ADuM4166 enter their low power mode and their internal control logic switches off many circuits to drastically reduce power consumption. The isolators automatically detect resume signals or new connections in order to exit low power mode at the appropriate times and to enable new USB communication.

These techniques working together give the following power consumption cases:

1. Approximately 48 mA or 59 mA per side for idle or busy high speed USB connections, respectively.
2. Approximately 21 mA or 30 mA per side for idle or busy, respectively, during full speed or low speed connections.
3. 1.7 mA for Side 1 and 20 µA or 40 µA for Side 2 during the low power mode, which is active when the USB is suspended or disconnected. When Side 1 is not powered, Side 2 enters low power mode with a supply current maximum of 40 µA (V_{BUS} = V_{DD2} = 3 V to 3.6 V) or 100 µA (V_{BUS2} = 4.5 V to 5.5 V). When both sides are powered, the average typical supply current for Side 1 is 1.7 mA, and the average typical supply currents for Side 2 are 20 µA or 40 µA.

Note that during suspended USB conditions, low power mode is active, and Side 1 (upstream) average power consumption is less than the 2.5 mA USB 2.0 requirement for the suspend current. Side 2 (downstream) average power consumption is even smaller, typically 20 µA or 40 µA. Enough circuits on Side 1 are kept awake to help resume active communications quickly, while Side 2 implements more aggressive power control to minimize power drawn from the peripheral. This behavior facilitates use of the isolators in battery-operated peripherals, where the peripherals may need to operate efficiently for long periods of idle time between bursts of communications.

Note that many USB systems send a keep alive signal to peripherals even when no data is required to keep the peripherals from going into a suspend state. Review the drivers when very low power is required so that the suspend state is allowed to occur.

These design features help minimize average power consumption from the isolators.

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The ADuM4165/ADuM4166 flexibly support three main implementations for isolating USB devices:

1. Isolating a USB host port, such as on an integrated PC for industrial or healthcare, or bench test and measurement equipment
2. Isolating a USB peripheral port for a USB device such as portable and battery-powered measurement equipment, or an RS-232 replacement debug for energy metering or industrial controllers
3. Integrated as a USB cable isolator or isolator box for flexible isolation of existing systems, both host and peripheral

The ADuM4165/ADuM4166 are transparent to USB traffic. No modifications to the peripheral design or isolator specific drivers are required to provide isolation, except for a requirement that while L2 suspend is implemented, L1 suspend (sleep) must not be implemented because it is not supported by the ADuM4165/ADuM4166. Another consideration is that the isolators add a propagation delay to the USB signals of between one and two hub plus cable delays. Isolated peripherals integrating the ADuM4165/ADuM4166 must be treated as if these devices contain two built-in hubs when determining the maximum number of hubs and/or tiers permitted in the end installation.

External pull-up resistors are not required because these resistors are integrated within the isolator to mirror the connection status of any USB devices attached to the downstream side of the isolator. Apart from electromagnetic compatibility (EMC) protection to meet system requirements, such as TVS diodes for ESD, the only external components required are decoupling capacitors and potentially a crystal (if a 24 MHz clock is not available from a microcontroller). The main design choices include using the ADuM4165 or the ADuM4166, implementing the required 24 MHz clock, and choosing the power supply option.

POWER SUPPLY OPTIONS

Power must be supplied separately to both sides of the ADuM4165/ADuM4166, using either 3.3 V or 5 V supplies. All combinations are supported across the full extended operating temperature range, whether using the same supply voltage on both sides, or 3.3 V on one side and 5 V on the other (either way for either the ADuM4165 or the ADuM4166). An example of the ADuM4166 with the required connections for the 5 V supply on Side 1 and the 3.3 V supply on Side 2 is shown in Figure 21.

External 5 V supplies (including from the USB cable) can be directly connected to the isolator via the V_{BUS1} pin (to power Side 1) or the V_{BUS2} pin (to power Side 2). In this configuration, the relevant V_{BUS1} or V_{BUS2} pin powers an internal LDO regulator on that side of the isolator. Either LDO regulator when connected in this configuration provides a 3.3 V output at the relevant V_{DD1} or V_{DD2} pin, which is used to power the internal circuits in the isolator including its USB transceivers. Do not use the output of either regulator to power external devices. The V_{DD1} and V_{DD2} pins require a bypass capacitor externally with a value of 0.1 µF (>0.1 µF can disrupt start-up sequencing when using the LDO regulator, while <0.1 µF can result in too much voltage ripple).

Alternatively, the LDO regulators can be bypassed and 3.3 V can be supplied directly instead to the V_{DD1} and V_{BUS1} pins together or to the V_{DD2} and V_{BUS2} pins together. This bypassing disables the relevant internal LDO regulator and may be preferred if there is already a 3.3 V supply present in the system, such as for microcontroller input and output, including a USB host or peripheral controller. Power dissipation within the isolator is lower when supplying one or both sides of the isolator with 3.3 V rather than 5 V because the supply current is similar in both cases. Both V_{DD1} and V_{DD2} must still have bypass capacitors connected; however, >0.1 µF can be used, if desired, without affecting isolator start-up sequencing.

When Side 2 is in low power mode (due to USB suspend or disconnected conditions, or the supply voltage of Side 1 is less than the UVLO thresholds), circuits within the isolator connect the V_{DD2} pin to the V_{BUS2} pin, and the V_{DD2} LDO regulator is then disabled to save power and achieve very low supply currents. If the LDO regulator was previously active (that is, V_{BUS2} connected to 5 V), V_{DD2} rises from 3.3 V to 5 V during low power mode. Upon exiting low power mode, the V_{DD2} LDO regulator is reenabled, and the V_{DD2} voltage returns to 3.3 V. By contrast, if the Side 2 LDO regulator was already inactive (V_{BUS2} = V_{DD2} = 3.3 V), the V_{DD2} voltage does not change from a nominal 3.3 V during entry to or exit from low power mode.

CLOCK OPTIONS

An external 24 MHz clock source is required by the ADuM4165/ADuM4166 to support high speed data recovery and retiming. USB 2.0 requires retiming of high speed data passing through repeaters, to prevent jitter from accumulating if data packets pass through a series of devices. The isolator performs the high speed retiming function with the aid of a precision clock input. For maximum flexibility and robustness, there are two options for implementation of the clock. A crystal can be connected between XI_1 and XO_1 for the ADuM4165 or XI_2 and XO_2 for the ADuM4166, or if a precision 24 MHz clock is available from the microprocessor, that signal can be connected to the XI_1 or XI_2 pin, and XO_1 or XO_2 can be left open.

The crystal choice and implementation are critical to proper functioning of the circuit. To meet ADuM4165/ADuM4166 specifications, a frequency tolerance of ≤50 ppm with ≤100 ppm stability is required. When using the isolator across the full extended temperature range, ensure that the system is built using a crystal meeting these requirements across the desired operating temperature range.

To comply with USB 2.0 requirements for suspend and resume, the crystal oscillator must start up within 0.3 ms as the isolator powers on initially or exits low power mode. To achieve this requirement, follow the PCB guidelines shown in Figure 21, together with a typical crystal capacitance of 10 pF and capacitive loads <10 pF to achieve timing specifications over temperature. Refer

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to EVAL-ADuM4165EBZ/EVAL-ADuM4166EBZ user guide for a specific example bill of materials (including a recommended crystal) and PCB layout.

Only one side of the isolator requires a clock input or crystal. A copy of the reference clock (internally generated for the PLL using the clock input) is passed to the other side through an isolation channel to keep both sides synchronized. For robustness, it is recommended that the clock or crystal be supplied to the side connected to the local controller. The ADuM4165 has the clock input on the upstream side (Side 1) to suit host applications, and the ADuM4166 has the clock input on the downstream side (Side 2) to suit peripheral applications. In applications like an isolated cable where there is no local controller, it is recommended to use the ADuM4165, connecting a crystal on Side 1 where power is available from the host.

PGOOD, CLOCK, AND POWER SEQUENCING

Either Side 1 or Side 2 can be powered up first (or both sides together). When Side 2 is powered up first, it enters low power mode until Side 1 is powered. When powering up Side 2 first and operating with V_{BUS2} = V_{DD2} = 3.3 V, ensure that the V_{DD2} supply voltage is not above 3.5 V until after power-up of Side 1. After the 3 ms power-up duration, the V_{DD2} supply can operate across the full 3 V to 3.6 V range.

The PGOOD output on Side 2 is only asserted once both Side 1 and Side 2 supply voltages are greater than the UVLO thresholds, and a valid clock is present (on XI_1 for the ADuM4165 or on XI_2 for the ADuM4166). Once the supplies drop to a voltage less than the UVLO thresholds, PGOOD no longer remains asserted (there may be a settling time before PGOOD = low).

When supplying the ADuM4165 with 5 V on V_{BUS1}, together with an external clock on XI_1 (rather than connecting a crystal across XI_1 and XO_1), only provide the external clock when the voltage on V_{BUS1} is greater than the 5 V UVLO thresholds. To ensure correct operation of the isolator and reliable indication of the power supply status on PGOOD, do not apply an external clock to XI_1 when V_{BUS1} is less than the 5 V UVLO thresholds. The same restriction applies to the ADuM4166 for the 5 V on V_{BUS2} and the external clock on XI_2.

The isolator can operate without this limitation by using a crystal for the clock source, or by operating the ADuM4165 with V_{BUS1} = V_{DD1} = 3.3 V, or by operating the ADuM4166 with V_{BUS2} = V_{DD2} = 3.3 V. However, it is still recommended not to apply an external clock to XI_1 or XI_2 when supply voltages are less than the 3.3 V UVLO thresholds for V_{DD1} (ADuM4165) or V_{DD2} (ADuM4166), respectively.

ISOLATED USB IMPLEMENTATIONS

Peripheral Applications

When isolating an upstream facing USB port for a USB peripheral device, choose the ADuM4166 rather than ADuM4165, to have the clock source on the controller side as shown in Figure 18. Key design points are as follows:

- Side 1 (upstream) power. Typically, the simplest solution is to power V_{BUS1} with 5 V from the USB cable (supplied by the connected USB host). When the USB cable is unplugged, Side 1 powers off and Side 2 of the ADuM4166 enters low power mode.
- Side 2 (downstream) power. If a 3.3 V rail is available for the microcontroller input and output, it can be directly applied to V_{DD2} (and also short V_{BUS2} to V_{DD2}) bypassing the internal LDO regulator of the ADuM4166. The peripheral can in theory derive power on the controller side from the USB cable via an isolated dc-to-dc converter. In this case, as well as considering the power loss due to the isolated dc-to-dc converter efficiency, the Side 1 power requirements of the ADuM4166 must also be considered. Alternatively, the peripheral can be powered from the mains or the battery. In the latter case, the ADuM4166 low power suspend automatically supports low power consumption by an unplugged peripheral in standby mode.
- USB signals. UD+ and UD− are connected via the upstream port to a USB host. Depending on the system requirements, additional EMC protection components, such as TVS diodes, may be required. DD+ and DD− are connected directly to the USB controller and have a retimed and jitter cleaned version of the USB signals.
- Clock source. Use a 24 MHz crystal connected to the XO_2 and XI_2 pins of the ADuM4166, or connect a clock from the microcontroller to XI_2 (leaving XO_2 open).
- PGOOD. For peripheral applications, once Side 2 of the ADuM4166 is powered, PGOOD can observe the status of Side 1. For example, if a USB cable providing 5 V to V_{BUS1} is unplugged, PGOOD drops low.

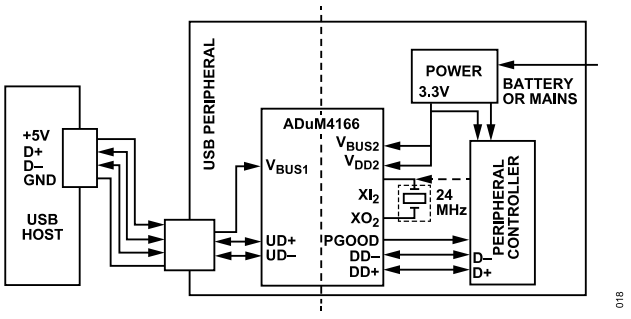

Figure 18. ADuM4166 Isolated USB Peripheral Application

When connected to a host, the isolated peripheral causes either the D+ or D− signal to be pulled high at the DFP of the host via the USB cable and the ADuM4166. The peripheral controller connects

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1.5 kΩ onto DD+ or DD−, and in response, the isolator connects 1.5 kΩ internally to GND_1 on UD+ or UD− accordingly, allowing enumeration to proceed.

Host Applications

When isolating a downstream facing USB port for a USB host, choose the ADuM4165 rather than ADuM4166 to have the clock source on the controller side as shown in Figure 19.

Key design points are as follows:

- Side 1 (upstream) power. If a 3.3 V rail is available for the microcontroller input and output, it can be directly applied to V_{DD1} (and short V_{BUS1} to V_{DD1}) bypassing the internal LDO regulator of the ADuM4165. A 5 V rail can be used if more convenient by connection to V_{BUS1} only.
- Side 2 (downstream) power. The most convenient solution is usually to power Side 2 from the same isolated power supply used to provide 5 V on the USB cable. The isolated dc-to-dc converter must provide sufficient power to meet USB requirements as well as meeting the ADuM4165 power requirements.
- USB signals. UD+ and UD− are connected directly to the USB host controller. DD+ and DD− are connected via the downstream port to a USB peripheral, and the ADuM4165 provides clean, retimed USB output signals for optimal signal integrity. Depending on the system requirements, additional EMC protection components, such as TVS diodes, may be required between DD+ and DD− and the USB port.
- Clock source. Use a 24 MHz crystal connected to the XO_1 and XI_1 pins of the ADuM4165, or connect a clock from the microcontroller to XI_1 (leaving XO_1 open).

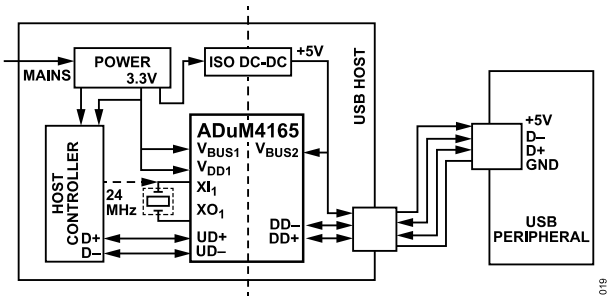

Figure 19. ADuM4165 Isolated USB Host Application

Any peripheral that is connected to the host pulls DD+ or DD− high by connecting 1.5 kΩ onto the D+ or D− signals at the peripheral end of the cable. The isolator connects 1.5 kΩ internally to GND_1 on UD+ or UD− accordingly, allowing enumeration to proceed.

Interface Applications

The ADuM4165/ADuM4166 can be used to implement USB isolation into a standalone cable isolator, connecting to both hosts and peripherals. Either the ADuM4165 or the ADuM4166 can be used.

In the example implementation shown in Figure 20, the ADuM4166 is used.

Key design points are as follows:

- Side 1 (upstream) power. Typically, the simplest solution is to power V_{BUS1} with 5 V from the USB cable (supplied by the connected USB host). When the USB cable is unplugged, Side 1 powers off and Side 2 of the ADuM4166 enters low power mode.
- Side 2 (downstream) power. The most convenient solution is usually to power Side 2 from the same power supply used to provide the 5 V on the USB cable. This power supply can be an independent supply, as shown in Figure 20, or via an isolated dc-to-dc converter that derives an isolated 5 V supply from the upstream USB cable power. When using an isolated dc-to-dc converter this way, it may be difficult to ensure the input current remains under the USB 2.0 limits for maximum permissible current drawn from the DFP of the host depending on the dc-to-dc converter efficiency and the output load, including Side 2 of the ADuM4166 together with any attached USB peripheral. An alternative in the case where an isolated dc-to-dc converter has an input current exceeding the USB 2.0 limits is to use an independent power supply for Side 2.
- USB signals. UD+ and UD− are connected via the upstream port to a USB host. Depending on the system requirements, additional EMC protection components, such as TVS diodes, may be required. DD+ and DD− are similarly connected via the downstream port to a USB peripheral, and the ADuM4166 provides a clean, retimed signal for optimal signal integrity. The same system EMC requirements typically apply to the downstream port, necessitating TVS diodes or other protection here as well.
- Clock source. Use a 24 MHz crystal connected to the XO_2 and XI_2 pins of the ADuM4166 (or connected to XO_1 and XI_1 if using the ADuM4165).

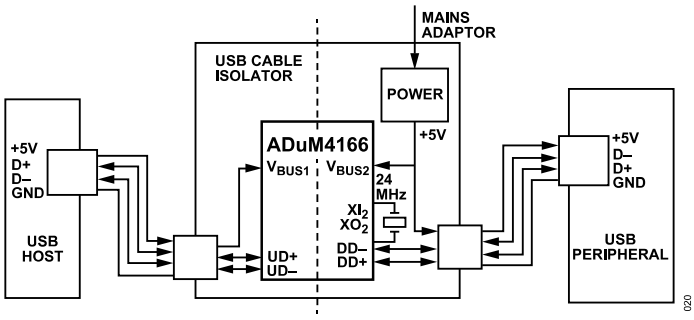

Figure 20. ADuM4166 USB Cable Isolator Application

When connected to a host via the USB cable isolator, an isolated peripheral causes either the D+ or D− signals to be pulled high at the host USB port. The peripheral controller connects 1.5 kΩ onto DD+ or DD− (via the USB cable), and in response, the isolator connects 1.5 kΩ internally to GND_1 on UD+ or UD− accordingly, allowing enumeration to proceed.

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PCB LAYOUT AND ELECTROMAGNETIC INTERFERENCE (EMI)

The ADuM4165/ADuM4166 digital isolators require no external circuitry for operation of the USB interfaces, though system EMC requirements can require additional protection components. For example, add Würth Elektronik 82402304 TVS diodes to achieve a Level 4 IEC 61000-4-2 ESD performance of ±8 kV contact discharge and ±15 kV air discharge. The ADuM4165/ADuM4166 have passed CISPR32/EN 55032 Class B limits for radiated emissions when tested on a PCB optimized for EMI by removing test points and including filtering for the off-board power supply and ground connections. The isolator remained under Class B limits while streaming high-definition video on a laptop from a USB memory stick connected via the isolator PCB. The same PCB was used to pass 10 V/m and 20 V/m field strengths for IEC 61000-4-20 radiated immunity over a frequency range of 80 MHz to 3 GHz, which is Test Level 3. The pass criteria were no loss of connection between a camera connected to a laptop via the isolator PCB and no significant variations in the image that could affect the quality of the connection during or after testing.

Power supply bypassing is required at the input and output supply pins, and possibly an external crystal oscillator, as shown in Figure 21.

Install bypass capacitors between V_{BUSx} and V_{DDx} and the local ground on each side of the chip, and connect only to the PCB ground or the specific GND_1 and GND_2 pins indicated in Pin Configurations and Function Descriptions. Connect all GND_x pins on each side together to the relevant PCB ground. The bypass capacitors must have a value of 0.1 µF for correct operation and be of a low ESR type. The total lead length between both ends of the capacitor and the power supply pin must not exceed 10 mm.

If connecting an external clock instead to XI_1 or XI_2, leave XO_1 or XO_2 open. Alternatively, if using an external crystal rather than a clock input, ensure that the trace lengths between the crystal and the relevant pins are minimized (XI_1 and XO_1, or XI_2 and XO_2) to minimize board parasitic effects.

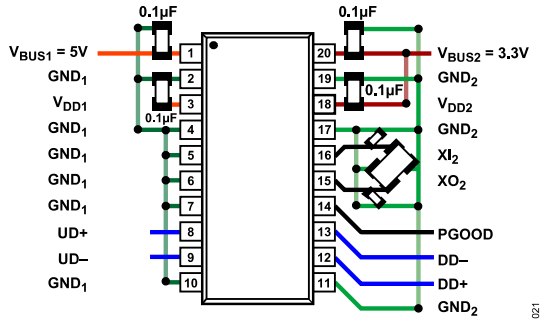

Figure 21. Required External Components and Connections (ADuM4166 with 5 V Supply to Side 1 and 3.3 V Supply to Side 2)

In applications involving high common-mode transients, it is important to minimize board capacitive coupling across the isolation barrier. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to minimize parasitic coupling can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, which allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation barrier, pollution degree, and material group. The material group and creepage for ADuM4165/ADuM4166 are detailed in Table 3.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness of the insulation, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this type of waveform reflects isolation

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from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the isolation barrier, as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 22 and the following equations.

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2}$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\ RMS}$ = 240 V rms

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. Table 10 compares the value to the limits for the working voltage for the expected lifetime. Note that the dc working voltage limit in Table 10 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

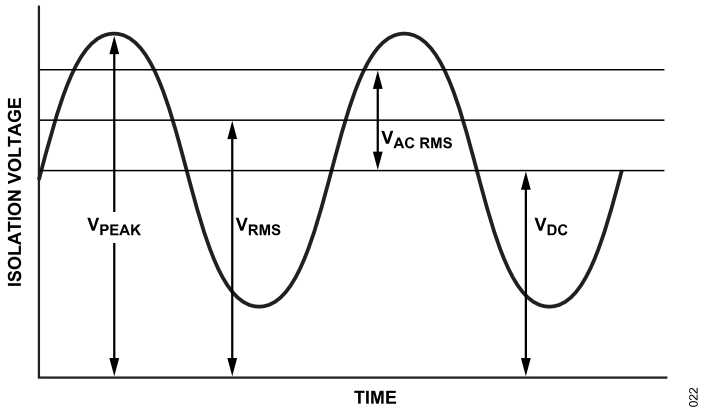

Figure 22. Critical Voltage Example

OUTLINE DIMENSIONS

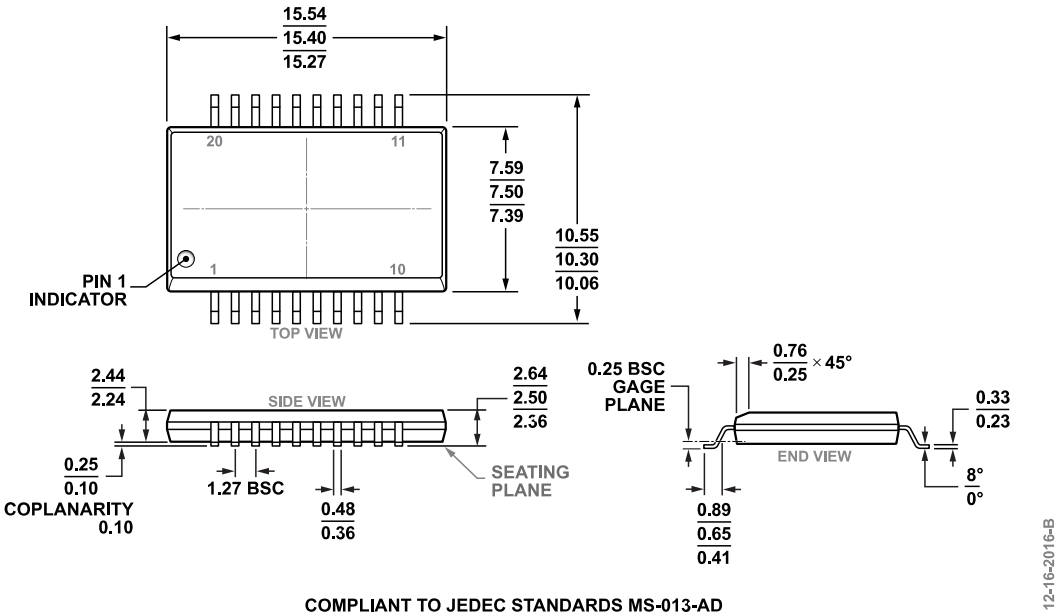

Figure 23. 20-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-20-1)
Dimensions shown in millimeters

Updated: January 29, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM4165BRIZ	−55°C to +125°C	20-Lead SOIC (Increased Creepage)	Tube, 31	RI-20-1
ADUM4165BRIZ-RL	−55°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4166BRIZ	−55°C to +125°C	20-Lead SOIC (Increased Creepage)	Tube, 31	RI-20-1
ADUM4166BRIZ-RL	−55°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuM4165EBZ	ADuM4165 Evaluation Board
EVAL-ADuM4166EBZ	ADuM4166 Evaluation Board

[1] Z = RoHS-Compliant Part.

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