

## I<sup>2</sup>C Isolator with Unidirectional SCL, Idle-bus Hot-Swap and Low VOL

**ADuM1255**

### General Description

The ADuM1255 offers two open-drain channels, one unidirectional and one bidirectional for applications, such as I<sup>2</sup>C, that require data to be transmitted in both directions on the same line, but have a unidirectional clock. To prevent latch-up action, side 1 outputs comprise special buffers that regulate the logic-low voltage at 0.64V, and the input logic-low threshold is at least 50mV lower than the output logic-low voltage. Side 2 features conventional buffers that do not regulate logic-low output voltage.

The ADuM1255 features independent 2.25V to 5.5V supplies on both side 1 and side 2 of the isolator. The device operates up to 2MHz.

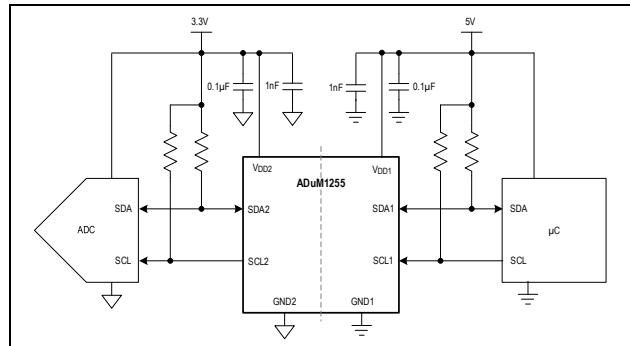
The ADuM1255 provides a disturbance-free bus connection for hot-plug connections on side 2 by first precharging the bus pins and then monitoring the bus state for either an idle bus or detection of an I<sup>2</sup>C stop condition before connecting side 1 and side 2.

The ADuM1255 is available in 8-pin narrow- and wide-body SOIC packages. The devices are rated for operation at ambient temperatures of -40°C to +125°C.

### Key Applications

- Isolated I<sup>2</sup>C/SMBus Interface
- Battery Management Systems
- Power Over Ethernet (PoE)
- Motor Control Systems

### Simplified Application Diagram



### Benefits and Features

- Low  $V_{OL(MAX)}$  for Greater I<sup>2</sup>C Device Compatibility
  - Side 1: 0.69V
  - Side 2: 0.4V
- Independent  $V_{DD1}/V_{DD2}$  Supplies Support 3.3V and 5V Logic Voltage Levels and Allow Level Shifting
  - 2.25V to 5.5V for Both Sides
- Hot-Swappable Side 2 I/O Prevents Data Corruption
  - Initial Side 2 Connection Occurs at Bus Idle or Stop States
- Bidirectional I<sup>2</sup>C Data Transfer up to 2MHz SCL
- Strong Current Sinking Enables Lower  $R_{PULL-UP}$  Values for Faster Bus Speeds
  - Side 1: 5mA
  - Side 2: 50mA
- Robust Galvanic Isolation of Digital Signals
  - Continuously Withstands ( $V_{IOWM}$ )
    - 8-Narrow SOIC: 445VRMS
    - 8-Wide SOIC: 848VRMS
  - Withstands  $\pm 10kV$  Surge per IEC 61000-4-5
  - Package Creepage and Clearance
    - 8-Narrow SOIC: 4mm
    - 8-Wide SOIC: 8mm
- Safety and Regulatory Approvals (Pending)
  - IEC60747-17 (Pending)
    - Reinforced  $V_{IORM}$  Narrow SOIC: 630VPEAK
    - Reinforced  $V_{IORM}$  Wide SOIC: 1200VPEAK
  - UL 1577 (Pending)
    - 8-Narrow SOIC: 3000VRMS for 1min
    - 8-Wide SOIC: 5000VRMS for 1min
  - IEC/EN/CSA 62368-1 (Pending)
  - IEC/EN/CSA 61010-1 (Pending)
  - CAN/CSA-C22.2 No. 14-18 (Pending)

[Ordering Information](#) appears at end of data sheet.

## Absolute Maximum Ratings

V <sub>DD1</sub> to GND1.....	-0.3V to +6.0V
V <sub>DD2</sub> to GND2 .....	-0.3V to +6.0V
SDA1, SCL1 to GND1.....	-0.3V to +6.0V
SDA2, SCL2 to GND2.....	-0.3V to +6.0V
Short-Circuit Continuous Current	
SDA1, SCL1 to V <sub>DD1</sub> .....	20mA
SDA2, SCL2 to V <sub>DD2</sub> .....	100mA
Continuous Power Dissipation	

8 NSOIC (Derate 5.49mW/°C above +70°C) .....	+440mW
8 WSOIC (Derate 5.88mW/°C above +70°C).....	+471mW
Temperature	
Operating Temperature Range.....	-40°C to +125°C
Junction Temperature.....	+150°C
Storage Temperature .....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+300°C
Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 8 Narrow SOIC

Outline Number	<a href="#">21-0041</a>
Land Pattern Number	<a href="#">90-0096</a>
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ )	182°C/W
Junction-to-Case Top Thermal Resistance ( $\theta_{JC(TOP)}$ )	50°C/W
Junction-to-Board Thermal Resistance ( $\theta_{JB}$ )	63.6°C/W
Junction-to-Case Top Thermal Characterization Parameter ( $\psi_{JT}$ )	8°C/W
Junction-to-Board Thermal Characterization Parameter ( $\psi_{JB}$ )	60°C/W
Moisture Sensitivity Level	3

**8 Wide SOIC**

Outline Number	<a href="#">21-100415</a>
Land Pattern Number	<a href="#">90-100146</a>
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ )	170°C/W
Junction-to-Case Top Thermal Resistance ( $\theta_{JC(TOP)}$ )	64°C/W
Junction-to-Board Thermal Resistance ( $\theta_{JB}$ )	60.9°C/W
Junction-to-Case Top Thermal Characterization Parameter ( $\psi_{JT}$ )	12°C/W
Junction-to-Board Thermal Characterization Parameter ( $\psi_{JB}$ )	62°C/W
Moisture Sensitivity Level	3

For the latest package outline information and land patterns (footprints), go to [www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html](#). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages](#).

**Electrical Characteristics**

( $V_{DD1} - V_{GND1} = +2.25V$  to  $+5.5V$ ,  $V_{DD2} - V_{GND2} = +2.25V$  to  $+5.5V$ ,  $C_L = 20pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted ([Note 1](#), [Note 2](#)). Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>POWER SUPPLY</b>							
Supply Voltage	$V_{DD1}$	Relative to GND1	2.25	5.5		V	
	$V_{DD2}$	Relative to GND2	2.25	5.5			
Undervoltage-Lockout Threshold Side	$V_{UVLO\_}$	$V_{DD\_}$ rising	1.48	1.6	1.65	V	
Undervoltage-Lockout Threshold Hysteresis	$V_{UVLO\_HYST}$	( <a href="#">Note 5</a> )		30		mV	
<b>SUPPLY CURRENT</b> ( <a href="#">Note 2</a> , <a href="#">Note 3</a> )							
Supply Current Side 1	$I_{DD1}$	$V_{DD1} = V_{DD2} = 2.25V$ - 5V		1		mA	
Supply Current Side 2	$I_{DD2}$	$V_{DD1} = V_{DD2} = 2.25V$ - 5V		1		mA	
<b>LOGIC INPUTS AND OUTPUTS</b>							
Input High Voltage, SDA1/SCL1	$V_{IH1}$	Relative to GND1	0.52	0.56	0.62	V	
Input Low Voltage, SDA1/SCL1	$V_{IL1}$	Relative to GND1	0.47	0.51	0.56	V	
Input Hysteresis, Side 1	$V_{HYS1}$	$V_{IH1} - V_{IL1}$	( <a href="#">Note 5</a> )		50	mV	
Output Low Voltage, SDA1	$V_{OL1}$	Relative to GND1	$I = 0.1mA$ - 5mA sink	0.59	0.64	0.69	V
Low-level Output Voltage to High-Level Input Voltage Threshold Difference, SDA1	$\Delta V_{O/IT}$	SDA1, $V_{OL} - V_{IH}$	( <a href="#">Note 4</a> )	45		mV	
Input High Voltage, SDA2	$V_{IH2}$	SDA2 to GND2	$0.52 \times V_{DD2}$	0.45 $\times V_{DD2}$		V	
Input Low Voltage, SDA2	$V_{IL2}$	SDA2 to GND2	$0.38 \times V_{DD2}$	$0.3 \times V_{DD2}$		V	

( $V_{DD1} - V_{GND1} = +2.25V$  to  $+5.5V$ ,  $V_{DD2} - V_{GND2} = +2.25V$  to  $+5.5V$ ,  $C_L = 20pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted ([Note 1](#), [Note 2](#)). Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Hysteresis, Side 2	$V_{HYS2}$	$V_{IH2} - V_{IL2}$		$0.07 \times V_{DD2}$			V
Output Low Voltage, Side 2	$V_{OL2}$	SDA2/SCL2 to GND2		I = 50mA sink		0.4	V
Static Output Loading	$I_{SDA1}$	Side 1		0.1	5		mA
	$I_{SDA2/SCL2}$	Side 2		0.1	50		
Leakage Current	$I_L$	Device unpowered	SDA1/SCL1 = 5.5V, $VDD1 = 0V$	-10	+10		$\mu A$
			SDA2/SCL2 = 5.5V, $VDD2 = 0V$	-10	+10		
		Device powered	SDA1 = SCL1 = $VDD1 = 5.5V$	-10	+10		
		Device powered and not in precharge	SDA2 = SCL2 = $VDD2 = 5.5V$	-10	+10		
Input Capacitance	$C_{IN}$	f = 1MHz	( <a href="#">Note 5</a> )		5		pF

#### ESD Protection ([Note 5](#))

ESD		Human Body Model	$V_{DD1}$ to same side pins, $V_{DD2}$ to same side pins	$\pm 8$	kV
			SDA1/SCL1 to GND1	$\pm 17$	
			SDA2/SCL2 to GND2	$\pm 17$	
		IEC 61000-4-2 contact discharge	SDA1/SCL1 to GND1 unpowered	$\pm 8$	
			SDA2/SCL2 to GND2 unpowered	$\pm 8$	
		IEC 61000-4-2 contact discharge (GND2 to GND1)	8 Wide SOIC	$\pm 5$	
			8 Narrow SOIC	$\pm 5$	

## Dynamic Characteristics

( $V_{DD1} - V_{GND1} = 2.25V$  to  $5.5V$ ,  $V_{DD2} - V_{GND2} = 2.25V$  to  $5.5V$ ,  $C_L = 20pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. ([Note 5](#)) Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	$CMTI$	( <a href="#">Note 6</a> )		100			$kV/\mu s$
Maximum Data Rate	$DR_{MAX}$			2			MHz
Fall Time	$t_{F1}$	SDA1 = $0.7 \times V_{DD1}$ to $0.3 \times V_{DD1}$	4.5V $\leq V_{DD1} \leq$ 5.5V, $C_{L1} = 40pF$ , $R_1 = 1.6k\Omega$	8.8	20.3	36.1	ns
			3.0V $\leq V_{DD1} \leq$ 3.6V, $C_{L1} = 40pF$ , $R_1 = 1k\Omega$	6.1	13.7	24.1	
			2.25V $\leq V_{DD1} \leq$ 2.75V, $C_{L1} = 40pF$ , $R_1 = 810\Omega$	4.6	10.4	18.5	

( $V_{DD1} - V_{GND1} = 2.25V$  to  $5.5V$ ,  $V_{DD2} - V_{GND2} = 2.25V$  to  $5.5V$ ,  $C_L = 20pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. ([Note 5](#))  
Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
t <sub>F2</sub>		SDA1 = $0.9 \times V_{DD1}$ to $0.9V$	$4.5V \leq V_{DD1} \leq 5.5V$ , $C_{L1} = 40pF$ , $R_1 = 1.6k\Omega$	15.4	34.7	64.7	
			$3.0V \leq V_{DD1} \leq 3.6V$ , $C_{L1} = 40pF$ , $R_1 = 1k\Omega$	9.1	19.7	35.9	
			$2.25V \leq V_{DD1} \leq 2.75V$ , $C_{L1} = 40pF$ , $R_1 = 810\Omega$	6.0	12.2	23.3	
		SDA2/SCL2 = $0.7 \times V_{DD2}$ to $0.3 \times V_{DD2}$	$4.5V \leq V_{DD2} \leq 5.5V$ , $C_{L2} = 400pF$ , $R_2 = 180\Omega$	11.8	18.6	30.0	
			$3.0V \leq V_{DD2} \leq 3.6V$ , $C_{L2} = 400pF$ , $R_2 = 120\Omega$	9.0	13.8	21.0	
			$2.25V \leq V_{DD2} \leq 2.75V$ , $C_{L2} = 400pF$ , $R_2 = 91\Omega$	7.6	11.6	17.0	
		SDA2/SCL2 = $0.9 \times V_{DD2}$ to $0.4V$	$4.5V \leq V_{DD2} \leq 5.5V$ , $C_{L2} = 400pF$ , $R_2 = 180\Omega$	25.7	41.0	63.0	
			$3.0V \leq V_{DD2} \leq 3.6V$ , $C_{L2} = 400pF$ , $R_2 = 120\Omega$	19.0	29.0	44.4	
			$2.25V \leq V_{DD2} \leq 2.75V$ , $C_{L2} = 400pF$ , $R_2 = 91\Omega$	15.5	24.0	36.3	
Propagation Delay	t <sub>PLH12</sub>	SDA1/SCL1 = $0.66V$ to SDA2/SCL2 = $0.7 \times V_{DD2}$	$4.5V \leq V_{DD\_} \leq 5.5V$ , $C_{L1} = 20pF$ , $R_1 = 1.6k\Omega$ , $C_{L2} = 20pF$ , $R_2 = 180\Omega$		37.6	50.0	ns
			$3.0V \leq V_{DD\_} \leq 3.6V$ , $C_{L1} = 20pF$ , $R_1 = 1k\Omega$ , $C_{L2} = 20pF$ , $R_2 = 120\Omega$		35.9	48.0	
			$2.25V \leq V_{DD\_} \leq 2.75V$ , $C_{L1} = 20pF$ , $R_1 = 810\Omega$ , $C_{L2} = 20pF$ , $R_2 = 91\Omega$		35.2	47.0	
	t <sub>PHL12</sub>	SDA1/SCL1 = $0.425V$ to SDA2/SCL2 = $0.3 \times V_{DD2}$	$4.5V \leq V_{DD\_} \leq 5.5V$ , $C_{L1} = 20pF$ , $R_1 = 1.6k\Omega$ , $C_{L2} = 20pF$ , $R_2 = 180\Omega$		93.7	133.3	
			$3.0V \leq V_{DD1\_} \leq 3.6V$ , $C_{L1} = 20pF$ , $R_1 = 1k\Omega$ , $C_{L2} = 20pF$ , $R_2 = 120\Omega$		84.2	116.4	
			$2.25V \leq V_{DD1\_} \leq 2.75V$ , $C_{L1} = 10pF$ , $R_1 = 810\Omega$ , $C_{L2} = 20pF$ , $R_2 = 91\Omega$		78.8	107.3	

( $V_{DD1} - V_{GND1} = 2.25V$  to  $5.5V$ ,  $V_{DD2} - V_{GND2} = 2.25V$  to  $5.5V$ ,  $C_L = 20pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. ([Note 5](#))  
Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse-Width Distortion	t <sub>PLH21</sub>	R <sub>1</sub> = 810Ω, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 91Ω				ns
		4.5V ≤ V <sub>DD</sub> ≤ 5.5V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 1.6kΩ, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 180Ω		86.7	95.8	
		3.0V ≤ V <sub>DD</sub> ≤ 3.6V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 1kΩ, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 120Ω		67.3	76.3	
	t <sub>PHL21</sub>	2.25V ≤ V <sub>DD</sub> ≤ 2.75V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 810Ω, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 91Ω		61.0	70.1	
		4.5V ≤ V <sub>DD</sub> ≤ 5.5V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 1.6kΩ, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 180Ω		82.6	128.4	
		3.0V ≤ V <sub>DD</sub> ≤ 3.6V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 1kΩ, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 120Ω		69.9	101.0	
	PWD <sub>12</sub>	2.25V ≤ V <sub>DD</sub> ≤ 2.75V, C <sub>L1</sub> = 20pF, R <sub>1</sub> = 810Ω, C <sub>L2</sub> = 20pF, R <sub>2</sub> = 91Ω		65.1	88.9	
		4.5V ≤ V <sub>DD</sub> ≤ 5.5V		56.1	94.2	
		3.0V ≤ V <sub>DD</sub> ≤ 3.6V		48.3	79.0	
Round-Trip Propagation Delay on Side 1	PWD <sub>21</sub>	2.25V ≤ V <sub>DD</sub> ≤ 2.75V		43.6	70.6	ns
		4.5V ≤ V <sub>DD</sub> ≤ 5.5V		5.9	50.7	
		3.0V ≤ V <sub>DD</sub> ≤ 3.6V		12.6	43.1	
	t <sub>LOOP1</sub>	2.25V ≤ V <sub>DD</sub> ≤ 2.75V		14.1	37.6	
		4.5V ≤ V <sub>DD</sub> ≤ 5.5V, C <sub>L1</sub> = 40pF, R <sub>1</sub> = 1.6kΩ, C <sub>L2</sub> = 400pF, R <sub>2</sub> = 180Ω		142.2	163.2	
		3.0V ≤ V <sub>DD</sub> ≤ 3.6V, C <sub>L1</sub> = 40pF, R <sub>1</sub> = 1kΩ, C <sub>L2</sub> = 400pF, R <sub>2</sub> = 120Ω		114.1	133.5	
		2.25V ≤ V <sub>DD</sub> ≤ 2.75V, C <sub>L1</sub> = 40pF, R <sub>1</sub> = 810Ω, C <sub>L2</sub> = 400pF, R <sub>2</sub> = 91Ω		101.3	122.8	
Side 1 Time from UVLO to Active State	t <sub>ACT</sub>	V <sub>DD1</sub> rising, V <sub>DD2</sub> powered up for more than t <sub>HS_EN</sub> and SDA <sub>1</sub> /SCL <sub>1</sub> high		1.1	1.7	ms

( $V_{DD1} - V_{GND1} = 2.25V$  to  $5.5V$ ,  $V_{DD2} - V_{GND2} = 2.25V$  to  $5.5V$ ,  $C_L = 20\text{pF}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. ([Note 5](#))  
Typical values are at  $V_{DD1} - V_{GND1} = 3.3V$ ,  $V_{DD2} - V_{GND2} = 3.3V$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Loss to Output High-Z	$t_{\text{Hi-Z}}$	Opposite $V_{DD}$ falling below $V_{UVLO}$				0.4	ms
<b>HOT SWAP/BUS STUCK TIMER, SIDE 2</b>							
Precharge Voltage	$V_{\text{PRECHG}}$	$SDA2/SCL2$ open, $V_{DD2} > 0.6V$	At power-up		$0.3 \times V_{DD2}$		V
Precharge Thevenin Equivalent Impedance	$R_{\text{PRECHG}}$	$SDA2/SCL2$ open, $V_{DD2} > 0.6V$	At power-up		140		$k\Omega$
Precharge Glitch Filter on $SDA2/SCL2$	$t_{\text{PRE\_GLITCH}}$	$V_{DD2}$ rising above $V_{UVLO}$	At power-up		220		ns
Hot-Swap Detection Enable Time	$t_{\text{HS\_EN}}$	At power-up			102		ms
$SDA2/SCL2$ Idle Detection Time	$t_{\text{IDLE}}$	After $t_{\text{HS\_EN}}$	At power-up		75		$\mu\text{s}$
Bus Stuck Timeout	$t_{\text{STUCK}}$	Either $SDA1$ or $SCL1$ low			102		ms

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ\text{C}$ . Specifications over temperature are guaranteed by design.

**Note 2:** All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GND1 or GND2), unless otherwise noted.

**Note 3:** The supply current does not include any current entering the  $SDA/SCL$  pins. Current is after successful hot-swap connection.  $R_1 = R_2 = 1\text{k}\Omega$ ,  $C_{L1} = C_{L2} = 10\text{pF}$ .

**Note 4:** This is the minimum difference between the output logic-low level and the input logic threshold. This ensures that there is no possibility of the part latching up the bus to which it is connected.

**Note 5:** Not production tested. Guaranteed by design.

**Note 6:** CMTI is the maximum sustainable common-mode voltage slew rate while maintaining operation. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GND1 and GND2 ( $V_{CM} = 1000\text{V}$ ).

## Timing Diagrams

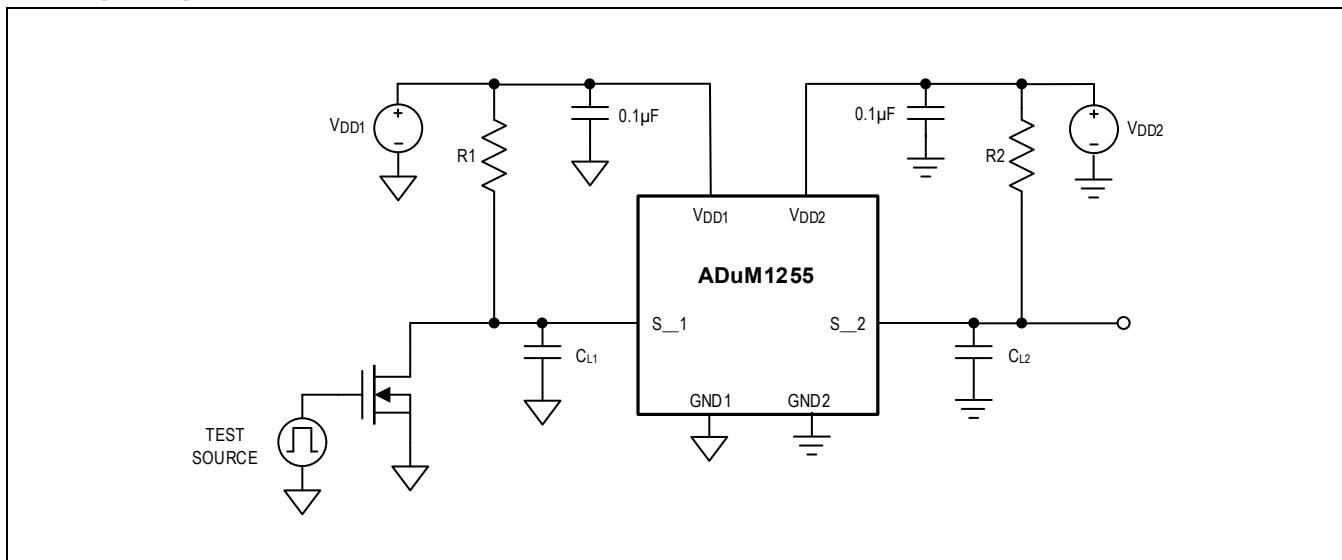


Figure 1. Timing Test Diagram

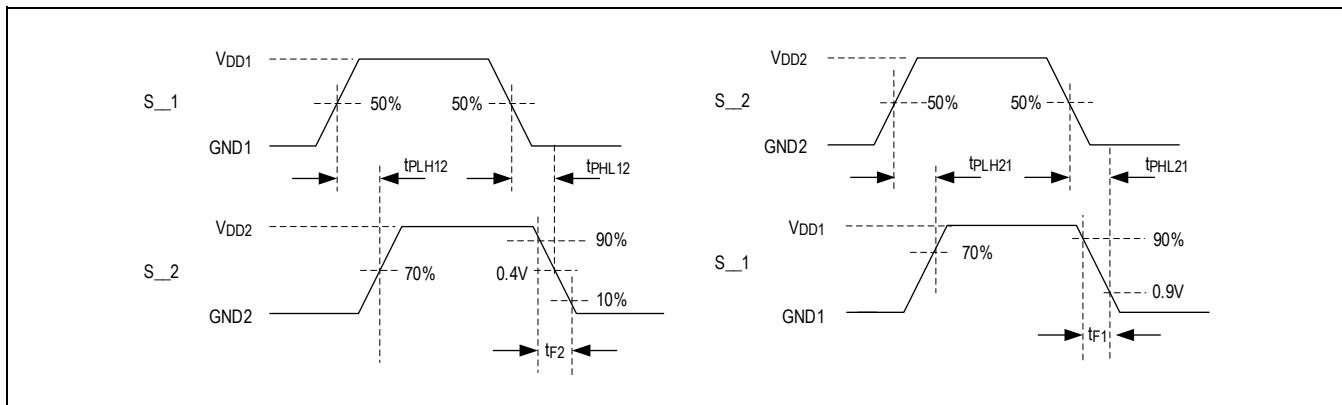


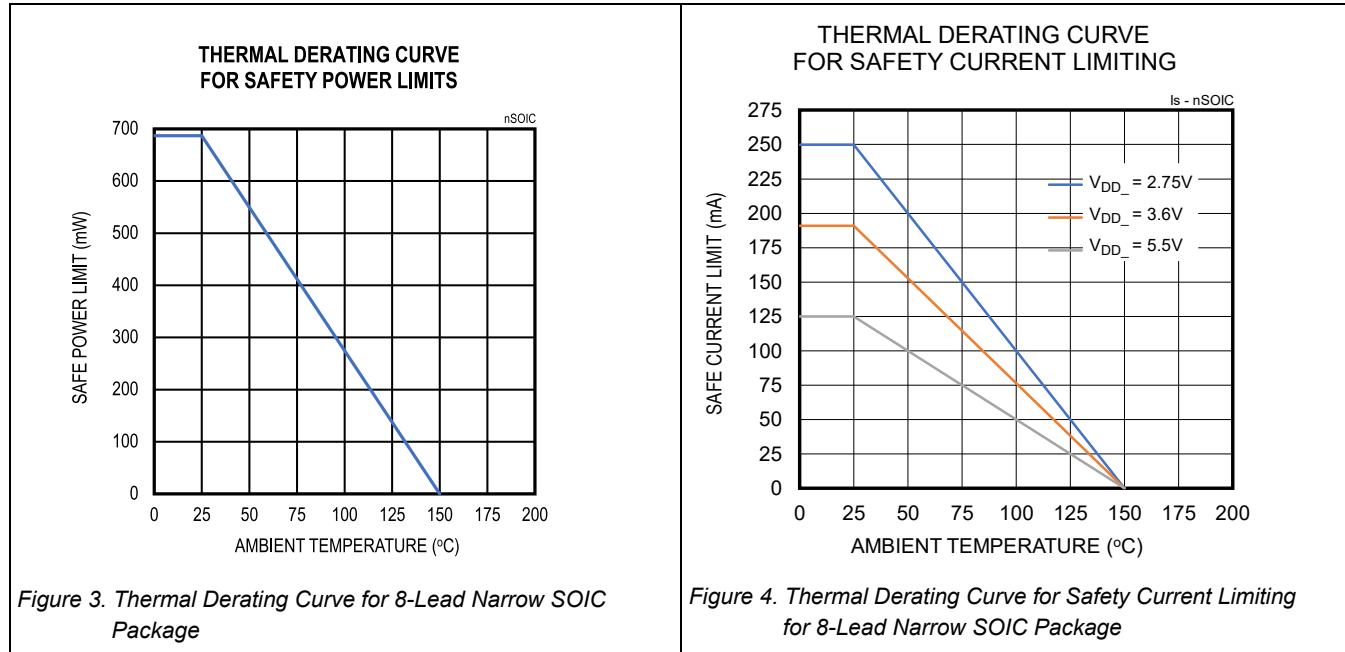
Figure 2. Timing Parameter Definition

## Safety Limits

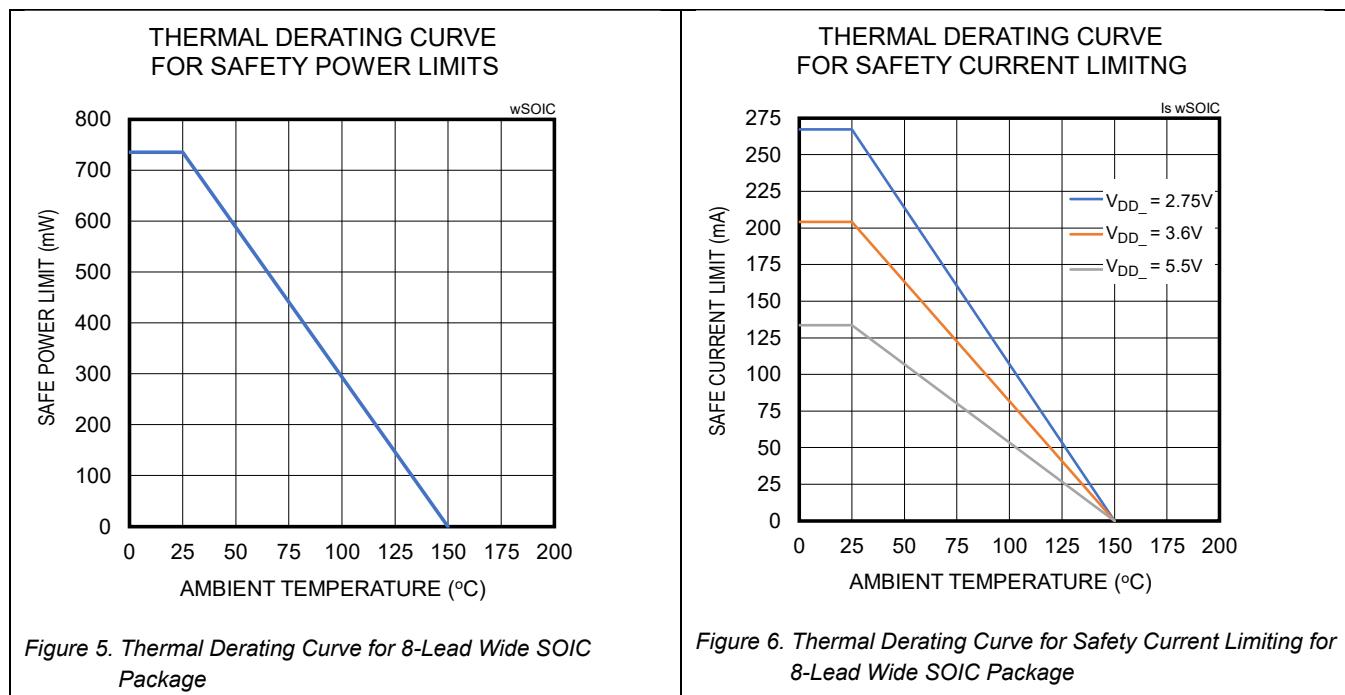
Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the ADuM1255 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. The safety limits for the ADuM1255 are listed in the package specific [Isolation Characteristics](#) table.

The maximum safety temperature ( $T_S$ ) for the device is the  $+150^\circ\text{C}$  maximum junction temperature specified in the [Absolute Maximum Ratings](#). See the [Thermal Considerations](#) section for details on determining the junction temperature.

[Figure 3](#) and [Figure 4](#) show the thermal derating curves for safety limiting the power and the current for the device in the 8-lead Narrow SOIC (21-0041) package when mounted on the JEDEC 2S2P test card. Ensure that the junction temperature does not exceed +150°C.



[Figure 5](#) and [Figure 6](#) show the thermal derating curves for safety limiting the power and the current of the device in the 8-lead Wide SOIC (21-100415) package when mounted on the JEDEC 2S2P test card. Ensure that the junction temperature does not exceed 150°C.



**Isolation Characteristics****8-Lead Narrow SOIC (21-0041) Isolation Characteristics**

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
<b>CLASSIFICATIONS</b>				
Overvoltage Category per IEC60664-1		For rated mains voltage $\leq 150\text{V}_{\text{RMS}}$	I to IV	—
		For rated mains voltage $\leq 300\text{V}_{\text{RMS}}$	I to III	—
Climatic Classification			40/125/21	—
Pollution Degree		Per DIN VDE V 0110 (refer to <a href="#">Table 1</a> of the DIN VDE standard)	2	—
<b>VOLTAGE</b>				
Maximum Working Isolation Voltage	$V_{\text{IOWM}}$	Continuous RMS voltage ( <a href="#">Note 1</a> )	445	$\text{V}_{\text{RMS}}$
Maximum Repetitive Isolation Voltage	$V_{\text{IORM}}$	( <a href="#">Note 1</a> )	630	$\text{V}_{\text{PEAK}}$
Maximum Transient Isolation Voltage	$V_{\text{IOTM}}$	$t = 1\text{s}$ ( <a href="#">Note 1</a> )	4242	$\text{V}_{\text{PEAK}}$
Maximum Withstanding Isolation Voltage	$V_{\text{ISO}}$	$f_{\text{TEST}} = 60\text{Hz}$ , duration = 60s ( <a href="#">Note 1</a> , <a href="#">Note 2</a> )	3000	$\text{V}_{\text{RMS}}$
Maximum Surge Isolation Voltage, Reinforced	$V_{\text{IOSM}}$	Test method per IEC 60065, $V_{\text{TEST}} = 1.6 \times V_{\text{IOSM}} = 10000\text{V}_{\text{PEAK}}$ ( <a href="#">Note 1</a> , <a href="#">Note 4</a> )	6250	$\text{V}_{\text{PEAK}}$
Maximum Impulse Voltage	$V_{\text{IMP}}$	Tested in air, $1.2\mu\text{s}/50\mu\text{s}$ waveform per IEC 62368-1	6000	$\text{V}_{\text{PEAK}}$
Input to Output Test Voltage	$V_{\text{PR}}$		1182	$\text{V}_{\text{PEAK}}$
Apparent Charge	$q_{\text{pd}}$	Method B1, $V_{\text{PR}} = 1.875 \times V_{\text{IORM}}$ ; $t = 1\text{s}$	5	pC
<b>PACKAGE CHARACTERISTICS</b>				
External Clearance	CLR	Measured from input terminals to output terminals, shortest distance through air	4	mm
External Creepage	CPG	Measured from input terminals to output terminals, shortest distance along body	4	mm
Internal Clearance	DTI	Distance through insulation	21	$\mu\text{m}$
Comparative Tracking Index	CTI		> 600	V
Material Group		Material group (IEC 60112)	I	—
Resistance (Input to Output)	$R_{\text{IO}}$	$V_{\text{IO}} = 500\text{V}$ , $T_{\text{A}} = +25^{\circ}\text{C}$ ( <a href="#">Note 3</a> )	$10^{12}$	$\Omega$
	$R_{\text{IO S}}$	$V_{\text{IO}} = 500\text{V}$ , $+100^{\circ}\text{C} \leq T_{\text{A}} \leq +125^{\circ}\text{C}$ ( <a href="#">Note 3</a> )	$10^{11}$	$\Omega$
Capacitance (Input to Output)	$C_{\text{IO}}$	$f_{\text{TEST}} = 1\text{MHz}$ ( <a href="#">Note 3</a> )	1.5	pF
<b>SAFETY LIMITING VALUES</b>				
Maximum Ambient Safety Temperature	$T_{\text{S}}$		150	$^{\circ}\text{C}$
Maximum Input Power Dissipation	$P_{\text{SI}}$	$\theta_{\text{JA}} = 182^{\circ}\text{C/W}$ , $T_{\text{J}} = +150^{\circ}\text{C}$ , $T_{\text{A}} = +25^{\circ}\text{C}$	687	mW
Maximum Output Current	$I_{\text{SO}}$	$\theta_{\text{JA}} = 182^{\circ}\text{C/W}$ , $T_{\text{J}} = +150^{\circ}\text{C}$ , $T_{\text{A}} = +25^{\circ}\text{C}$ , $V_{\text{DD}} = 5.5\text{V}$	124	mA
		$\theta_{\text{JA}} = 182^{\circ}\text{C/W}$ , $T_{\text{J}} = +150^{\circ}\text{C}$ , $T_{\text{A}} = +25^{\circ}\text{C}$ , $V_{\text{DD}} = 3.6\text{V}$	190	mA
		$\theta_{\text{JA}} = 182^{\circ}\text{C/W}$ , $T_{\text{J}} = +150^{\circ}\text{C}$ , $T_{\text{A}} = +25^{\circ}\text{C}$ , $V_{\text{DD}} = 2.75\text{V}$	249	mA

Note 1:  $V_{\text{ISO}}$ ,  $V_{\text{IOTM}}$ ,  $V_{\text{IOWM}}$ ,  $V_{\text{IORM}}$  and  $V_{\text{IOSM}}$  are defined by the IEC 60747-17 standard.

Note 2: Product is qualified at  $V_{\text{ISO}}$  for 60s and 100% production tested at 120% of  $V_{\text{ISO}}$  for 1s.

Note 3: Device is measured as a 2-terminal device with Pin 1 through Pin 4 connected and Pin 5 through Pin 8 connected.

Note 4: Devices are immersed in oil during surge characterization.

## 8-Lead Wide SOIC (21-100415) Isolation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
<b>CLASSIFICATIONS</b>				
Overvoltage Category per IEC60664-1		For rated mains voltage $\leq 150 \text{ V}_{\text{RMS}}$	I to IV	—
		For rated mains voltage $\leq 300 \text{ V}_{\text{RMS}}$	I to IV	—
		For rated mains voltage $\leq 600 \text{ V}_{\text{RMS}}$	I to IV	—
Climatic Classification			40/125/21	—
Pollution Degree		Per DIN VDE V 0110 (refer to <a href="#">Table 1</a> of the DIN VDE standard)	2	—
<b>VOLTAGE</b>				
Maximum Working Isolation Voltage	$V_{\text{IOWM}}$	Continuous RMS voltage ( <a href="#">Note 1</a> )	848	$\text{V}_{\text{RMS}}$
Maximum Repetitive Isolation Voltage	$V_{\text{IORM}}$	( <a href="#">Note 1</a> )	1200	$\text{V}_{\text{PEAK}}$
Maximum Transient Isolation Voltage	$V_{\text{IOTM}}$	$t = 1\text{s}$ ( <a href="#">Note 1</a> )	7070	$\text{V}_{\text{PEAK}}$
Maximum Withstanding Isolation Voltage	$V_{\text{ISO}}$	$f_{\text{TEST}} = 60\text{Hz}$ , duration = 60s ( <a href="#">Note 1</a> , <a href="#">Note 2</a> )	5000	$\text{V}_{\text{RMS}}$
Maximum Surge Isolation Voltage, Reinforced	$V_{\text{IOSM}}$	Test method per IEC 60065, $V_{\text{TEST}} = 1.6 \times V_{\text{IOSM}} = 10000\text{V}_{\text{PEAK}}$ ( <a href="#">Note 1</a> , <a href="#">Note 4</a> )	6250	$\text{V}_{\text{PEAK}}$
Maximum Impulse Voltage	$V_{\text{IMP}}$	Tested in air, $1.2\mu\text{s}/50\mu\text{s}$ waveform per IEC 62368-1	8000	$\text{V}_{\text{PEAK}}$
Input to Output Test Voltage	$V_{\text{PR}}$		2250	$\text{V}_{\text{PEAK}}$
Apparent Charge	$q_{\text{pd}}$	Method B1, $V_{\text{PR}} = 1.875 \times V_{\text{IORM}}$ , $t = 1\text{s}$	5	pC
<b>PACKAGE CHARACTERISTICS</b>				
External Clearance	CLR	Measured from input terminals to output terminals, shortest distance through air	8	mm
External Creepage	CPG	Measured from input terminals to output terminals, shortest distance along body	8	mm
Internal Clearance	DTI	Distance through insulation	21	$\mu\text{m}$
Comparative Tracking Index	CTI		> 600	V
Material Group		Material group (IEC 60112)	I	—
Resistance (Input to Output)	$R_{\text{IO}}$	$V_{\text{IO}} = 500\text{V}$ , $T_A = +25^\circ\text{C}$ ( <a href="#">Note 3</a> )	1012	$\Omega$
	$R_{\text{IO\_S}}$	$V_{\text{IO}} = 500\text{V}$ , $+100^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ( <a href="#">Note 3</a> )	1011	$\Omega$
Capacitance (Input to Output)	$C_{\text{IO}}$	$f_{\text{TEST}} = 1\text{MHz}$ ( <a href="#">Note 3</a> )	1.5	pF
<b>SAFETY LIMITING VALUES</b>				
Maximum Ambient Safety Temperature	$T_S$		150	$^\circ\text{C}$
Maximum Input Power Dissipation	$P_{\text{SI}}$	$\theta_{JA} = 170^\circ\text{C/W}$ , $T_J = +150^\circ\text{C}$ , $T_A = +25^\circ\text{C}$	735	mW
Maximum Output Current	$I_{\text{SO}}$	$\theta_{JA} = 170^\circ\text{C/W}$ , $T_J = +150^\circ\text{C}$ , $T_A = +25^\circ\text{C}$ , $V_{\text{DD}} = 5.5\text{V}$	133	mA
		$\theta_{JA} = 170^\circ\text{C/W}$ , $T_J = +150^\circ\text{C}$ , $T_A = +25^\circ\text{C}$ , $V_{\text{DD}} = 3.6\text{V}$	204	mA
		$\theta_{JA} = 170^\circ\text{C/W}$ , $T_J = +150^\circ\text{C}$ , $T_A = +25^\circ\text{C}$ , $V_{\text{DD}} = 2.75\text{V}$	267	mA

**Note 1:**  $V_{\text{ISO}}$ ,  $V_{\text{IOTM}}$ ,  $V_{\text{IOWM}}$ ,  $V_{\text{IORM}}$  and  $V_{\text{IOSM}}$  are defined by the IEC 60747-17 standard.

**Note 2:** Product is qualified at  $V_{\text{ISO}}$  for 60s and 100% production tested at 120% of  $V_{\text{ISO}}$  for 1s.

**Note 3:** Device is measured as a 2-terminal device with Pin 1 through Pin 4 connected and Pin 5 through Pin 8 connected.

**Note 4:** Devices are immersed in oil during surge characterization.

## Regulatory Information

The ADuM1255 has been approved by the organizations listed below. Certifications are available at [Safety and Regulatory Certifications for Digital Isolation](#).

### 8-Lead Narrow SOIC (21-0041) Package Certifications

REGULATORY AGENCY	STANDARD CERTIFICATION/APPROVAL	FILE
UL	UL 1577 component recognition program ( <a href="#">Note 1</a> ): Single/basic 3000VRMS isolation voltage.	(Pending)
CSA	CSA No 14-18 ( <a href="#">Note 2</a> and <a href="#">Note 3</a> ): CSA 62368-1:19, IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 400VRMS. CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed.: Basic insulation at 300VRMS from mains, 400VRMS from secondary circuit.	(Pending)
VDE	IEC 60747-17 ( <a href="#">Note 4</a> ): Reinforced insulation, maximum transient isolation voltage 4242V <sub>PK</sub> , maximum repetitive peak isolation voltage 630V <sub>PK</sub> .	(Pending)
CQC	GB 4943.1-2022: Basic insulation at 400VRMS (565V <sub>PEAK</sub> ) maximum working voltage, tropical climate, altitude < 5000m	(Pending)
TUV Sud	IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 400VRMS	(Pending)

**Note 1:** In accordance with UL 1577, each ADuM1255ASA+ is proof tested by applying an insulation test voltage  $\geq 3600\text{VRMS}$  for 1 second (current leakage detection limit =  $5\mu\text{A}$ ).

**Note 2:** Working voltages are quoted for material group III case material in pollution degree 2. ADuM1255ASA+ case material has been evaluated by CSA as material group I.

**Note 3:** The creepage and clearance distances have been evaluated for altitudes < 2000m, material group III, in pollution degree 2 and overvoltage category II, except where specified above.

**Note 4:** In accordance with IEC 60747-17, each ADuM1255 is proof tested by applying an insulation test voltage  $\geq 1182\text{V}$  peak for 1s (partial discharge detection limit = 5 pC). This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 8-Lead Wide SOIC (21-00415) Package Certifications

REGULATORY AGENCY	STANDARD CERTIFICATION/APPROVAL	FILE
UL	UL 1577 component recognition program ( <a href="#">Note 1</a> ): Single/basic 5000VRMS isolation voltage.	(Pending)
CSA	CSA No 14-18 ( <a href="#">Note 2</a> and <a href="#">Note 3</a> ): CSA 62368-1:19, IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 800VRMS. CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed.: Basic insulation at 600VRMS from mains, 800VRMS from secondary circuit	(Pending)

VDE	IEC 60747-17 ( <a href="#">Note 4</a> ): Reinforced insulation, maximum transient isolation voltage 7070V <sub>PK</sub> , maximum repetitive peak isolation voltage 1200V <sub>PK</sub> .	(Pending)
CQC	GB 4943.1-2022: Basic insulation at 800V <sub>RMS</sub> (1131V <sub>PEAK</sub> ) maximum working voltage, tropical climate, altitude < 5000m	(Pending)
TUV Sud	IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 800V <sub>RMS</sub>	(Pending)

**Note 1:** In accordance with UL 1577, each ADuM1255AWA+ is proof tested by applying an insulation test voltage  $\geq 6000\text{V}_{\text{RMS}}$  for 1 second (current leakage detection limit =  $5\mu\text{A}$ ).

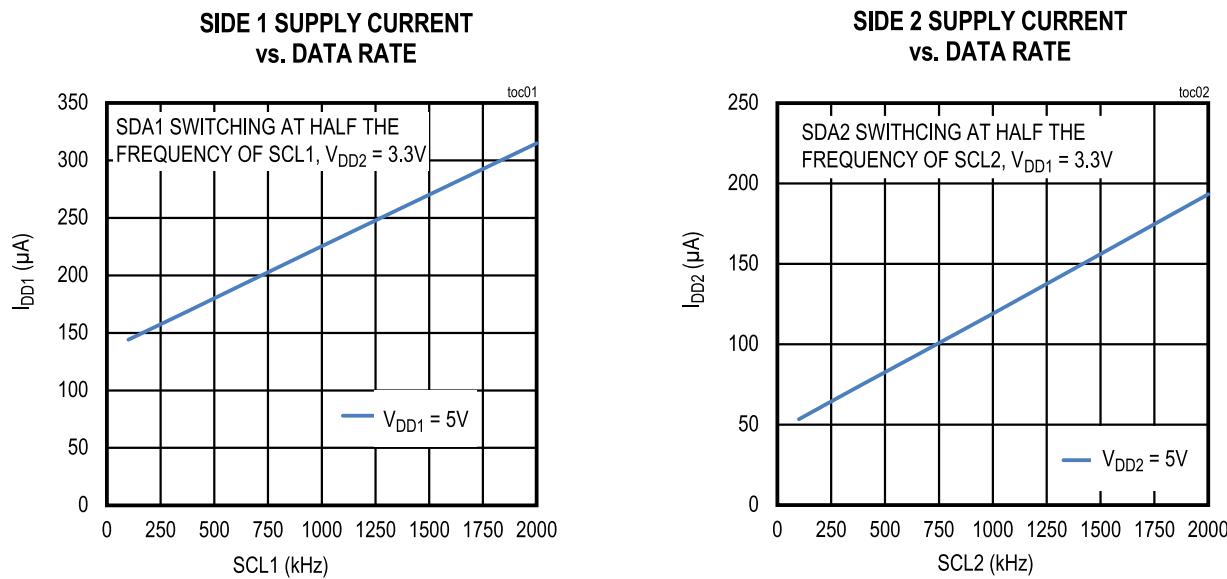
**Note 2:** Working voltages are quoted for material group III case material in pollution degree 2. ADuM1255AWA+ case material has been evaluated by CSA as material group I.

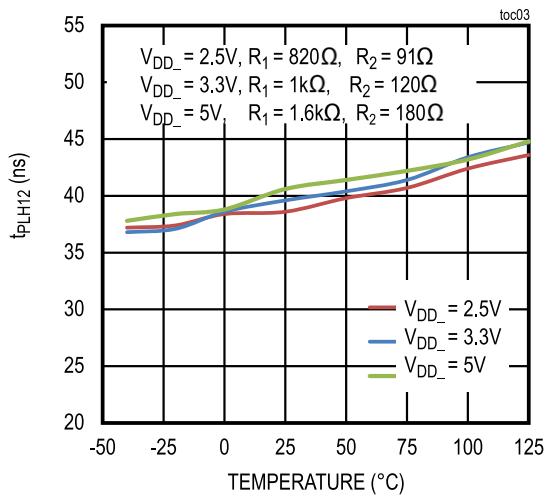
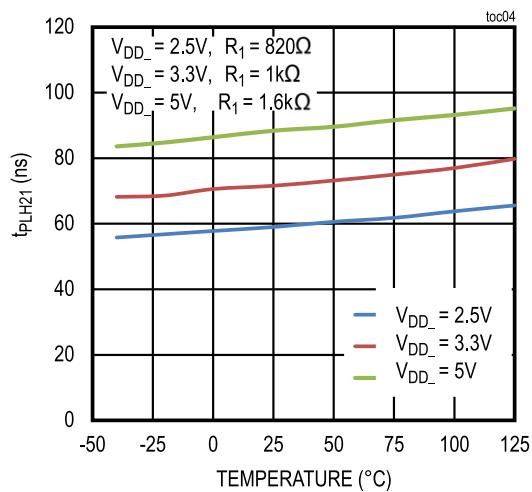
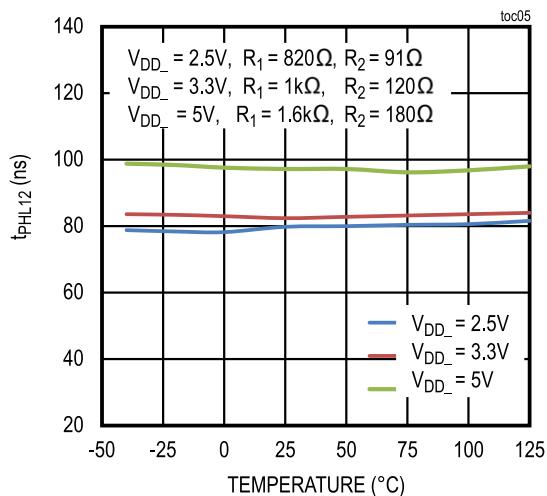
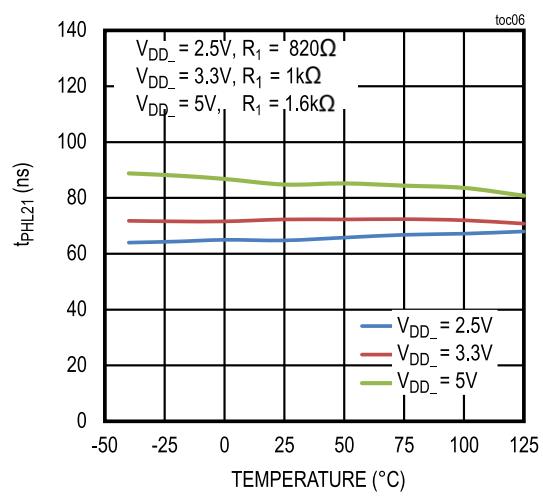
**Note 3:** The creepage and clearance distances have been evaluated for altitudes < 2000m, material group III, in pollution degree 2 and overvoltage category II, except where specified above.

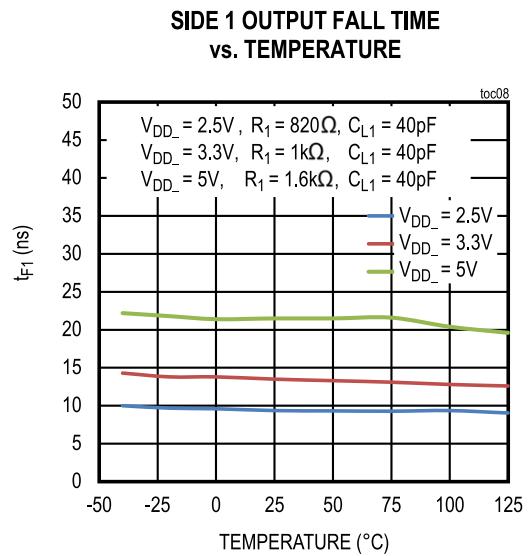
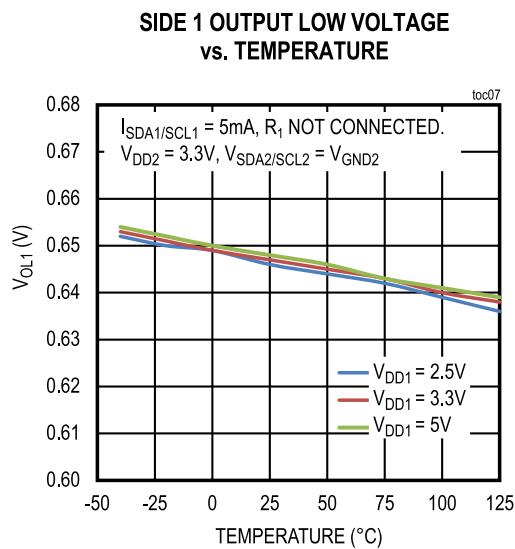
**Note 4:** In accordance with IEC 60747-17, each ADuM1255 is proof tested by applying an insulation test voltage  $\geq 2250\text{V}$  peak for 1s (partial discharge detection limit =  $5\text{ pC}$ ). This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

## Typical Operating Characteristics

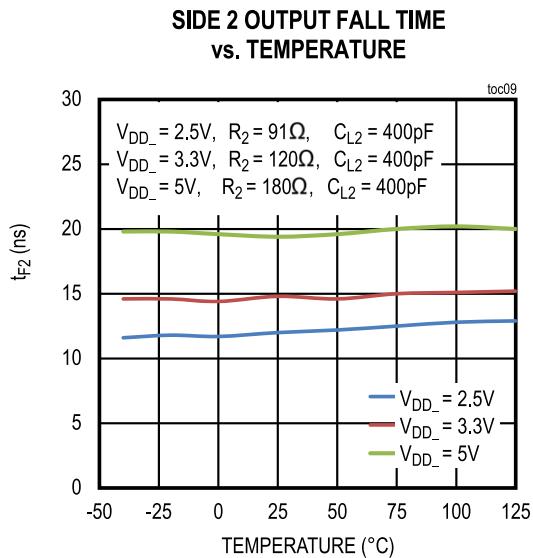
(Typical values are at  $V_{\text{DD1}} = V_{\text{DD2}} = 3.3\text{V}$ ,  $\text{GND1} = \text{GND2}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.  $C_L = 20\text{pF}$ ,  $R_{\text{PULLUP}} = 1\text{k}\Omega$  and  $1\text{nF}$ ,  $100\text{nF}$ , and  $1\mu\text{F}$  decoupling capacitors are on  $V_{\text{DD1}}$  and  $V_{\text{DD2}}$ . All tests were performed using the ADuM1252SEVKIT#.)



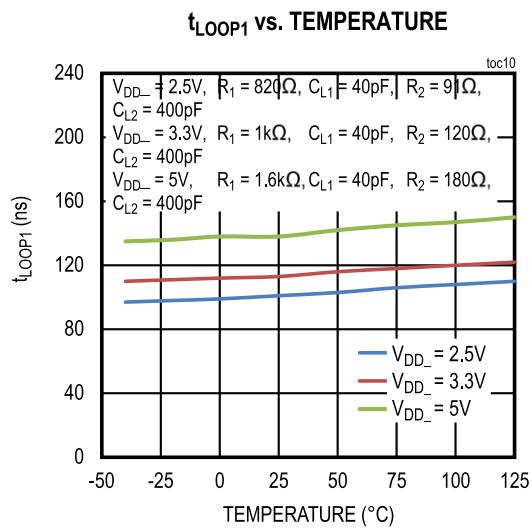
PROPAGATION DELAY  $t_{PLH12}$  vs. TEMPERATUREPROPAGATION DELAY  $t_{PLH21}$  vs. TEMPERATUREPROPAGATION DELAY  $t_{PHL12}$  vs. TEMPERATUREPROPAGATION DELAY  $t_{PHL21}$  vs. TEMPERATURE



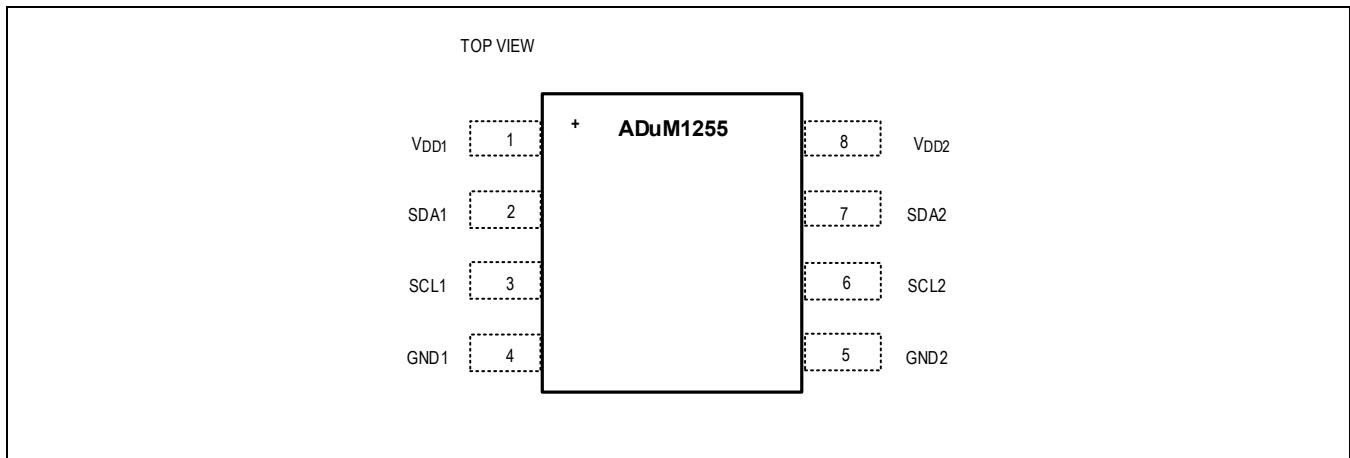
$t_F1$  MEASURED FROM  $0.7V_{DD1}$  TO  $0.3V_{DD1}$



$t_F2$  MEASURED FROM  $0.7V_{DD2}$  TO  $0.3V_{DD2}$



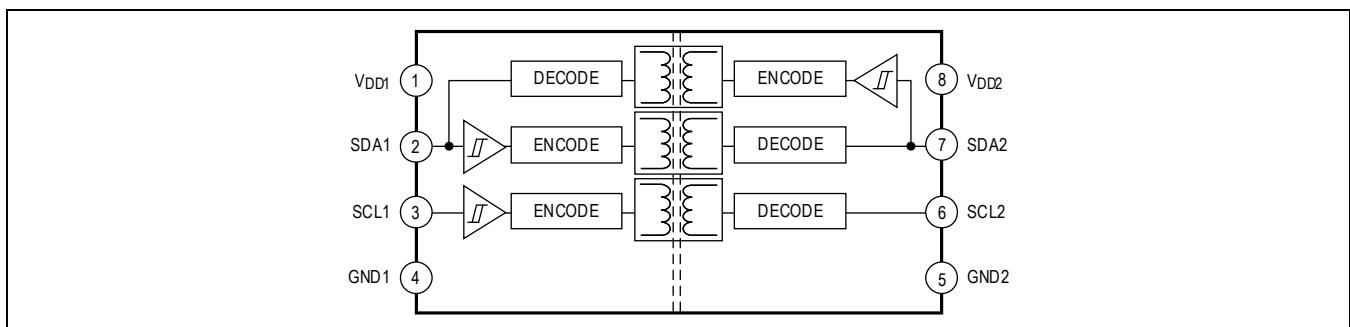
## Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
1	V <sub>DD1</sub>	Supply Voltage Side 1. Bypass V <sub>DD1</sub> with a 1nF and a 0.1μF ceramic capacitor as close as possible to the pin.
2	SDA1	Serial Data Input/Output on Side 1. SDA1 is translated to/from SDA2 and is an open-drain output.
3	SCL1	Serial Clock Input on Side 1. SCL1 is translated to SCL2 and is an input.
4	GND1	Ground Reference for Side 1
5	GND2	Ground Reference for Side 2
6	SCL2	Serial Clock Output on Side 2. SCL2 is translated from SCL1 and is an open-drain output.
7	SDA2	Serial Data Input/Output on Side 2. SDA2 is translated to/from SDA1 and is an open-drain output.
8	V <sub>DD2</sub>	Supply Voltage Side 2. Bypass V <sub>DD2</sub> with a 1nF and a 0.1μF ceramic capacitor as close as possible to the pin.

## Functional Diagram



## Detailed Description

The ADuM1255 is a two-channel I<sup>2</sup>C isolator utilizing Analog Devices, Inc. proprietary process technology. The device transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two open-drain channels, one bidirectional for data and one unidirectional for clock and is suitable for I2C applications where only a single clock direction across the isolation barrier is required. Example applications include I2C bus topologies where all I2C controllers are located on one side of the isolation barrier and/or where clock stretching is not used by devices on the non-controller side of the isolation barrier.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates with SCL frequencies up to 2MHz. The wide temperature range and high isolation voltage make the device ideal for use in harsh industrial environments.

### Digital Isolation

The ADuM1255 provides reinforced galvanic isolation for digital signals that are transmitted between two ground domains.

In the 8-pin narrow SOIC package (21-0041), the ADuM1255 withstands voltage differences of up to 3kVRMS for up to 60 seconds and up to 630VPEAK of continuous isolation.

In the 8-pin wide SOIC package (21-100415), the ADuM1255 withstands voltage differences of up to 5kVRMS for up to 60 seconds and up to 1200VPEAK of continuous isolation.

### Bidirectional Channels

The ADuM1255 device features one bidirectional channel which has open-drain outputs.

The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device due to the coordination of the side 1 output logic-low voltage ( $V_{OL1}$ ) and input logic-low threshold ( $V_{IL1}$ ). The side 1 outputs utilize special buffers that regulate  $V_{OL1}$  to approximately 0.64V while keeping  $V_{IL1}$  at least 50mV lower than  $V_{OL1}$ . This difference prevents an output logic-low on side 1 from being accepted as an input low and subsequently transmitted to side 2, thus, preventing a latching action. SDA2 and SCL2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their special nature, the side 1 SDA/SCL pins of different ADuM1255 devices cannot be connected together. This restriction also includes pins on other devices which employ similar buffers or rise-time accelerators. The side 2 pins do not have this restriction. Therefore, the side 2 pins of the ADuM1255 can be connected to each other or to any other bidirectional buffer or level translator's pin, including the side 1 pins of the ADuM1255.

The ADuM1255's outputs are all open-drain and require pull-up resistors to their respective supplies to generate the logic-high output voltage. The output low voltages are guaranteed for sink currents of up to 50mA for side 2 and 5mA for side 1 (see the [Electrical Characteristics](#) table).

### Startup and Undervoltage Lockout

The  $V_{DD1}$  and  $V_{DD2}$  supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs as seen in [Table 1](#).

**Table 1. Output Behavior During Undervoltage Condition**

$V_{DD1}$	$V_{DD2}$	INPUT	$V_{OUT1}$	$V_{OUT2}$
Powered	Powered	High	High-Z	High-Z
Powered	Powered	Low	Low	Low
Undervoltage	Powered	Don't care	High-Z	High-Z
Powered	Undervoltage	Don't care	High-Z	High-Z

### Level Shifting

The wide supply voltage range of both  $V_{DD1}$  and  $V_{DD2}$  allows the ADuM1255 to be used for level translation in addition to isolation.  $V_{DD1}$  and  $V_{DD2}$  can be independently set to any voltage from 2.25V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

## Hot Swap

The ADuM1255 includes special precharge circuitry on SDA2/SCL2 to prevent loading on the I<sup>2</sup>C bus lines while the supply is either unpowered or in the process of being powered on. When the supply is below the UVLO threshold, the ADuM1255 bus lines do not load the bus to avoid disrupting or corrupting an active I<sup>2</sup>C bus. If the isolator is plugged into a live backplane using a staggered connector, where the supply and ground make connection first followed by the bus lines, the SDA2 and SCL2 lines are precharged to  $V_{DD2}/3$  to minimize the current required to charge the parasitic capacitance of the device. Once the device is fully powered on, the device I/O pins become active. However, the connection between side 1 and side 2 does not occur until after the side 2 bus either detects an I<sup>2</sup>C stop condition or the bus has been idle for 125 $\mu$ s. See [Figure 7](#).

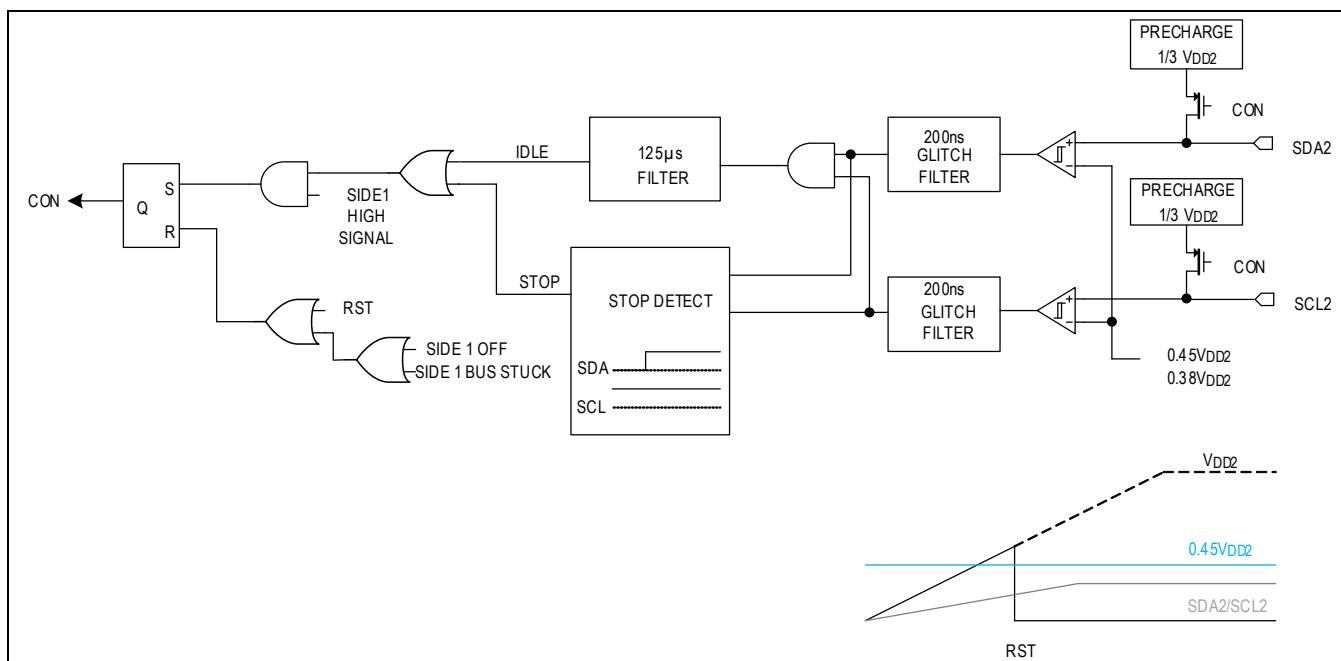


Figure 7. Bus Connection Logic

## Bus Connection

The ADuM1255 connects the side 1 bus to the side 2 bus when both busses are idle or when side 1 is high and an I<sup>2</sup>C stop condition has been detected on side 2. If a stuck bus condition is detected on side 1, then the ADuM1255 disconnects the two busses to allow the external system to attempt a recovery.

## Applications Information

### Power-Supply Sequencing

The ADuM1255 does not require special power-supply sequencing. The logic levels are set independently on either side by  $V_{DD1}$  and  $V_{DD2}$ . Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

### Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors especially if large common-mode transients are expected in the application, bypass  $V_{DD1}$  and  $V_{DD2}$  with 100nF and 1nF low-ESR ceramic capacitors to GND1 and GND2, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

### Thermal Considerations

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to the PCB thermal design.

Thermal parameter values are specified in the [Package Information](#) section.  $\theta_{JA}$  and  $\theta_{JB}$  are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar.  $\Psi_{JB}$  or  $\Psi_{JT}$  can be used to estimate the junction temperature when an accurate thermal measurement of the board temperature is available. The temperature measurement must be near the device under test (DUT) or directly on the package top surface, operating in the system environment.

$\theta_{JA}$  can be used for a first-order approximation to calculate the junction temperature in the system environment. The power dissipation ( $P_D$ ), junction-to-ambient thermal impedance ( $\theta_{JA}$ ), and ambient temperature ( $T_A$ ) determine the junction temperature ( $T_J$ ) according to the expression:

$$T_J = T_A + (P_D \times \theta_{JA})$$

A more accurate estimate of the junction temperature can be found using  $\Psi_{JT}$ . Measure the device package temperature ( $T_{PACKAGE}$ ) in the center of the package using an IR camera or thermocouple and then use the following expression:

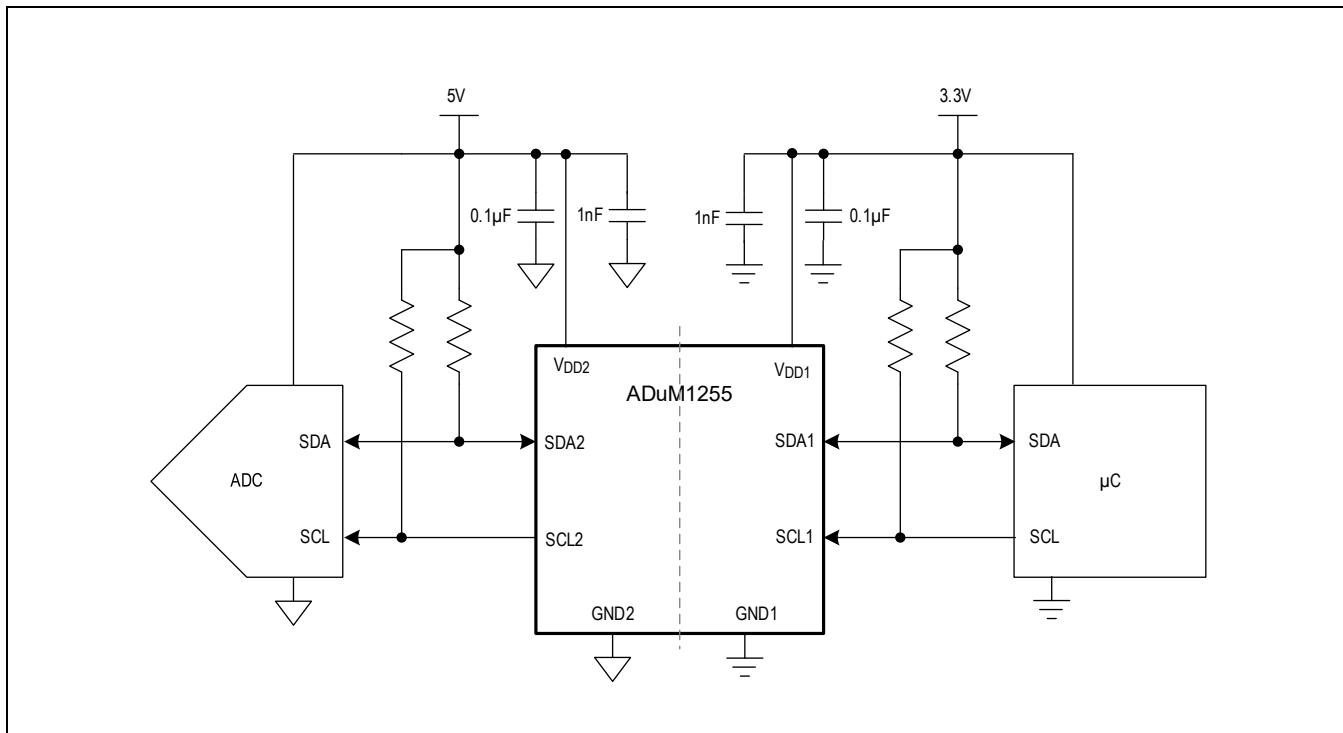
$$T_J = T_{PACKAGE} + \Psi_{JT} \times P_D$$

## Layout Considerations

The PCB designer should follow some critical recommendations to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the ADuM1255 free from ground and signal planes. Any galvanic or metallic connection between side 1 and side 2 defeats the isolation.

## Typical Application Circuit



## Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
ADuM1255ASA+	-40°C to +125°C	8 Narrow SOIC
ADuM1255ASA+T	-40°C to +125°C	8 Narrow SOIC
ADuM1255AWA+	-40°C to +125°C	8 Wide SOIC
ADuM1255AWA+T	-40°C to +125°C	8 Wide SOIC

+ Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

## Chip Information

PROCESS: BiCMOS

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Initial release	—
1	5/24	Addition of Wide SOIC package. Change Narrow SOIC safety limit current VDD from 5.6V to 5.5V. Move ESD characteristics to Electrical Characteristics table. Clarified which parameters are guaranteed by design. Removed statement that asterisk (*) marking branded on the component designates DIN IEC60747-17 approval and added statement on safe electrical isolation to Package Certifications table Note 4.	1-13, 17, 20



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