High Power, 40 W Peak, Silicon SPDT, Reflective Switch, 8 GHz to 11 GHz

FEATURES

- Frequency range: 8 GHz to 11 GHz
- Low insertion loss: 1.2 dB (typical)
- High isolation: 40 dB (typical)
- High input linearity
  - 0.1 dB power compression (P0.1dB): 46 dBm
  - Third-order intercept (IP3): 70 dBm
- High power handling at T_{CASE} = 85°C:
  - Insertion loss path
    - Average: 41 dBm
    - Pulsed (> 100 ns pulse width, 15% duty cycle): 44 dBm
    - Peak (≤ 100 ns peak duration, 5% duty cycle): 46 dBm
  - Hot switching at RFC (Pin 3): 41 dBm
- Fast switching time: 60 ns
- 0.1 dB RF settling time: 65 ns
- No low frequency spurious
- Positive control interface: CMOS-/LVTTL-compatible
- 20-lead, 3.0 mm × 3.0 mm LGA package
- Pin compatible with ADRF5141 and ADRF5144

APPLICATIONS

- X-band communications and radars
- Electronic warfare
- Satellite communications
- Gallium nitride (GaN) and PIN diode replacement

FUNCTIONAL BLOCK DIAGRAM

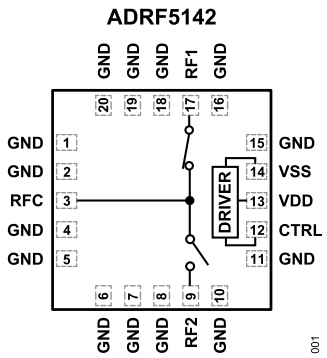

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5142 is a reflective single-pole, double-throw (SPDT) switch manufactured in the silicon process.

The ADRF5142 operates from 8 GHz to 11 GHz with a 1.2 dB typical insertion loss and a 40 dB typical isolation. The device has a radio frequency (RF) input power handling capability of 41 dBm average power and 46 dBm peak power for the insertion loss path.

The ADRF5142 draws a low current of 130 µA on the positive supply of +3.3 V and 500 µA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low-voltage transistor to transistor logic (LVTTL)-compatible controls. The ADRF5142 requires no additional driver circuitry, which makes it an ideal alternative to GaN and PIN diode-based switches.

The ADRF5142 comes in a 20-lead, 3.0 mm × 3.0 mm, RoHS-compliant, land grid array (LGA) package and operates from −40°C to +85°C.

TABLE OF CONTENTS

REVISION HISTORY

4/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		8		11	GHz
INSERTION LOSS						
Between RFC and RF1/RF2 (ON)		8 GHz to 11 GHz		1.2		dB
RETURN LOSS						
RFC and RF1/RF2 (ON)		8 GHz to 11 GHz		20		dB
ISOLATION						
Between RFC and RF1/RF2 (OFF)		8 GHz to 11 GHz		40		dB
Between RF1 and RF2		8 GHz to 11 GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		40		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		60		ns
RF Settling Time						
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		65		ns
INPUT LINEARITY		f = 8 GHz to 11 GHz				
0.1 dB Power Compression	P0.1dB			46		dBm
Input Third-Order Intercept	IIP3	Two tone input power = 26 dBm each tone, Δf = 1 MHz		70		dBm
SUPPLY CURRENT		V_{DD}, V_{SS} pins				
Positive Supply Current	I_{DD}			130		µA
Negative Supply Current	I_{SS}			500		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<0.1		µA
RECOMMENDED OPERATING CONDITONS						
Positive Supply Voltage	V_{DD}		3.15		3.45	V
Negative Supply Voltage	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[1]	P_{IN}	f = 8 GHz to 11GHz, T_{CASE} = 85°C				
Insertion Loss Path		RF signal applied to the RFC or through connected RF1/RF2				
Average					41	dBm
Pulsed[2]		> 100 ns pulse width, 15% duty cycle			44	dBm
Peak		≤ 100 ns peak duration, 5% duty cycle			46	dBm
Hot Switching						
Input at RFC					41	dBm
Input at RFx					27	dBm
Case Temperature	T_{CASE}		−40		+85	°C

[1] For power derating over frequency, see Figure 2.

[2] For different pulsed conditions, contact Applications Support.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[1] (f = 8 GHz to 11 GHz, T_{CASE} = 85°C)	
Insertion Loss Path	
Average	41.5 dBm
Pulsed	44.5 dBm
Peak	46.5 dBm
Hot Switching	
Input at RFC	41.5 dBm
Input at RFx	27.5 dBm
RF Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	
Input at RFC or RFx	
Average	38 dBm
Pulsed	38 dBm
Peak	38 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating over frequency, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at a time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to the case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-9	18.5	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

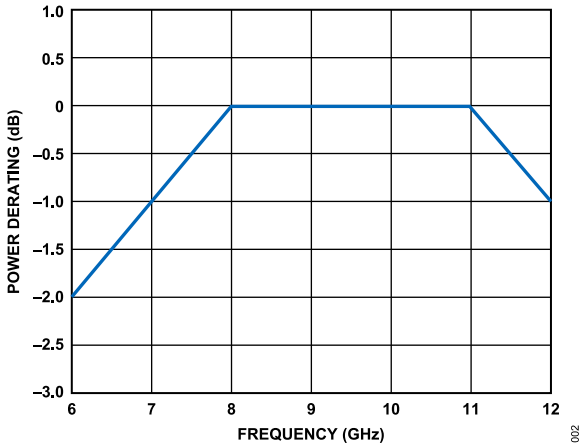

Figure 2. Power Derating vs. Frequency, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5142

Table 4. ADRF5142, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±2000 for all pins	2
CDM	±500 for all pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

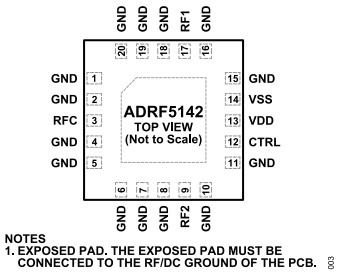

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 8, 10, 11, 15, 16, 18 to 20	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
3	RFC	RF Common Port. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
9	RF2	RF Throw Port 2. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
12	CTRL	Control Input. For the truth table, see Table 6.
13	VDD	Positive Supply Voltage.
14	VSS	Negative Supply Voltage.
17	RF1	RF Throw Port 1. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

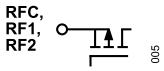

Figure 4. RF Pins (RFC, RF1, and RF2) Interface Schematic

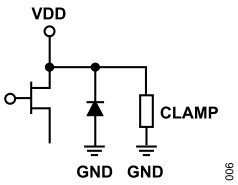

Figure 5. VDD Pin Interface Schematic

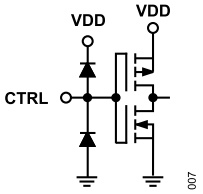

Figure 6. Digital Pin (CTRL) Interface Schematic

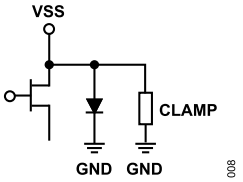

Figure 7. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD} V, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. Measured on the ADRF5142-EVALZ.

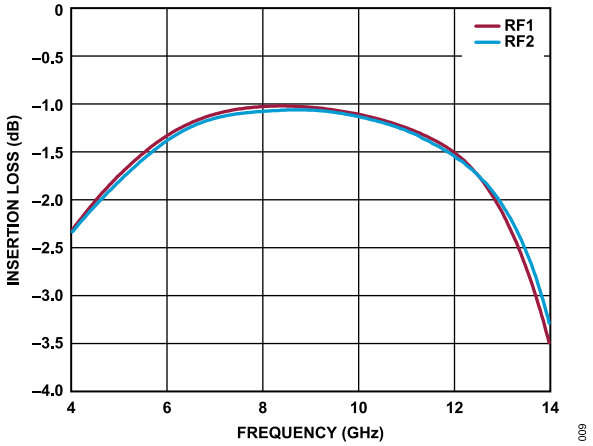

Figure 8. Insertion Loss vs. Frequency at Room Temperature for RF1 and RF2

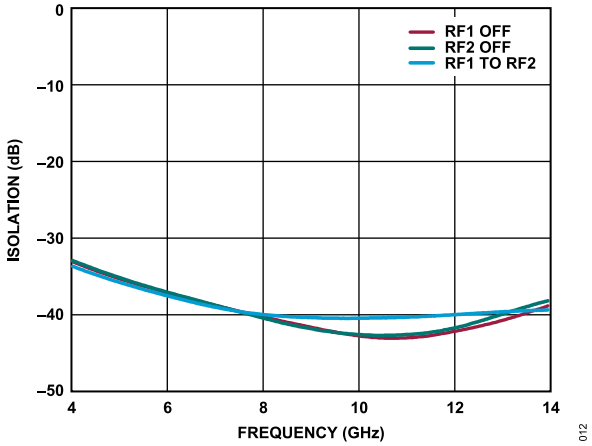

Figure 11. Isolation vs. Frequency

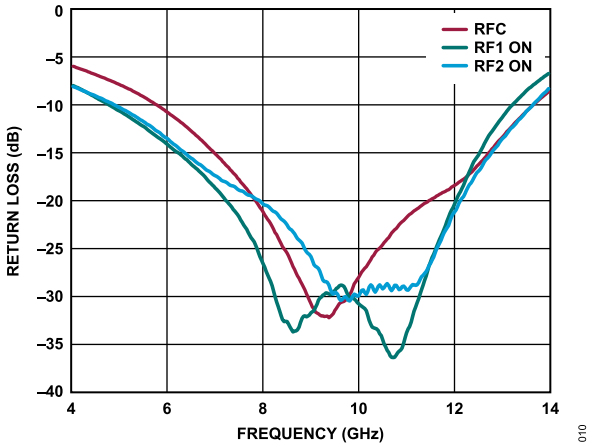

Figure 9. Return Loss vs. Frequency

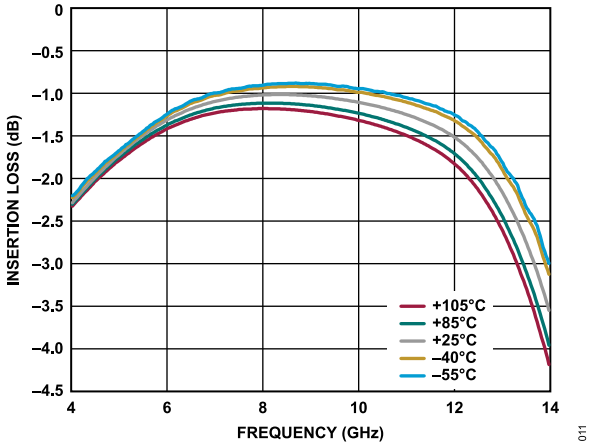

Figure 10. Insertion Loss vs. Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD} V, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. The large-signal performance parameter is measured on the ADRF5142-EVALZ.

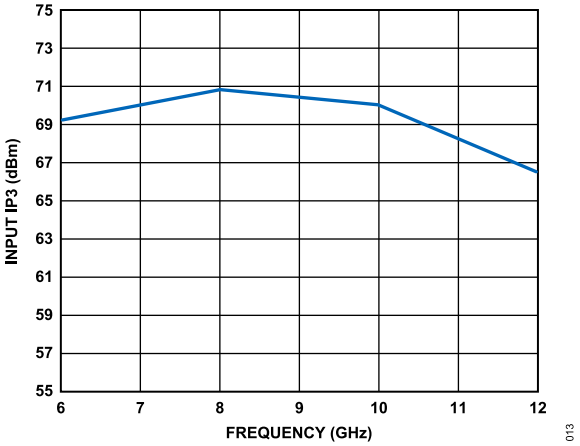

Figure 12. Input IP3 vs. Frequency

THEORY OF OPERATION

The ADRF5142 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features a single control input pin, CTRL, that controls the state of RF paths to determine which RF port is in an insertion loss state or in an isolation state (see Table 6).

POWER SUPPLY

The ADRF5142 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect the ground.
2. Power up V_{DD} and V_{SS}. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control inputs. Power the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after V_{DD} is powered up, and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.
5. The ideal power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port. The unselected RF port of the ADRF5142 is reflective.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

Table 6. Control Voltage Truth Table

	RF Paths	
Digital Control Input, V_{CTRL}	**RF1 to RFC**	**RF2 to RFC**
Low	Insertion loss (on)	Isolation (off)
High	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

The ADRF5142 has two power supply pins (VDD and VSS) and one control pin (CTRL). Figure 13 shows the external components and connections for the supply and control pins. The VDD pin is decoupled with 100 pF and 100 nF multilayer ceramic capacitors. The VSS and control pins are decoupled with 100 pF multilayer ceramic capacitors. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC-blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Pin Configuration and Function Descriptions section.

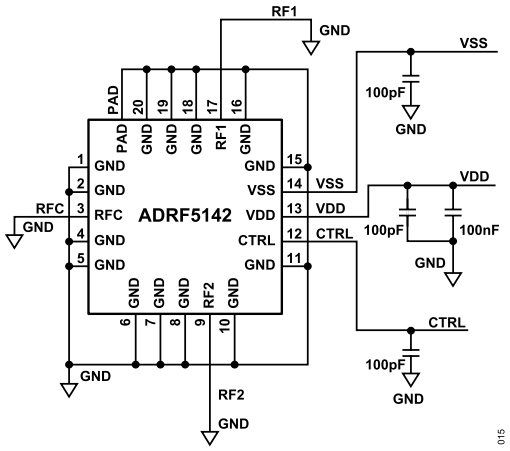

Figure 13. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. Figure 14 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. An RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

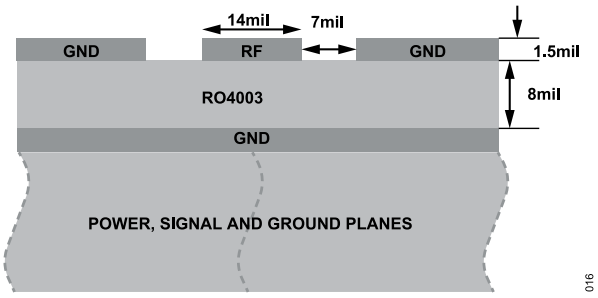

Figure 14. Example PCB Stack Up

Figure 15 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled as allowed through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side, and therefore, a heatsink is required under the PCB to ensure maximum heat dissipation and to reduce thermal rise on the PCB during high-power applications.

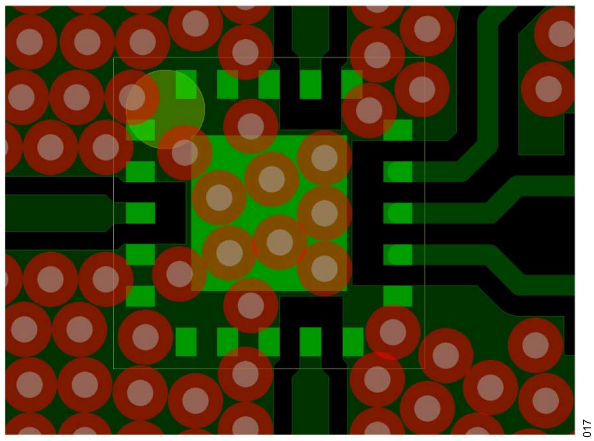

Figure 15. PCB Routings

Figure 16 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn as soldermask defined. The signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width up to the package edge and tapered to an RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

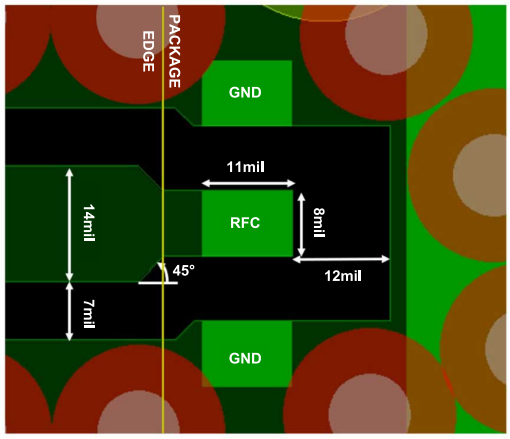

Figure 16. Recommended RF Pin Transitions

For further recommendations and alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-20-9	LGA	20-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Quantity	Package Option
ADRF5142BCCZN	−40°C to +85°C	20-Terminal Land Grid Array [LGA]	Reel, 500	CC-20-9
ADRF5142BCCZN-R7	−40°C to +85°C	20-Terminal Land Grid Array [LGA]	Reel, 500	CC-20-9

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADRF5142-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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