Data Sheet

ADRF5023

Silicon SPDT Switch, Nonreflective, 9 kHz to 45 GHz

FEATURES

- Ultra-wideband frequency range: 9 kHz to 45 GHz
- Nonreflective design
- Low insertion loss
  - 0.9 dB typical to 18 GHz
  - 1.6 dB typical to 40 GHz
  - 1.7 dB typical to 45 GHz
- High Isolation: 42 dB typical to 45 GHz
- High input linearity
  - 0.1 dB power compression (P0.1dB): 31 dBm
  - Third-order intercept (IP3): 53 dBm
- High power handling at T_{CASE} = 85°C
  - 30 dBm through path
  - 24 dBm terminated path
  - 30 dBm hot switching (RFC port)
- RF settling time (0.1 dB final RF output): 3.5 μs
- No low-frequency spurious signals
- All off state control
- Positive Control Interface: CMOS-/LVTTL-compatible
- 20-lead, 3.0 mm × 3.0 mm LGA package

APPLICATIONS

- Test and instrumentation
- Cellular Infrastructure: 5G millimeter wave
- Military radios, radars, and electronic countermeasures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)
- Industrial scanner

FUNCTIONAL BLOCK DIAGRAM

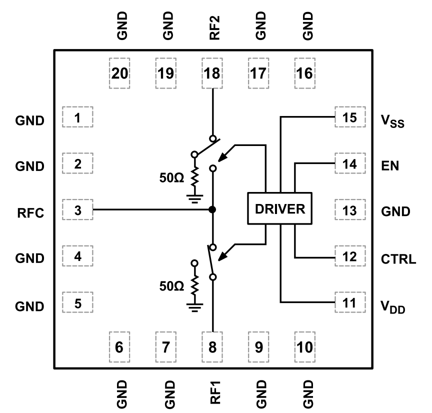

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5023 is a nonreflective, single-pole double-throw (SPDT) switch manufactured in the silicon process.

The ADRF5023 operates from 9 kHz to 45 GHz with a typical insertion loss of 1.7 dB and isolation of 42 dB. The device has a RF input power handling capability of 30 dBm for the through path, 24 dBm for the terminated path, and 30 dBm for the hot switching at the RF common port.

The ADRF5023 requires a positive supply of 3.3 V and a negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5023 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See Table 2 for more details.

The ADRF5023 is pin-compatible with the ADRF5022, a fast switching version that operates from 100 MHz to 45 GHz.

The ADRF5023 comes in a 20-lead, 3.0 mm × 3.0 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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10/2023—Rev. 0 to Rev. A

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1/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, CTRL voltage (V_{CTRL})/EN voltage (V_{EN}) = 0 V or V_{DD}, and T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		45,000	MHz
INSERTION LOSS						
Between RFC and RF1/RF2 (On)		9 kHz to 18 GHz		0.9		dB
		18 GHz to 26 GHz		1.1		dB
		26 GHz to 35 GHz		1.4		dB
		35 GHz to 40 GHz		1.6		dB
		40 GHz to 45 GHz		1.7		dB
RETURN LOSS						
RFC and RF1/RF2 (On)		9 kHz to 18 GHz		20		dB
		18 GHz to 26 GHz		20		dB
		26 GHz to 35 GHz		18		dB
		35 GHz to 40 GHz		18		dB
		40 GHz to 45 GHz		18		dB
RF1/RF2 (Off)		9 kHz to 18 GHz		21		dB
		18 GHz to 26 GHz		21		dB
		26 GHz to 35 GHz		16		dB
		35 GHz to 40 GHz		13		dB
		40 GHz to 45 GHz		12		dB
ISOLATION						
Between RFC and RF1/RF2 (Off)		9 kHz to 18 GHz		55		dB
		18 GHz to 26 GHz		55		dB
		26 GHz to 35 GHz		55		dB
		35 GHz to 40 GHz		50		dB
		40 GHz to 45 GHz		49		dB
Between RF1 and RF2		9 kHz to 18 GHz		60		dB
		18 GHz to 26 GHz		56		dB
		26 GHz to 35 GHz		48		dB
		35 GHz to 40 GHz		44		dB
		40 GHz to 45 GHz		42		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		0.5		μs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		1.8		μs
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		3.5		μs
INPUT LINEARITY[1]		f = 1 MHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			31		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 14 dBm each tone, Δf = 1 MHz		53		dBm
SUPPLY CURRENT		V_{DD}, V_{SS} pins				
Positive Supply Current	I_{DD}			150		μA
Negative Supply Current	I_{SS}			520		μA
DIGITAL CONTROL INPUTS						
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			< 1		μA
High	I_{INH}	CTRL		< 1		μA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		EN		33		μA
RECOMMENDED OPERATING CONDITONS						
Positive Supply Voltage	V_{DD}		3.15		3.45	V
Negative Supply Voltage	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2, 3]	P_{IN}	f = 1 MHz to 40 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1/RF2			30	dBm
Terminated Path		RF signal is applied to terminated RF1/RF2			24	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1/RF2			30	dBm
Case Temperature	T_{CASE}		−40		+105	°C

1 For input linearity performance over frequency, see Figure 14 to Figure 17.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0 V, V_{CTRL}/V_{EN} = 0 V or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operational Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		45,000	MHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		2.2		μs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		5.8		μs
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		7.8		μs
INPUT LINEARITY		f = 1 MHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			16		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, Δf = 1 MHz		43		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1, 2]	P_{IN}	f = 1 MHz to 40 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1/RF2			16	dBm
Terminated Path		RF signal is applied to terminated RF1/RF2			12	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1/RF2			16	dBm

1 For power derating over frequency, see Figure 2 and Figure 3.

2 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[1] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 1 MHz to 40 GHz, T_{CASE} = 85°C)	
Through Path	31 dBm
Terminated Path	25 dBm
Hot Switching (RFC port)	31 dBm
RF Input Power, Single Supply[1] (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 1 MHz to 40 GHz, T_{CASE} = 85°C)	
Through Path	17 dBm
Terminated Path	13 dBm
Hot Switching (RFC port)	17 dBm
RF Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	17 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating over frequency, see Figure 2 and Figure 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-19		
Through path	160	°C/W
Terminated path	200	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

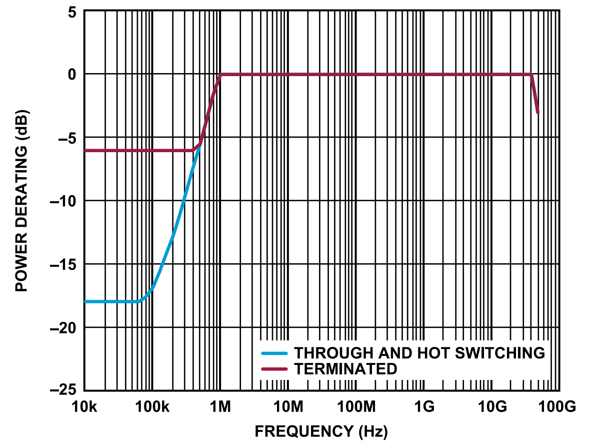

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

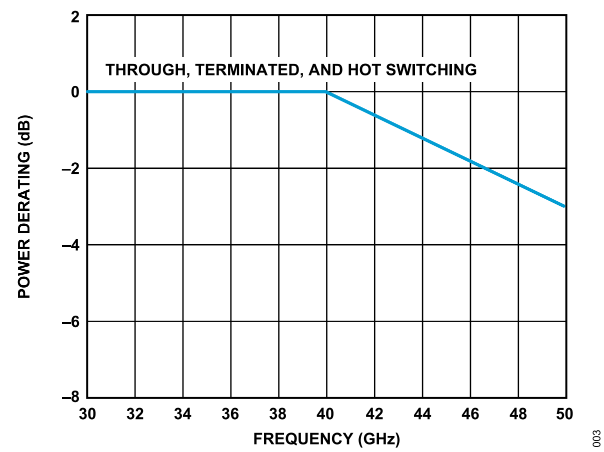

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5023

Table 5. ADRF5023, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	± 2000 for all pins	2
CDM	± 500 for all pins	C2

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

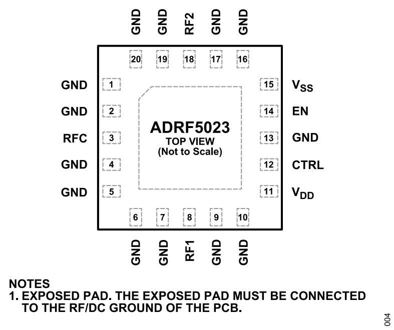

Figure 4. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
3	RFC	RF Common Port. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
8	RF1	RF Throw Port 1. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
11	V_{DD}	Positive Supply Voltage.
12	CTRL	Control Input Voltage.
14	EN	Enable Input Voltage.
15	V_{SS}	Negative Supply Voltage.
18	RF2	RF Throw Port 2. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

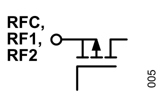

Figure 5. RF Pins (RFC, RF1, RF2) Interface Schematic

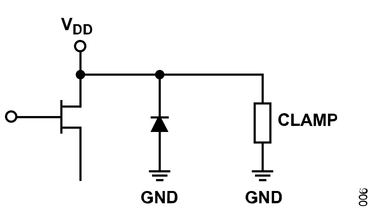

Figure 6. V_{DD} Pin Interface Schematic

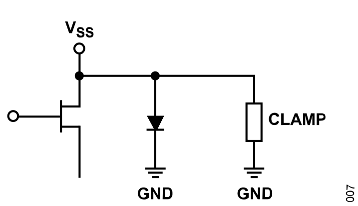

Figure 7. V_{SS} Pin Interface Schematic

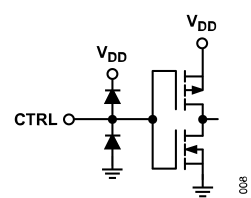

Figure 8. CTRL Pin Interface Schematic

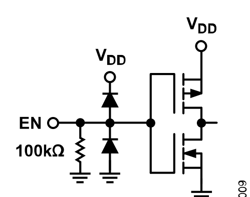

Figure 9. EN Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V or 0 V, V_{CTRL}/V_{EN} = 0 V or V_{DD}, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. Measured on the ADRF5023-EVALZ.

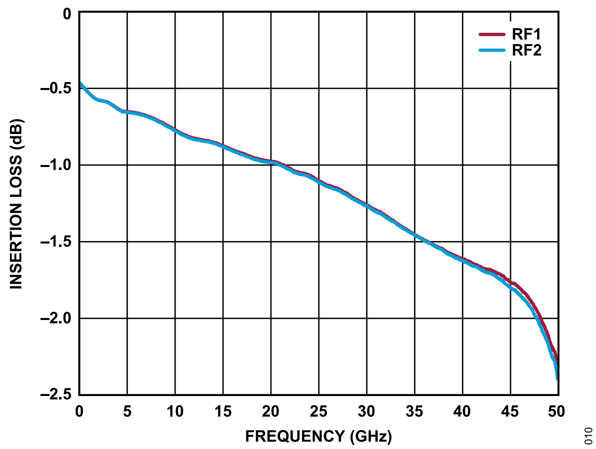

Figure 10. Insertion Loss vs. Frequency at Room Temperature for RF1 and RF2

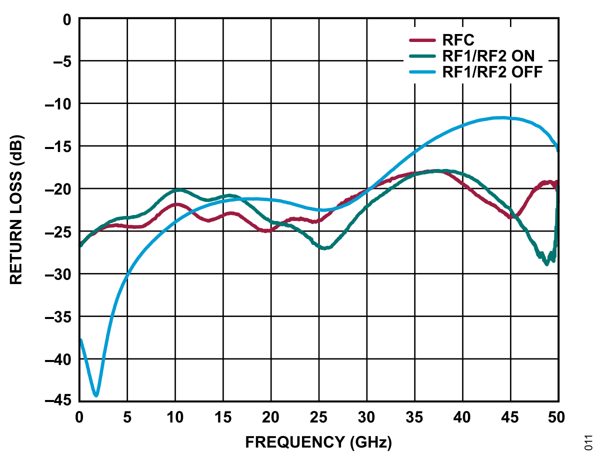

Figure 11. Return Loss vs. Frequency

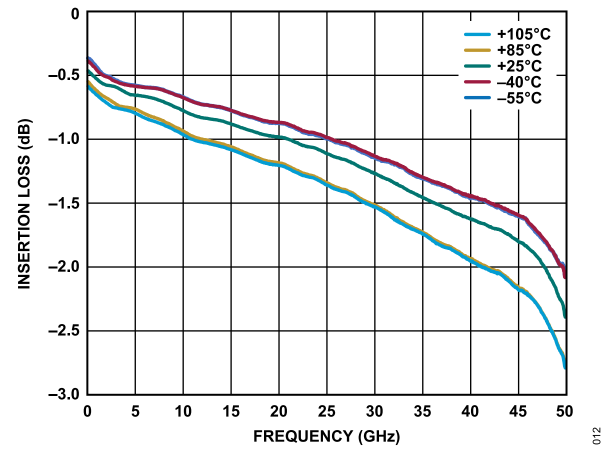

Figure 12. Insertion Loss vs. Frequency over Temperature

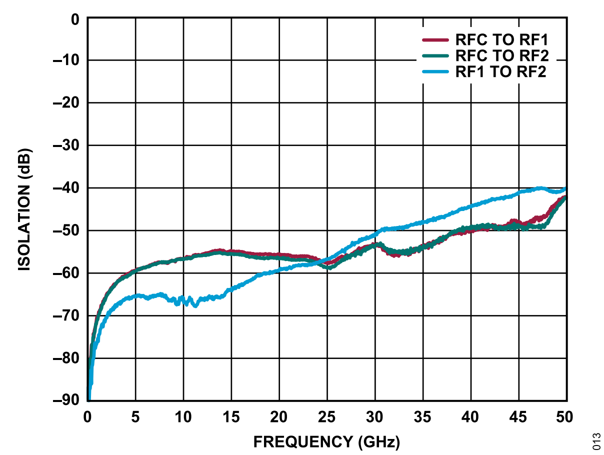

Figure 13. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL}/V_{EN} = 0 V or V_{DD}, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. The large-signal performance parameters are measured on the ADRF5023-EVALZ.

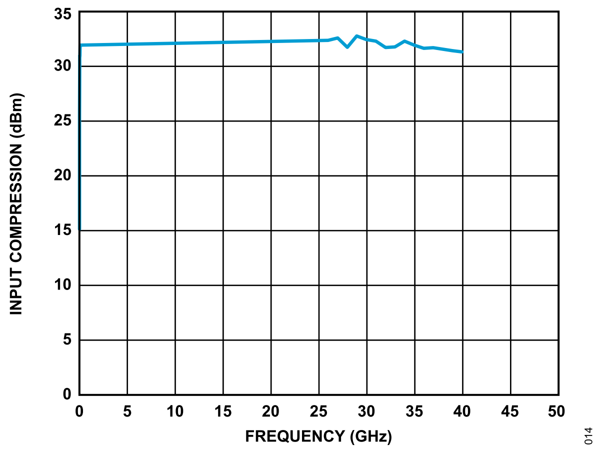

Figure 14. Input 0.1 dB Power Compression vs. Frequency

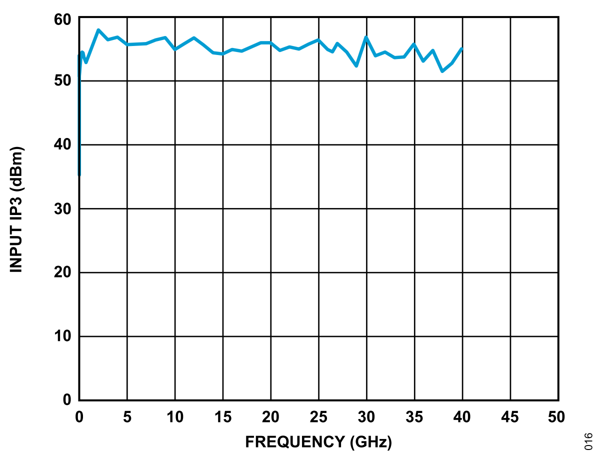

Figure 15. Input IP3 vs. Frequency

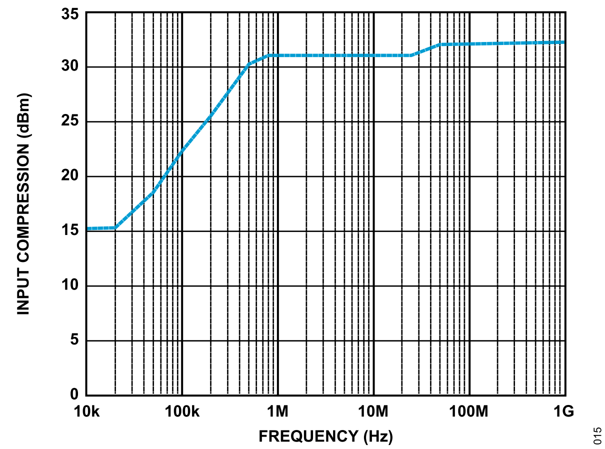

Figure 16. Input 0.1 dB Power Compression vs. Frequency, Low Frequency Detail

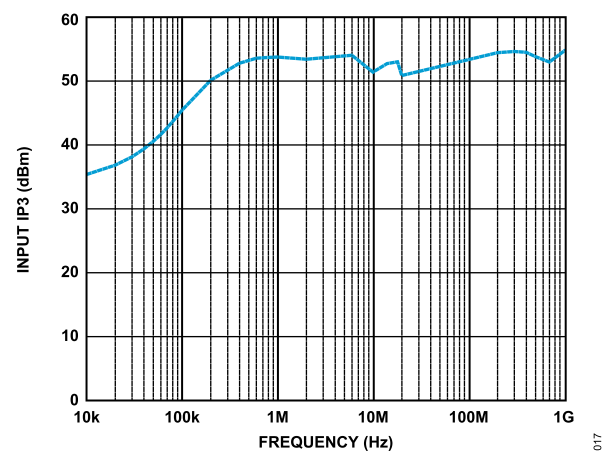

Figure 17. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5023 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features two digital control input pins (CTRL and EN) that control the state of RF paths, determining which RF port is in insertion loss state and which RF port is in isolation state (see Table 7).

POWER SUPPLY

The ADRF5023 requires a positive supply voltage applied to the V_{DD} pin and a negative supply voltage applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect the ground.
2. Power up V_{DD} and V_{SS}. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control inputs. Power the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after V_{DD} is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.
5. The ideal power-down sequence is the reverse order of the power-up sequence.

Single-Supply Operation

The ADRF5023 can operate with a single positive supply voltage applied to the V_{DD} pin and V_{SS} pin connected to ground. However, some performance difference can occur in switching characteristics and large signal, see Table 1 for more details.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF port is in insertion loss state and which RF port is in isolation state. The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50 Ω resistor.

When the EN pin is logic high, the switch is in an all-off state regardless of the logic state of the CTRL pin. Both the RF1 to RFC path and the RF2 to RFC path are in an isolation state. The RF1 and RF2 ports are terminated to internal 50 Ω resistors, and the RFC port becomes reflective open.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

Table 7. Control Voltage Truth Table

Digital Control Inputs		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

The ADRF5023 has two power supply pins (V_{DD} and V_{SS}) and two control pins (CTRL and EN). Figure 18 shows the external components and connections for supply and control pins. The V_{DD} pin and the V_{SS} pin are decoupled with a 100pF multilayer ceramic capacitor. The device pin-out allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Pin Configuration and Function Descriptionssection.

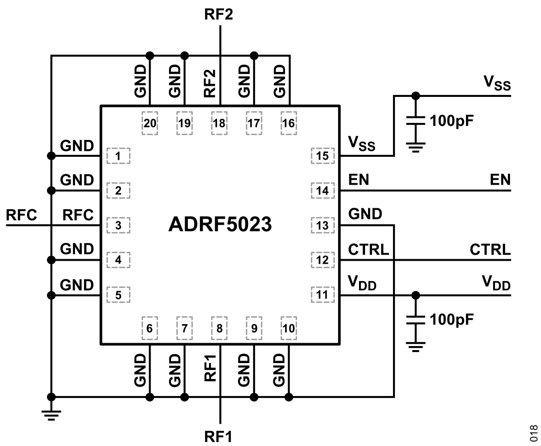

Figure 18. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally, and the pin out is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. Figure 19 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

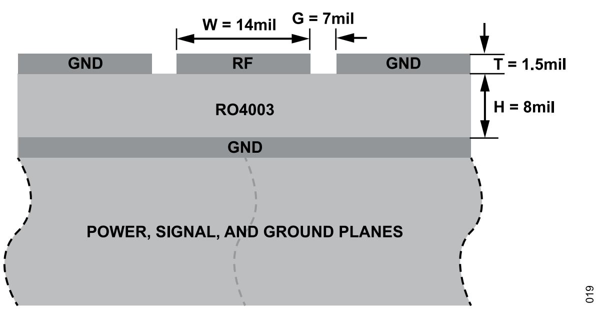

Figure 19. Example PCB Stack Up

Figure 20 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF, and thermal performance. The primary thermal path for the device is the bottom side.

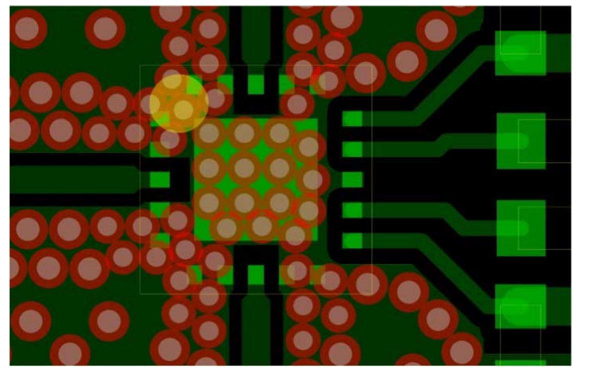

Figure 20. PCB Routings

Figure 21 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction and is divided into multiple openings for the paddle.

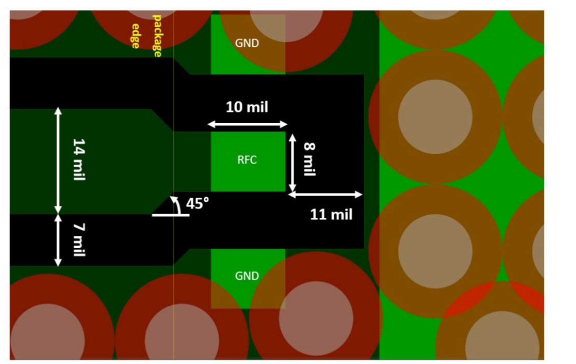

Figure 21. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Technical Support for further recommendations.

OUTLINE DIMENSIONS

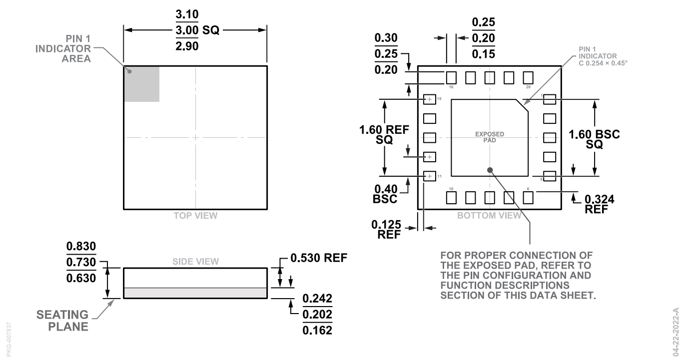

Figure 22. 20-Terminal Land Grid Array [LGA]
3.0 mm × 3.0 mm Body and 0.730 mm Package Height
(CC-20-19)
Dimensions shown in millimeters

Updated: August 11, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADRF5023BCCZN	-40°C to +105°C	20-Terminal Land Grid Array (LGA)	Reel, 500	CC-20-19	023
ADRF5023BCCZN-R7	-40°C to +105°C	20-Terminal Land Grid Array (LGA)	Reel, 1500	CC-20-19	023

1 Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model[1]	Description
ADRF5023-EVALZ	Evaluation Board

1 Z = RoHS-Compliant Part.