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Evaluating the ADPA7006 18 GHz to 44 GHz, GaAs, pHEMT, >25 dBm (>0.5 W), MMIC Power Amplifier

FEATURES

Fully featured evaluation board for the ADPA7006
2-layer Rogers 4350B evaluation board with heat sink
End launch 2.9 mm RF connectors
Through calibration path

EVALUATION KIT CONTENTS

ADPA7006-EVALZ evaluation board

EQUIPMENT NEEDED

RF signal generator
RF spectrum analyzer
RF network analyzer
5 V, 1 A power supply
−1.5 V, 100 mA power supply

GENERAL DESCRIPTION

The ADPA7006-EVALZ evaluation board consists of a 2-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B, copper clad mounted to an aluminum heat sink. The heat sink provides thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat sink allow attachment to larger heat sinks for improved thermal management.

The RFIN and RFOUT ports on the ADPA7006-EVALZ are populated by 2.9 mm, female coaxial connectors. The respective RF traces of the ports have a 50 Ω characteristic impedance. The ADPA7006-EVALZ is populated with components suitable for use over the entire −40°C to +85°C operating temperature range of the device. To calibrate evaluation board trace losses, a through calibration path is provided between the J3 and J4 connectors. J3 and J4 must be populated with RF connectors to use the through calibration path. See Table 1 and Figure 3 for the through calibration path performance.

The power, ground, gate control voltages, and detector output voltages are accessed through two 8-pin headers (see Table 1).

RF traces are 50 Ω grounded, coplanar waveguide. Package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat sink.

The power supply decoupling capacitors on the ADPA7006-EVALZ represent the configuration used to characterize and qualify the device. It is possible to reduce the number of capacitors with a scope, but the scope varies from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device.

For more information about the ADPA7006, refer to the ADPA7006 data sheet. Consult the data sheet in conjunction with this user guide when using the ADPA7006-EVALZ evaluation board.

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REVISION HISTORY

4/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

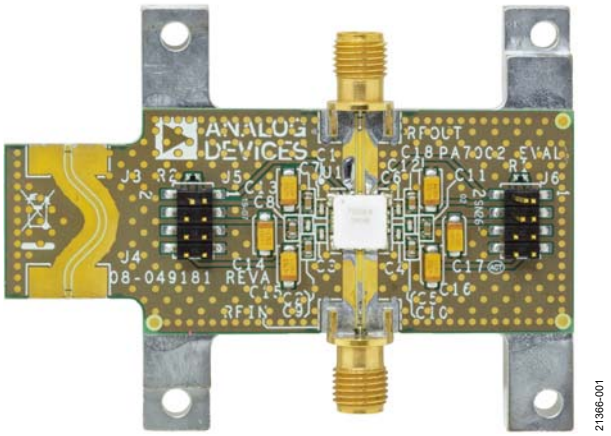

Figure 1. ADPA7006-EVALZ Top Side Photo

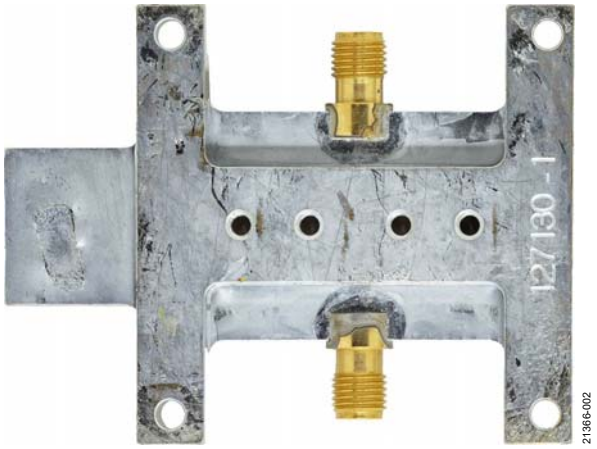

Figure 2. ADPA7006-EVALZ Bottom Side Photo

OPERATING THE ADPA7006-EVALZ

A 5 V, 1 A power supply is required to provide the main bias to the ADPA7006-EVALZ board. The 5 V power supply must be connected in parallel to all of the VDD lines (VDD1, VDD2, VDD3, and VDD4) through the J5 and J6 headers. Additionally, a 0 V to −1.5 V, 100 mA power supply is required to provide the required gate control voltage. Connect the −1.5 V power supply in parallel to the two VGG1 lines through the J5 and J6 headers.

POWER-UP

During power-up, use the following biasing sequence:

1. Connect the ADPA7006 GND pin to the RF ground and dc ground.
2. Initially, set the gate voltages (V_{GG1}) and drain voltages (V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}) to 0 V.
3. Set the ADPA7006 V_{GG1} pin voltages to −1.5 V.
4. Set all the drain bias voltages (V_{DDX} pin voltages) to 5 V.
5. Increase the V_{GG1} pin and V_{GG2} pin voltages to achieve a quiescent drain current of 800 mA.
6. Apply the RF signal to the device.

POWER-DOWN

During power-down, use the following biasing sequence:

1. Turn off the RF signal.
2. Decrease the V_{GG1} pin and V_{GG2} pin voltages to −1.5 V to achieve I_{DQ} = 0 mA (approximately, where I_{DQ} is the quiescent drain current).
3. Decrease all V_{DDX} pin voltages to 0 V.
4. Decrease the V_{GG1} pin voltage and V_{GG2} pin voltage to 0 V.

Table 1. J5 and J6 Header Connections to the ADPA7006

Connector	Header	ADPA7006 Pin
J5	1	VREF
J5	2	VREF (through a 100 kΩ resistor)
J5	3, 5, 7	GND
J5	4	V_{DD3}
J5	6	V_{DD1}
J5	8	V_{GG1}
J6	1	VDET (through a 100 kΩ resistor)
J6	2	VDET
J6	3	V_{DD4}
J6	4, 6, 8	GND
J6	5	V_{DD2}
J7	7	V_{GG1}

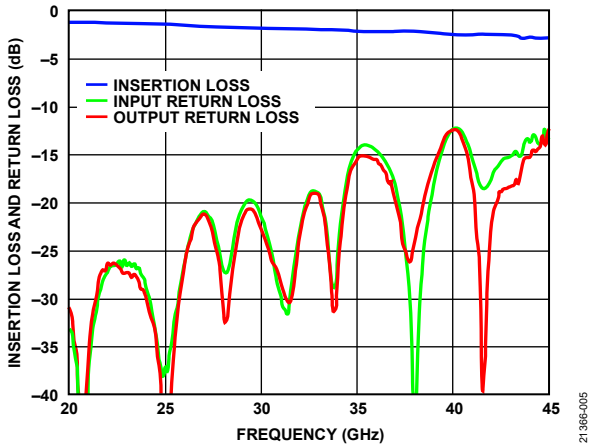

Figure 3. Insertion Loss and Return Loss of Through Calibration Path

Table 2. Insertion Loss and Return Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
18	−1.1
20	−1.2
22.5	−1.3
25	−1.4
27.5	−1.6
30	−1.8
32.5	−1.9
35	−2.1
37.5	−2.1
40	−2.6
42.5	−2.5
45	−3

EVALUATION BOARD SCHEMATICS AND ARTWORK

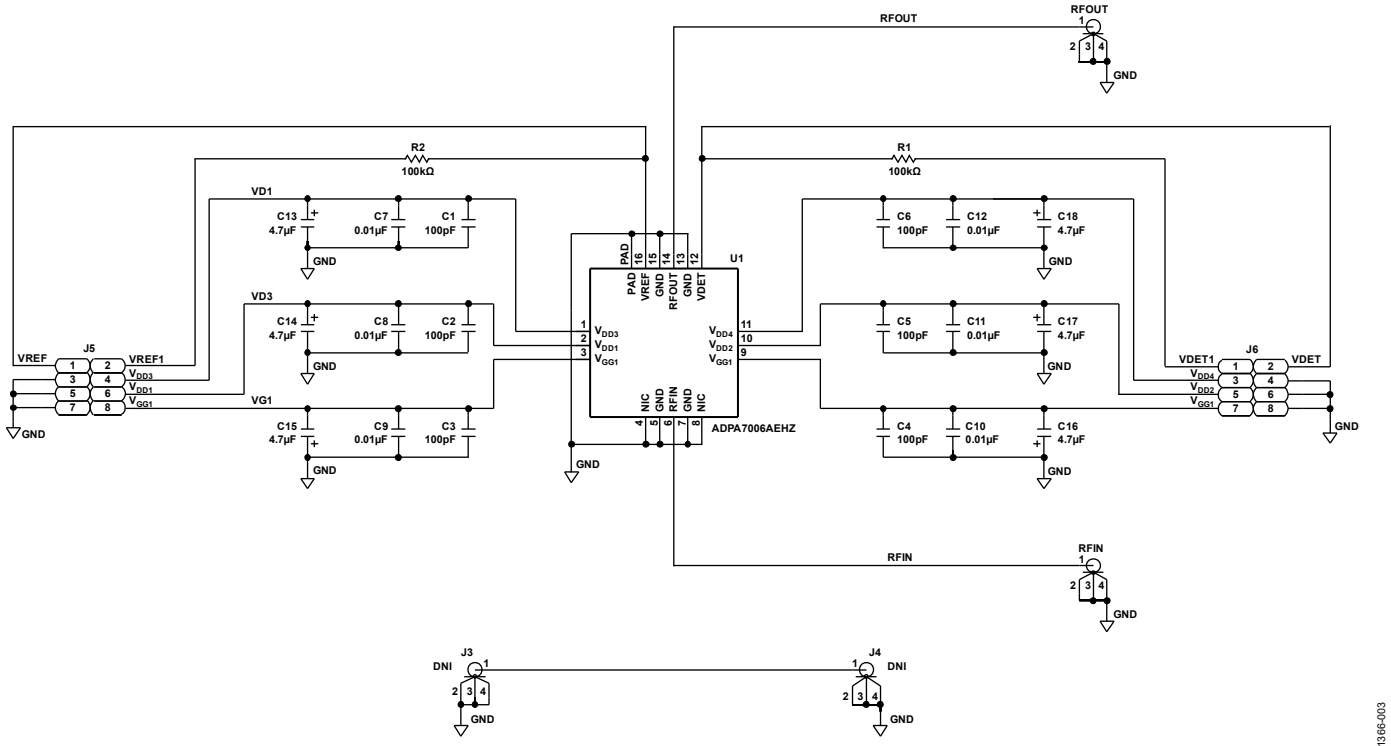

Figure 4. ADPA7006-EVALZ Evaluation Board Schematic

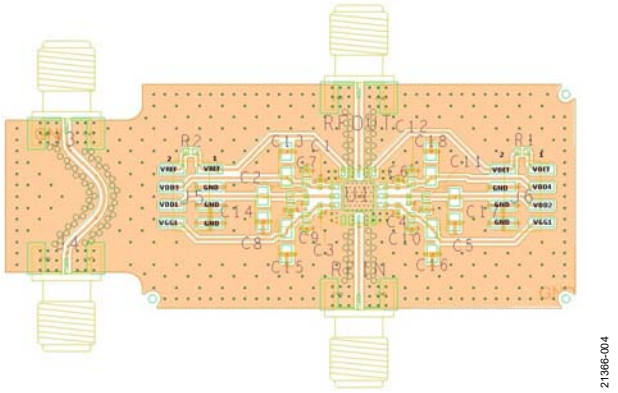

Figure 5. ADPA7006-EVALZ Assembly Drawing (J3 and J4 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer	Part Number
6	C1 to C6	Ceramic capacitors, 100 pF	Kemet	C0402C101J5GACTU
6	C7 to C12	Multilayer ceramic capacitors, XR7, 0.01 µF	Kemet	C0603C103K5RECAUTO
6	C13 to C18	Tantalum capacitors, 4.7 µF	AVX	TAJA475K020RNJ
2	J3 and J4	Connectors, 2.9 mm, jack, PCB mount receptacle, do not install	SRI Connector Gage Co	25-146-1000-92
2	J5 and J6	PCB connector headers, 8-position, vertical, dual-row, 2 mm pitch	Molex	87759-0814
2	R1 and R2	Thick film chip resistors, 100 kΩ	Panasonic	ERJ-2GEJ104X
2	RFIN, RFOUT	Connectors, 2.9 mm, jack, PCB mount receptacle	SRI Connector Gage Co	25-146-1000-92
1	U1	18 GHz to 44 GHz gallium arsenide (GaAs), pseudo morphic high electron mobility transfer (pHEMPT), monolithic microwave integrated circuit (MMIC) power amplifier, 0.5 W	Analog Devices	ADPA7006AEHZ
1	Not applicable	2.51 inch × 1.9 inch aluminum heat sink	Not applicable	Not applicable

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ADPA7006-EVALZ