3-Channel Isolated Micropower Management Unit with Seven Digital Isolators and Programmable Power Control

FEATURES

- Wide input supply voltage range: 4.5 V to 60 V
- Integrated flyback power switch
- Generates isolated, independent, resistor-programmable bipolar outputs and factory-programmable buck output
  - V_{OUT1}: 6 V to 28 V
  - V_{OUT2}: 5.0 V
  - V_{OUT3}: −24 V to −2 V
- 86% typical efficiency at 2.61 W output power
- Programmable power control pin (PPC_IN) for adjusting V_{OUT1} through serial command
- Uses a 1:1 ratio transformer for simplified transformer design
- Adjustable switching frequency via SYNC input
- Peak current limiting and overvoltage protection
- Internal compensation and soft start control per regulator
- Precision enable input
- High speed, low propagation delay, SPI signal isolation channels
- Three 100 kbps general-purpose isolated data channels
- 41-lead, 9 mm × 7 mm LFCSP form factor enables small overall solution size
- −40°C to +125°C operating junction temperature range
- Safety and regulatory approvals (pending)
  - CISPR11 Class B radiated emission
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
    - 300 V rms basic insulation between slave, master, and field power domains (IEC 61010-1, pending)
  - VDE certificate of conformity
    - DIN V VDE 0884-10 (VDE 0884-10):2006-12
    - V_{IORM} = 565 V peak

APPLICATIONS

- Industrial automation and process control
- Instrumentation and data acquisition systems
- Data and power isolation

TYPICAL APPLICATION CIRCUIT

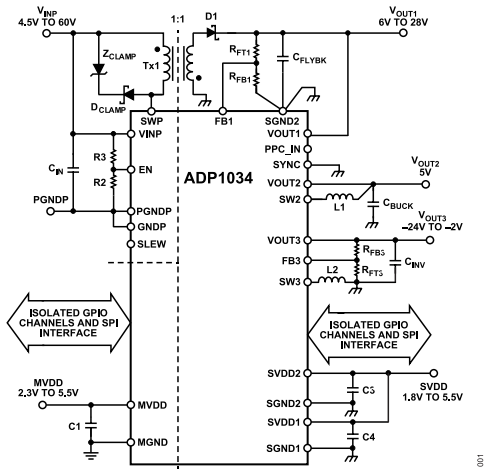

Figure 1.

GENERAL DESCRIPTION

The ADP1034 is high performance, isolated micropower management unit (PMU) that combines an isolated flyback dc-to-dc regulator, an inverting buck boost dc-to-dc regulator, and a buck dc-to-dc regulator, providing three isolated power rails. The ADP1034 includes four high speed serial peripheral interface (SPI) isolation channels and three general-purpose isolators for channel to channel applications where low power dissipation and small solution size are required.

Operating over an input voltage range of 4.5 V to 60 V, the ADP1034 generates isolated output voltage ranges of 6 V to 28 V for V_{OUT1}, −24 V to −2 V for V_{OUT3}, and a factory-programmable voltage of 5 V for V_{OUT2}. Additionally, a PPC_IN pin is provided for adjusting the V_{OUT1} setting on demand through a serial command that allows higher efficiency in system level applications.

By default, the ADP1034 flyback regulator operates at a 250 kHz switching frequency, and the buck and inverting regulators operate at 125 kHz. The ADP1034 can be driven by an external oscillator in the range of 350 kHz to 750 kHz to ease noise filtering in sensitive applications.

The digital isolators integrated in the ADP1034 use Analog Devices, Inc., *i*Coupler® chip scale transformer technology optimized for low power and low radiated emissions. The ADP1034 is available in a 9 mm × 7 mm, 41-lead lead frame chip scale package (LFCSP) and is rated for a −40°C to +125°C operating junction temperature range.

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. 0

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REVISION HISTORY

5/2022—Revision 0: Initial Version

SPECIFICATIONS

VINP voltage (V_{VINP}) = 24 V, MVDD voltage (V_{MVDD}) = 3.3 V, SVDDx voltage (V_{SVDDx}) = 3.3 V, VOUT1 voltage (V_{OUT1}) = 24 V, VOUT2 voltage (V_{OUT2}) = 5 V, VOUT3 voltage (V_{OUT3}) = −15 V, and T_A = 25°C for typical specifications. Minimum and maximum specification apply over the entire operating range of 4.5 V ≤ V_{VINP} ≤ 60 V, 2.3 V ≤ V_{MVDD} ≤ 5.5 V, 1.8 V ≤ V_{SVDDx} ≤ 5.5 V, and −40°C ≤ T_J ≤ +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Supply voltage Range						
VINP	V_{VINP}	4.5		60	V	
MVDD	V_{MVDD}	2.3		5.5	V	
SVDD	V_{SVDDx}	1.8		5.5	V	Applies to SVDD1 and SVDD2
OUTPUT POWER AND EFFICIENCY						Transformer = ZA9644-AED
Total Output Power			690		mW	V_{OUT1} current (I_{OUT1}) = 25 mA, V_{OUT2} current (I_{OUT2}) = 6 mA, V_{OUT3} current (I_{OUT3}) = −4 mA
			2610		mW	I_{OUT1} = 105 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
Efficiency			83.9		%	I_{OUT1} = 25 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
			86		%	I_{OUT1} = 105 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
Power Dissipation			132		mW	I_{OUT1} = 25 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
			427		mW	I_{OUT1} = 105 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
QUIESCENT CURRENT						
VINP						
Operating Current	I_{Q_VINP}		1.9		mA	Normal operation, V_{OUT1}, V_{OUT2}, V_{OUT3} = no load
Shutdown Current	I_{SHDN_VINP}		125	175	µA	EN voltage (V_{EN}) = 0 V
MVDD						
SPI Active Mode	$I_{Q\_MVDD\ (SPI\_ACTIVE)}$		4.1	6.5	mA	V_{Ix}[1] = logic low, $\overline{MSS}$ = logic low
			9.2	14	mA	V_{Ix}[1] = logic high, $\overline{MSS}$ = logic low
SPI Low Power Mode	$I_{Q\_MVDD\ (SPI\_LOWPWR)}$		1.6	2.5	mA	V_{Ix}[1] = logic low, $\overline{MSS}$ = logic high
			1.6	2.5	mA	V_{Ix}[1] = logic high, $\overline{MSS}$ = logic high
SVDD1						
SPI Active Mode	$I_{Q\_SVDD1\ (SPI\_ACTIVE)}$		1.8	2.7	mA	V_{Ix}[1] = logic low, $\overline{SSS}$ = logic low
			5.7	8.6	mA	V_{Ix}[1] = logic high, $\overline{SSS}$ = logic low
SPI Low Power Mode	$I_{Q\_SVDD1\ (SPI\_LOWPWR)}$		1.8	2.7	mA	V_{Ix}[1] = logic low, $\overline{SSS}$ = logic high
			1.8	2.7	mA	V_{Ix}[1] = logic high, $\overline{SSS}$ = logic high
SVDD2	I_{Q_SVDD2}		15.5	22	µA	V_{Ix}[1] = logic low
			15.5	22	µA	V_{Ix}[1] = logic high
UVLO						
VINP						Relative to PGNDP
Rising Threshold	$V_{UVLO\_FLYBACK\ (RISE)}$		4.44	4.49	V	
Falling Threshold	$V_{UVLO\_FLYBACK\ (FALL)}$	4.29	4.34		V	
Hysteresis			100		mV	
MVDD						Relative to MGND
Rising Threshold	$V_{UVLO\_MVDD\ (RISE)}$		2.14	2.28	V	
Falling Threshold	$V_{UVLO\_MVDD\ (FALL)}$	1.9	2		V	
Hysteresis			140		mV	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		150		°C	
Hysteresis	T_{HYS}		15		°C	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PRECISION ENABLE						
Rising Input Threshold	V_{EN_RISING}	1.10	1.135	1.20	V	
Input Hysteresis	V_{EN_HYST}		100		mV	
Leakage Current			0.03	0.5	µA	$V_{EN} = V_{VINP}$
SLEW						
Voltage Level Threshold						
Slow Slew Rate				0.8	V	
Normal Slew Rate		2			V	
Input Current						
Slow Slew Rate		−10			µA	Slew voltage (V_{SLEW}) = 0 V to 0.8 V
Normal Slew Rate				10	µA	V_{SLEW} = 2 V to V_{VINP}
Fast Slew Rate		−1		+1	µA	SLEW pin not connected
CLOCK SYNCHRONIZATION						
SYNC Input						
Input Clock						
Range	f_{SYNC}	350		750	kHz	
Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	150			ns	
High Logic	$V_{H\ (SYNC)}$	1.3			V	
Low Logic	$V_{L\ (SYNC)}$			0.4	V	
Leakage Current		−1	+0.005	+1	µA	SYNC voltage (V_{SYNC}) = V_{SVDDx}
FLYBACK REGULATOR						
Output Voltage Range	V_{OUT1}	6		28	V	
Feedback Voltage	V_{FB1}		0.8		V	
Feedback Voltage Accuracy		−1.5		+1.5	%	
Feedback Bias Current	I_{FB1}			0.05	µA	
Load Regulation	$(\Delta V_{FB1}/V_{FB1})/\Delta I_{OUT1}$		−0.0005		%/mA	I_{OUT1} = 0 mA to 110 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{VINP}$		0.0002		%/V	V_{VINP} = 18 V to 32 V, I_{OUT1} = 26 mA, I_{OUT2} = 6 mA, I_{OUT3} = −4 mA
Power Field Effect Transistor (FET) On Resistance	$R_{ON\ (FLYBACK)}$		3		Ω	SWP current (I_{SWP}) = 100 mA
Current-Limit Threshold	$I_{LIM\ (FLYBACK)}$	400	440	480	mA	
SWP Leakage Current			0.03	0.5	µA	SWP voltage (V_{SWP}) = 60 V
SWP Capacitance	C_{SWP}		50		pF	
Switching Frequency	$f_{SW\ (FLYBACK)}$	235	250	265	kHz	SYNC = low or high
			$f_{SYNC}/2$		kHz	SYNC = external clock
Minimum On Time			425		ns	
Minimum Off Time			220		ns	
Soft Start Timer	$t_{SS\ (FLYBACK)}$		8		ms	
Severe Overvoltage Threshold	$SOVP_{FLYBACK}$	29.4	30	30.6	V	Flyback regulator stops switching until the overvoltage is removed
Severe Overvoltage Hysteresis	$SOVP_{FLYBACK\_HYST}$		500		mV	
PROGRAMMABLE POWER CONTROL (PPC) INTERFACE						
Valid Code Range		54		255	Code	Equivalent of 6 V to 28 V V_{OUT1} range, minimum code may be different if maximum V_{OUT1} is set to a different voltage
Input Threshold						
Logic High	V_{IH}	1.3			V	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Low	V_{IL}			0.4	V	
BUCK REGULATOR						
Output Voltage	V_{OUT2}		5.0		V	
Output Voltage Accuracy		−1.5		+1.5	%	I_{OUT2} = 10 mA
Load Regulation	$(\Delta V_{OUT2}/V_{OUT2})/\Delta I_{OUT2}$		−0.0005		%/mA	I_{OUT2} = 2 mA to 50 mA
Line Regulation	$(\Delta V_{OUT2}/V_{OUT2})/\Delta V_{OUT1}$		0.0004		%/V	V_{OUT1} = 6 V to 28 V, I_{OUT2} = 7 mA
Power FET On Resistance	$R_{ON\_NFET\ (BUCK)}$		1		Ω	SW2 current (I_{SW2}) = 100 mA
	$R_{ON\_PFET\ (BUCK)}$		2.5		Ω	I_{SW2} = 100 mA
Current-Limit Threshold	$I_{LIM\ (BUCK)}$	280	300	320	mA	
SW2 Leakage Current						
P Type Metal-Oxide Semiconductor (PMOS)			0.03	0.5	µA	V_{SW2} = 0 V
N Type Metal-Oxide Semiconductor (NMOS)			0.03	0.5	µA	V_{SW2} = 28 V
Switching Frequency	$f_{SW\ (BUCK)}$	117.5	125	132.5	kHz	SYNC = low or high
			$f_{SYNC}/4$		kHz	SYNC = external clock
Minimum On Time			200		ns	
Soft Start Timer	$t_{SS\ (BUCK)}$		8		ms	
Active Pull-Down Resistor	$R_{PD\ (BUCK)}$		1.7		kΩ	1.23 V < V_{OUT1} < 4.5 V
INVERTING REGULATOR						
Output Voltage Range	V_{OUT3}	−24		−2	V	
Feedback Voltage	V_{FB3}		0.8		V	In reference to V_{OUT3}
Feedback Voltage Accuracy		−1.5		+1.5	%	Adjustable output option
Feedback Bias Current	I_{FB3}			0.05	µA	
Load Regulation	$(\Delta V_{FB3}/V_{FB3})/\Delta I_{OUT3}$		−0.01		%/mA	I_{OUT3} = −1 mA to −15 mA
Line Regulation	$(\Delta V_{OUT3}/V_{OUT3})/\Delta V_{OUT1}$		0.0005		%/V	V_{OUT1} = 6 V to 28 V, I_{OUT3} = −15 mA
Power FET On Resistance	$R_{ON\_NFET\ (INVERTER)}$		1.45		Ω	SW3 current (I_{SW3}) = 100 mA
	$R_{ON\_PFET\ (INVERTER)}$		2.2		Ω	I_{SW3} = 100 mA
Current-Limit Threshold	$I_{LIM\ (INVERTER)}$	280	300	320	mA	
SW3 Leakage Current						
PMOS			0.03	0.5	µA	V_{SW3} = −24 V
NMOS			0.03	0.5	µA	V_{SW3} = 24 V
Switching Frequency	$f_{SW\ (INVERTER)}$	117.5	125	132.5	kHz	SYNC = low or high
			$f_{SYNC}/4$		kHz	SYNC = external clock
Minimum On Time			178		ns	
Soft Start Timer	$t_{SS\ (INVERTER)}$		8		ms	
Active Pull-Down Resistor	$R_{PD\ (INVERTER)}$		350		Ω	1.23 V < V_{OUT1} < 4.5 V
ISOLATORS DC SPECIFICATIONS[2]						
MCK, $\overline{MSS}$, MO, SO, SGPI1, MGPI2, SGPI3						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{xVDD}			V	V_{xVDD} = V_{MVDD} or V_{SVDDx}
Logic Low	V_{IL}			0.3 × V_{xVDD}	V	V_{xVDD} = V_{MVDD} or V_{SVDDx}
Input Current[3]	I_I	−1		+1	µA	0 V ≤ V_{INPUT} ≤ V_{xVDD}
SCK, $\overline{SSS}$, SI, MI						
Output Voltage						

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High	V_{OH}	V_{xVDD} − 0.1			V	I_{Ox}[4] = −20 µA, V_{Ix} = V_{IxH}[5]
		V_{xVDD} − 0.4			V	I_{Ox}[4] = −2 mA, V_{Ix} = V_{IxH}[5]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[4] = 20 µA, V_{Ix} = V_{IxL}[6]
			0.2	0.4	V	I_{Ox}[4] = 2 mA, V_{Ix} = V_{IxL}[6]
MGPO1, SGPO2, MGPO3						
Output Voltage						
Logic High	V_{OH}	V_{xVDD} − 0.1			V	I_{Ox}[4] = −20 µA, V_{Ix} = V_{IxH}[5]
		V_{xVDD} − 0.4			V	I_{Ox}[4] = −500 µA, V_{Ix} = V_{IxH}[5]
Logic Low	V_{OL}			0.1	V	I_{Ox}[4] = 20 µA, V_{Ix} = V_{IxL}[6]
			0.15	0.4	V	I_{Ox}[4] = 500 µA, V_{Ix} = V_{IxL}[6]
SCK, SI, MI						
Tristate Leakage		−1	+0.01	+1	µA	$\overline{MSS}$ = logic high
		−1	+0.01	+1	µA	V_{Ox}[7] = V_{xVDD}
ISOLATORS SWITCHING SPECIFICATION						
MCK, $\overline{MSS}$, MO, SO						
SPI Clock Rate	SPI_{MCK}			16.6	MHz	
Latency			100	125	ns	Delay from $\overline{MSS}$ going low to the first data output is valid
Input Pulse Width	t_{PW}	17			ns	Within PWD limit
Input Pulse Width Distortion (PWD)	t_{PWD}		0.25	6.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Channel Matching						
Codirectional	t_{PSKCD}		0.5	5.5	ns	
Opposing Direction	t_{PSKOD}		0.5	4	ns	
Propagation Delay	t_{PHL}, t_{PLH}					50% input to 50% output
			7	11	ns	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			7	12	ns	V_{MVDD} = 3.3 V, V_{SVDD1} = 5 V
			7	15	ns	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			8.5	12	ns	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
Jitter			620		ps p-p	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			100		ps rms	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			440		ps p-p	V_{MVDD} = 3.3 V, V_{SVDD1} = 5 V
			80		ps rms	V_{MVDD} = 3.3 V, V_{SVDD1} = 5 V
			290		ps p-p	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			60		ps rms	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			410		ps p-p	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
			110		ps rms	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
SGPI1, MGPI2, SGPI3						
Data Rate				100	kbps	
Input Pulse Width	t_{PW}	10			µs	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			14	µs	50% input to 50% output
Jitter				10	µs	
ISOLATORS AC SPECIFICATIONS						
General-Purpose Input/Output (GPIO)						
Output Rise Time/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[8]	|CM|		25		kV/µs	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SPI						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[8]	|CM|		100		kV/µs	

[1] V_{Ix} is the Channel x logic input, where Channel x can be MCK, MO, SO, SGPI1, MGPI2, or SGPI3.

[2] V_{xVDD} is either V_{MVDD} or V_{SVDDx} depending on whether the input side is master or slave.

[3] V_{INPUT} is the voltage at the input of the digital pins.

[4] I_{Ox} is the output current of the pin.

[5] V_{IxH} is the input side logic high.

[6] V_{IxL} is the input side logic low.

[7] V_{Ox} is the voltage where the output is pulled.

[8] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining VOUT > 0.8 MVDD and/or SVDDx. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING CHARACTERISTICS

1-Wire Serial Interface Timing Specifications

V_{VINP} = 24 V, V_{MVDD} = 3.3 V, V_{SVDDx} = 3.3 V, V_{OUT1} = 24 V, V_{OUT2} = 5 V, V_{OUT3} = −15 V, and T_A = 25°C for typical specifications. Minimum and maximum specification apply over the entire operating range of 4.5 V ≤ V_{VINP} ≤ 60 V, 2.3 V ≤ V_{MVDD} ≤ 5.5 V, 1.8 V ≤ V_{SVDDx} ≤ 5.5 V, and −40°C ≤ T_J ≤ +125°C, unless otherwise noted. Refer to the 1-Wire Serial Interface section for more information on the 1-wire serial interface.

Table 2. 1-Wire Serial Interface

Parameter[1, 2]	Description	Min	Typ	Max	Unit	Test Conditions / Comments
$t_{PPC\_TOTAL\_RES}$	Response time		1		ms	PPC transaction time plus V_{OUT1} settling time from 6 V to 28 V
t_{PPC1}	Bit period	4500	5000	6600	ns	
t_{PPC2}	Start detect high time	60	200	400	ns	
t_{PPC3}	Start detect low time	60	200	400	ns	
t_{PPC4}	Start detect sample time	900	1000	1100	ns	Time for two consecutive pulses
t_{PPC5}	Logic low time	60	400	800	ns	
t_{PPC6}	Logic high time	1200	3500	4400	ns	
t_{PPC7}	Slave pull down window	2200		2700	ns	Time window for slave to control the bus during acknowledge or parity
t_{PPC8}	Time when the master takes back control of the bus when there is no response from the slave	3400		3600	ns	
t_{PPC9}	Time when the master takes back control of the bus when the slave responds by pulling low			2727	ns	
t_{LP}	Bus lockup protection	1350	1500	1650	ns	Analog watchdog timer

[1] All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of the voltage on the VOUT2 pin (V_{OUT2}) and timed from a voltage level of V_{OUT2}/2.

[2] Guaranteed by design and characterization; not production tested.

SPECIFICATIONS

1-Wire Serial Interface Timing Diagram

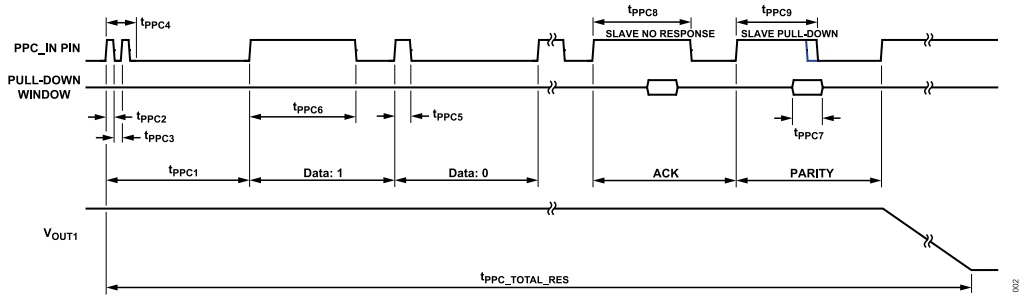

Figure 2. PPC Timing Diagram for a Complete Transmission

REGULATORY INFORMATION

See Table 10 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 3. Safety Certifications

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized Under UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
2500 V rms Single Protection	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: basic insulation at 300 V rms (424 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: basic insulation at 300 V rms mains, 300 V rms (424 V peak) secondary	Basic insulation, 565 V peak

ELECTROMAGNETIC COMPATIBILITY

Table 4.

Regulatory Body	Standard	Comment
SGS/Compliance Certification Services, Inc. (CCSrf)	CISPR11 Class B	Pending

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)				
Field Power Domain to Master Domain		2.15	mm min	Measured from field power pins and pads to master pins and pads, shortest distance through air
Field Power Domain to Slave Domain		2.15	mm min	Measured from field power pins and pads to slave pins and pads, shortest distance through air
Master Domain to Slave Domain		2.15	mm min	Measured from master pins and pads to slave pins and pads, shortest distance through air
Minimum External Tracking (Creepage)				
Field Power Domain to Master Domain		2.15	mm min	Measured from field power pins and pads to master pins and pads, shortest distance path along body
Field Power Domain to Slave Domain		2.15	mm min	Measured from field power pins and pads to slave pins and pads, shortest distance path along body
Master Domain to Slave Domain		2.15	mm min	Measured from master pins and pads to slave pins and pads, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	µm min	Insulation distance through insulation

SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			I to I	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\,(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1060	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	847	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		678	V peak
Highest Allowable Overvoltage		V_{IOTM}	3537	V peak
Surge Isolation Voltage	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.48	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

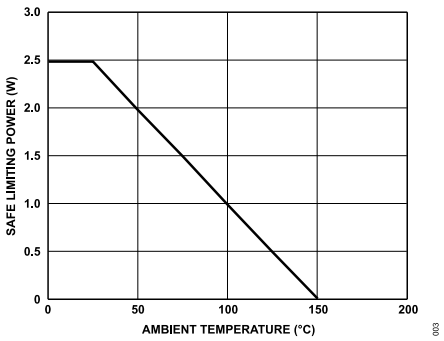

Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VINP to PGNDP	61 V
SWP to PGNDP	VINP + 70 V or 110 V, whichever is lower
SWP to VINP	110 V – VINP or 70 V, whichever is lower
SLEW to GNDP	−0.3 V to VINP + 0.3 V
EN to GNDP	−0.3 V to +61 V
VOUT1 to SGND2	35 V
FB1 to SGND2	−0.3 V to +3.3V
VOUT1 to VOUT3	61 V
SW2 to SGND2	−0.3 V to VOUT1 + 0.3 V
VOUT2 to SGND2	6 V
SW3 to SGND2	VOUT3 − 0.3 V to VOUT1 + 0.3 V
VOUT3 to SGND2	−26 V to +0.3 V
FB3 to VOUT3	−0.3 V to +3.3V
SVDD1 to SGND1	6.0 V
SVDD2 to SGND2	6.0 V
$\overline{SSS}$, SCK, SI, SO to SGND1	−0.3 V to SVDD1 + 0.3 V
SGPI1, SGPO2, SGPI3 to SGND2	−0.3 V to SVDD2 + 0.3 V
SYNC to SGND2	−0.3 V to +6 V
PPC_IN to SGND2	−0.3 V to +6 V
MVDD to MGND	6.0 V
$\overline{MSS}$, MCK, MO, MI to MGND	−0.3 V to MVDD + 0.3 V
MGPO1, MGPI2, MGPO3 to MGND	−0.3 V to MVDD + 0.3 V
Common-Mode Transients	±100 kV/µs
Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	JEDEC industry standard
Soldering Conditions	JEDEC J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is measured at the top of the package and is independent of the PCB. The Ψ_{JT} value is appropriate for calculating junction to case temperature in the application.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
CP-41-1[1, 2, 3]	50.4	33.1	25	°C/W

[1] 9 mm × 7 mm LFCSP with omitted pins for isolation purposes.

[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 19 thermal vias. See JEDEC JESD-51.

[3] Case temperature was measured at the center of the package.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADP1034

Table 9. ADP1034, 41-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
FICDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	300 V rms	20-year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	424 V peak	Limited by the creepage of the package, Pollution Degree 2, Material Group II[2, 3]

[1] See the Insulation Lifetime section for more details.

[2] Other pollution degree and material group requirements yield a different limit.

[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

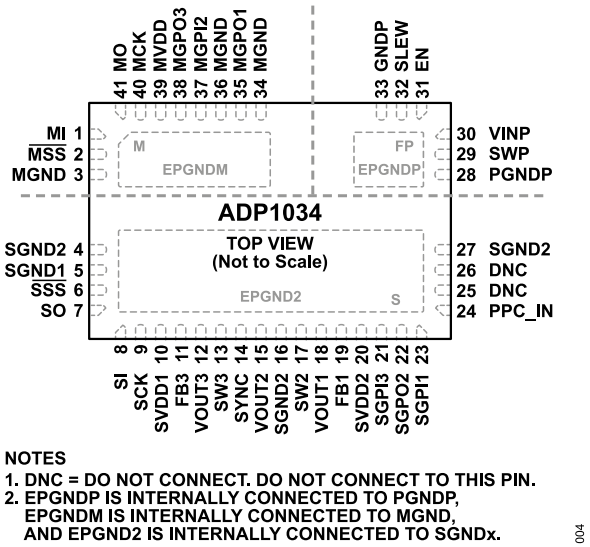

Figure 4. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Isolation Domain	Direction	Description
1	MI	Master	Output	SPI Data Output from the Slave MI and SO Line. This pin is paired with SO. On the slave domain, SO drives this pin.
2	$\overline{\text{MSS}}$	Master	Input	SPI Slave Select Input from the Master Controller. This pin is paired with $\overline{\text{SSS}}$. On the slave domain, this pin drives $\overline{\text{SSS}}$. This signal uses an active low logic.
3	MGND	Master	Ground	Master Domain Signal Ground Connection.
4	SGND2	Slave	Ground	Slave Domain Ground Connection. This pin can be left unconnected.
5	SGND1	Slave	Ground	Slave Domain SPI Isolator Ground.
6	$\overline{\text{SSS}}$	Slave	Output	SPI Slave Select Output. This pin is paired with $\overline{\text{MSS}}$. On the master domain, $\overline{\text{MSS}}$ drives this pin.
7	SO	Slave	Input	SPI Data Input Going to the Master MI and SO Line. This pin is paired with MI. On the master domain, this pin drives MI.
8	SI	Slave	Output	SPI Data Output from the Master MO and SI Line. This pin is paired with MO. On the master domain, MO drives this pin.
9	SCK	Slave	Output	SPI Clock Output from the Master. This pin is paired with MCK. On the master domain, MCK drives this pin.
10	SVDD1	Slave	Power	SPI Isolator Power Supply. Connect a 100 nF decoupling capacitor from SVDD1 to SGND1.
11	FB3	Slave		Inverting Regulator Feedback Pin.
12	VOUT3	Slave	Power	Inverting Regulator Output and Overvoltage Sense.
13	SW3	Slave		Inverting Regulator Switch Node.
14	SYNC	Slave	Input	Synchronization Pin. To synchronize the switching frequency, connect the SYNC pin to an external clock at twice the required switching frequency. Do not leave this pin floating. Connect a 100 kΩ pull-down resistor from the SYNC pin to SGND2.
15	VOUT2	Slave	Power	Buck Regulator Output Feedback.
16	SGND2	Slave	Ground	Slave Power Ground. Ground return for inverting and buck regulator output capacitors.
17	SW2	Slave		Buck Regulator Switch Node.
18	VOUT1	Slave	Power	Flyback Regulator Output and Overvoltage Sense. This pin is the input to the buck and inverting regulators.
19	FB1	Slave		Feedback Node for the Flyback Regulator.
20	SVDD2	Slave	Power	GPIO Isolators Power Supply. Connect a 100 nF decoupling capacitor from SVDD2 to SGND2.
21	SGPI3	Slave	Input	General-Purpose Input 3. This pin is paired with MGPO3.
22	SGPO2	Slave	Output	General-Purpose Output 2. This pin is paired with MGPI2.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Isolation Domain	Direction	Description
23	SGPI1	Slave	Input	General-Purpose Input 1. This pin is paired with MGPO1.
24	PPC_IN	Slave	Input	Programmable Power Control Input. Single pin access for PPC communication for adjusting V_{OUT1} setting through a serial command.
25	DNC	Slave		Do not connect. Do not connect to this pin.
26	DNC	Slave		Do not connect. Do not connect to this pin.
27	SGND2	Slave	Ground	Slave Domain Ground Connection. This pin can be left unconnected.
28	PGNDP	Field power	Ground	Ground Return for Flyback Regulator Power Supply.
29	SWP	Field power		Flyback Regulator Switching Node. Primary side transformer connection.
30	VINP	Field power	Power	Flyback Regulator Supply Voltage. Connect a minimum of 3.3 µF capacitor from VINP to PGNDP.
31	EN	Field power	Input	Precision Enable. Compare the EN pin to an internal precision reference to enable the flyback regulator output. Use a resistor divider that is between 10 kΩ and 1 MΩ.
32	SLEW	Field power	Input	Flyback Regulator Slew Rate Control. The SLEW pin sets the slew rate for the SWP driver. For the fastest slew rate (best efficiency), leave the SLEW pin open. For the normal slew rate, connect the SLEW pin to VINP. For the slowest slew rate (lowest EMI), connect the SLEW pin to GNDP.
33	GNDP	Field power	Ground	Field Power Signal Ground Connection.
34	MGND	Master	Ground	Master Domain Power Ground Connection.
35	MGPO1	Master	Output	General-Purpose Output 1. This pin is paired with SGPI1.
36	MGND	Master	Ground	Master Domain Power Ground Connection.
37	MGPI2	Master	Input	General-Purpose Input 2. This pin is paired with SGPO2.
38	MGPO3	Master	Output	General-Purpose Output 3. This pin is paired with SGPI3.
39	MVDD	Master	Power	Master Domain Power. Connect a 100 nF decoupling capacitor from MVDD to MGND.
40	MCK	Master	Input	SPI Clock Input from the Master Controller. Paired with SCK. On the slave domain, this pin drives SCK.
41	MO	Master	Input	SPI Data Input Going to Slave MO and SI Line. Paired with SI. On the slave domain, this pin drives SI.
	EPGNDP	Field power	Ground	PGNDP Exposed Pad. This pad is internally connected to PGNDP.
	EPGNDM	Master	Ground	MGND Exposed Pad. This pad is internally connected to MGND.
	EPGND2	Slave	Ground	SGND Exposed Pad. This pad is internally connected to SGNDx.

TYPICAL PERFORMANCE CHARACTERISTICS

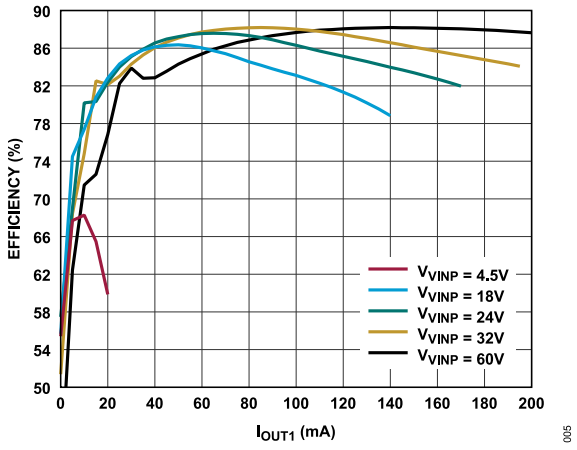

Figure 5. Overall Efficiency at Various Input Voltages, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

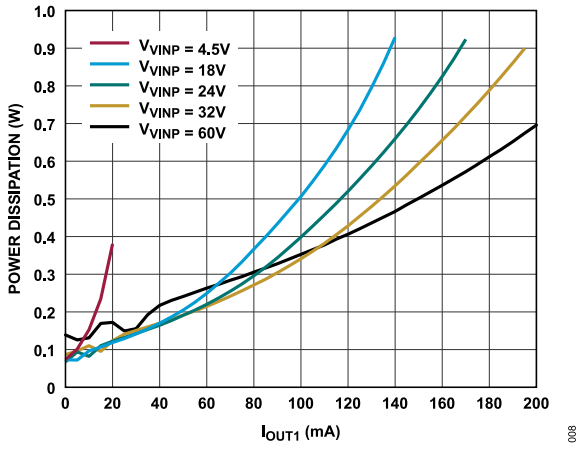

Figure 8. Power Dissipation at Various Input Voltages, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

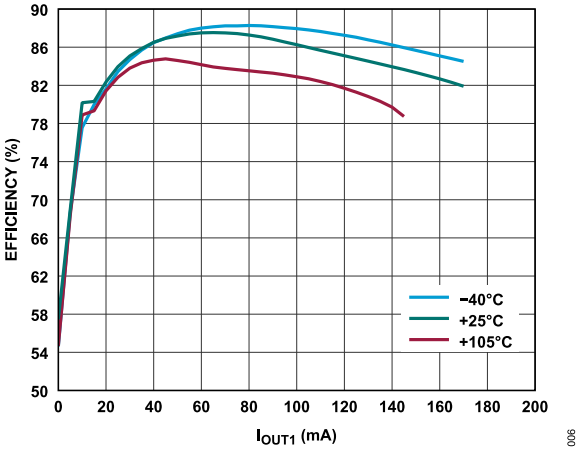

Figure 6. Overall Efficiency Across Temperature, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

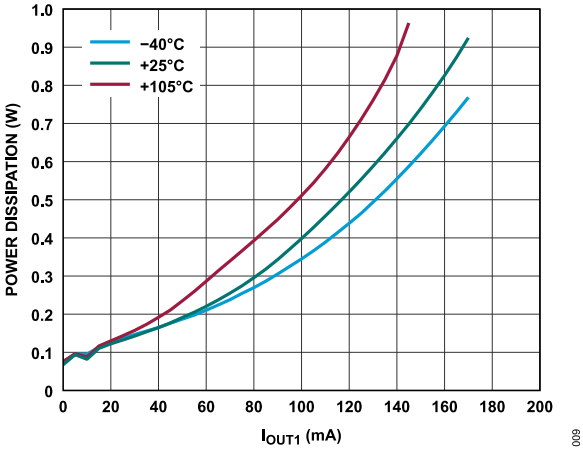

Figure 9. Power Dissipation Across Temperature, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

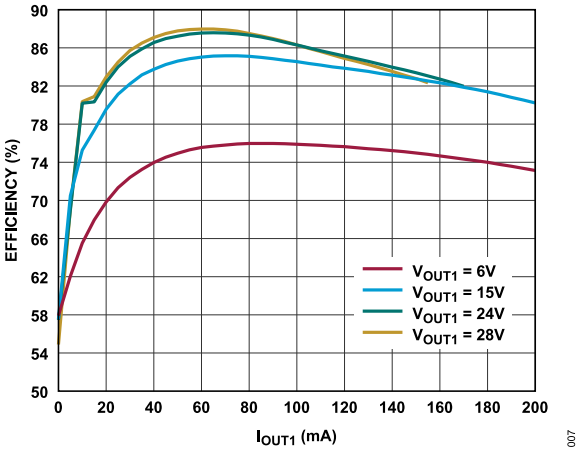

Figure 7. Overall Efficiency at Various V_{OUT1} Output Voltages, T_A = 25°C, V_{VINP} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

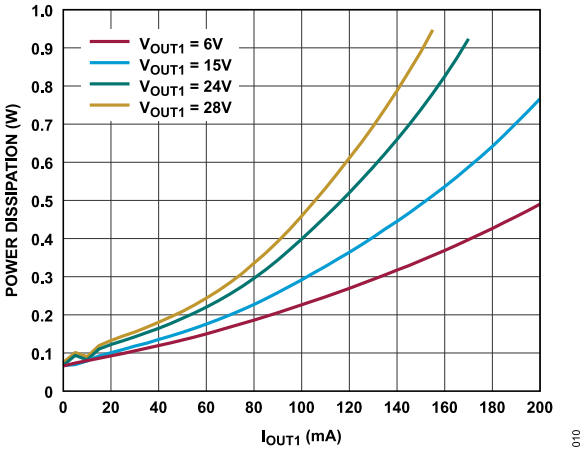

Figure 10. Power Dissipation at Various V_{OUT1} Output Voltages, T_A = 25°C, V_{VINP} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

TYPICAL PERFORMANCE CHARACTERISTICS

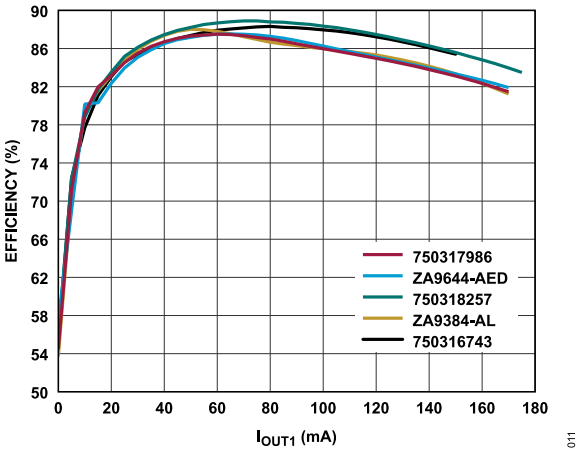

Figure 11. Overall Efficiency Using Various Transformers, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

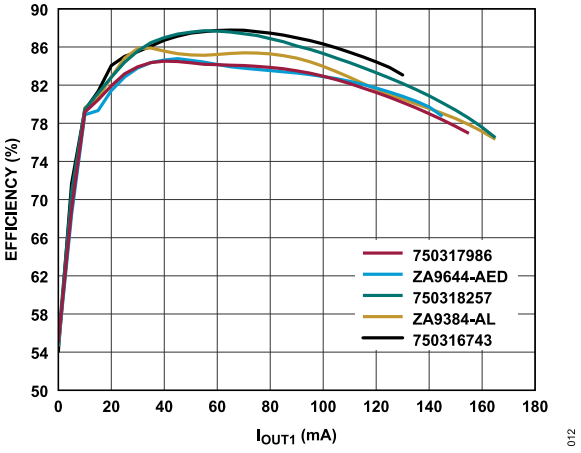

Figure 12. Overall Efficiency Using Various Transformers, T_A = 105°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

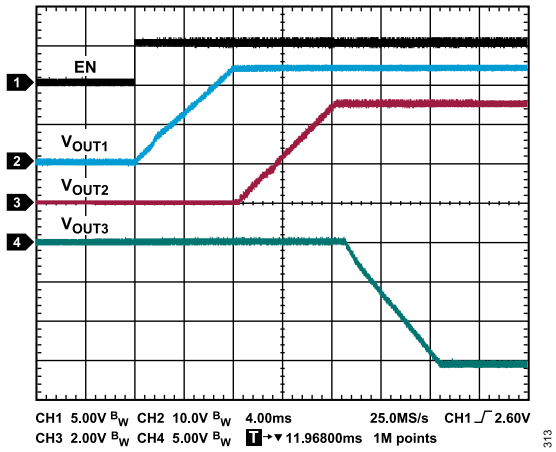

Figure 13. Power-Up Sequence, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 25 mA, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

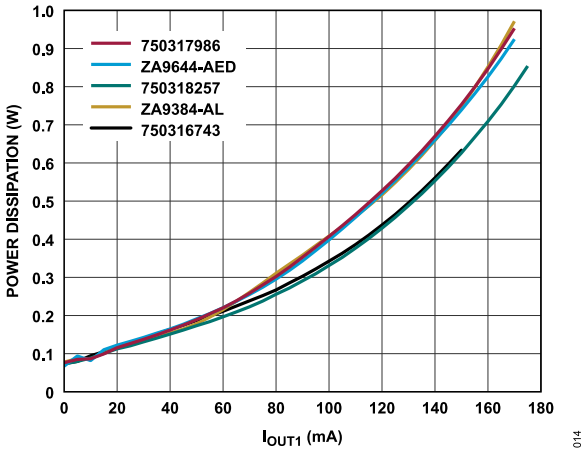

Figure 14. Power Dissipation Using Various Transformers, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

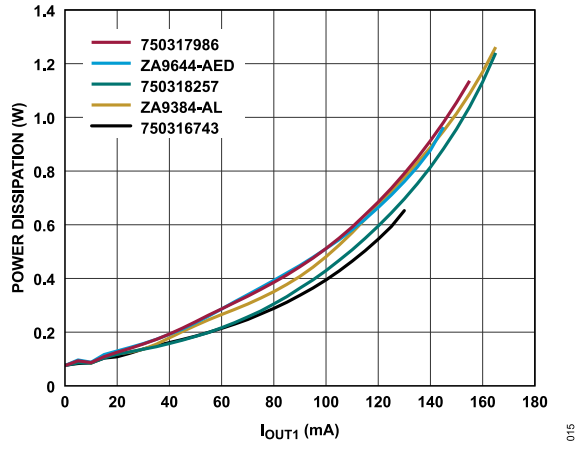

Figure 15. Power Dissipation Using Various Transformers, T_A = 105°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

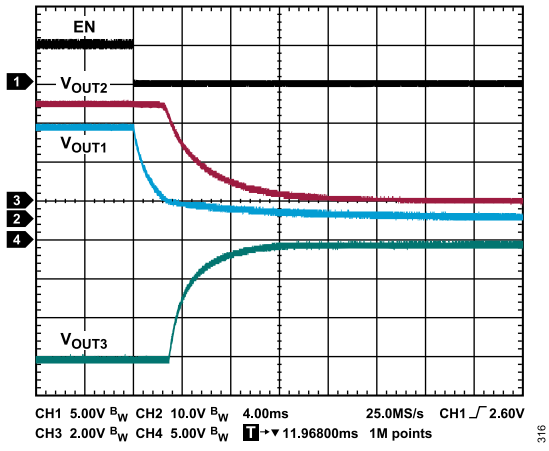

Figure 16. Shutdown Sequence, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 25 mA, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA

TYPICAL PERFORMANCE CHARACTERISTICS

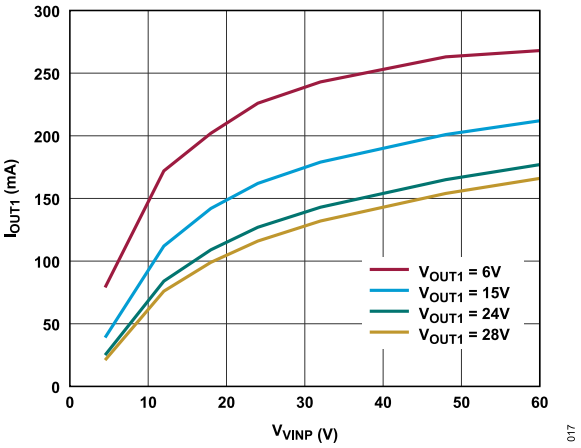

Figure 17. Flyback Regulator Maximum Output Current (I_{OUT1}) at Various Output Voltages, T_A = 25°C, Using a Coilcraft ZA9644-AED Transformer and a Zener Clamp Circuit, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

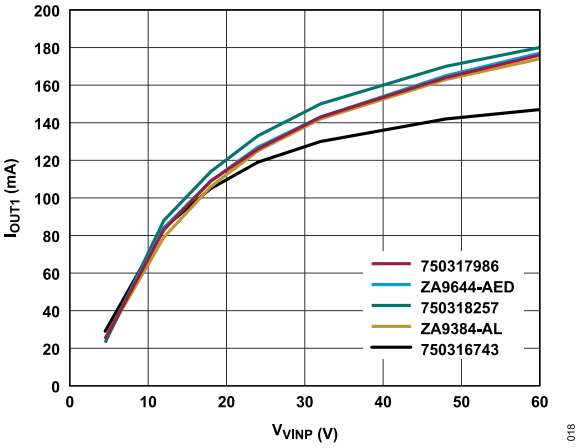

Figure 18. Flyback Regulator Maximum Output Current (I_{OUT1}) vs. V_{VINP} Over Various Transformers, T_A = 25°C, V_{OUT1} = 24 V, Using a Zener Clamp Circuit, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

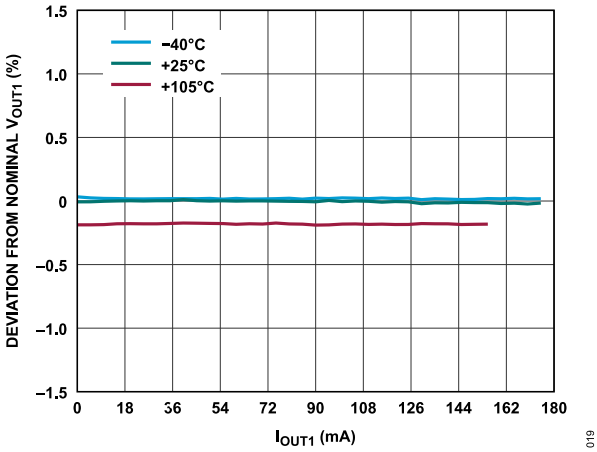

Figure 19. Flyback Regulator Load Regulation Across Temperature, V_{VINP} = 24 V, V_{OUT1} = 24 V, Nominal = V_{OUT1} at 25 mA Load

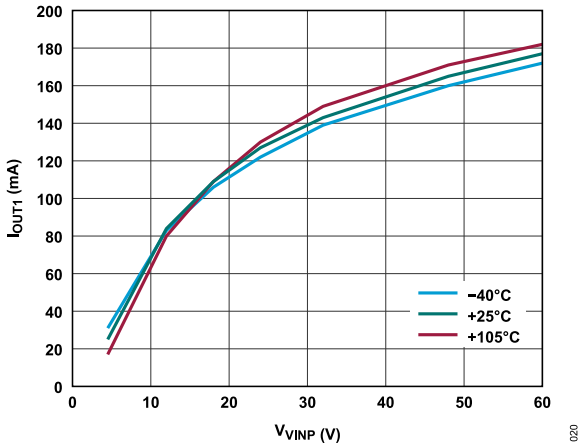

Figure 20. Flyback Regulator Maximum Output Current (I_{OUT1}) vs. V_{VINP} Across Temperature, V_{OUT1} = 24 V, Using a Coilcraft ZA9644-AED Transformer and a Zener Clamp Circuit, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

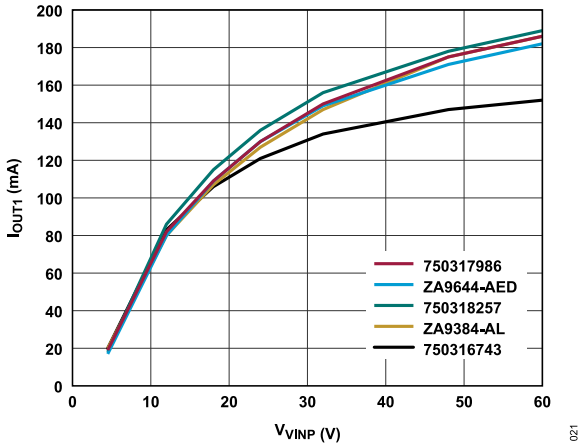

Figure 21. Flyback Regulator Maximum Output Current (I_{OUT1}) vs. V_{VINP} Over Various Transformers, T_A = 105°C, V_{OUT1} = 24 V, Using a Zener Clamp Circuit, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

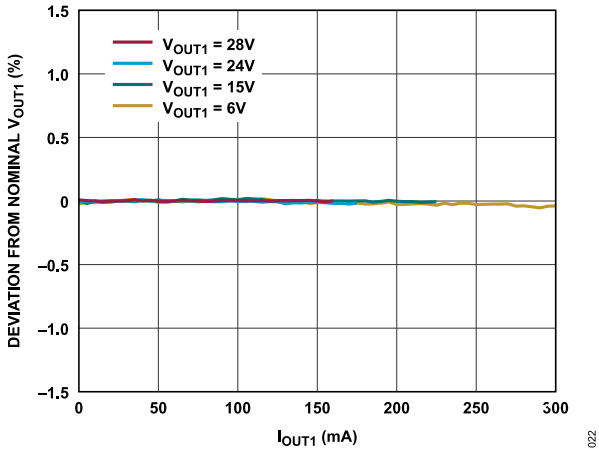

Figure 22. Flyback Regulator Load Regulation at Various Output Voltages, T_A = 25°C, V_{VINP} = 24 V, Nominal = V_{OUT1} at 25 mA Load

TYPICAL PERFORMANCE CHARACTERISTICS

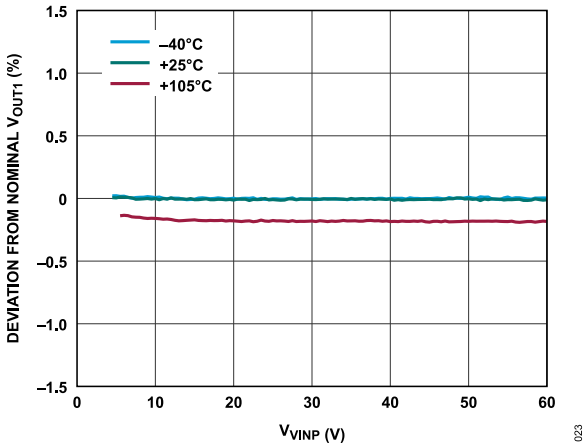

Figure 23. Flyback Regulator Line Regulation Across Temperature, V_{OUT1} = 24 V, I_{OUT1} = 25 mA, Nominal = V_{OUT1} with V_{VINP} = 24 V

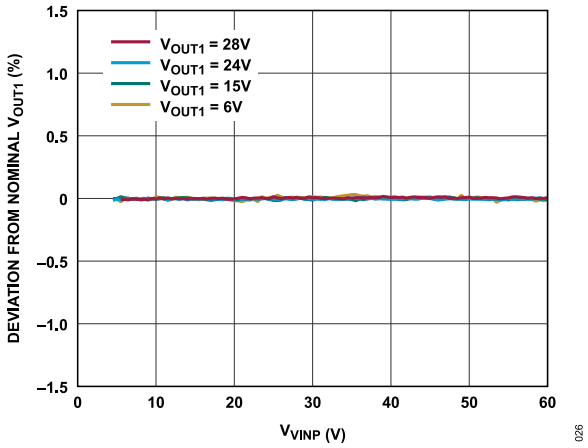

Figure 26. Flyback Regulator Line Regulation at Various Output Voltages, T_A = 25°C, I_{OUT1} = 25 mA, Nominal = V_{OUT1} with V_{VINP} = 24 V

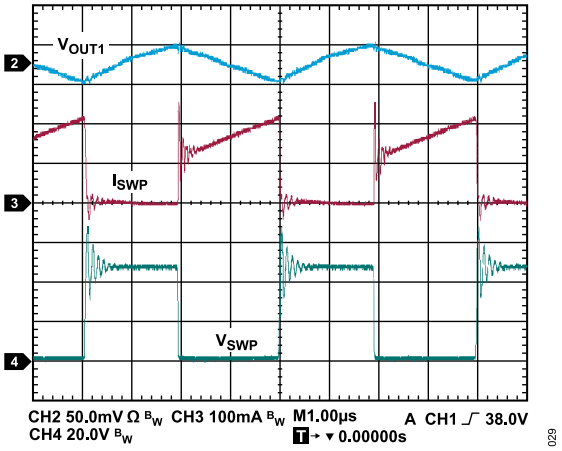

Figure 24. Flyback Regulator Continuous Conduction Mode Operation Showing I_{SWP}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 80 mA

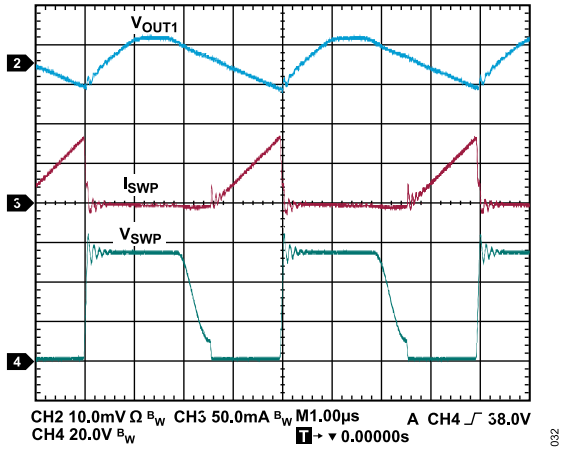

Figure 27. Flyback Regulator Discontinuous Conduction Mode Operation Showing I_{SWP}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 20 mA

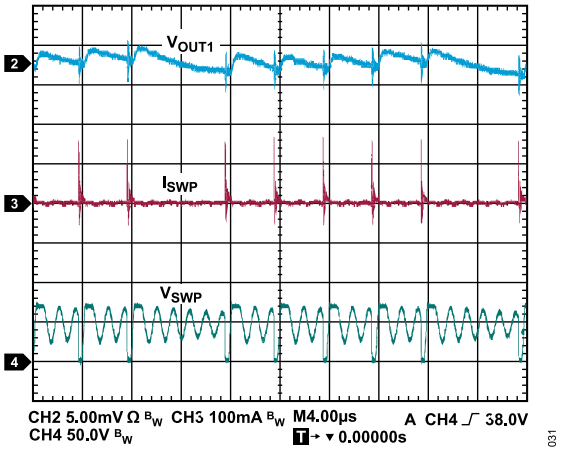

Figure 25. Flyback Regulator Pulse Skipping Operation Showing Inductor Current (I_{SWP}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{VINP} = 48 V, V_{OUT1} = 24 V, I_{OUT1} = 4 mA

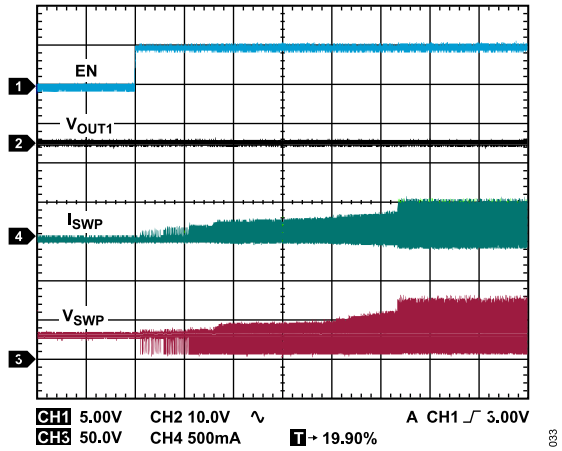

Figure 28. Flyback Regulator Short-Circuit Current Limit During Startup, V_{VINP} = 24 V, V_{OUT1} = SGND2, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

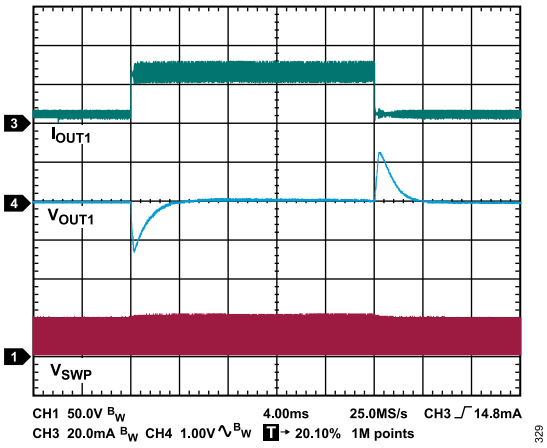

Figure 29. Flyback Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 4 mA to 25 mA Step, T_A = 25°C

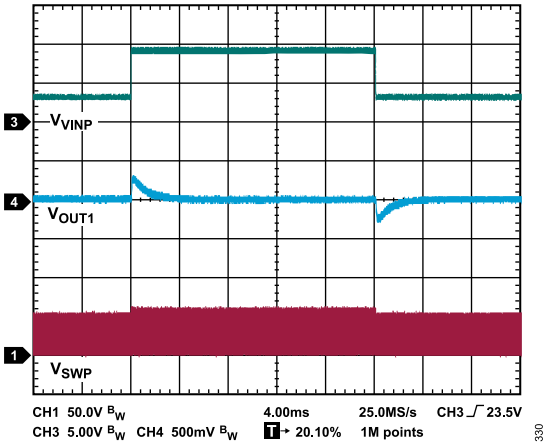

Figure 30. Flyback Regulator Line Transient Response, V_{VINP} = 18 V to 24 V, V_{OUT1} = 24 V, I_{OUT1} = 25 mA, T_A = 25°C

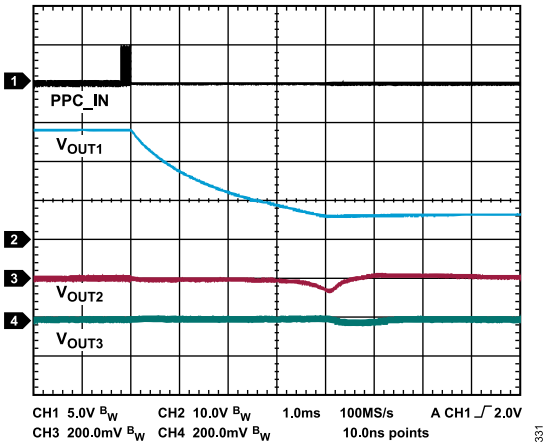

Figure 31. Programmable Power Control (PPC) Full Output Range Step, from V_{OUT1} = 28 V to 6 V, V_{VINP} = 24 V, V_{OUT1} Load = 1 kΩ, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

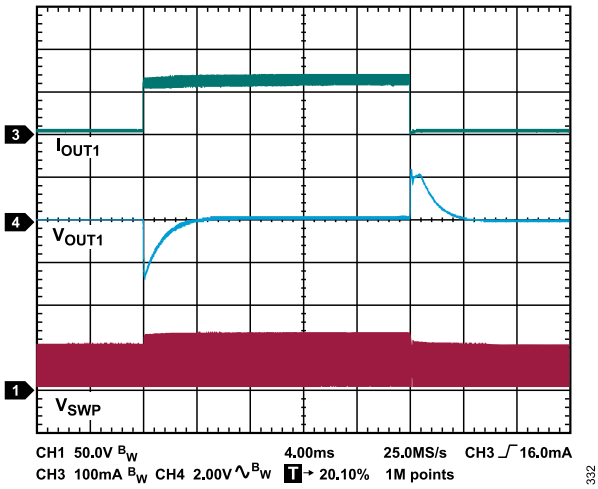

Figure 32. Flyback Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 4 mA to 120 mA Step, T_A = 25°C

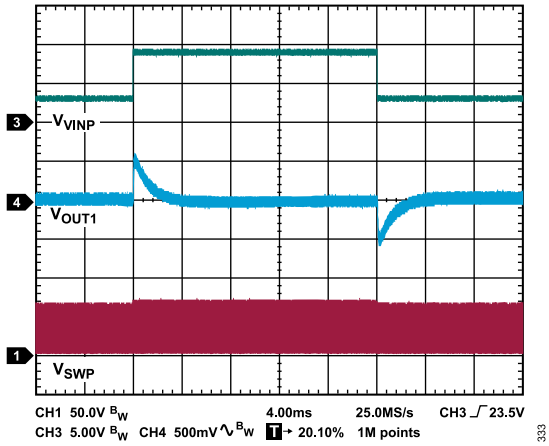

Figure 33. Flyback Regulator Line Transient Response, V_{VINP} = 18 V to 24 V, V_{OUT1} = 24 V, I_{OUT1} = 100 mA, T_A = 25°C

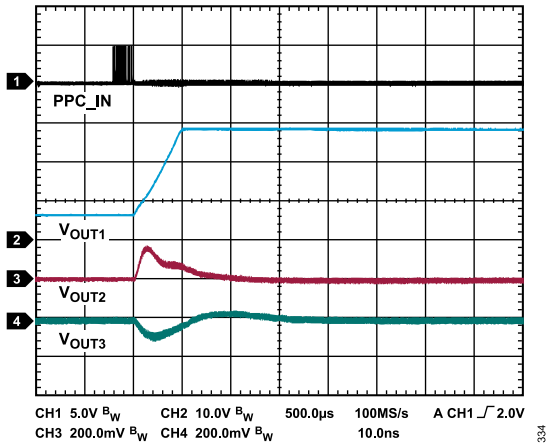

Figure 34. PPC Full Output Range Step, from V_{OUT1} = 6 V to 28 V, V_{VINP} = 24 V, V_{OUT1} Load = 1 kΩ, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

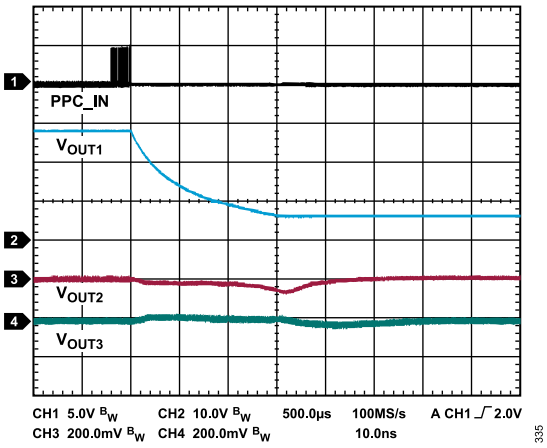

Figure 35. PPC Full Output Range Step, from V_{OUT1} = 28 V to 6 V, V_{VINP} = 24 V, V_{OUT1} Load = 250 Ω, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

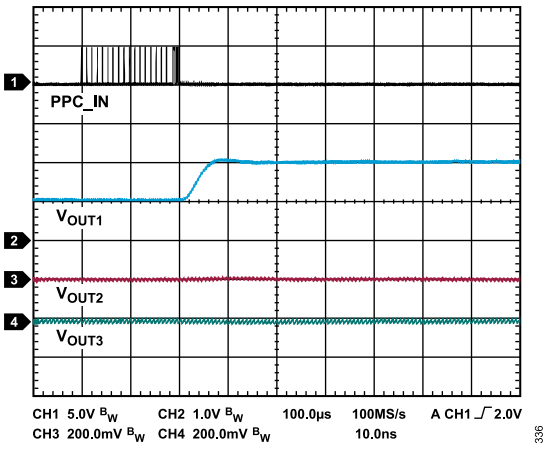

Figure 36. PPC with Step of Nine Codes, from V_{OUT1} 16 V to 17 V, V_{VINP} = 24 V, V_{OUT1} Load = 1 kΩ, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

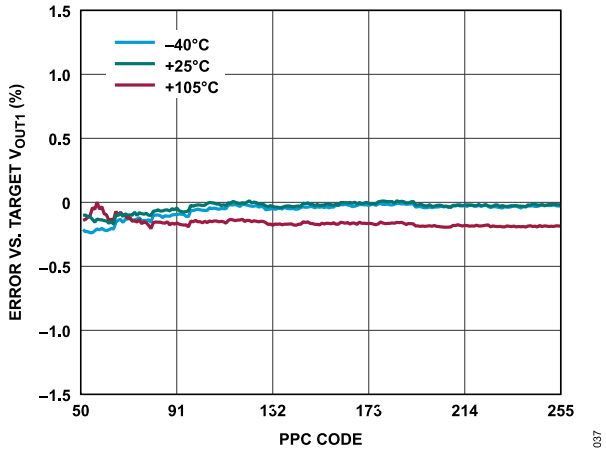

Figure 37. Flyback Regulator Accuracy vs. PPC Code Across Temperature, I_{OUT1} = 20 mA, Full-Scale V_{OUT1} = 28 V

Figure 38. PPC Full Output Range Step, from V_{OUT1} = 6 V to 28 V, V_{VINP} = 24 V, V_{OUT1} Load = 250 Ω, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

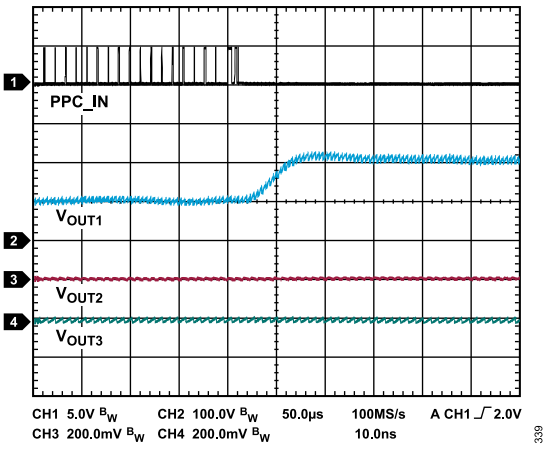

Figure 39. PPC with Step of One Code, V_{OUT1} = 10 V + 1 LSB (0.111 V), V_{VINP} = 24 V, V_{OUT1} Load = 1 kΩ, V_{OUT2} = 5.0 V, I_{OUT2} = 6 mA, V_{OUT3} = −15 V, I_{OUT3} = −4 mA, T_A = 25°C

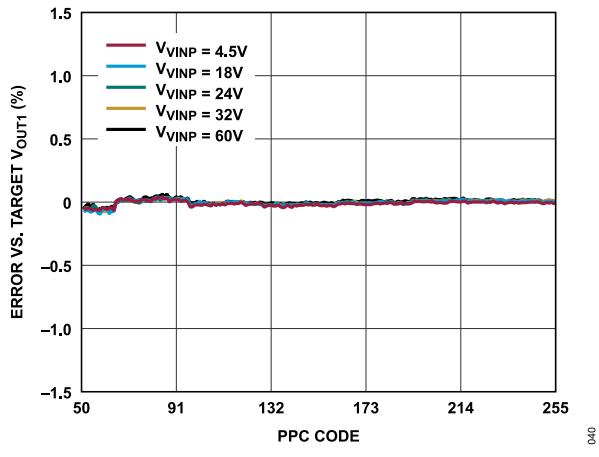

Figure 40. Flyback Regulator Accuracy vs. PPC Code Across VINP, I_{OUT1} = 20 mA, Full-Scale V_{OUT1} = 28 V

TYPICAL PERFORMANCE CHARACTERISTICS

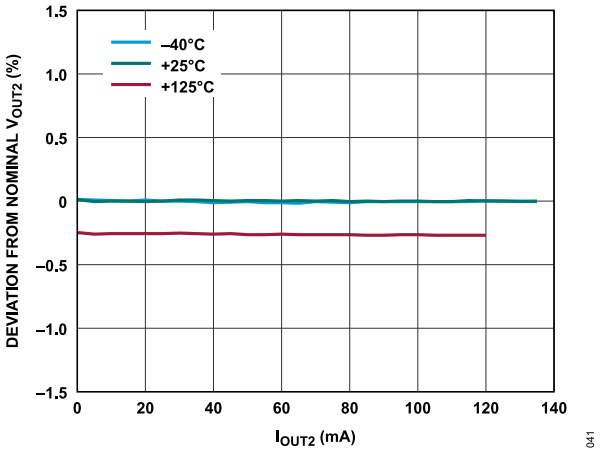

Figure 41. Buck Regulator Load Regulation Across Temperature, V_{OUT2} = 5 V, V_{OUT1} = 24 V, Nominal Conditions = V_{OUT2} at 10 mA I_{OUT2}

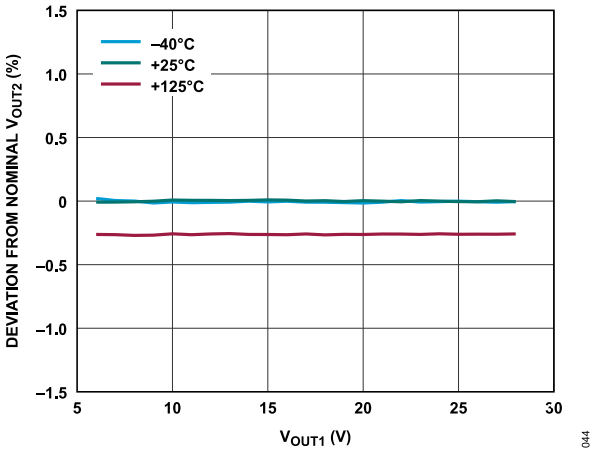

Figure 44. Buck Regulator Line Regulation Across Temperature, V_{OUT2} = 5 V, I_{OUT2} = 10 mA, Nominal Conditions = V_{OUT2} at 24 V V_{OUT1}

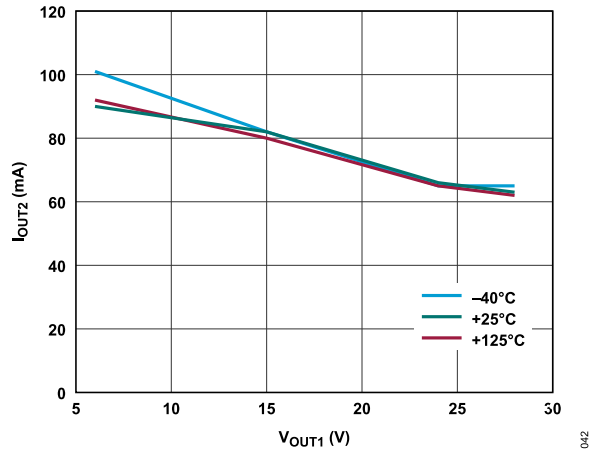

Figure 42. Buck Regulator Maximum Output Current (I_{OUT2}) vs. V_{OUT1} Across Temperature, V_{VINP} = 24 V, V_{OUT2} = 5 V, I_{OUT1} = 0 mA, I_{OUT3} = 0 mA, Based on Target of 70% $I_{LIM\ (FLYBACK)}$ or $I_{LIM\ (BUCK)}$, Whichever Comes First

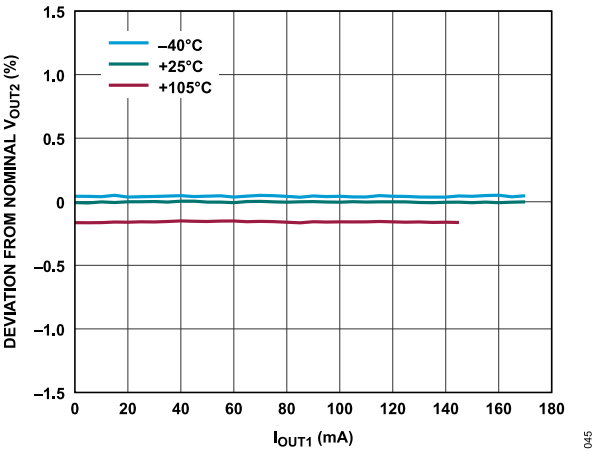

Figure 45. Buck Regulator Cross Regulation Across Temperature, V_{VINP} = 24 V, V_{OUT2} = 5 V, I_{OUT2} = 10 mA

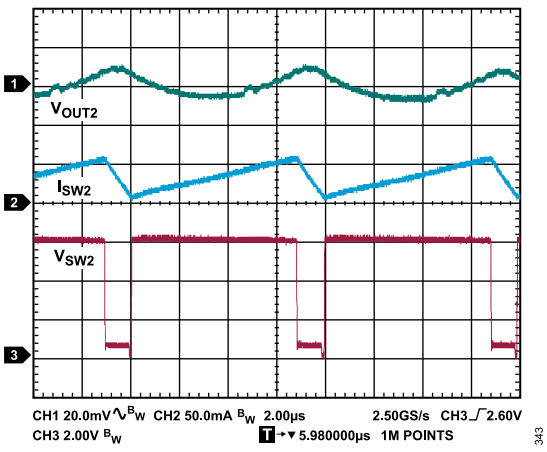

Figure 43. Buck Regulator Continuous Conduction Mode Operation Showing Inductor Current 2 (I_{SW2}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 6 V, V_{OUT2} = 5 V, I_{OUT2} = 30 mA

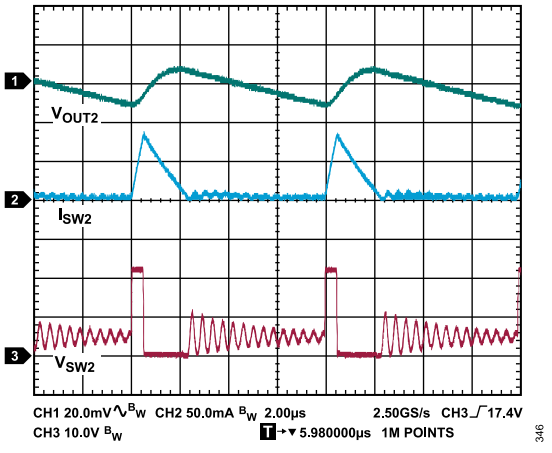

Figure 46. Buck Regulator Discontinuous Conduction Mode Operation Showing I_{SW2}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT2} = 5 V, I_{OUT2} = 11 mA

TYPICAL PERFORMANCE CHARACTERISTICS

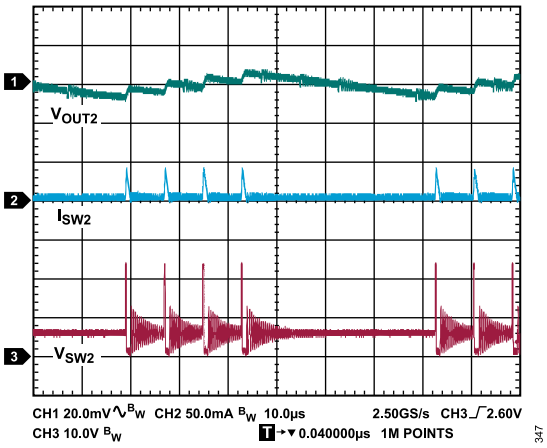

Figure 47. Buck Regulator Pulse Skipping Operation Showing (I_{SW2}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT2} = 5 V, I_{OUT2} = 0.3 mA

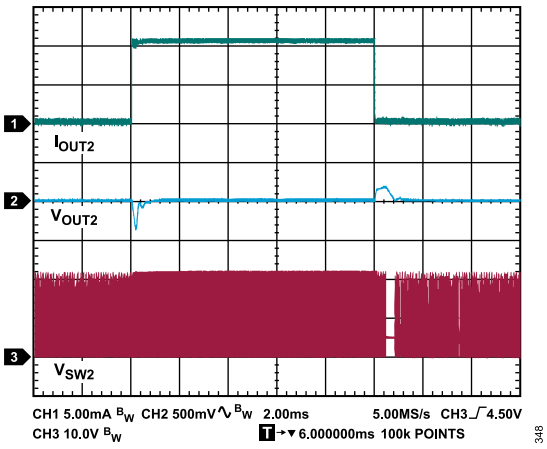

Figure 48. Buck Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5 V, I_{OUT2} = 0.3 mA to 11 mA Step, T_A = 25°C

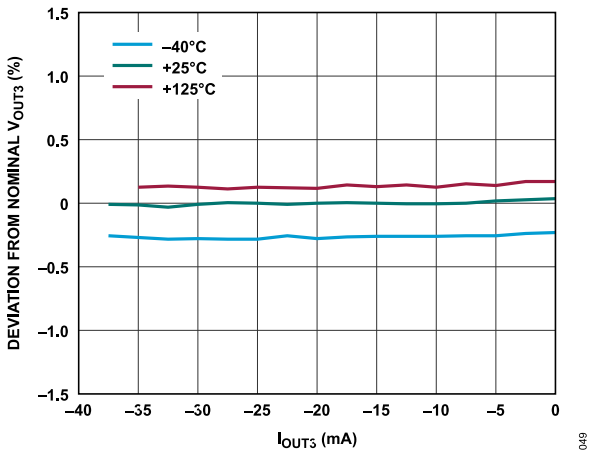

Figure 49. Inverting Regulator Load Regulation Across Temperature, V_{OUT1} = 24 V, V_{OUT3} = −15 V, Nominal = V_{OUT3} at −7 mA I_{OUT3}

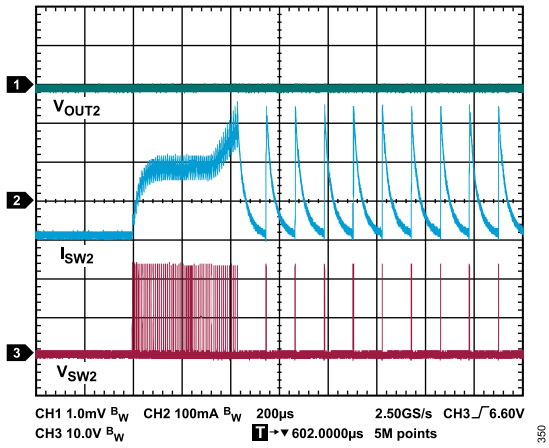

Figure 50. Buck Regulator Short-Circuit Current Limit During Startup, V_{OUT1} = 24 V, V_{OUT2} = SGND2, T_A = 25°C

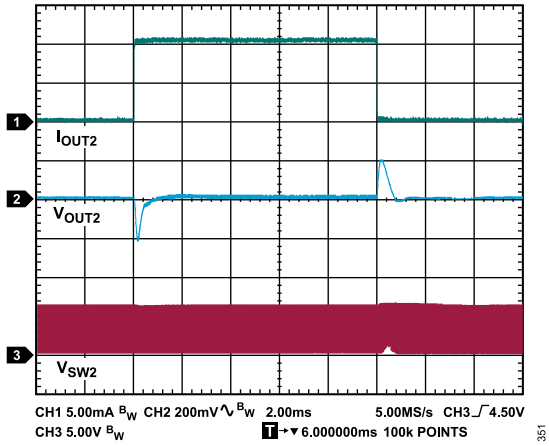

Figure 51. Buck Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 6 V, V_{OUT2} = 5 V, I_{OUT2} = 0.3 mA to 11 mA Step, T_A = 25°C

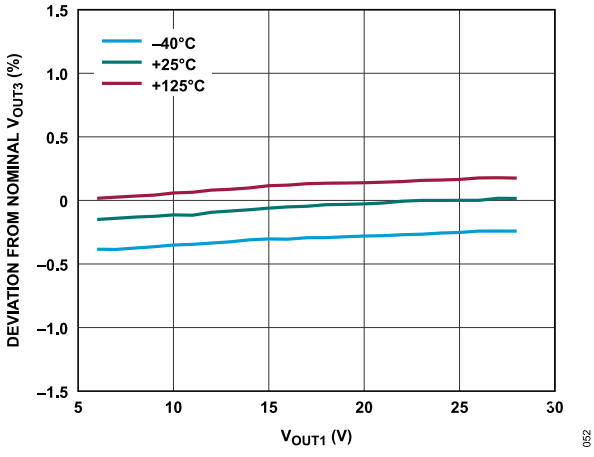

Figure 52. Inverting Regulator Line Regulation Across Temperature, V_{OUT3} = −15 V, I_{OUT3} = −7 mA, Nominal = V_{OUT3} at 24 V V_{OUT1}

TYPICAL PERFORMANCE CHARACTERISTICS

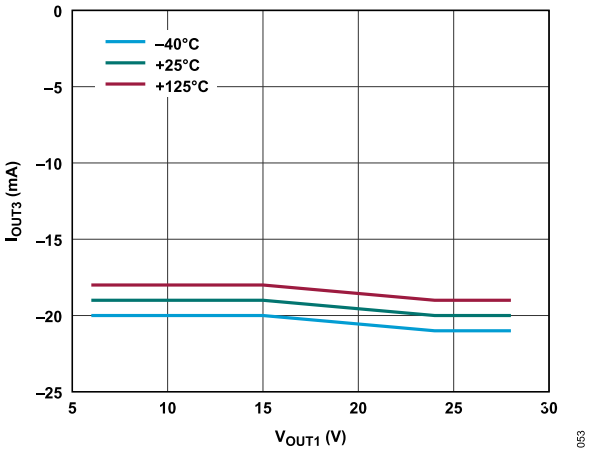

Figure 53. Inverting Regulator Maximum Output Current, V_{VINP} = 24 V, V_{OUT3} = −15 V, I_{OUT1} = 0 mA, I_{OUT2} = 0 mA, Based on Target of 70% $I_{LIM\ (FLYBACK)}$ or $I_{LIM\ (INVERTER)}$, Whichever Comes First

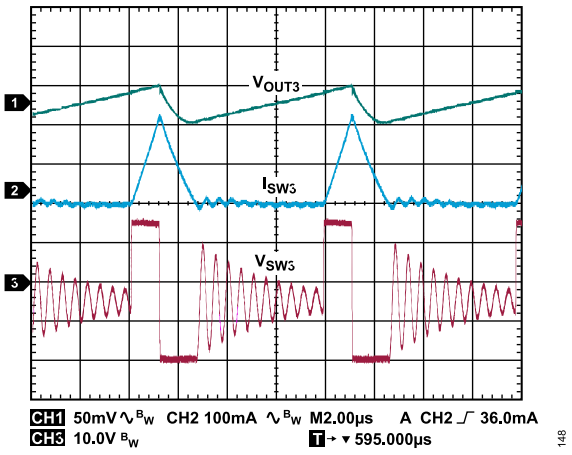

Figure 54. Inverting Regulator Discontinuous Conduction Operation Showing Inductor Current (I_{L3}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT3} = −15 V, I_{OUT3} = −20 mA

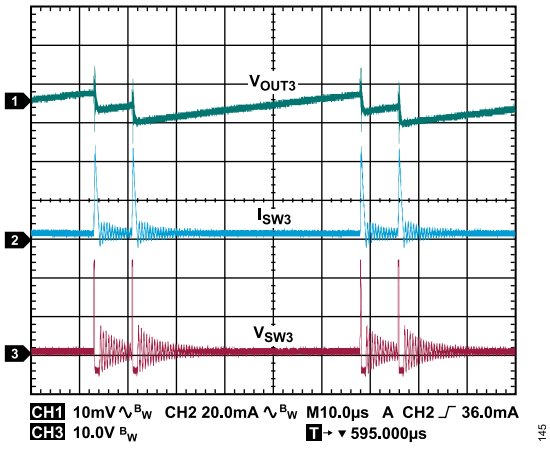

Figure 55. Inverting Regulator Pulse Skipping Operation Showing I_{L3}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT3} = −6 V, I_{OUT3} = −0.3 mA

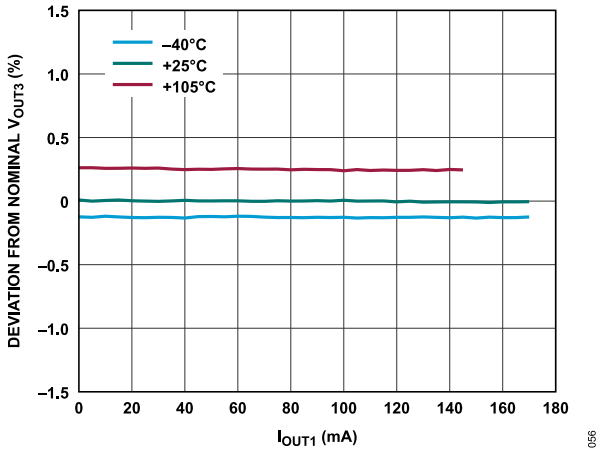

Figure 56. Inverting Regulator Cross Regulation Across Temperature, V_{VINP} = 24 V, V_{OUT3} = −15 V, I_{OUT2} = −4 mA

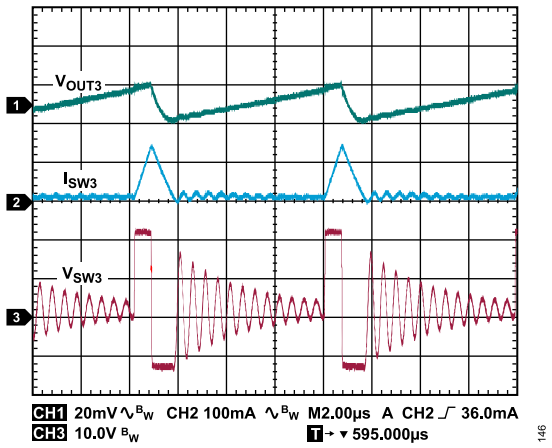

Figure 57. Inverting Regulator Discontinuous Conduction Operation Showing I_{L3}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT3} = −15 V, I_{OUT3} = −7 mA

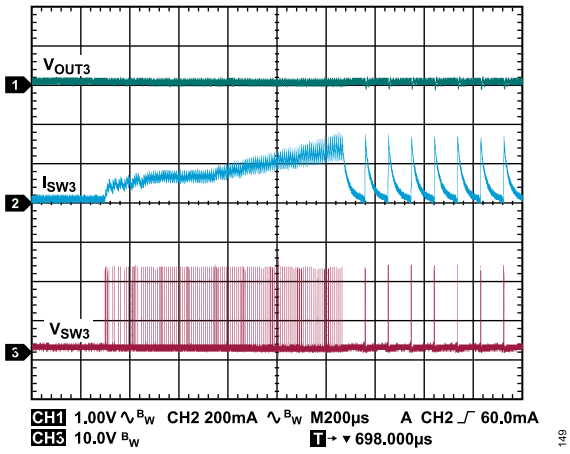

Figure 58. Inverting Regulator Short-Circuit Current Limit During Startup, V_{OUT1} = 24 V, V_{OUT3} = SGND2, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

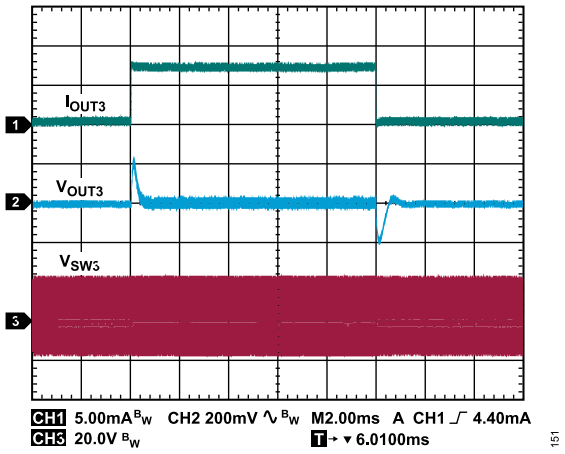

Figure 59. Inverting Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 0 mA, V_{OUT2} = 5 V, I_{OUT2} = 0 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA to −7 mA Step, T_A = 25°C

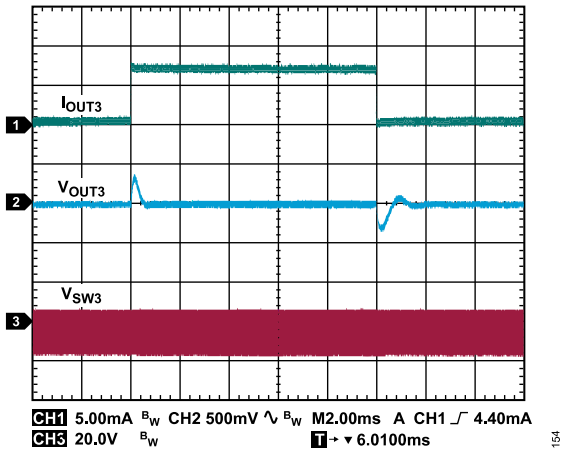

Figure 62. Inverting Regulator Load Transient Response, V_{VINP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 26 mA, V_{OUT2} = 5 V, I_{OUT2} = 11 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA to −7 mA Step, T_A = 25°C

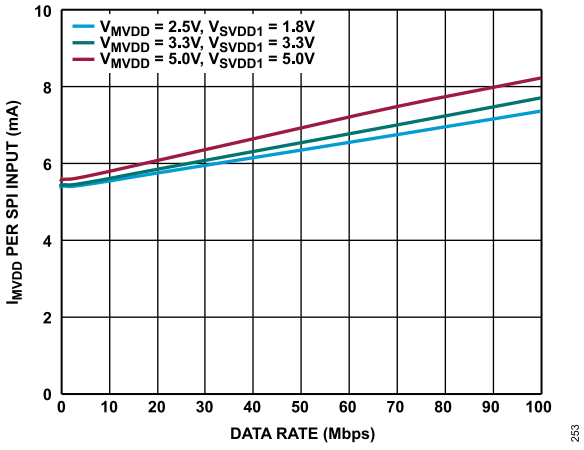

Figure 60. MVDD Supply Current (I_{MVDD}) per SPI Input vs. Data Rate at Various Supply Voltages, $\overline{MSS}$ = Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

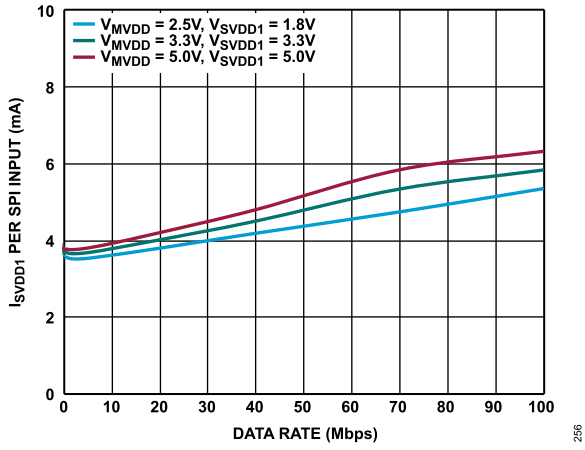

Figure 63. SVDD1 Supply Current (I_{SVDD1}) per SPI Input vs. Data Rate at Various Supply Voltages, $\overline{SSS}$ = Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

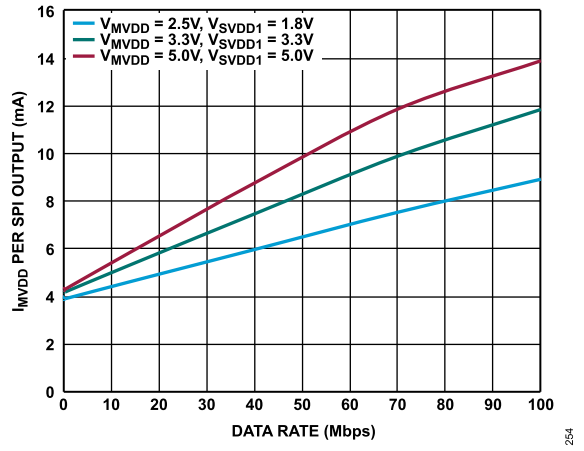

Figure 61. I_{MVDD} per SPI Output vs. Data Rate at Various Supply Voltages, $\overline{MSS}$ = Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

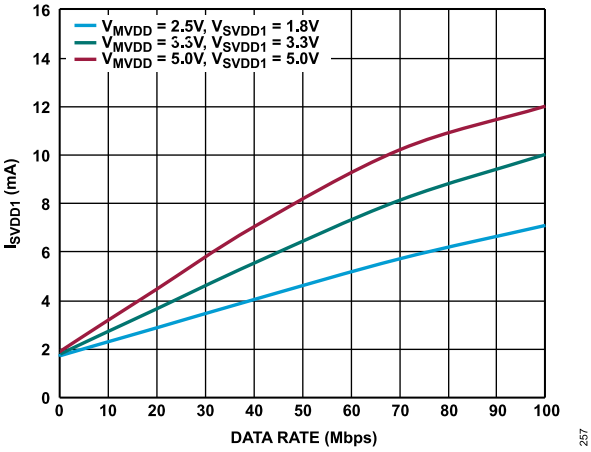

Figure 64. I_{SVDD1} vs. Data Rate at Various Supply Voltages, $\overline{SSS}$ = Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

TYPICAL PERFORMANCE CHARACTERISTICS

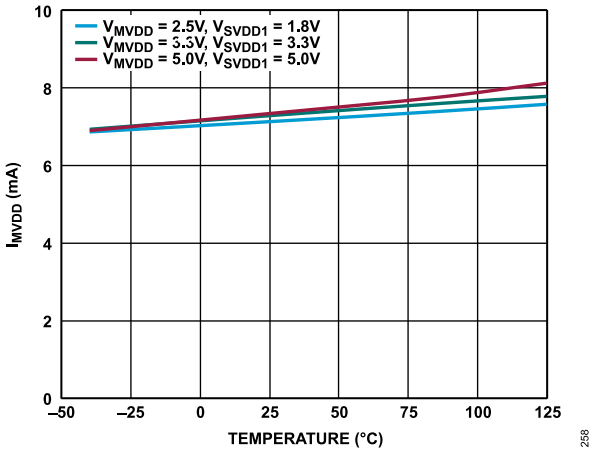

Figure 65. I_{MVDD} vs. Temperature at Various Supply Voltages, $\overline{MSS}$ = Low, Data Rate = 10 Mbps on All SPI Channels

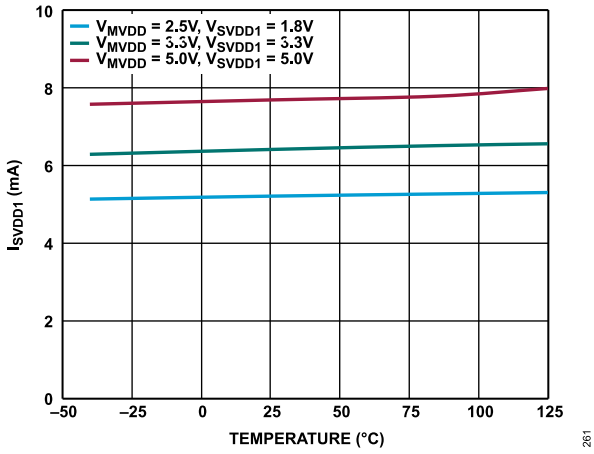

Figure 68. I_{SVDD1} vs. Temperature at Various Supply Voltages, $\overline{SSS}$ = Low, Data Rate = 10 Mbps on All SPI Channels

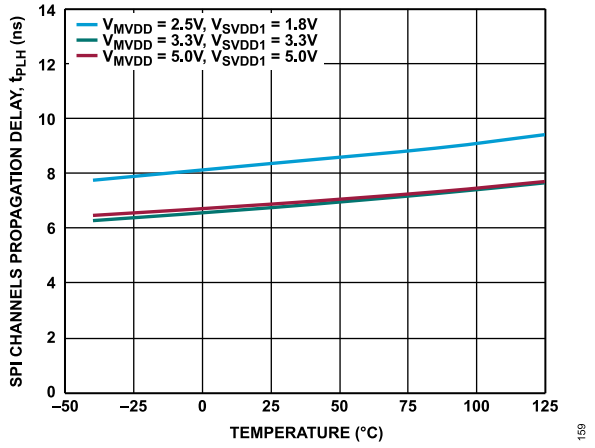

Figure 66. SPI Channels Propagation Delay (t_{PLH}) vs. Temperature at Various Supply Voltages

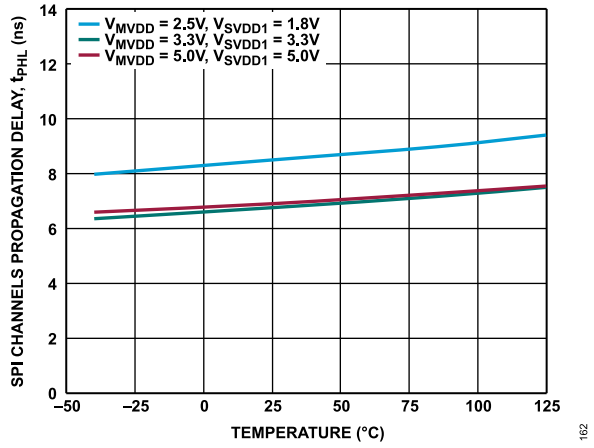

Figure 69. SPI Channels Propagation Delay (t_{PHL}) vs. Temperature at Various Supply Voltages

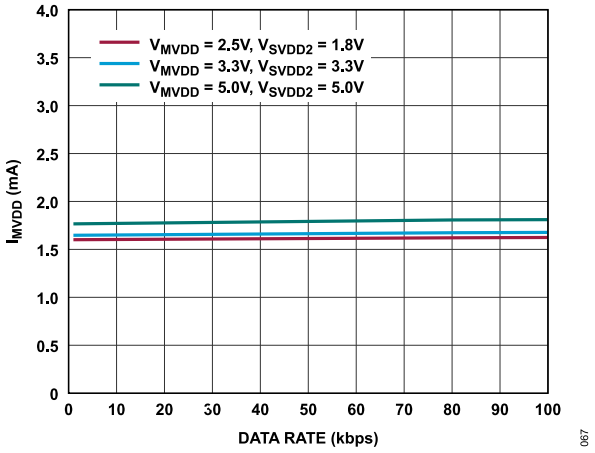

Figure 67. I_{MVDD} vs. Data Rate on All GPIO Channels at Various Supply Voltages, $\overline{MSS}$ = High

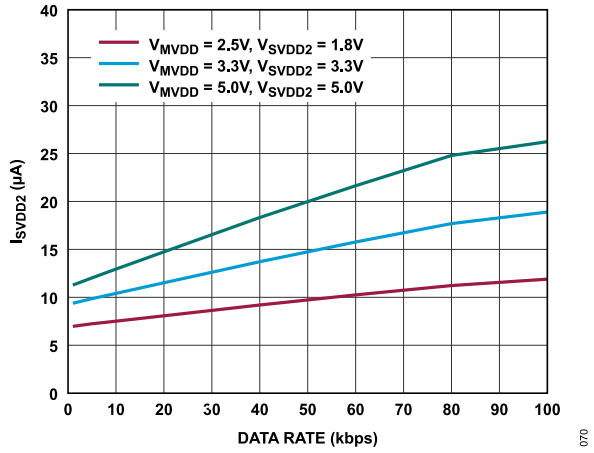

Figure 70. SVDD2 Supply Current (I_{SVDD2}) vs. Data Rate on All GPIO Channels at Various Supply Voltages, $\overline{MSS}$ = High

TYPICAL PERFORMANCE CHARACTERISTICS

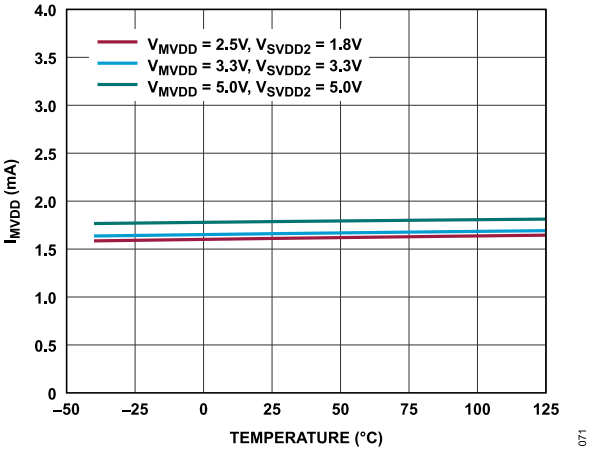

Figure 71. I_{MVDD} vs. Temperature at Various Supply Voltages, $\overline{MSS}$ Is Low, Data Rate = 40 kbps on All GPIO Channels

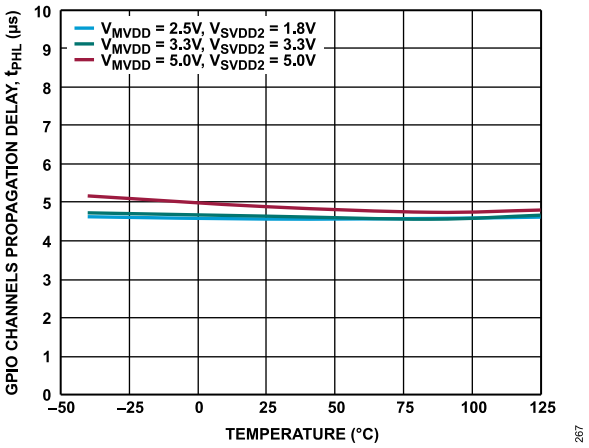

Figure 74. GPIO Channels Propagation Delay (t_{PHL}) vs. Temperature at Various Supply Voltages

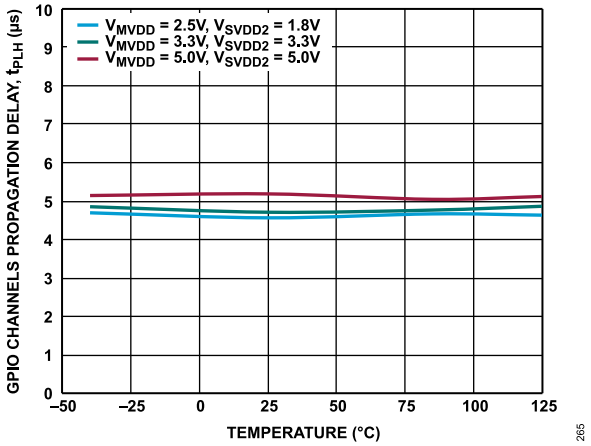

Figure 72. GPIO Channels Propagation Delay (t_{PLH}) vs. Temperature at Various Supply Voltages

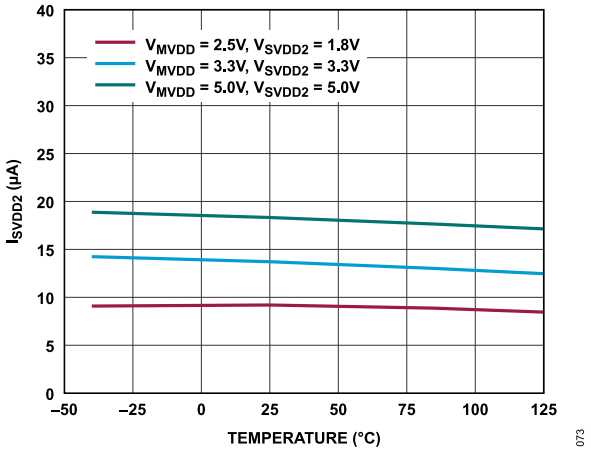

Figure 73. I_{SVDD2} vs. Temperature at Various Supply Voltages, $\overline{SSS}$ = Low, Data Rate = 40 kbps on All GPIO Channels

THEORY OF OPERATION

The ADP1034 is a high performance, isolated micro PMU combining an isolated flyback regulator, an inverting buck boost regulator, and a buck regulator. The ADP1034 provides three isolated power rails and integrates seven low power digital isolators in a 41-lead LFCSP for channel to channel isolated applications where power dissipation and board space are at a premium. Also, a PPC_IN pin is provided for adjusting the V_{OUT1} setting on demand through a serial command.

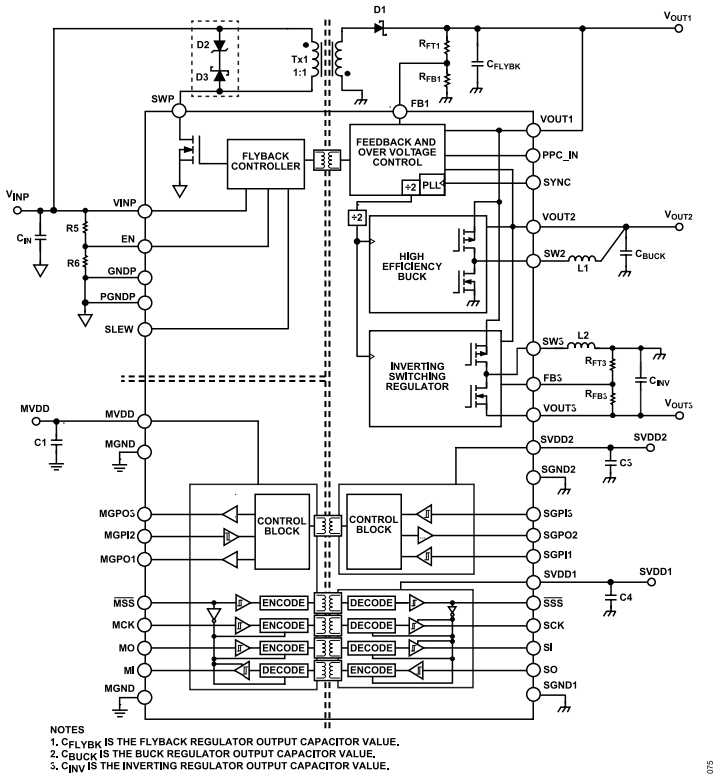

Figure 75. Simplified Block Diagram

THEORY OF OPERATION

FLYBACK REGULATOR

Flyback Regulator Operation

The flyback regulator in the ADP1034 generates an isolated output supply rail that can be programmed from 6 V to 28 V. The flyback regulator adopts current mode control, resulting in a fast inner current controlled loop that regulates the peak inductor current and a slower outer loop via an isolated *i*Coupler channel that adjusts the current controlled loop to define a regulated output voltage. When the high voltage switch is on, the diode on the secondary side of the transformer is reverse biased, which causes an increase in the current in the primary inductance of the transformer, and is stored as magnetic energy. When the switch turns off, the diode becomes forward biased and energy stored in the transformer is transferred to the load.

Traditionally, in an isolated flyback regulator, a discrete optocoupler is used in the feedback path to transmit the signal from the secondary side to the primary side. However, the current transfer ratio (CTR) of the optocouplers degrades over time and over temperature. Therefore, the optocoupler must be replaced every 5 years to 10 years. The ADP1034 eliminates the use of an optocoupler and the associated problems by integrating Analog Devices *i*Coupler technology for feedback, thus reducing system cost, PCB area, and complexity while improving system reliability without the issue of CTR degradation.

A flyback transformer with a single primary and secondary winding is used. This configuration is possible because *i*Coupler technology is used to send an isolated control signal to the primary side controller so that a primary sense winding is not required. In addition, because the secondary and tertiary rails are generated using high efficiency switching regulators, extra secondary windings are not required. This approach offers a number of advantages over an alternative multiwinding solution, such as the following:

- A smaller transformer solution size due to a lower number of turns required on the core and fewer pins.
- Each output can be independently set—the multitap approach requires a custom multitap transformer for different output voltage combinations.
- Outputs are more accurate because the outputs do not rely on the discrete ratios between the transformer windings.
- Output accuracy is unaffected by load changes on each rail.

Power Saving Mode (PSM)

During light load operation, the regulators can skip pulses to maintain output voltage regulation. Therefore, no minimum load is required. Skipping pulses increases the device efficiency but results in larger output ripple.

Flyback Undervoltage Lockout (UVLO)

The UVLO circuitry monitors the VINP pin voltage level. If the input voltage drops below the $V_{UVLO\_FLYBACK\ (FALL)}$ threshold, the flyback regulator turns off. After the VINP pin voltage rises above the $V_{UVLO\_FLYBACK\ (RISE)}$ threshold, the soft start period initiates, and the flyback regulator enables.

Flyback Regulator Precision Enable Control

The flyback regulator in the ADP1034 features a precision enable circuit with an accurate reference voltage. If the voltage at the EN pin rises above the V_{EN_RISING} threshold, the flyback regulator soft start period initiates, and the regulator enables. If the EN pin voltage falls below the $V_{EN\_RISING} - V_{EN\_HYST}$ threshold, the flyback regulator turns off.

Flyback Regulator Soft Start

The flyback regulator includes a soft start function that limits the inrush current from the supply and ramps up the output voltage in a controlled manner. The flyback regulator soft start period initiates when the voltage at the EN pin rises above the V_{EN_RISING} threshold.

Flyback Slew Rate Control

The flyback regulator employs programmable output driver slew rate control circuitry. This circuitry adjusts the slew rate of the switching node, as shown in Figure 76, where lower EMI and reduced ringing can be achieved at slightly lower efficiency operation and vice versa. To program the slew rate, connect the SLEW pin to the VINP pin for normal mode, to the GNDP pin for slow mode, or leave it open for fast mode.

Note that slew rate control causes a trade-off between efficiency and low EMI.

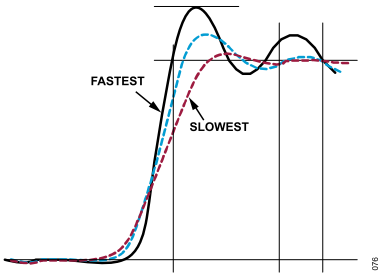

Figure 76. Switching Node at Various Slew Rate Settings

Table 12. Slew Rate Settings

SLEW Pin Connection	Slew Rate	Comment
GNDP	Slow	Lowest EMI
VINP	Normal	Optimized efficiency and EMI
Unconnected	Fast	Highest efficiency

THEORY OF OPERATION

Flyback Regulator Overcurrent Protection

The flyback regulator features a current-limit function that senses the forward current in the switching metal-oxide semiconductor field effect transistor (MOSFET) on a cycle by cycle basis. If the current exceeds the $I_{LIM\ (FLYBACK)}$ threshold, the switch turns off.

Flyback Regulator Overvoltage Protection (OVP)

The flyback regulator of the ADP1034 implements a number of OVP methods to detect and prevent an overvoltage condition on the flyback regulator output, such as the following:

- If the voltage on the FB1 pin exceeds V_{FB1} by 10% for the adjustable output version, an OVP fault is detected, which prevents the flyback regulator switch from turning on. The flyback regulator primary switch stays off until the OVP condition is no longer present.
- If communication across the isolation barrier from the secondary controller to the primary controller fails, the flyback regulator shuts down and a new soft start power-up cycle initiates.
- If the voltage on the output of the flyback regulator exceeds the severe overvoltage threshold ($SOVP_{FLYBACK}$), the primary controller does not turn on the primary side switch. The flyback regulator primary switch stays off until the voltage on the VOUT1 pin falls below the $SOVP_{FLYBACK} - SOVP_{FLYBACK\_HYST}$ threshold.

Flyback Programmable Power Control (PPC)

A PPC_IN pin is provided to allow communications between the ADP1034 and a microcontroller unit (MCU) for adjusting the ADP1034 feedback voltage of the flyback regulator (V_{FB1}) through a serial command. The ADP1034 uses an exclusive, proprietary intellectual property 1-wire serial interface protocol. This communications protocol is designed such that an MCU (or a companion product) acts as the master while the ADP1034 acts as the slave when configuring the output settings of the flyback regulator. The MCU actively determines if the power needs of its load changes before triggering an on demand request to the ADP1034 to adjust its output voltage to meet the power needs of the load.

During startup and when programming the flyback output (V_{OUT1}) below 4.5 V, the PPC interface puts the flyback regulator in its default state of PPC Code 251. PPC Code 252 to Code 255 are reserved for factory trimming purposes and are clamped to Code 251 when written.

1-Wire Serial Interface

PPC is implemented via a 1-wire serial interface in the ADP1034. An OWSI transaction requires several elements, as shown in Figure 77. The OWSI frame is broken into bit periods. Each start event, data bit, and acknowledge bit occur within a bit period, and each timing specification is defined from the start of that bit period.

A start sequence is defined by two successive rising edge pulses. After the start command is transmitted, 16 data bits follow to make up the address (default = 000), data, and CRC bits (MSB first). Finally, an acknowledge sequence is required from the slave. The acknowledge is composed of two bits: an acknowledge bit (ACK in Figure 77) and a parity bit.

The MCU pulls the 1-wire serial interface bus high at the start of the acknowledge and parity bit periods. The 1-wire serial interface bus is sampled by the MCU for a fixed time during the acknowledge and parity bit periods. At this time, the slave may drive the bus low. If the slave does not pull the bus low, the MCU drives low later in the acknowledge and parity bit periods. Refer to Figure 2 for a detailed view of the 1-wire serial interface timing and Table 2 for the appropriate timing specifications.

In a successful transaction, the slave remains high during the acknowledge bit period and drives the bus low during the parity bit period. In an unsuccessful transaction, the slave drives the bus low during the acknowledge bit and remains high during the parity bit period.

1-Wire Serial Interface CRC

To ensure that data is received correctly in noisy environments, a cyclic redundancy check (CRC) is implemented in the 1-wire serial interface. This CRC is based on a 5-bit frame with the check sequence using the following polynomial:

$$C(x) = x^5 + x^2 + 1$$

This 5-bit frame check sequence is added to the end of the 11-bit data-word, and the full 16-bit word is sent by the MCU to the ADP1034. Then the MCU expects an acknowledge sequence from the ADP1034. If the corresponding CRC check on the ADP1034 is valid, the ADP1034 responds with an acknowledge sequence, which means that a write was completed. Then, the flyback output, V_{OUT1}, of the ADP1034 is adjusted according to the 8-bit data written. If the CRC on the ADP1034 is not valid, the no acknowledge sequence is issued, and the data is ignored. Then, the flyback output, V_{OUT1}, does not change.

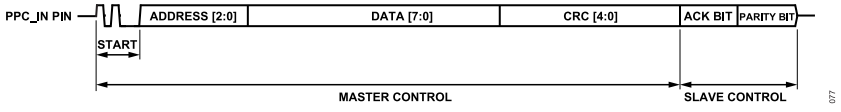

Figure 77. 1-Wire Serial Interface Write with Acknowledge

THEORY OF OPERATION

BUCK REGULATOR

Buck Regulator Operation

The step down dc-to-dc (or buck) regulator in the ADP1034 uses a current mode controlled scheme, operating at a fixed frequency set by an internal oscillator. Current mode uses a fast inner current controlled loop to regulate peak inductor current and a slower outer loop to adjust the current loop to regulate the output voltage. At the start of each oscillator cycle, the high-side MOSFET switch turns on, applying the input voltage to one end of the inductor. The voltage across the inductor causes the buck regulator inductor current (I_{L_BUCK}) to increase until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch. The error amplifier output sets this threshold. During the high-side MOSFET off time, the inductor current declines through the low-side MOSFET switch until either the next oscillator clock pulse starts a new cycle that results in continuous conduction mode (CCM) operation, or the inductor current reaches zero. The low-side MOSFET switch turns off, and the control system waits for the next oscillator clock pulse to start a new cycle, resulting in discontinuous mode (DCM) operation. Under light load conditions, the regulator can skip pulses to maintain regulation and increase power conversion efficiency.

Buck Regulator UVLO

The step down regulator of theADP1034 features an internal undervoltage lockout circuit that monitors the input voltage to the regulator or VOUT1. If the voltage at VOUT1 drops below the internal threshold level of 4.5 V, the regulator turns off. If the output at VOUT1 rises above the internal threshold, the regulator soft start period initiates, and the regulator enables.

Buck Regulator Soft Start

The step down regulator in the ADP1034 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current.

Buck Regulator Current-Limit Protection

The step down regulator in the ADP1034 includes a current-limit protection circuit to limit the amount of forward current through the high-side MOSFET switch. The inductor peak current is monitored cycle by cycle to detect an overload condition. When the overload condition occurs, the current-limit protection limits the peak inductor current to $I_{LIM\ (BUCK)}$, resulting in a drop in the output voltage.

Buck Regulator OVP

The step down regulator of the ADP1034 features an OVP circuit that monitors the output voltage. If the voltage on the VOUT2 pin exceeds the nominal output voltage by 10%, the step down, dc-to-dc regulator stops switching until the voltage falls below the threshold again.

Buck Regulator Active Pull-Down Resistor

The buck regulator has an active pull-down resistor that discharges the output capacitor when the output of VOUT1 is between 1.23 V and 4.5 V. The pull-down resistor connects between VOUT2 and SGND2.

INVERTING REGULATOR

Inverting Regulator Operation

The inverting dc-to-dc regulator in the ADP1034 uses a current mode controlled scheme, operating at a fixed frequency set by an internal oscillator. Current mode uses a fast inner current controlled loop to regulate the peak inductor current and a slower outer loop to adjust the current loop to regulate the output voltage. At the start of each oscillator cycle, the high-side MOSFET switch turns on, applying the input voltage to one end of the inductor, which normally causes the inverting regulator inductor current ($I_{INV\_INDUCTOR}$) to increase until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch. The error amplifier output sets this threshold. During the high-side MOSFET off time, the inductor current declines through the low-side MOSFET switch until one of the following occurs:

- The next oscillator clock pulse starts a new cycle, which results in CCM operation.
- The inductor current reaches zero, the low-side MOSFET switch is turned off, and the control system waits for the next oscillator clock pulse to start a new cycle, resulting in DCM operation.

Under light load conditions, the regulator can skip pulses to maintain regulation and increase power conversion efficiency.

Inverting Regulator UVLO

The inverting dc-to-dc regulator of the ADP1034 features an internal UVLO circuit that monitors the input voltage to the regulator or the VOUT1. If the voltage at VOUT1 drops below the internal threshold level of 4.5 V, the regulator turns off. If the output of VOUT1 rises above the internal threshold, the regulator soft start period initiates, and the regulator enables.

Inverting Regulator Soft Start

The inverting, dc-to-dc regulator in the ADP1034 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current.

Inverting Regulator Current-Limit Protection

The inverting dc-to-dc regulator in the ADP1034 includes a current-limit protection circuit to limit the amount of forward current through the high-side MOSFET switch. The inductor peak current is monitored cycle by cycle to detect an overload condition. When the overload condition occurs, the current-limit protection limits the

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peak inductor current to $I_{LIM\ (INVERTER)}$, resulting in a drop in the output voltage.

Inverting Regulator OVP

The inverting, dc-to-dc regulator of the ADP1034 features an OVP circuit that monitors the voltage on the FB3 pin. If the voltage on this pin falls below V_{FB3} by 10%, the inverting regulator stops switching until the voltage rises above the threshold again.

Inverting Regulator Active Pull-Down Resistor

The inverting regulator has an active pull-down resistor that discharges the output capacitor when the output of VOUT1 is between 1.23 V and 4.5 V. The pull-down resistor connects between VOUT3 and SGND2.

POWER-UP SEQUENCE

The power-up sequence is shown in Figure 78.

1. The flyback regulator powers up first.
2. When V_{OUT1} rises above 90% of the target V_{OUT1}, the buck regulator turns on.
3. When the buck regulator output (V_{OUT2}) rises above 90% of the target V_{OUT2}, the inverting regulator turns on.

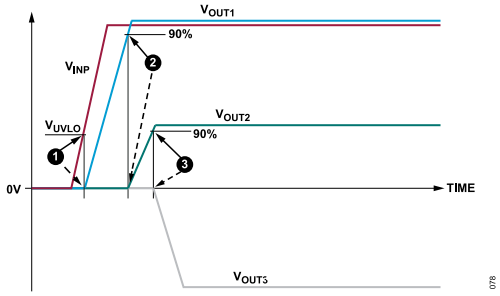

Figure 78. Power-Up Sequencing

OSCILLATOR AND SYNCHRONIZATION

A phase-locked loop (PLL)-based oscillator generates the internal clock for the flyback, buck, and inverter regulators, and offers an internally generated frequency or external clock synchronization. Connect the SYNC pin as described in Table 13 to configure the switching frequency, f_{SW}. For external synchronization, connect the SYNC pin to a suitable clock source. The PLL locks to an input clock within the range specified by f_{SYNC}.

Table 13. SYNC Pin Functionality

SYNC Pin State and Frequency	Flyback f_{SW}	Buck f_{SW}	Inverter f_{SW}
SYNC Pin State: Low or High	250 kHz	125 kHz	125 kHz
f_{SYNC}: 350 kHz to 750 kHz	f_{SYNC} ÷ 2	f_{SYNC} ÷ 4	f_{SYNC} ÷ 4

THERMAL SHUTDOWN

If the ADP1034 junction temperature rises above T_{SHDN}, the thermal shutdown circuit turns the flyback regulator off. Extreme junction temperatures can be the result of prolonged high current operation, poor circuit board design, and/or high ambient temperatures. When thermal shutdown occurs, hysteresis is included so that the ADP1034 does not return to operation until the on-chip temperature drops below $T_{SHDN} - T_{HYS}$. When resuming from thermal shutdown, the ADP1034 performs a soft start.

DATA ISOLATION

High Speed SPI Channels

The ADP1034 has four high speed channels. The first three, CLK, MI/SO, and MO/SI (the slash indicates the connection of the input and output, forming a datapath across the isolator that corresponds to an SPI bus signal) are optimized for low propagation delay. With a maximum propagation delay of 15 ns, the ADP1034 supports read and write clock rates up to 16.6 MHz in the standard 4-wire SPI. However, the total round trip delay of the system determines the maximum clock rate and is less than that value.

The relationship between the SPI signal paths, the ADP1034 pin mnemonics, and the data directions are detailed in Table 14.

Table 14. Relationship Between Pin Mnemonics and SPI Signal Path Names

SPI Signal Path	Master Side	Data Direction	Slave Side
Clock (CLK)	MCK	→	SCK
MO/SI	MO	→	SI
MI/SO	MI	←	SO
Slave Select Bar ($\overline{SS}$)	$\overline{MSS}$	→	$\overline{SSS}$

The datapaths are SPI mode agnostic. The CLK and MO/SI SPI datapaths are optimized for propagation delay and channel to channel matching. The MI/SO SPI datapath is optimized for propagation delay. The device does not synchronize to the clock channels. Therefore, there are no constraints on the clock polarity or timing with respect to the data lines.

$\overline{SS}$ is an active low signal. To save power in a multichannel system, $\overline{SS}$ puts the other SPI isolator channels in a low power state when the channels are not in use ($\overline{SS}$ = high), and these channels are only active when required, which is when $\overline{SS}$ is low. The clock and data channels are gated to the $\overline{SS}$ as shown in Figure 79. However, this power saving mode adds 100 ns of latency. This latency is the time required for the internal circuitry to wake up from the low power state and to start transmitting data to the isolation barrier. Conversely, the latency is the delay from the falling edge of $\overline{MSS}$ to the first clock edge or data edge that appears on the slave side, as shown in Figure 80.

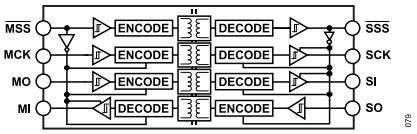

Figure 79. iCoupler Gating

THEORY OF OPERATION

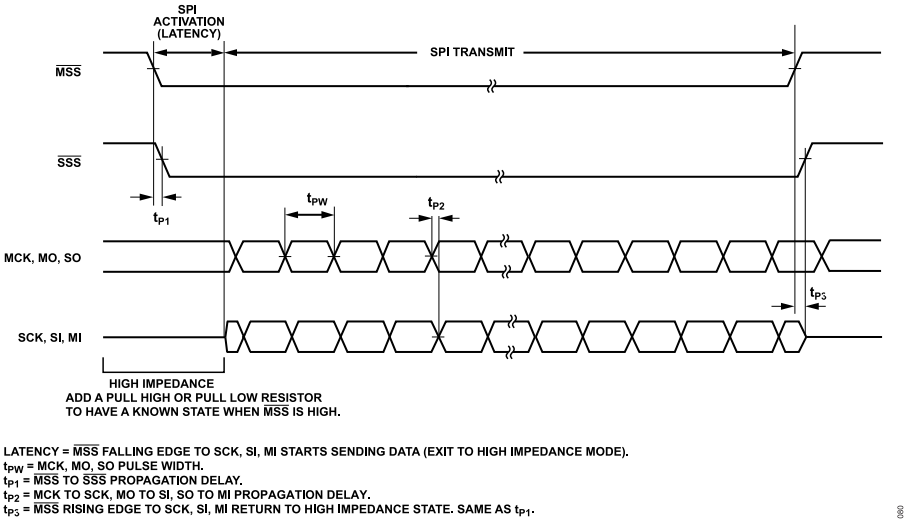

Figure 80. SPI Isolators Timing Diagram

The MI, SCK, and SI outputs are also tristated when $\overline{MSS}$ is high (see Table 15) to allow a more flexible design and to avoid the requirement for external multiplexing of MI in a multichannel system. Figure 81 shows how the SPI busses from multiple ADP1034 devices can be connected together.

Table 15. SPI $\overline{MSS}$ Gating

Parameter	$\overline{MSS}$ High	$\overline{MSS}$ Low
$\overline{SSS}$	High	Low
SCK	Tristate	MCK
SI	Tristate	MO
MI	Tristate	SO

Connect a pull-up or pull-down resistor to MI, SCK, and SI to pull these pins to the desired logic state when $\overline{MSS}$ is high.

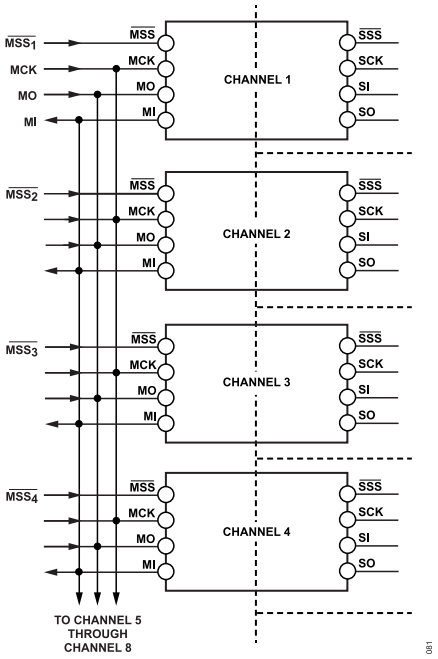

Figure 81. Multichannel SPI Muxing Scheme

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GPIO Data Channels

The general-purpose data channels are provided as space-saving isolated datapaths where timing is not critical. The dc values of all low speed general-purpose inputs on a given side of the device are sampled simultaneously, packetized, and shifted across a single isolation coil. The process is then reversed by reading the inputs on the opposite side of the device, packetizing the inputs and sending these inputs back for similar processing. Because of the sampled nature of this process, the general-purpose data channels exhibit a sampling uncertainty that resembles 10 µs of peak jitter.

For proper operation of the GPIO channels, refer to Table 16. Power both MVDD and SVDD2 within the specified input voltage range for these pins.

Table 16. Truth Table for GPIO Channels

MVDD State	SVDD2 State	xGPIx	MGPOx	SGPOx	Test Conditions/Comments
Unpowered	Powered	Don't care	Low	Low	During startup
Powered	Unpowered	Don't care	Low	Low	During startup
Powered	Powered	High	High	High	Normal operation
Powered	Powered	Low	Low	Low	Normal operation
Powered	Powered to Unpowered	Don't care	Hold	Low	Hold means that the current state of the outputs are preserved
Powered to Unpowered	Powered	Don't care	Low	Hold	Hold means that the current state of the outputs are preserved

APPLICATIONS INFORMATION

COMPONENT SELECTION

Feedback Resistors

The ADP1034 provides an adjustable output voltage for both flyback and inverting regulators. An external resistor divider sets the output voltages for V_{OUT1} and V_{OUT3}. To limit the output voltage accuracy degradation due to the feedback bias current, ensure that the current through the divider is at least 10 times I_{FB1} or I_{FB3}. The recommended R_{FB1} and R_{FB3} values are in the range of 50 kΩ to 250 kΩ to minimize the output voltage error due to the bias current and to lessen the power dissipation across the feedback resistors.

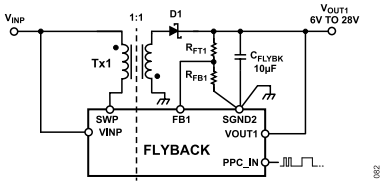

Figure 82. Flyback Regulator Output Voltage Setting

Set the maximum output for the flyback regulator by

$$V_{OUT1\_MAX} = 252/256 \times V_{FB1} \times (1 + (R_{FT1}/R_{FB1}))$$

where:
V_{OUT1_MAX} is the maximum flyback output voltage.
V_{FB1} is the flyback feedback voltage.
R_{FT1} is the feedback resistor from VOUT1 to FB1.
R_{FB1} is the feedback resistor from FB1 to SGND2.

Table 17. Recommended Feedback Resistor Values for Flyback Regulator

	Flyback Regulator		
Maximum V_{OUT1} (V)	R_{FT1} (MΩ)	R_{FB1} (kΩ)	Calculated V_{OUT1_MAX} (V)
12	1.5	105	12.037
15	2.05	113	15.074
24	3.48	118	24.012
28	3.3	95.3	28.056

Calculate the desired V_{OUT1_PPC} for PPC code by

$$V_{OUT1\_PPC} = ((PPC_{CODE} + 1)/252) \times V_{OUT1\_MAX}$$

where:
PPC_{CODE} is the PPC data that corresponds to the desired flyback output voltage, V_{OUT1_PPC}.
V_{OUT1_PPC} is the target flyback output voltage through PPC programming.

The LSB size for the V_{OUT1_PPC} is calculated by

$$V_{OUT1\_PPC\_LSB} = V_{OUT1\_MAX}/252$$

Code 251 is the maximum PPC code that corresponds to the maximum V_{OUT1}. PPC Code 252 to Code 255 are reserved for factory trimming purposes and is clipped to Code 251 when written through PPC programming. Figure 83 shows the V_{OUT1} output vs. PPC_{CODE}.

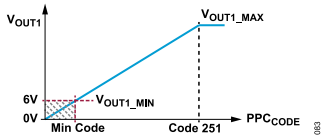

Figure 83. V_{OUT1} Output vs. PPC_{CODE}

The secondary side circuitry is supplied from V_{OUT1} with a minimum allowable V_{OUT1} level of 6 V. Avoid programming the V_{OUT1} lower than 6 V because doing so may cause the regulators to reset. Figure 84 shows the output response after programming PPC to 4 V.

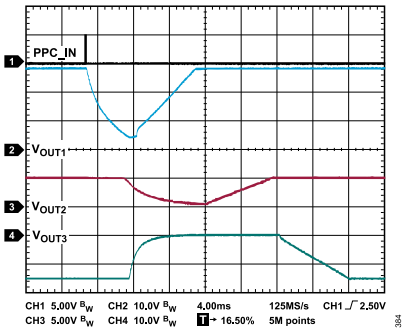

Figure 84. Output Response After Programming PPC to 4 V

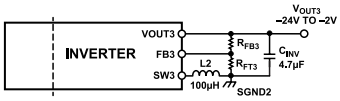

Figure 85. Inverting Regulator Output Voltage Setting

Set the negative output for the inverting regulator by

$$V_{OUT3} = V_{FB3} \times (1 + (R_{FT3}/R_{FB3}))$$

where:
V_{OUT3} is the inverting regulator output voltage (negative sign disregarded).
V_{FB3} is the inverting regulator feedback voltage in reference to VOUT3.
R_{FT3} is the feedback resistor from FB3 to SGND2.
R_{FB3} is the feedback resistor from VOUT3 to FB3.

As with the flyback regulator, calculate the value of the top resistor for the target V_{OUT3} by the following equation:

$$R_{FT3} = R_{FB3} \times ((V_{OUT3}/V_{FB3}) - 1)$$

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Table 18. Recommended Feedback Resistor Values for Inverting Regulator

	Inverting Regulator		
Target V_{OUT3} (V)	R_{FT3} (MΩ)	R_{FB3} (kΩ)	Calculated V_{OUT3} (V)
−2	0.130	86.6	−2.000
−6	0.715	110	−6.000
−9	1.24	121	−8.998
−12	1.54	110	−12.000
−15	2.15	121	−15.015
−24	3.48	120	−24.000

Capacitor Selection

Higher output capacitor values reduce the output voltage ripple and improve the load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with voltage ratings of 25 V to 50 V (depending on output) are recommended for optimal performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Calculate the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage using the following equation:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - Tempco) \times (1 - DCBIASCO) \times (1 - Tolerance)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal capacitance shown in the capacitor data sheet.
Tempco is the worst case capacitor temperature coefficient.
DCBIASCO is the dc bias coefficient derating at the output voltage.
Tolerance is the worst case component tolerance.

To guarantee the performance of the device, it is imperative to evaluate the effects of dc bias, temperature, and tolerances on the behavior of the capacitors for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize voltage ripple.

FLYBACK REGULATOR COMPONENTS SELECTION

Input Capacitor

An input capacitor must be placed between the VINP pin and ground. Ceramic capacitors greater than or equal to 4.7 µF over temperature and voltage are recommended. The input capacitor reduces the input voltage ripple caused by the switching current. Place the input capacitor as close as possible to the VINP and PGNDP pins to reduce input voltage spikes. The voltage rating of the input capacitor must be greater than the maximum input voltage.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias. A 10 µF capacitor is recommended as a balance between performance and size.

Ripple Current vs. Capacitor Value

The output capacitor value must be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Use the following equation to calculate the output capacitance:

$$C_{OUT} = (L_{PRI} \times I_{SWP}^2)/(2 \times V_{OUT1} \times \Delta V_{OUT1})$$

where:
C_{OUT} is the capacitance of the flyback output capacitor.
L_{PRI} is the primary inductance of the transformer.
I_{SWP} is the peak switch current.
V_{OUT1} is the flyback regulator output voltage.
ΔV_{OUT1} is the allowable flyback regulator output ripple.

Schottky Diode

A Schottky diode with low junction capacitance is recommended for D1. At higher output voltages and especially at higher switching frequencies, the junction capacitance is a significant contributor to efficiency. Choose an output diode with a forward current rating (I_F) that is greater than the maximum load requirement and with a reverse voltage rating (V_R) that is greater than the summation of the maximum supply voltage (V_{VINP_MAX}) and the maximum output voltage (V_{OUT1_MAX}).

Transformer

The transformer used with the ADP1034 is an important component within the system, in terms of efficiency and maximum output power capability. Analog Devices worked with a number of leading magnetic component suppliers to develop transformer designs for use with the ADP1034. These designs are listed in Table 19. A number of factors must be taken into account when designing a transformer for use with the ADP1034.

Turn Ratio

The ADP1034 requires the use of a transformer with a primary to secondary turn ratio of 1:1 to start up properly.

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Primary Inductance

The ADP1034 operates with a transformer with an inductance in the 80 µH to 560 µH range. However, it is recommended to choose an inductance value that results in the flyback output voltage (V_{OUT1}) divided by the transformer primary inductance being less than or equal to 140,000 to maintain control loop stability.

$$V_{OUT1}/L_{PRI} \leq 140{,}000$$

where:
V_{OUT1} is the flyback regulator output voltage.
L_{PRI} is the primary side inductance of the transformer.

Using a transformer at the lower end of the inductance range may result in a smaller transformer but also reduces the output power capabilities due to larger ac ripple current through the transformer. Conversely, operating at a higher inductance can result in higher output power at the expense of a potentially larger transformer.

Flyback Transformer Saturation Current

Do not exceed the saturation current of the transformer in operation or much higher losses and overall lower system efficiency may result. Choose a transformer with a saturation current rating that is greater than the expected peak switch current (I_{SWP}) across line and load conditions.

Series Winding Resistance

In power loss sensitive applications, keep the series resistance of the primary and secondary windings as low as possible to improve overall efficiency.

Leakage Inductance and Clamping Circuits

When choosing a transformer to operate with the ADP1034, minimize transformer leakage inductance. Leakage inductance causes a voltage spike to appear on the SWP node when the flyback regulator switch is off due to energy storage in the leakage inductance that is not transferred to the output. The voltage spike is more prominent at higher load currents and increases with higher leakage inductance. It is important to keep the voltage spikes lower than the voltage rating of the flyback switch that drives the SWP pin. Margin must be built into any design to avoid exceeding this limit if no clamp or snubber circuit is used to protect the flyback switch.

To estimate the leading voltage spike at the SWP pin when the switch turns off, use the following equation:

$$V_{PEAK} = I_{PEAK} \times (L_{LEAK}/(C_P + C_{SWP}))^{1/2} + V_{VINP} + V_{OUT1} + V_D$$

where:
V_{PEAK} is the voltage spike amplitude.
I_{PEAK} is the peak current on the flyback switch.
L_{LEAK} is the leakage inductance of the transformer.
C_P is the parasitic capacitance of the transformer.
C_{SWP} is the capacitance on the flyback switch.
V_{VINP} is the input supply voltage.
V_{OUT1} is the output voltage of the flyback regulator.
V_D is the forward voltage drop across the rectifier diode.

A snubber or clamp circuit can protect the flyback switch for cases where the leakage inductance is too high for application conditions. Two common types of a clamping circuit are the resistor, capacitor, diode clamp shown in Figure 86 and the diode, Zener diode clamp shown in Figure 87. The resistor, capacitor, diode clamp quickly dampens the voltage spike and provides improved EMI performance, and the diode, Zener diode clamp can be used when the clamping level must be consistent and well defined. The diode, Zener diode clamp has slightly higher power efficiency over the resistor, capacitor, diode clamp. However, the cost of the diode, Zener diode clamp solution is typically higher than the resistor, capacitor, diode clamp solution.

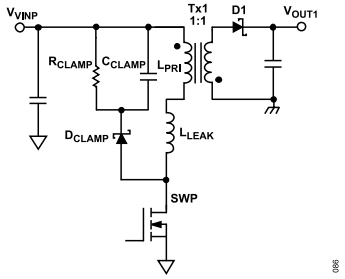

Figure 86. Resistor, Capacitor, Diode Clamp

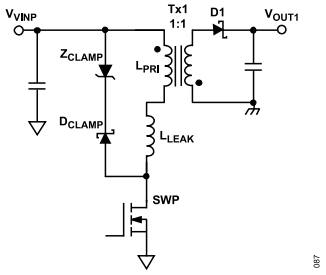

Figure 87. Diode, Zener Diode Clamp

Clamping Resistor

To calculate the clamping resistor (R_{CLAMP}) value, the clamping voltage (V_{CLAMP}) must be determined. The clamping voltage is the voltage on which any voltage spike that occurs on the flyback switch is clamped. Choose a V_{CLAMP} that is lower than the SWP maximum voltage rating (SWP_{VMAX}) specified in the Absolute Maximum Ratings section and is greater than the summation of the maximum input supply (V_{VINP_MAX}) and the maximum flyback output voltage (V_{OUT1_MAX}) of the application as given by

$$SWP_{VMAX} > V_{VINP\_MAX} + V_{CLAMP} > V_{VINP\_MAX} + V_{OUT1\_MAX}$$

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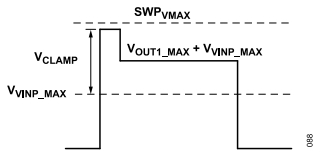

Figure 88. Clamping Waveform

Use the following equation to calculate the value of the clamping resistor for a given V_{CLAMP} value:

$$R_{CLAMP} = (2 \times V_{CLAMP} \times (V_{CLAMP} - V_{OUT1}))/(L_{LEAK} \times I_{PEAK}^2 \times f_{SW})$$

where:
R_{CLAMP} is the value of the clamping resistor.
V_{CLAMP} is the clamping voltage.
V_{OUT1} is the output voltage of the flyback regulator.
L_{LEAK} is the leakage inductance of the transformer.
I_{PEAK} is the peak current on the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.

To calculate the power dissipation across the snubber resistor, use the following equation:

$$P_{RCLAMP} = (V_{CLAMP})^2/(R_{CLAMP})$$

where P_{RCLAMP} is the power dissipation across R_{CLAMP}. Choose R_{CLAMP} with a power rating of about twice the P_{RCLAMP} value to have a margin.

Clamping Capacitor

The clamping capacitor (C_{CLAMP}) is used to minimize the voltage ripple level (V_{RIPPLE}) superimposed in V_{CLAMP}. Calculate the clamping capacitor by using the following equation for the desired V_{RIPPLE} level and the calculated R_{CLAMP}:

$$C_{CLAMP} = V_{CLAMP}/(V_{RIPPLE} \times f_{SW} \times R_{CLAMP})$$

where:
C_{CLAMP} is the value of the clamping capacitor.
V_{CLAMP} is the clamping voltage.
V_{RIPPLE} is the voltage ripple superimposed in V_{CLAMP}. A V_{RIPPLE} of about 5% to 10% of V_{CLAMP} is reasonable.
f_{SW} is the switching frequency of the flyback regulator.
R_{CLAMP} is the value of the clamping resistor.

Clamping Diode

Schottky diodes are typically the ideal choice for clamping diodes. However, fast recovery diodes can also be used. The diode reverse voltage rating must be higher than the maximum SWP pin voltage rating.

Diode, Zener Diode Clamp

A Zener diode can replace the RC network on the resistor, capacitor, diode clamp when the clamping level must be consistent and well defined. Choose the Zener diode breakdown voltage to balance power loss and switch voltage protection. Calculate the Zener voltage by using the following equation:

$$V_{ZENER\ (MAX)} \leq SWP_{VMAX} - V_{VINP\_MAX}$$

where:
$V_{ZENER\ (MAX)}$ is the maximum Zener diode breakdown voltage or the Zener voltage, which can be the same as the clamping voltage, V_{CLAMP}.
SWP_{VMAX} is the absolute maximum rating of the SWP pin.
V_{VINP_MAX} is the maximum input supply voltage.

The power loss in the clamp determines the power requirement for the Zener diode. Use the following equation to calculate the Zener diode power dissipation:

$$P_{ZENER} = (V_{ZENER} \times L_{LEAK} \times I_{PEAK}^2 \times f_{SW})/(2 \times (V_{ZENER} - V_{OUT1}))$$

where:
P_{ZENER} is the Zener diode power dissipation. Choose a Zener diode with power rating higher than the calculated value.
V_{ZENER} is the Zener diode breakdown voltage or the Zener voltage.
L_{LEAK} is the leakage inductance of the transformer.
I_{PEAK} is the peak current on the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.
V_{OUT1} is the output voltage of the flyback regulator.

Ripple Current (I_{AC}) vs. Inductance

Calculate the ripple current by first determining the duty cycle in continuous conduction mode.

$$D_{CCM} = (V_{OUT1} + V_D)/(V_{OUT1} + V_D + V_{INP})$$

where:
D_{CCM} is the duty cycle of the flyback switch.
V_{OUT1} is the output voltage of the flyback regulator.
V_D is the forward voltage drop across the rectifier diode.
V_{INP} is the input supply voltage.

Then, from the duty cycle, calculate I_{AC} in the flyback switch and transformer primary.

$$I_{AC} = (V_{INP} \times D_{CCM})/(f_{SW} \times L_{PRI})$$

where:
I_{AC} is the ripple current through the primary side of the transformer and flyback switch.
V_{INP} is the input supply voltage.
D_{CCM} is the duty cycle of the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.
L_{PRI} is the primary side inductance of the transformer.

Maximum Output Current Calculation

The maximum output power and current that can be achieved from the flyback output depends on a number of variables within the regulator. These variables include the transformer choice, the operating frequency, and the rectifier diode choice. The flyback regulator output is the supply to the buck regulator that drives

APPLICATIONS INFORMATION

V_{OUT2} and the inverting regulator that drives V_{OUT3}. Determine the maximum output power capability by

$$P_{VOUT1\ (MAX)} = 0.5 \times (I_{PEAK}^2 - (I_{PEAK} - I_{AC}/2)^2) \times L_{PRI} \times f_{SW} \times \eta$$

where:
$P_{VOUT1\ (MAX)}$ is the maximum output power from V_{OUT1}.
I_{PEAK} is the peak current on the flyback switch.
I_{AC} is the ripple current through the primary side of the transformer and flyback switch.
L_{PRI} is the primary side inductance of the transformer.
f_{SW} is the switching frequency of the flyback regulator.
η is the expected efficiency of the flyback regulator.

The lower limit of the flyback current-limit threshold, $I_{LIM\ (FLYBACK)}$, limits the maximum I_{PEAK}. However, it is not recommended to operate at this level to avoid unwanted current-limit events due to variation in transformer inductance, efficiency, flyback switching frequency, and rectifier diode forward voltage drop. If the load on the flyback causes the current limit to trip, the output voltage may not regulate as expected. Choose a peak operating current with built in margin for the variations mentioned or to calculate the maximum output power or output load using the worst case transformer inductance, efficiency, diode forward voltage drop, and flyback switching frequency.

Calculate the maximum load current on V_{OUT1} by

$$I_{VOUT1\ (MAX)} = P_{VOUT1\ (MAX)}/V_{OUT1}$$

where:
$I_{VOUT1\ (MAX)}$ is the maximum output current from V_{OUT1}.
$P_{VOUT1\ (MAX)}$ is the maximum output power from V_{OUT1}.
V_{OUT1} is the output voltage of the flyback regulator.

Table 19. Transformer Selection

			Primary					
Part Number	**Manufacturer**	**Turn Ratio[1]**	**Inductance (µH)**	**Resistance (Ω)**	**Saturation Current[2] (mA)**	**Maximum Leakage Inductance (µH)**	**Isolation Voltage[3] (V rms)**	**Size: Length × Width × Height (mm)**
ZA9644-AED	Coilcraft	1:1	470	1.8	490	3.8	2000	10.92 × 9.25 × 10
750317986R6A	Würth Elektronik	1:1	470	1.27	480	7.0	1500	10.8 × 13.35 × 9.76
ZA9384-AL	Coilcraft	1:1	470	1.1	800	4.0	2000	15.3 × 16.5 × 6.7
750318257R6A	Würth Elektronik	1:1	470	1.56	550	2.0	1500	16 × 16.8 × 7.62
750316743	Würth Elektronik	1:1	280	1.1	250	0.7	2000	8.26 × 8.6 × 9.65

[1] Turn ratio between the primary and secondary coils.

[2] 20% drop from initial.

[3] 1 minute duration. Basic insulation.

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BUCK REGULATOR COMPONENT SELECTION

Inductor

The value of the inductor for the ADP1034 buck regulator affects the efficiency and the output voltage ripple. Larger value inductors typically improve efficiency. However, for a given package size, as load increases, the dc resistance (DCR) and core losses eventually have an increased negative impact on efficiency. Using a smaller value inductor reduces output voltage ripple but can decrease the overall efficiency due to increased switching losses.

Output Capacitor

The output capacitor selection affects the output ripple voltage, load step transient, and the loop stability of the regulator. A 10 µF capacitor is recommended as a balance between performance and size, but larger capacitor can be used to reduce output ripple.

INVERTING REGULATOR COMPONENT SELECTION

Inductor

The value of the inductor for the ADP1034 inverting regulator affects the efficiency and the output voltage ripple. Larger value inductors typically improve efficiency. However, for a given package size, as load increases, the DCR and core losses eventually have an increased negative impact on efficiency. Using a smaller value inductor reduces output voltage ripple but can decrease the overall efficiency due to increased switching losses.

Output Capacitor

The output capacitor selection affects the output ripple voltage, load step transient, and the loop stability of the regulator. A minimum of 4.7 µF capacitor is recommended to maintain stability across VOUT1 and the output load.

Inverting Regulator Stability

The ADP1034 inverting regulator uses internal compensation and operates with an inductance of 100 µH and a typical capacitance of 4.7 µF. Using different component values may result in instability of VOUT3, particularly if lower capacitance and smaller inductor values are used. Consult Analog Devices for guidance. Operating the inverter with the recommended inductor and output capacitor, the output is stable from no load to a 15 mA load for any output from −24 V to −2 V. When increasing the load beyond 15 mA, use a larger output capacitor to stabilize the feedback loop, particularly for lower output voltages.

Table 20. Buck Regulator and Inverting Regulator Recommended Inductors

Part Number	Manufacturer	Inductance (µH)	DCR (Ω)	Saturation Current[1] (mA)	Size: Length × Width × Height (mm)
744043101	Würth Elektronik	100	0.55	290	4.8 × 4.8 × 2.8
XFL3012-104MEB	Coilcraft	100	2.63	280	3.2 × 3.2 × 1.3
LQH3NPN101MMEL	Murata	100	1.59	260	3 × 3 × 1.4
SRN3015-101M	Bourns	100	2.92	270	3 × 3 × 1.5
SRU2016-101Y	Bourns	100	4.9	150	2.8 × 2.8 × 1.65
XFL2006-104MEB	Coilcraft	100	11.1	115	2 × 2 × 0.6

[1] 30% drop in inductance.

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INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking. Therefore, lower material group ratings provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is determined in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADP1034 isolators are shown in Table 5.

Insulation Wear Out

The lifetime of insulation is determined by thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation. This displacement current causes incremental damage to the insulation. The stress on the insulation can be broken down into broad categories: dc stress and ac component time varying voltage stress. DC stress causes very little insulation wear out because there is no displacement current. AC component time varying voltage stress causes insulation wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

THERMAL ANALYSIS

For the purpose of thermal analysis, the ADP1034 die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} values from Table 8. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADP1034 operates at a full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout Considerations section decreases thermal resistance to the PCB, allowing increased thermal margins in high ambient temperatures. Each switching regulator in the ADP1034 has a thermal shutdown circuit that turns off the dc-to-dc converter and the outputs when a die temperature of approximately 150°C is reached. When the die cools below approximately 135°C, the ADP1034 dc-to-dc converter outputs turn on again.

DETAILED TYPICAL APPLICATION CIRCUIT

Figure 89 shows a detailed typical application circuit for the ADP1034.

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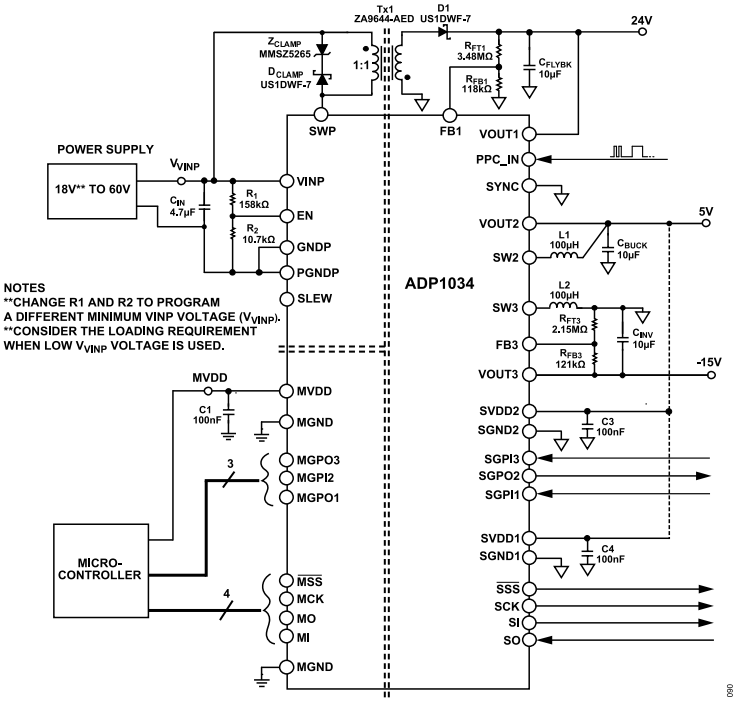

Figure 89. Detailed Typical Application Circuit

PCB LAYOUT CONSIDERATIONS

To achieve optimum efficiency, proper regulation, strong stability, and proper PPC operation, a well designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep the input bypass capacitor, C_{IN}, close to the VINP pin, and the PGNDP pin.
- Keep the high current paths as short and wide as possible to minimize parasitic series inductance, which causes spiking and EMI. These paths include the connections between the following:
  - C_{IN}, VINP, transformer primary, and PGNDP
  - VOUT1, C_{FLYBK}, D1, transformer secondary, and SGND2
  - VOUT2, SW2, L1, C_{BUCK}, and SGND2
  - VOUT3, SW3, L2, C_{INV}, and SGND2
- Avoid routing high impedance traces like feedback and PPC_IN traces near or directly under any of the high current switching paths to prevent radiated switching noise injection.
- Place the feedback resistors as close to the FB1 and FB3 pins as possible to prevent high frequency switching noise injection.
- To minimize EMI, place the MVDD decoupling capacitor (C1) close to MVDD (Pin 39) and MGND (Pin 3).
- To minimize EMI, place the SVDD1 decoupling capacitor (C3) close to SVDD1 (Pin 10) and SGND1 (Pin 5), and place the SVDD2 decoupling capacitor (C7) close to SVDD2 (Pin 20) and SGND2 (Pin 16).

Figure 90 shows a suggested top layer layout for the ADP1034.

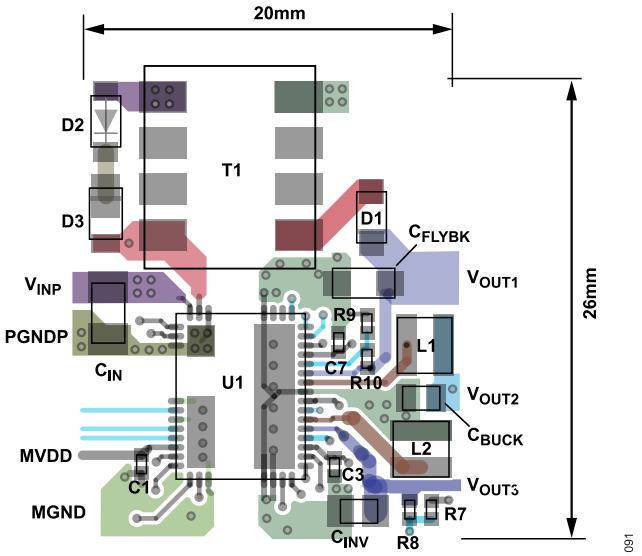

Figure 90. Suggested ADP1034 Top Layer Layout

OUTLINE DIMENSIONS

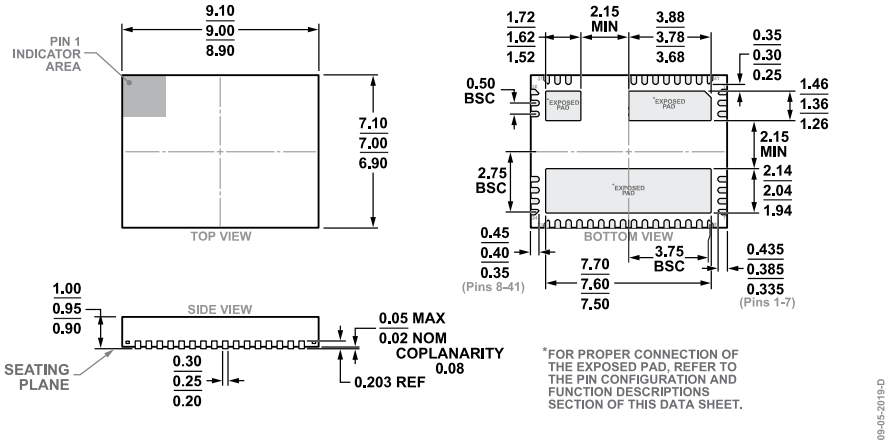

Figure 91. 41-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 7 mm Body and 0.95 mm Package Height
(CP-41-1)
Dimensions shown in millimeters

Updated: September 21, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADP1034ACPZ-1-R7	-40°C to +125°C	41-Lead LFCSP (9mm x 7mm)	Reel, 750	CP-41-1
ADP1034ACPZ-1-U1	-40°C to +125°C	41-Lead LFCSP (9mm x 7mm)	Tray, 260	CP-41-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADP1034CP-1-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

ADP1034ACPZ-1-R7