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Evaluating the ADMV8818 2 GHz to 18 GHz, Digitally Tunable, High-Pass and Low-Pass Filter

FEATURES

Fully featured evaluation board for the ADMV8818
On-board SDP-S connector for the SPI
Evaluation using on-board LDO regulators powered by the USB
ACE software interface for SPI control

EQUIPMENT NEEDED

Network analyzer
Windows® PC
USB cable
EVAL-SDP-CS1Z (SDP-S) controller board

DOCUMENTS NEEDED

ADMV8818 data sheet

SOFTWARE NEEDED

ACE software

GENERAL DESCRIPTION

The ADMV8818-EVALZ is available for evaluating the ADMV8818 digitally tunable, high-pass and low-pass filter. The ADMV8818-EVALZ incorporates the ADMV8818 chip, as well as a negative voltage generator, low dropout (LDO) regulators, and an interface to the EVAL-SDP-CS1Z (SDP-S) system demonstration platform (SDP) to allow simple and efficient evaluation. The negative voltage generator and LDO regulators allow the ADMV8818 to be powered by either the 5 V USB supply voltage from the PC via the SDP-S or by using two external power supplies.

The ADMV8818 is a fully monolithic microwave integrated circuit (MMIC) that features a digitally selectable frequency of operation. The chip features four independently controlled high-pass and low-pass filters that span from 2 GHz to 18 GHz. The chip can be programmed using a 4-wire serial port interface (SPI). The SDP-S controller allows the user to interface with the ADMV8818 SPI through the Analog Devices, Inc., Analysis | Control | Evaluation (ACE) software.

For full details on the ADMV8818, see the ADMV8818 data sheet, which must be consulted in conjunction with this user guide when using the ADMV8818-EVALZ.

EVALUATION BOARD PHOTOGRAPH

Figure 1.

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REVISION HISTORY

12/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV8818-EVALZ has the ADMV8818 chip on board. The ADMV8818-EVALZ also includes a negative voltage generator and three LDO regulators to provide the necessary supply voltages for the chip. The regulators can be entirely powered by the 5 V USB supply voltage from the PC via the SDP-S.

To power the ADMV8818-EVALZ using the 5 V USB supply, slide the S2 switch downward (as shown in Figure 2) to power the on-board negative voltage generator and LDO regulators. Alternatively, the ADMV8818-EVALZ can be powered externally by sliding the S2 switch upward and then connecting power supplies to the VPOS and VNEG Subminiature Version A (SMA) ports or test points. The applicable voltage range for the positive input VPOS is between 3.5 V and 5.5 V, and the applicable voltage range for the negative input VNEG is between −5.5 V and −2.7 V.

Figure 2 shows an example lab bench setup for the ADMV8818-EVALZ. To observe the filter response from the ADMV8818-EVALZ, connect the RF input (RFIN) and RF output (RFOUT) ports to a network analyzer (or a similar instrument). Typically, RFIN and RFOUT are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.

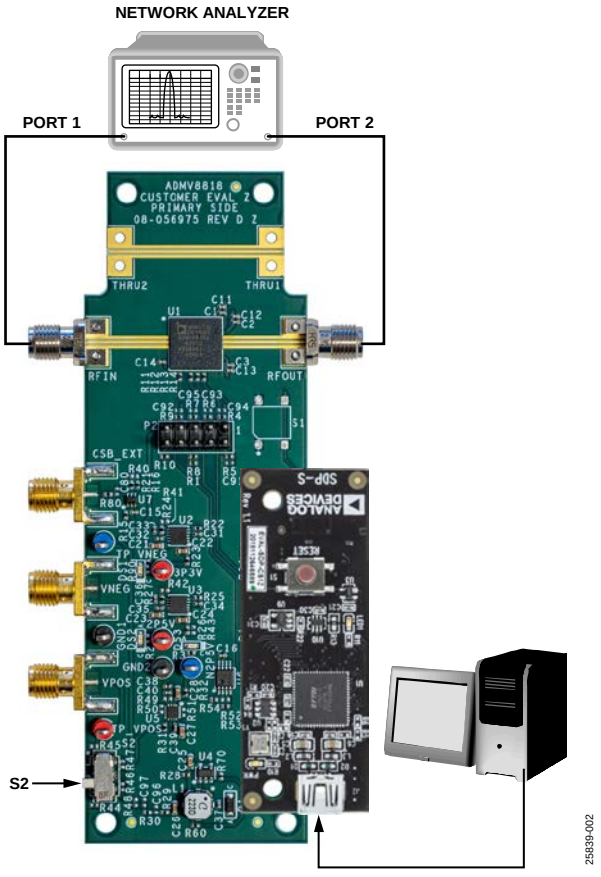

Figure 2. Lab Bench Setup

EVALUATION BOARD SOFTWARE

INSTALLING THE ACE SOFTWARE, ADMV8818 PLUGINS, AND DRIVERS

The ADMV8818-EVALZ uses the Analog Devices ACE software. For instructions on how to install and use the ACE software, go to the ACE software page.

If the ACE software is already installed on the PC, ensure that the installed software is the latest version, as shown on the ACE software page. If the installed software is not the latest version, take the following steps to install the updated ACE software:

1. Uninstall the current version of the ACE software on the PC.
2. Delete the ACE folder found in **C:\ProgramData\Analog Devices** and **C:\Program Files (x86)\Analog Devices**.
3. Install the latest version of the ACE software. During the installation, ensure that the .**NET 40 Client**, **SDP Drivers**, and **LRF Drivers** components are selected (see Figure 3).

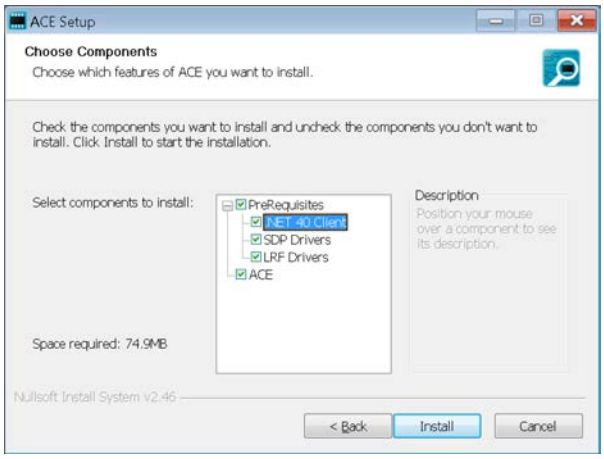

Figure 3. Required Driver Installations with the ACE Software

Once the installation finishes, the **ADMV8818 Board** plugin appears in the **Attached Hardware** section of the **Start** tab when the ACE software is running. (see Figure 4).

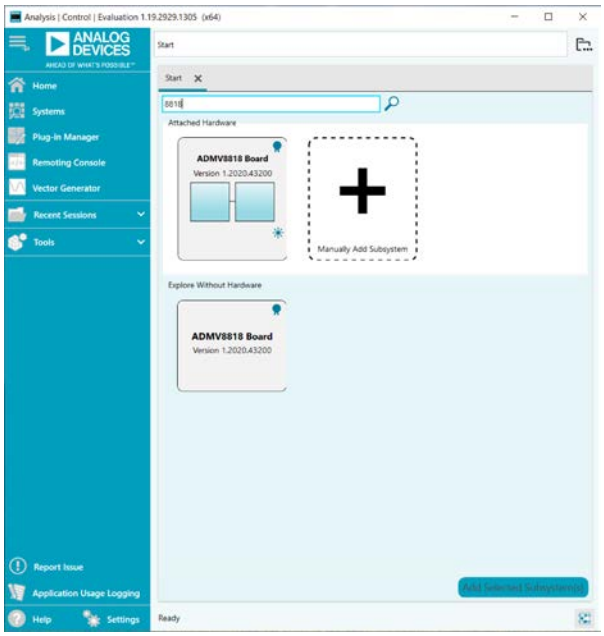

*Figure 4. **ADMV8818 Board** Plugin Window after Opening the ACE Software*

PLUGIN OVERVIEW

When the ADMV8818-EVALZ is connected to the PC, the **ADMV8818 Board** appears in the **Attached Hardware** section of the **Start** tab. Double click the **ADMV8818 Board** plugin to open two tabs, the board level plugin and the chip level plugin, which are the **ADMV8818 Board** plugin view (see Figure 5) and the **ADMV8818** chip plugin (see Figure 6), respectively.

The **ADMV8818** chip plugin includes the following feature sections (see Table 1 for additional information on these sections):

- The **CONFIGURATION** section (load from CSV)
- The **Logic Pins** section
- The **SFL Settings** section
- The chip **Status** section
- The **Display** controls section
- The **Filter Settings** section

The ACE software provides a simple tutorial for testing the ADMV8818. For a more customized and detailed implementation, refer to ADMV8818 data sheet for a full description of the functionality, registers, and corresponding settings.

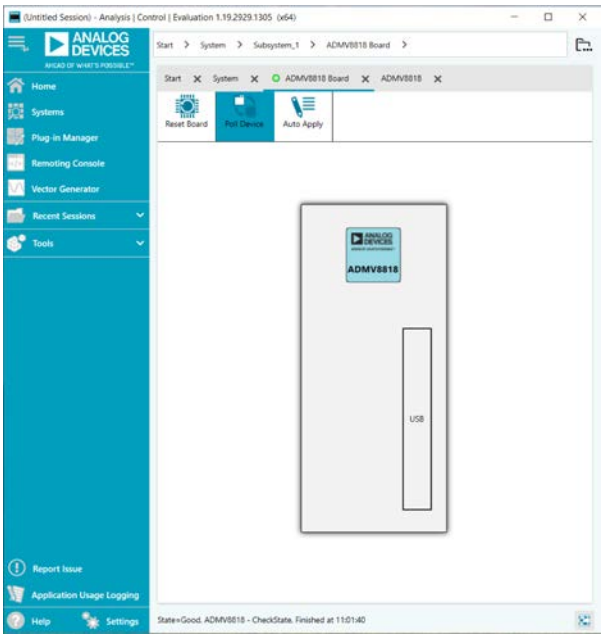

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*Figure 5. **ADMV8818 Board** Plugin View*

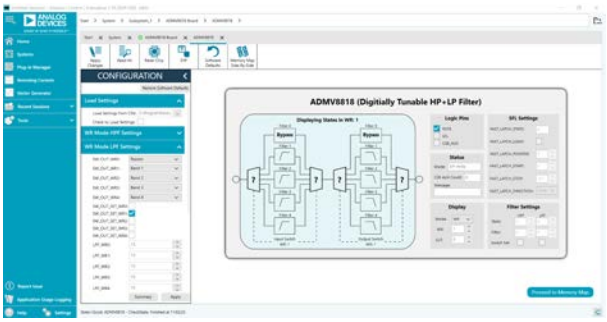

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*Figure 6. **ADMV8818** Chip Plugin*

PLUGIN DETAILS

The full screen **ADMV8818** chip plugin with labels is shown in Figure 7. The labels correspond to items listed in Table 1, which describes the functionality of each section. For additional detailed programming, refer to the ADMV8818 data sheet.

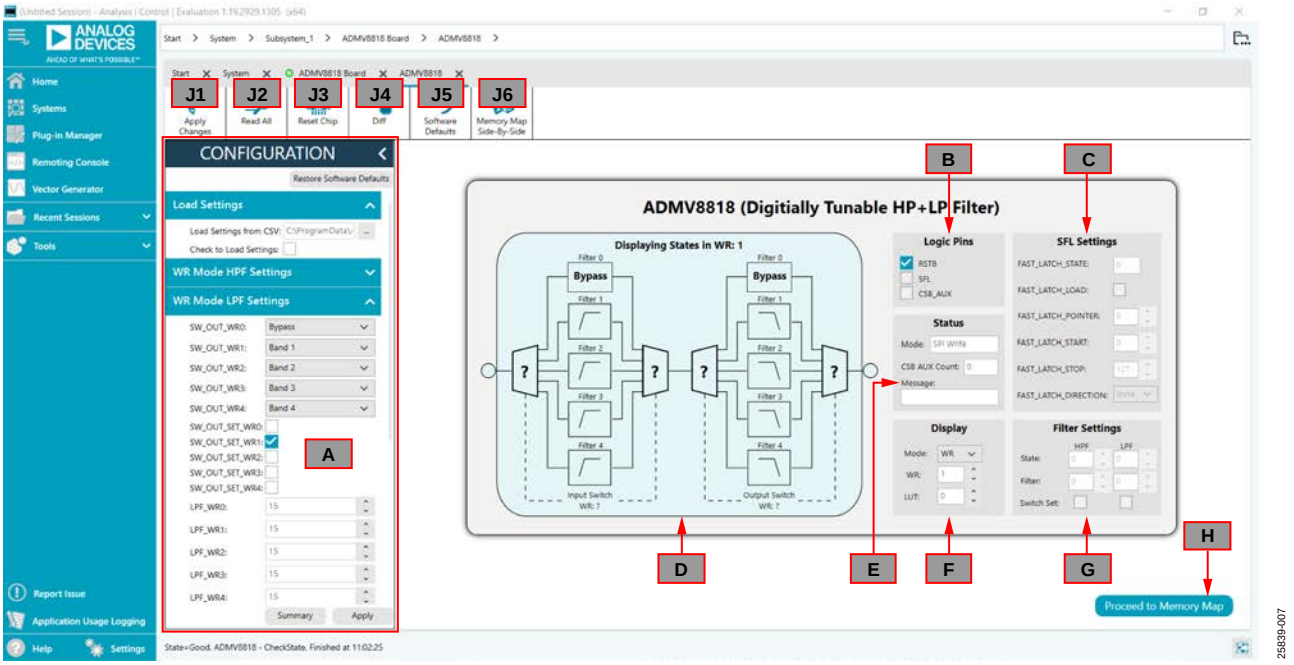

*Figure 7. **ADMV8818** Chip Plugin with Labels*

Table 1. ADMV8818 Chip Plugin Label Functions (See Figure 7)

Label	Function
A	Use the **CONFIGURATION** section to initialize the ADMV8818-EVALZ. **Load Settings from CSV**: click the **…** button to select which CSV file to load into the **CONFIGURATION** section. **Check to Load Settings**: once a file has been selected, select this check box to load the CSV file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected. **WR Mode HPF Settings**: select the input switch and high-pass filter (HPF) settings for SPI write mode. **WR Mode LPF Settings**: select the output switch and low-pass filter (LPF) settings for SPI write mode. **SFL Settings**: select the SPI fast latch (SFL) settings that are used when the chip is placed into the SPI fast latch mode. Note that this function is not shown in Figure 7. Scroll down in the **CONFIGURATION** section to view this function. **Lookup Table 0 to 15**: define the configuration for lookup table (LUT)0 to LUT15. Note that these functions are not shown in Figure 7. Scroll down in the **CONFIGURATION** section to view these functions. **Lookup Table 16 to 31**: define the configuration for LUT16 to LUT31. **Lookup Table 32 to 47**: define the configuration for LUT32 to LUT47. **Lookup Table 48 to 63**: define the configuration for LUT48 to LUT63. **Lookup Table 64 to 79**: define the configuration for LUT64 to LUT79. **Lookup Table 80 to 95**: define the configuration for LUT80 to LUT95. **Lookup Table 96 to 111**: define the configuration for LUT96 to LUT111. **Lookup Table 112 to 127**: define the configuration for LUT112 to LUT 127. **Summary**: click this button to review the settings for the initial setup. **Apply**: click this button to apply the settings to the chip. Note that clicking **Apply Changes** (J1) does not update the changes in this section. Also, at startup, the main diagram user controls cannot be updated until the **Apply** button is clicked at least once. **Restore Software Defaults**: click this button to zero out the **CONFIGURATION** section prior to loading a different CSV file.

Label	Function
B	Use the **Logic Pins** section to toggle the SDP-S logic pins, which are connected to the logic pins on the ADMV8818 chip. This section includes the following: **RSTB**: clear the check box to bring the ADMV8818 $\overline{\text{RST}}$ pin low, which holds the chip in reset. Select the check box again to bring the chip out of reset. **SFL**: select the check box to bring the ADMV8818 SFL pin high, which places the chip in SFL mode. This action also toggles the on board ADG749BKSZ switch connected to the ADMV8818 $\overline{\text{CS}}$ pin (see Figure 10). While in SFL mode, the ADMV8818 $\overline{\text{CS}}$ pin is connected to the SDP-S logic pin, CSB_AUX, and normal SPI transactions are disallowed. **CSB_AUX**: this pin is only available in SFL mode. Selecting the check box brings the SDP-S logic pin, CSB_AUX, high, which advances the internal state machine pointer to the next lookup table. If an external waveform generator is connected to the CSB_EXT port on the ADMV8818-EVALZ, the CSB_AUX pin has no effect and the CSB_EXT port takes precedence.
C	Use the **SFL Settings** section to configure the SPI fast latch settings on the chip when in the SFL mode. Refer to the ADMV8818 data sheet for more information regarding the internal state machine and SFL mode functionality. This section includes the following: **FAST_LATCH_STATE**: this value is the next state of the internal state machine pointer (read only). **FAST_LATCH_LOAD**: set this bit to load the pointer into the internal state machine. **FAST_LATCH_POINTER**: use this value to adjust the pointer location of the internal state machine. **FAST_LATCH_START**: this bit determines the start location within the internal state machine. **FAST_LATCH_STOP**: this bit determines the stop location within the internal state machine. **FAST_LATCH_DIRECTION**: this bit determines the direction that the internal state machine advances for each rising edge of the $\overline{\text{CS}}$ pin when in SFL mode.
D	The displayed block diagram section shows the actively selected WR or LUT number. This section includes the following: **Displaying States in…**: the title updates to show the actively selected WR or LUT number. Displayed States (or **Bypass**): depending on which filter band number is selected, the filter state value or **Bypass** populates into the appropriate block. **Input Switch**: this section displays the configuration of the input switch. When displaying a WR number, the input switch position updates based on the **SW_IN_SET_WRx** bit fields, where x is a number from 0 to 4. If multiple bit fields are set, the priority is WR0 to WR4. If no bit fields are set, the **Input Switch** position shows **WR ?**. When displaying an LUT number, the **Input Switch** position reflects the **SW_IN_SET_y** bit fields, where y is a number from 0 to 127, depending on the LUT number selected. **Output Switch**: this section displays the configuration of the output switch. When displaying a WR number, the output switch position updates based on the **SW_OUT_SET_WRx** bit fields, where x is a number from 0 to 4. If multiple bit fields are set, the priority is WR0 to WR4. If no bit fields are set, the **Output Switch** position shows **WR ?**. When displaying an LUT number, the **Output Switch** position reflects the **SW_OUT_SET_y** bit fields, where y is a number from 0 to 127, depending on the LUT number selected.
E	The **Status** section includes the following: **Mode**: when the SFL pin is low, the mode is **SPI Write**. When the SFL pin is high, the mode is **SPI Fast Latch** and the chip uses the LUT. **CSB_AUX Count**: when in SFL mode, this field displays the number of times the CSB_AUX pin has been toggled. **Message**: upon entering SFL mode, the **Message** field displays **Waiting for CSB**. Once the CSB_AUX pin has been toggled, the **Message** field displays the current LUT number followed by the next LUT number.
F	The **Display** section determines the actively selected WR or LUT number. This section includes the following: **Mode**: use the dropdown menu to select either **WR** or **LUT** display mode. **WR**: when the **Mode** is set to **WR**, scroll up and down to set the WR number (0 to 4) that is currently being configured and displayed on the diagram. Changing the WR number automatically changes the **Mode** to **WR**. **LUT**: when the **Mode** is set to **LUT**, scroll up and down to set the LUT number (0 to 127) that is currently being configured and displayed on the diagram. Changing to the LUT number automatically changes the **Mode** to **LUT**.
G	The **Filter Settings** section shows the filter states, filter band selection, and switch set for the actively selected WR or LUT number. This section includes the following: **State**: scroll up and down to set the desired filter state value (0 to 15). Changing the HPF state updates the **HPF_WRx** or **HPF_y** bit fields, and changing the LPF state updates the **LPF_WRx** or **LPF_y** bit fields, where x is the selected WR number, and y is the selected LUT number. **Filter**: scroll up and down to set the desired filter band value (0 to 4). A value of 0 corresponds to the bypass configuration, and all other values correspond to the filter band number. Changing the HPF band updates the **SW_IN_WRx** or **SW_IN_y** bit fields. Changing the LPF band updates the **SW_OUT_WRx** or **SW_OUT_y** bit fields. **Switch Set**: these check boxes determine if the input and output switches change. Toggling the **Switch Set** for HPF sets the **SW_IN_SET_WRx** or **SW_IN_SET_y** bit fields. Toggling the **Switch Set** for LPF sets the **SW_OUT_SET_WRx** or **SW_OUT_SET_y** bit fields.

Label	Function
H	Click **Proceed to Memory Map** to open the **ADMV8818 Memory Map** (see Figure 8).
J1	All changes, except within the **CONFIGURATION** section, do not take effect until clicking **Apply Changes**. If **Auto Apply** is highlighted in the **ADMV8818 Board** tab (see Figure 5), the **Apply Changes** feature continuously runs every few seconds, and **Apply Changes** does not need clicking to apply or read back the block diagram settings.
J2	To read back all of the SPI registers of the chip, click **Read All**.
J3	Click **Reset Chip** to reset the chip.
J4	Click **Diff** to show registers that are different on the chip.
J5	Click **Software Defaults** to restore the software defaults to the chip, and then click **Apply Changes**. The software defaults for the ADMV8818 is for all registers to be zero, except for Register 0x011, which is set to 0x7F.
J6	Click **Memory Map Side-By-Side** to enable the side by side memory map view.

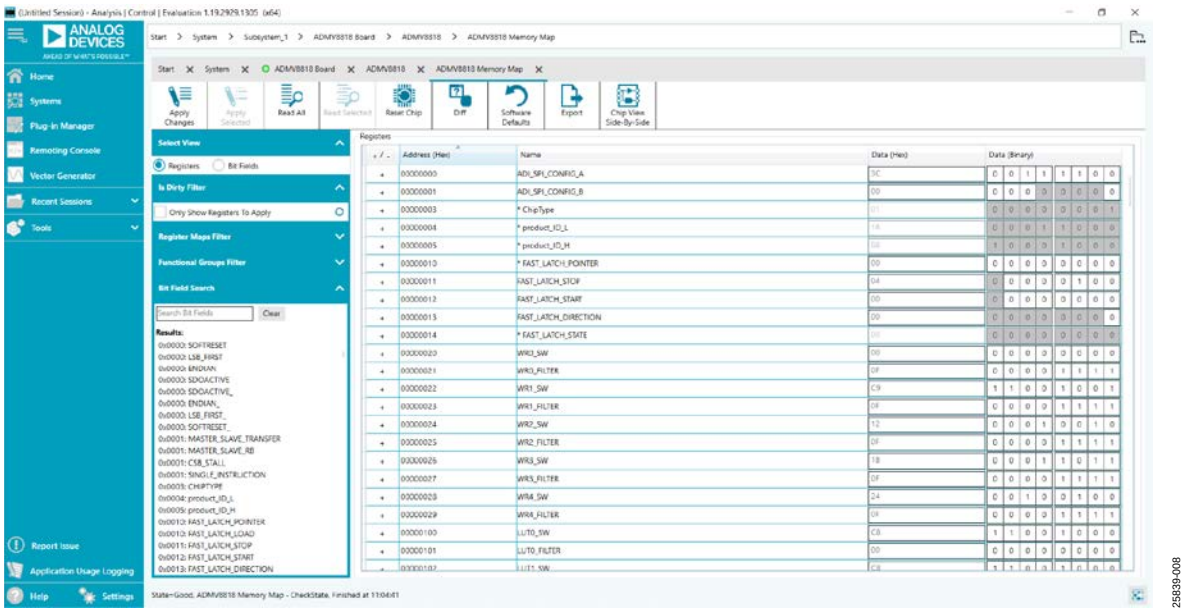

*Figure 8. **ADMV8818 Memory Map** in the ACE Software*

PERFORMING THE EVALUATION

ADMV8818-EVALZ QUICK START

To set up the ADMV8818-EVALZ, take the following steps:

1. Connect the RFIN and RFOUT ports to a network analyzer (or a similar instrument). Typically, RFIN and RFOUT are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.
2. Connect the SDP-S to the 120-pin connector on the ADMV8818-EVALZ. Do not connect the SDP-S to the PC until after completing Step 3 or Step 4.
3. On the ADMV8818-EVALZ, slide the S2 switch downward (as shown in Figure 2) to power the ADMV8818-EVALZ from the 5 V USB supply voltage from the PC via the SDP-S.
4. Alternatively (to Step 3), slide the S2 switch upward and connect power supplies to the VPOS and VNEG ports. The applicable voltage range for VPOS is between 3.5 V and 5.5 V, and the applicable voltage range for VNEG is between −5.5 V and −2.7 V. The external supply current limits must be set to 20 mA. Expected supply current draw for VPOS is 12 mA to 14 mA and for VNEG is 2 mA to 3 mA. The ADMV8818 chip current drawn per supply pin is typically 10s of microamps or less. Most of the current drawn from the ADMV8818-EVALZ comes from the LDO regulators and the status indicator light emitting diodes (LEDs), DS1 to DS3.
5. Connect a USB cable between the PC and the SDP-S.
6. Open the ACE software. The **ADMV8818 Board** appears in the **Attached Hardware** section of the **Start** tab. Double click the **ADMV8818 Board** plugin to open two tabs, one for the **ADMV8818 Board** plugin view and one for the **ADMV8818** chip plugin.
7. Use the **CONFIGURATION** section (see Figure 9) in the ACE software to initialize the chip. By default, the **ADMV8818_Register_Load_1.csv** file is loaded into this section. Click **Apply** to send the default settings to the chip and to allow the main diagram user controls to become editable.

NETWORK ANALYZER SETTINGS

When evaluating the ADMV8818-EVALZ, a good starting point for configuring the network analyzer is as follows:

- Start frequency = 0.1 GHz
- Stop frequency = 40 GHz
- Number of points = 400
- Step size = 100 MHz
- Power level = −10 dBm
- Measure types = S-parameters (S21, S11, and S22)
- Format = log magnitude
- Calibration = full 2-port

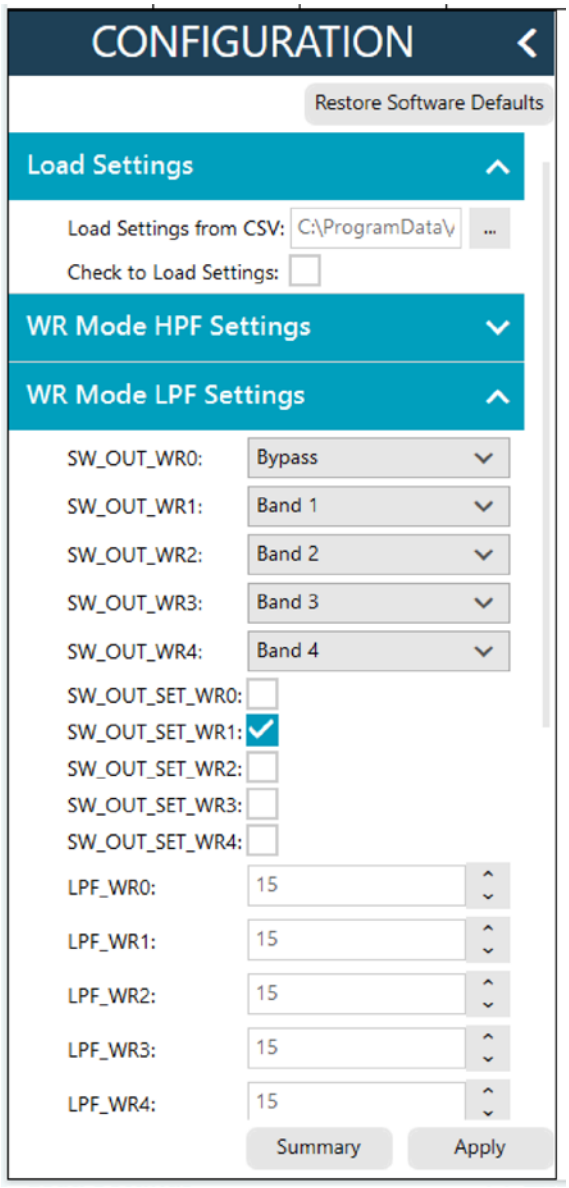

*Figure 9. ADMV8818 **CONFIGURATION** Section*

CSV FILES

By default, the **ADMV8818_Register_Load_1.csv** file is loaded into the **CONFIGURATION** section. To load a different CSV file in the **CONFIGURATION** section, take the following steps:

1. If the **Modify** button is visible, click to allow changes.
2. Click **Restore Software Defaults** to zero out the **CONFIGURATION** section.
3. Click the **…** button next to **Load Settings from CSV** to select which CSV file to load (see Figure 9).
4. Select the **Check to Load Settings** check box to load the CSV file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected.
5. Click **Apply** to send out the settings to the hardware.

AUTOMATIC CHIP RESET

If a reset of the ADMV8818 chip is required on the ADMV8818-EVALZ, click **Reset Chip** (see Figure 7 and Label J3 in Table 1 for additional information). This automated sequence performs the following actions:

- Toggles all SDP-S general-purpose input/output (GPIO) logic pins to a low state, which brings the $\overline{\text{RST}}$ pin low to initiate a hard reset of the ADMV8818.
- Toggles the $\overline{\text{RST}}$ pin high to bring the ADMV8818 chip back to the normal operating state.
- Programs Register 0x000 to 0x81, which also resets the ADMV8818. This step covers legacy boards that did not have the $\overline{\text{RST}}$ pin connected.
- Programs Register 0x000 to 0x3C to enable the SDO pin on the ADMV8818 and to allow SPI streaming with Endian register ascending order.
- Reads back the register settings of the ADMV8818.

LOSS OF BOARD COMMUNICATION

When the ADMV8818 is turned off and then on, or if the USB cable is disconnected and connected while the ACE software is running, communication with the ADMV8818 may be lost. To regain communication, take the following steps:

1. Click the **System** tab.
2. Click the USB symbol in the **SDP-S Controller** subsystem.
3. Click **Acquire**.

If this action does not work, restart the ACE software to reinitiate communication with the ADMV8818-EVALZ.

REGULATOR BYPASS

The ADMV8818-EVALZ has a negative voltage generator and three LDO regulators on board that allow the user to operate using the 5 V USB supply voltage from the PC via the SDP-S. These on board LDO regulators provide the three necessary supply voltages, −2.5 V, 2.5 V, and 3.3 V. If desired, these LDO regulators can be bypassed by removing the 0 Ω resistors (R23, R26, and R32) from the ADMV8818-EVALZ, and then applying each voltage independently by using the corresponding test points. Bypassing the on board regulators is useful for measuring the ADMV8818 supply current, but it must be noted that each supply pin is also connected to status indicator LEDs, DS1 to DS3, and each LED draws approximately 2 mA of current. Remove the R2, R3, and R90 resistors to disable these status indicators. See Figure 10 for more details.

PLUGIN SPI REGISTER CONTROLLER

The ADMV8818 plugin utilizes an SPI register controller to communicate with the ADMV8818. When using the ADMV8818 in a system, it is recommended to follow a similar methodology for implementing SPI communication. The following is a summary of the SPI register controller:

1. Determine if Register 0x000 is not set to a value of 0x3C.
2. If Step 1 is true, set Register 0x000 to a value of 0x3C to enable the SDO pin on the ADMV8818 and allow SPI streaming with Endian register ascending order.
3. Determine if the values have changed for any of the WR registers (Register 0x020 to Register 0x029).
4. If Step 3 is true, write Register 0x020 to Register 0x029 by pointing to Register 0x020 and streaming out 10 bytes of data. The transaction is 96 bits in total (R/W bit + 15 address bits + 80 data bits). Streaming out the data in this order ensures that the switch position priority is WR0 to WR4.
5. If Step 4 has occurred, write dummy data to Address 0x0A. Note that Address 0x0A does not exist in the ADMV8818, and the written dummy data is ignored. This step is microcontroller architecture dependent and can be ignored in most cases. It is necessary for the SDP-S to clear the SPI bus and reconfigure for a standard 24-bit SPI transaction.
6. Determine if the values have changed for any of the LUT registers (Register 0x100 to Register 0x1FF).
7. If Step 6 is true, write Register 0x100 to Register 0x1FF by performing the following:
    - Pointing to Register 0x100 and streaming out 64 bytes of data.
    - Pointing to Register 0x140 and streaming out 64 bytes of data.
    - Pointing to Register 0x180 and streaming out 64 bytes of data.
    - Pointing to Register 0x1C0 and streaming out 64 bytes of data.
8. If Step 7 has occurred, repeat Step 5.
9. Write out any remaining registers that may have changed.

EVALUATION BOARD SCHEMATICS AND ARTWORK

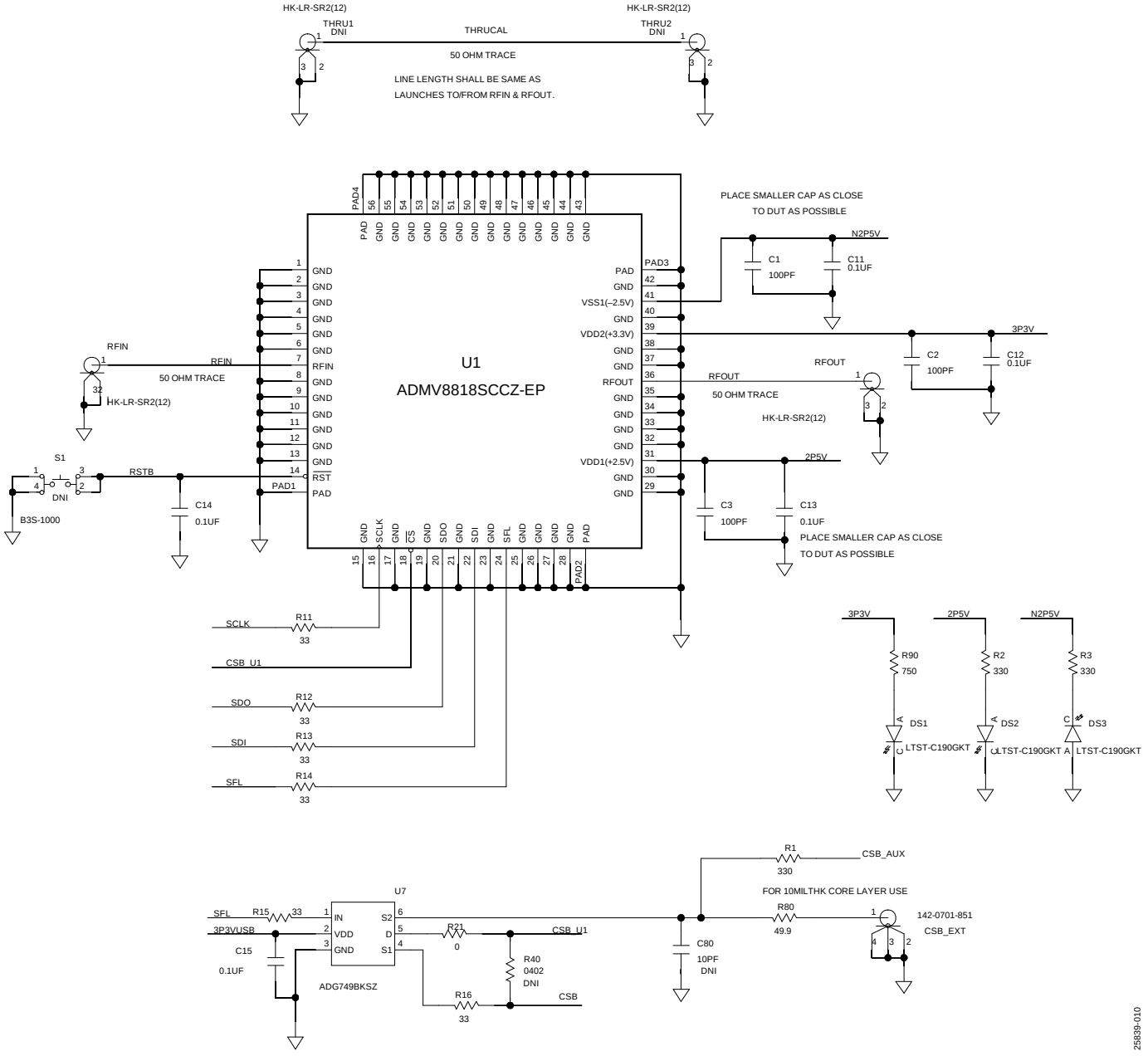

Figure 10. ADMV8818-EVALZ Schematic, Page 1

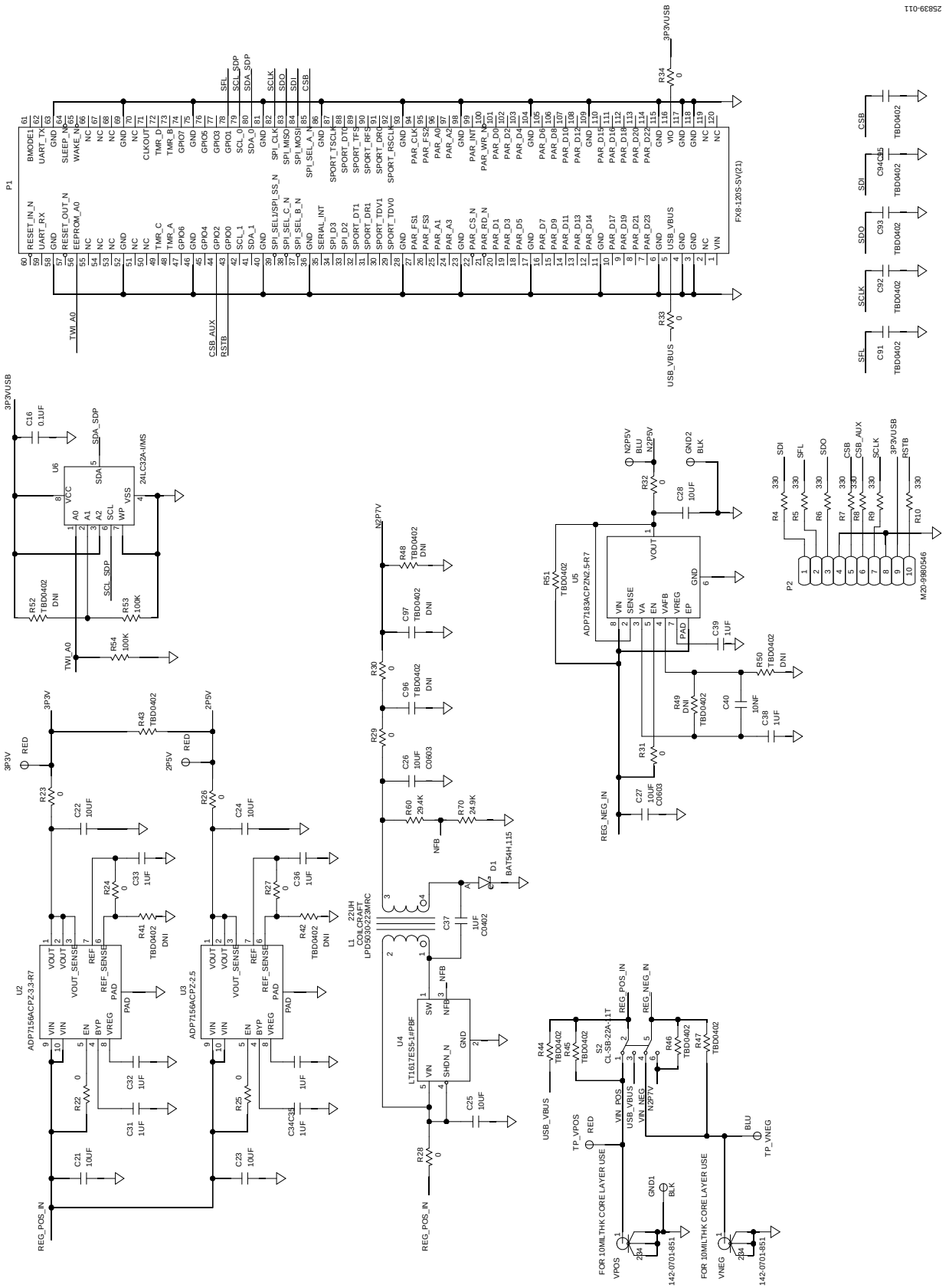

Figure 11. ADMV8818-EVALZ Schematic, Page 2

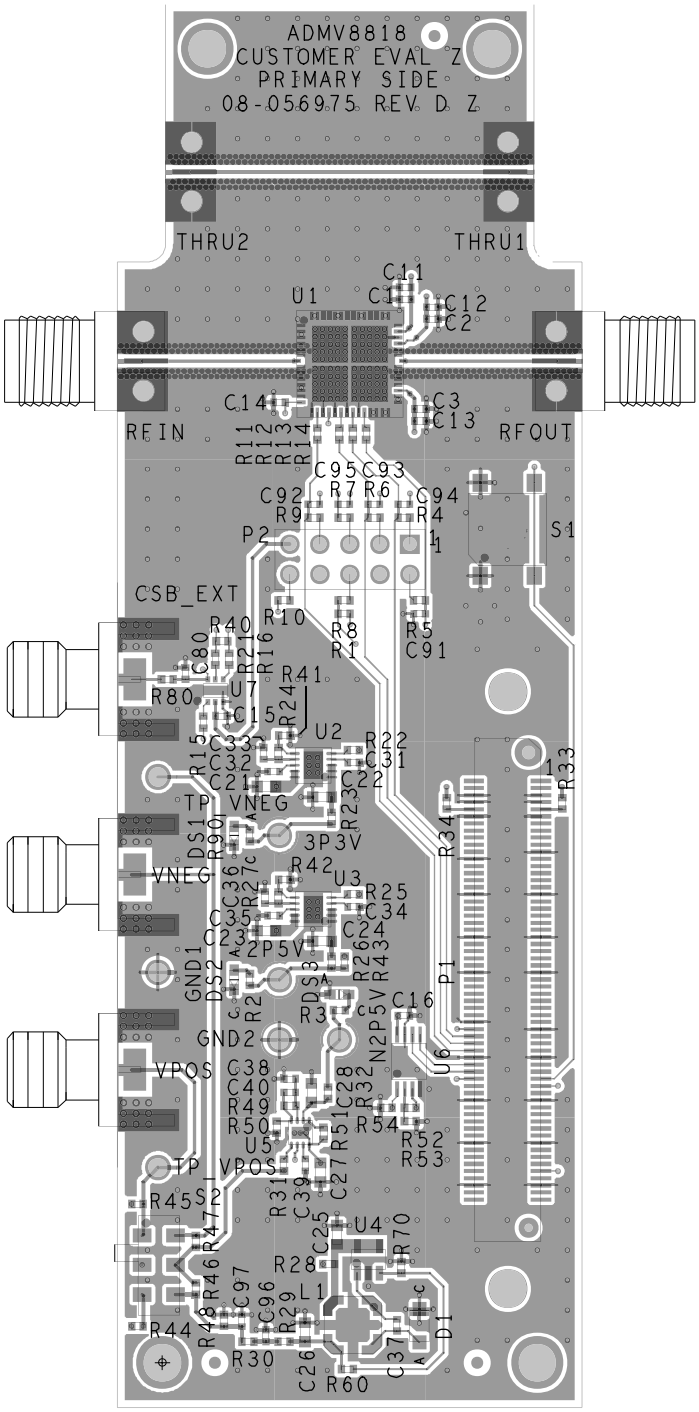

Figure 12. ADMV8818-EVALZ Layer 1

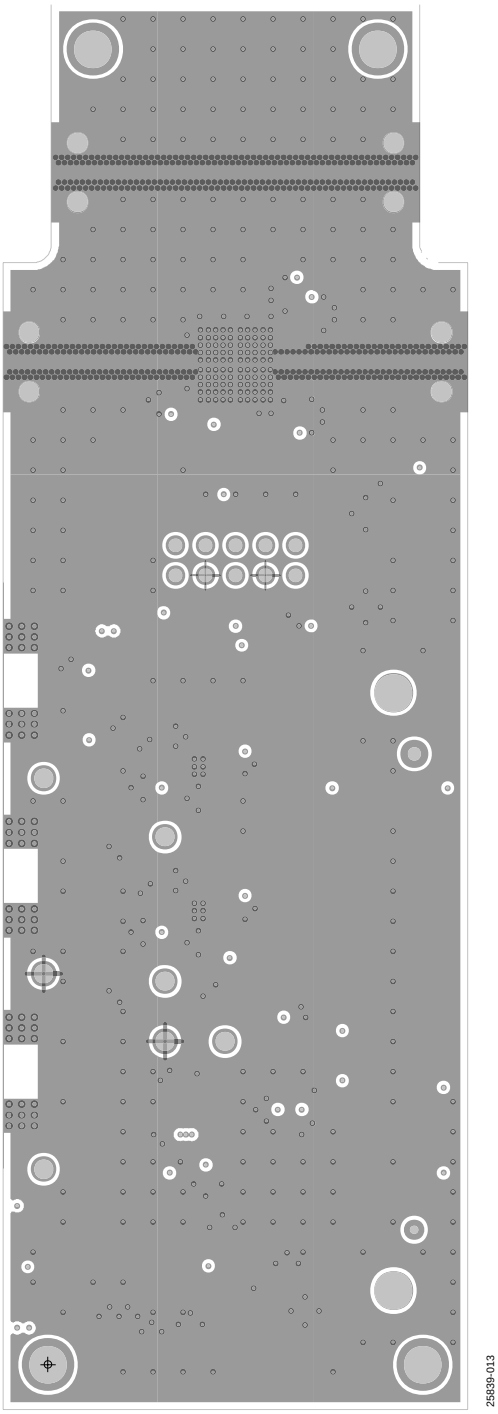

Figure 13. ADMV8818-EVALZ Layer 2

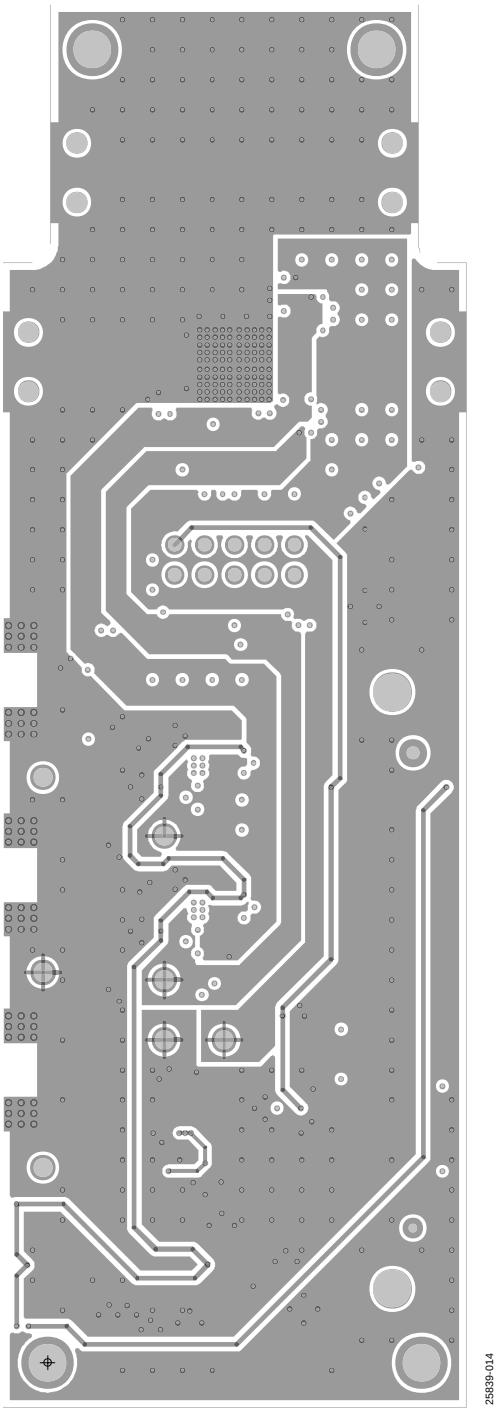

Figure 14. ADMV8818-EVALZ Layer 3

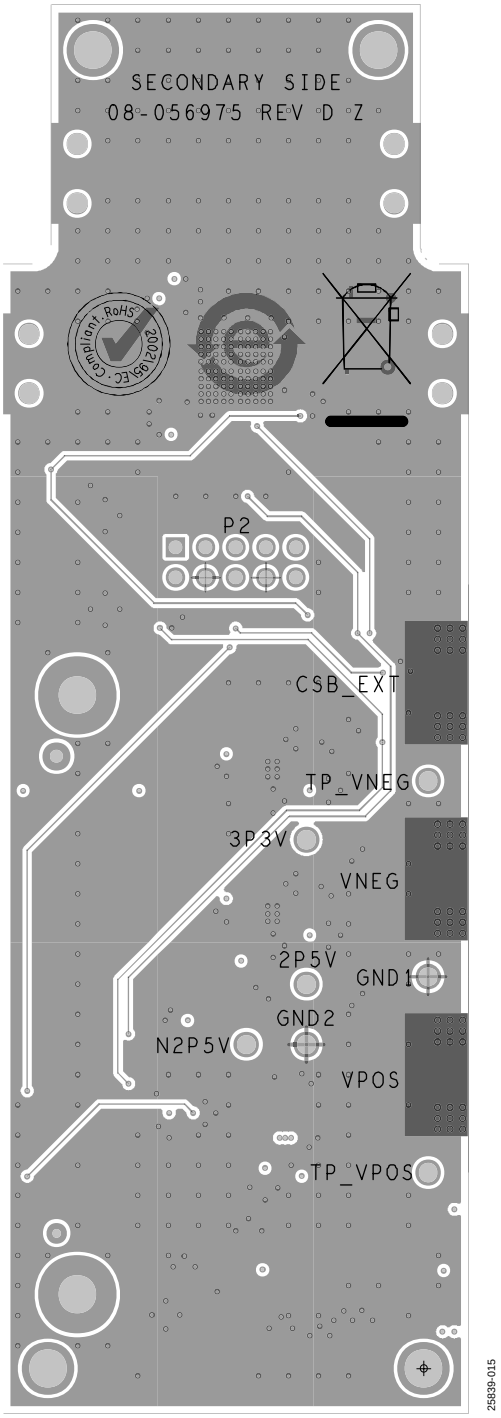

Figure 15. ADMV8818-EVALZ Layer 4

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. ADMV8818-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
3	2P5V, 3P3V, TP_VPOS	Test points, red	Components Corporation	TP-104-01-02
2	GND1, GND2	Test points, black	Components Corporation	TP-104-01-00
2	N2P5V, TP_VNEG	Test points, blue	Components Corporation	TP-104-01-06
3	CSB_EXT, VNEG, VPOS	Connectors, edge launch, SMA	Cinch Connectivity	142-0701-851
2	RFIN, RFOUT	Connector, 2.92 mm, 40 GHz	Hirose Electric Co.	HK-LR-SR2(12)
3	C1 to C3	Capacitors, 100 pF, 50 V, 5%, 0402	Johanson Dielectrics	500R07N101JV4T
6	C11 to C16	Capacitors, 0.1 µF, 16 V, 5%, 0402	Kemet	C0402C104J4RACTU
8	C21 to C28	Capacitors, 10 µF, 16 V, 10%, 0603	Murata	GRM188R61C106KAALD
9	C31 to C39	Capacitors, 1 µF, 16 V, 20%, 0402	Murata	GRM155R61C105MA12D
1	C40	Capacitor, 10 nF, 25 V, 10%, 0402	Samsung	CL05B103KA5NNNC
1	D1	Diode, BAT54H, 30 V, SOD123F	NXP Semiconductor	BAT54H,115
3	DS1 to DS3	LEDs, LTST-C190GKT, green, 0603	Lite-On Technology	LTST-C190GKT
1	L1	Coupled inductor, 22 µH, 20%	Coilcraft	LPD5030-223MRC
1	P1	Connector, vertical, surface-mount technology (SMT), 120-pin	Hirose Electric Co.	FX8-120S-SV(21)
1	P2	Connector, vertical, header, 10-pin	Harwin Inc.	M20-9980546
10	R1 to R10	Resistors, 330 Ω, 1/16 W, 5%, 0402	Panasonic	ERJ-2GEJ331X
6	R11 to R16	Resistors, 33 Ω, 1/10 W, 5%, 0402	Panasonic	ERJ-2GEJ330X
14	R21 to R34	Resistors, 0 Ω, 1/16 W, 0402	Stackpole	RMCF0402ZT0R00
2	R53, R54	Resistors, 100 kΩ, 1/16 W, 5%, 0402	Yageo	RC0402JR-07100KL
1	R60	Resistor, 29.4 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF2942X
1	R70	Resistor, 24.9 kΩ, 1/16 W, 1%, 0402	Panasonic	ERJ-2RKF2492X
1	R80	Resistor, 49.9 Ω, 1/16 W, 1%, 0402	Panasonic	ERJ-2RKF49R9X
1	R90	Resistor, 750 Ω, 1/16 W, 5%, 0402	Panasonic	ERJ-2GEJ751X
1	S2	Switch, mechanical, slide, DPDT, 0.2 A	Nidec Copal Electronics	CL-SB-22A-11T
1	U1	ADMV8818, 2 GHz to 18 GHz, digitally tunable, high-pass and low-pass filter	Analog Devices	ADMV8818SCCZ-EP
1	U2	IC, LDO regulator, 3.3 V	Analog Devices	ADP7156ACPZ-3.3-R7
1	U3	IC, LDO regulator, 2.5 V	Analog Devices	ADP7156ACPZ-2.5-R7
1	U4	IC, inverting dc-to-dc converter	Analog Devices	LT1617ES5-1#TRPBF
1	U5	IC, LDO regulator, −2.5 V	Analog Devices	ADP7183ACPZN2.5-R7
1	U6	IC, 24LC32A, electronically erasable programmable read-only memory (EEPROM), I^2C	Microchip Technology	24LC32A-I/MS
1	U7	IC, CMOS, SPDT switch	Analog Devices	ADG749BKSZ
1	C80	Capacitor, 10 pF, 50 V, 5%, 0402, do not install (DNI)	Yageo	CC0402JRNPO9BN100
7	C91 to C97	Capacitors, 0402, DNI	Not applicable	Not applicable
13	R40 to R52	Resistors, 0402, DNI	Not applicable	Not applicable
1	S1	Switch, mechanical, push button, DNI	Omron Electronics Inc.	B3S1000
2	THRU1, THRU2	Connector, 2.92 mm, 40 GHz	Hirose Electric Co.	HK-LR-SR2(12)

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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