

0.5  $\Omega$   $R_{ON}$ ,  $\pm 20$  V, +36 V, Quad SPST Switch

## FEATURES

- ▶ Low  $R_{ON}$  0.5  $\Omega$
- ▶ High continuous current of up to 847 mA
- ▶ Flat  $R_{ON}$  across signal range, 0.003  $\Omega$
- ▶ THD of -127 dB at 1 kHz
- ▶ Improved balance between on resistance and on capacitance
  - ▶ Low  $R_{ON}$  (0.5  $\Omega$ ) and  $C_{ON}$  (25 pF)
- ▶ 1.8 V, 3.3 V, and 5 V Logic compatibility
- ▶ 16-lead, 4 mm x 4 mm LFCSP
  - ▶ Pin to pin compatible with the [ADG5412](#) and [ADG5412F](#)
- ▶ Fully specified at  $\pm 20$  V and +36 V
- ▶ Operational with asymmetric power supplies
- ▶  $V_{SS}$  to  $V_{DD}$  - 2 V analog signal range

## APPLICATIONS

- ▶ Automatic test equipment
- ▶ Data acquisition
- ▶ Instrumentation
- ▶ Avionics
- ▶ Audio and video switching
- ▶ Communication systems
- ▶ Relay replacement

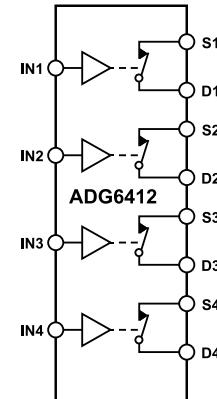
## GENERAL DESCRIPTION

The ADG6412 contains four independent single-pole/single-throw (SPST) switches. The ADG6412 switches turn on with logic 1 on the digital control inputs. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends from  $V_{SS}$  to  $V_{DD}$  - 2 V. When switches are open, signal levels up to the supplies are blocked.

The digital inputs are compatible with 5 V, 3.3 V, and 1.8 V logic inputs without the requirement for a separate digital logic supply pin.

The on-resistance profile is exceptionally flat over the full-analog input range, which ensures good linearity and low distortion when switching audio signals.

## FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT 001

Figure 1. Functional Block Diagram

## PRODUCT HIGHLIGHTS

1. Low  $R_{ON}$  of 0.5  $\Omega$ .
2. High continuous current carrying capability, see [Table 4](#) to [Table 7](#).
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG6412 can be operated from dual supplies up to  $\pm 22$  V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG6412 can be operated from a single rail power supply up to 40 V.
5. 1.8 V logic-compatible digital inputs:  $V_{INH} = 1.3$  V,  $V_{INL} = 0.8$  V.
6. No  $V_L$  logic power supply required.

## TABLE OF CONTENTS

Features.....	1	I <sub>INL</sub> and I <sub>INH</sub> .....	15
Applications.....	1	C <sub>S</sub> (Off) and C <sub>D</sub> (Off).....	15
General Description.....	1	C <sub>D</sub> (On) and C <sub>S</sub> (On).....	15
Functional Block Diagram.....	1	C <sub>IN</sub> .....	15
Product Highlights.....	1	t <sub>ON</sub> .....	15
Specifications.....	3	t <sub>OFF</sub> .....	15
Operating Supply Voltages.....	3	t <sub>D</sub> .....	15
±20 V Dual Supply.....	3	Off Isolation.....	15
36 V Single Supply.....	4	Charge Injection.....	15
Continuous Current Per Channel, Sx or Dx.....	6	Channel-to-Channel Crosstalk.....	15
Absolute Maximum Ratings.....	7	Bandwidth.....	15
Thermal Resistance.....	7	On Response.....	15
Electrostatic Discharge (ESD) Ratings.....	7	Insertion Loss.....	15
ESD Caution.....	7	Total Harmonic Distortion + Noise (THD + N) ..	15
Pin Configurations and Function Descriptions.....	8	AC Power Supply Rejection Ratio (AC PSRR).....	15
Typical Performance Characteristics.....	9	Theory of Operations.....	16
Test Circuits.....	13	Switch Architecture.....	16
Terminology.....	15	1.8 V Logic Compatibility.....	16
I <sub>DD</sub> .....	15	Applications Information.....	17
I <sub>SS</sub> .....	15	Large Voltage, High Frequency Signal Tracking.....	17
V <sub>D</sub> and V <sub>S</sub> .....	15	Power Supply Recommendations.....	17
V <sub>TRACK</sub> .....	15	High-Current Drive and Precision Current-Sense.....	17
R <sub>ON</sub> .....	15	Digital Audio Channel to Ultra-Low THD.....	17
ΔR <sub>ON</sub> .....	15	Outline Dimensions.....	18
R <sub>FLAT(ON)</sub> .....	15	Ordering Guide.....	18
I <sub>S</sub> (Off).....	15	Evaluation Boards.....	18
I <sub>D</sub> (Off).....	15		
I <sub>D</sub> (On) and I <sub>S</sub> (On).....	15		
V <sub>INL</sub> .....	15		
V <sub>INH</sub> .....	15		

## REVISION HISTORY

1/2023—Revision 0: Initial Version

## SPECIFICATIONS

## OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Supply Voltage	Min	Max	Unit
Dual Supply	$\pm 4.5$	$\pm 22$	V
Single Supply	+5	+40	V

 **$\pm 20$  V DUAL SUPPLY**

$V_{DD} = +20 \text{ V} \pm 10\%$ ,  $V_{SS} = -20 \text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 2.  $\pm 20$  V Dual-Supply Specifications

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range				V	$V_{DD} = +18 \text{ V}$ , $V_{SS} = -18 \text{ V}$
On Resistance, $R_{ON}$	0.50		$V_{DD} - 2 \text{ V}$ to $V_{SS}$	$\Omega$ typ	Source voltage ( $V_S$ ) = -18 V to +14.5 V, source current ( $I_S$ ) = -100 mA, see <a href="#">Figure 26</a>
	0.65	0.8	0.95	$\Omega$ max	$V_S = -18 \text{ V}$ to +15.5 V, $I_S = -100 \text{ mA}$
	0.54			$\Omega$ typ	
	0.7	0.85	1.0	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.003			$\Omega$ typ	$V_S = -18 \text{ V}$ to +15.5 V, $I_S = -100 \text{ mA}$
	0.085	0.1	0.1	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.003			$\Omega$ typ	$V_S = -18 \text{ V}$ to +14.5 V, $I_S = -100 \text{ mA}$
	0.035	0.035	0.035	$\Omega$ max	
	0.04			$\Omega$ typ	$V_S = -18 \text{ V}$ to +15.5 V, $I_S = -100 \text{ mA}$
	0.08	0.1	0.1	$\Omega$ max	
LEAKAGE CURRENTS					
Source Off Leakage, $I_S$ (Off)	$\pm 3.5$			nA typ	$V_{DD} = +22 \text{ V}$ , $V_{SS} = -22 \text{ V}$
					$V_S = \pm 15 \text{ V}$ , drain current ( $V_D$ ) = $\mp 15 \text{ V}$ , see <a href="#">Figure 29</a>
Drain Off Leakage, $I_D$ (Off)	$\pm 12.5$	+70/-14	+205/-14	nA max	
	$\pm 3.5$			nA typ	$V_S = \pm 15 \text{ V}$ , $V_D = \mp 15 \text{ V}$ , see <a href="#">Figure 29</a>
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 12.5$	+70/-14	+205/-14	nA max	
	$\pm 0.1$			nA typ	$V_S = V_D = \pm 15 \text{ V}$ , see <a href="#">Figure 25</a>
	$\pm 1.3$	$\pm 3$	+13/-3	nA max	
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			1.3	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.01			$\mu\text{A}$ typ	Input voltage ( $V_{IN}$ ) = GND voltage ( $V_{GND}$ ) or 5 V
			$\pm 0.15$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4.6			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, $t_{ON}$	366			ns typ	Load resistance ( $R_L$ ) = 300 $\Omega$ , load capacitance ( $C_L$ ) = 35 pF
	439	481	529	ns max	$V_S = 10 \text{ V}$ , see <a href="#">Figure 32</a>
Off Time, $t_{OFF}$	169			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	204	204	204	ns max	$V_S = 10 \text{ V}$ , see <a href="#">Figure 32</a>
Charge Injection, $Q_{INJ}$	-2.2			nC typ	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see <a href="#">Figure 33</a>
Off Isolation	-77			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 100 kHz, see <a href="#">Figure 28</a>

## SPECIFICATIONS

Table 2.  $\pm 20$  V Dual-Supply Specifications (Continued)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 100 kHz, see <a href="#">Figure 27</a>
Total Harmonic Distortion + Noise, THD + N	0.002			% typ	$R_L = 1 \text{ k}\Omega$ , 20 V p-p, frequency = 20 Hz to 20 kHz, see <a href="#">Figure 30</a>
Total Harmonic Distortion, THD	-127			dB typ	$R_L = 1 \text{ k}\Omega$ , 20 V p-p, frequency = 1 kHz
	-101			dB typ	$R_L = 1 \text{ k}\Omega$ , 20 V p-p, frequency = 20 kHz
	-85			dB typ	$R_L = 1 \text{ k}\Omega$ , 20 V p-p, frequency = 100 kHz
-3 dB Bandwidth	184			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , signal = 0 dBm, see <a href="#">Figure 31</a>
Insertion Loss	-0.04			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 1 MHz see <a href="#">Figure 31</a>
Source Off Capacitance, $C_S$ (Off)	70			pF typ	$V_S = 0 \text{ V}$ , frequency = 1 MHz
Drain Off Capacitance, $C_D$ (Off)	70			pF typ	$V_S = 0 \text{ V}$ , frequency = 1 MHz
Drain On Capacitance, $C_D$ (On), Source On Capacitance, $C_S$ (On)	25			pF typ	$V_S = 0 \text{ V}$ , frequency = 1 MHz
Match On Capacitance, $C_{\text{MATCH}}$ (On)	0.83			pF typ	$V_S = 0 \text{ V}$ , frequency = 1 MHz
POWER REQUIREMENTS					
Power Supply Current, $I_{DD}$	170			µA typ	$V_{DD} = +22 \text{ V}$ , $V_{SS} = -22 \text{ V}$
	260		260	µA max	Digital inputs = 0 V or 5 V
	225			µA typ	
	330		330	µA max	Digital inputs = 1.3 V
Negative Supply Current, $I_{SS}$	85			µA typ	Digital inputs = 0 V or 5 V
	140		140	µA max	

## 36 V SINGLE SUPPLY

$V_{DD} = 36 \text{ V} \pm 10\%$ ,  $V_{SS} = 0 \text{ V}$ , GND = 0 V, unless otherwise noted.

Table 3. 36 V Single-Supply Specifications

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to $V_{DD} - 2 \text{ V}$	V	$V_{DD} = 32.4 \text{ V}$ , $V_{SS} = 0 \text{ V}$
On Resistance, $R_{ON}$	0.50			Ω typ	Source voltage ( $V_S$ ) = 0 V to 28.9 V, source current ( $I_S$ ) = -100 mA, see <a href="#">Figure 26</a>
	0.65	0.8	0.95	Ω max	
	0.54			Ω typ	$V_S = 0 \text{ V}$ to 29.9 V, $I_S = -100 \text{ mA}$
	0.7	0.85	1.0	Ω max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.003			Ω typ	$V_S = 0 \text{ V}$ to 29.9 V, $I_S = -100 \text{ mA}$
	0.085	0.1	0.1	Ω max	
On-Resistance Flatness, $R_{\text{FLAT(ON)}}$	0.003			Ω typ	$V_S = 0 \text{ V}$ to 28.9 V, $I_S = -100 \text{ mA}$
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	$V_S = 0 \text{ V}$ to 29.9 V, $I_S = -100 \text{ mA}$
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, $I_S$ (Off)	±3.5			nA typ	$V_{DD} = 39.6 \text{ V}$ , $V_{SS} = 0 \text{ V}$
	±12.5	+70/-14	+205/-14	nA max	$V_S = 1 \text{ V}/30 \text{ V}$ , drain voltage ( $V_D$ ) = 30 V/1 V, see <a href="#">Figure 29</a>

## SPECIFICATIONS

Table 3. 36 V Single-Supply Specifications (Continued)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, $I_D$ (Off)	±3.5			nA typ	$V_S = 1 \text{ V}/30 \text{ V}$ , $V_D = 30 \text{ V}/1 \text{ V}$ , see Figure 29
Channel On Leakage, $I_D$ (On), $I_S$ (On)	±12.5 ±0.1 ±1.3	+70/-14 ±3	+205/-14 +13/-3	nA max nA typ nA max	$V_S = V_D = 1 \text{ V}/30 \text{ V}$ , see Figure 25
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			1.3	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ , or $I_{INH}$	0.01			μA typ ±0.15	Input voltage ( $V_{IN}$ ) = GND voltage ( $V_{GND}$ ) or 5 V
Digital Input Capacitance, $C_{IN}$	4.6			μA max pF typ	
DYNAMIC CHARACTERISTICS					
On Time, $t_{ON}$	216			ns typ	Load resistance ( $R_L$ ) = 300 Ω, load capacitance ( $C_L$ ) = 35 pF
	256	276	299	ns max	$V_S = 18 \text{ V}$ , see Figure 32
Off Time, $t_{OFF}$	261			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	309	319	329	ns max	$V_S = 18 \text{ V}$ , see Figure 32
Charge Injection, $Q_{INJ}$	-2.0			nC typ	$V_S = 18 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 33
Off Isolation	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 100 kHz, see Figure 28
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 100 kHz, see Figure 27
Total Harmonic Distortion + Noise, THD + N	0.005			% typ	$R_L = 1 \text{ k}\Omega$ , 18 V p-p, frequency = 20 Hz to 20 kHz, see Figure 30
Total Harmonic Distortion, THD	-113			dB typ	$R_L = 1 \text{ k}\Omega$ , 18 V p-p, frequency = 1 kHz
	-87			dB typ	$R_L = 1 \text{ k}\Omega$ , 18 V p-p, frequency = 20 kHz
	-73			dB typ	$R_L = 1 \text{ k}\Omega$ , 18 V p-p, frequency = 100 kHz
-3 dB Bandwidth	134			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , signal = 0 dBm, see Figure 31
Insertion Loss	-0.05			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency = 1 MHz, see Figure 31
Source Off Capacitance, $C_S$ (Off)	72			pF typ	$V_S = 18 \text{ V}$ , frequency = 1 MHz
Drain Off Capacitance, $C_D$ (Off)	72			pF typ	$V_S = 18 \text{ V}$ , frequency = 1 MHz
Drain On Capacitance, $C_D$ (On), Source On Capacitance, $C_S$ (On)	26			pF typ	$V_S = 18 \text{ V}$ , frequency = 1 MHz
Match On Capacitance, $C_{MATCH}$ (On)	0.84			pF typ	$V_S = 18 \text{ V}$ , frequency = 1 MHz
POWER REQUIREMENTS					
Power Supply Current, $I_{DD}$	170			μA typ	$V_{DD} = 39.6 \text{ V}$
	260		260	μA max	Digital inputs = 0 V or 5 V
	225			μA typ	Digital inputs = 1.3 V
	330		330	μA max	
Negative Supply Current, $I_{SS}$	85			μA typ	Digital inputs = 0 V or 5 V
	140		140	μA max	

**SPECIFICATIONS****CONTINUOUS CURRENT PER CHANNEL, SX OR DX****Table 4. One Channel On, Per Channel Specifications**

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx  $V_{DD} = +20\text{ V}$ , $V_{SS} = -20\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	847	325	123	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$
$V_{DD} = 36\text{ V}$ , $V_{SS} = 0\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	847	325	123	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$

**Table 5. Two Channels On, Per Channel Specifications**

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx  $V_{DD} = +20\text{ V}$ , $V_{SS} = -20\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	646	289	120	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$
$V_{DD} = 36\text{ V}$ , $V_{SS} = 0\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	646	289	120	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$

**Table 6. Three Channels On, Per Channel Specifications**

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx  $V_{DD} = +20\text{ V}$ , $V_{SS} = -20\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	548	265	117	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$
$V_{DD} = 36\text{ V}$ , $V_{SS} = 0\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	548	265	117	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$

**Table 7. Four Channels On, Per Channel Specifications**

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx  $V_{DD} = +20\text{ V}$ , $V_{SS} = -20\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	488	248	115	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$
$V_{DD} = 36\text{ V}$ , $V_{SS} = 0\text{ V}$ LFCSP ( $\theta_{JA} = 44^\circ\text{C/W}$ )	488	248	115	mA maximum	$V_S = V_{SS}$ to $V_{DD} - 3.5\text{ V}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 8. Absolute Maximum Ratings

Parameter	Rating
$V_{DD}$ to $V_{SS}$	46 V
$V_{DD}$ to GND	-0.3 V to +46 V
$V_{SS}$ to GND	+0.3 V to -46 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to +6 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins <sup>2</sup>	2.6 A (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx <sup>2</sup>	Data <sup>3</sup> + 15%
Temperature	
Operating Range	-40°C to +125°C
Storage Range	-65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

<sup>1</sup> Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

<sup>3</sup> See Table 4 to Table 7.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and  $\theta_{JCB}$  is the junction to the bottom of the case value.

Table 9. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JCB}$	Unit
CP-16-17 <sup>1</sup>	44	17.4	°C/W

<sup>1</sup> Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for the ADG6412

Table 10. ADG6412, 16-Lead LFCSP

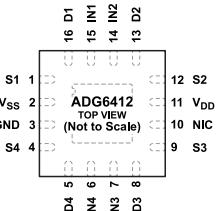
ESD Model	Withstand Threshold (V)	Class
HBM	±2000	2
FICDM	±1250	C3

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
 1. NIC = NOT INTERNALLY CONNECTED.  
 2. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR  
 INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM  
 THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE  
 SOLDERED TO THE SUBSTRATE,  $V_{SS}$ .

002

Figure 2. Pin Configuration

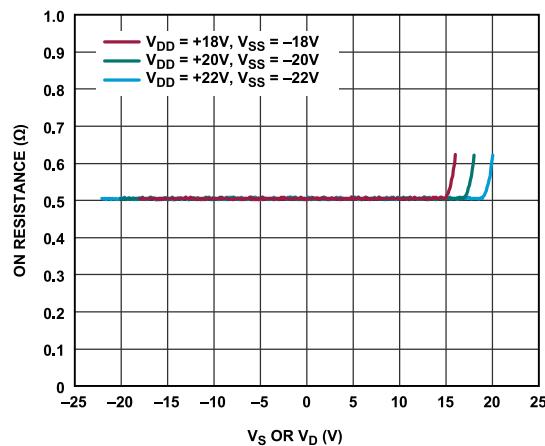
Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	S1	Source Terminal 1. This pin can be an input or output.
2	$V_{SS}$	Most Negative Power-Supply Potential. Decouple the $V_{SS}$ pin using a 0.1 $\mu F$ capacitor to GND.
3	GND	Ground (0 V) Reference.
4	S4	Source Terminal 4. This pin can be an input or output.
5	D4	Drain Terminal 4. This pin can be an input or output.
6	IN4	Logic Control Input 4.
7	IN3	Logic Control Input 3.
8	D3	Drain Terminal 3. This pin can be an input or output.
9	S3	Source Terminal 3. This pin can be an input or output.
10	NIC	Not Internally Connected.
11	$V_{DD}$	Most Positive Power-Supply Potential. Decouple the $V_{DD}$ pin using a 0.1 $\mu F$ capacitor to GND.
12	S2	Source Terminal 2. This pin can be an input or output.
13	D2	Drain Terminal 2. This pin can be an input or output.
14	IN2	Logic Control Input 2.
15	IN1	Logic Control Input 1.
16	D1	Drain Terminal 1. This pin can be an input or output.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $V_{SS}$ .

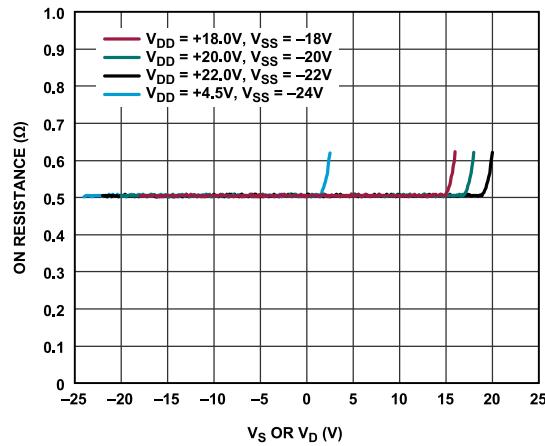
Table 12. ADG6412 Truth Table

INx	Switch Condition
1	On
0	Off

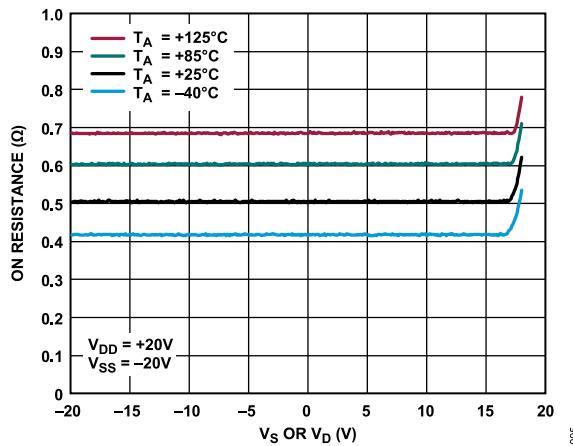
## TYPICAL PERFORMANCE CHARACTERISTICS



003

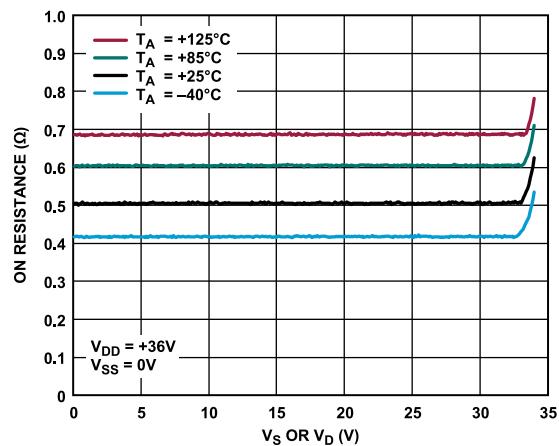


004



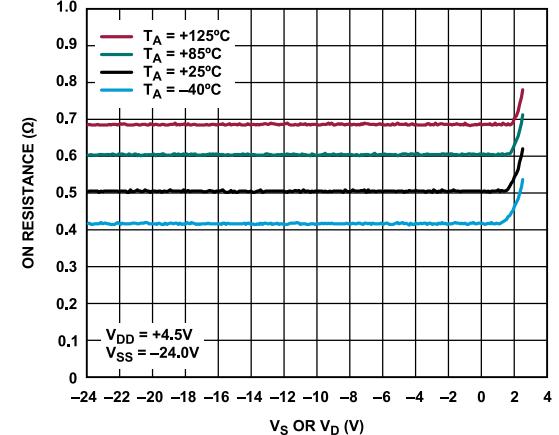
005

Figure 5.  $R_{ON}$  as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, ±20 V Dual Supply



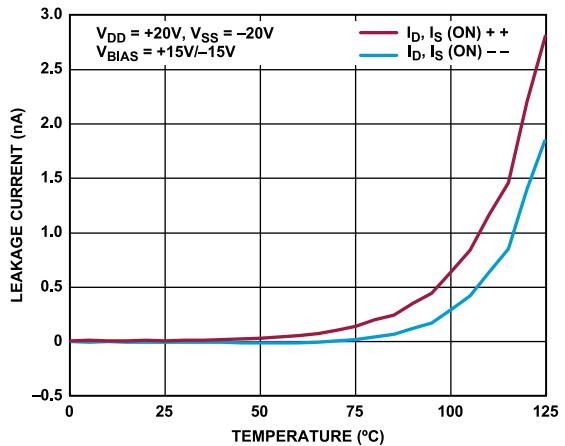
006

Figure 6.  $R_{ON}$  as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, 36 V Single Supply



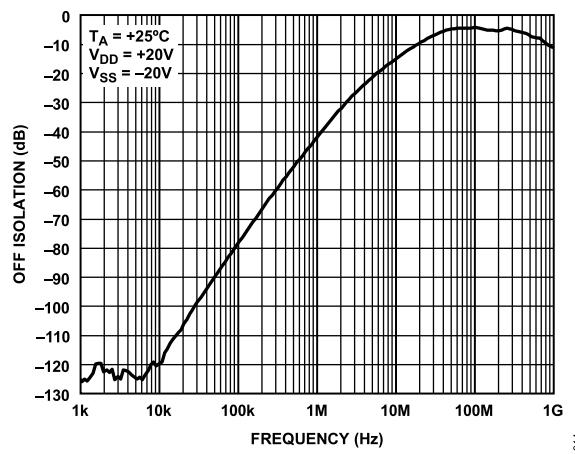
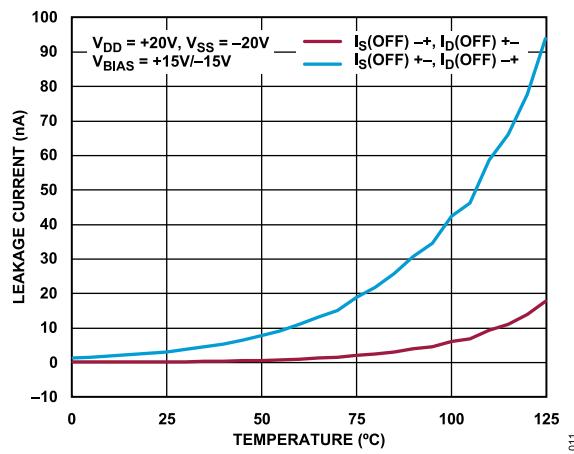
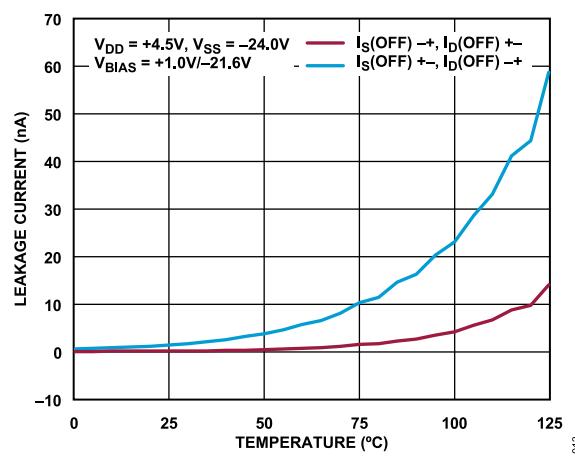
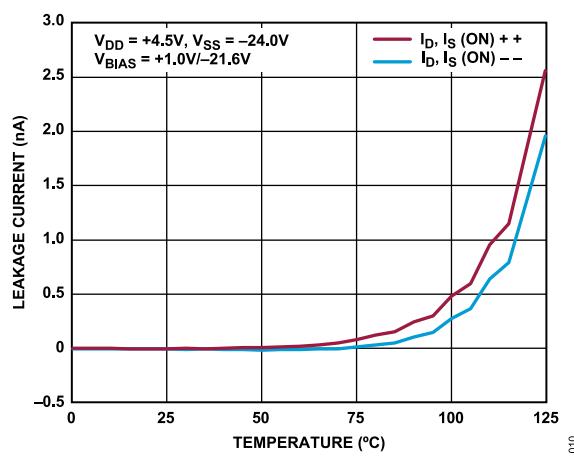
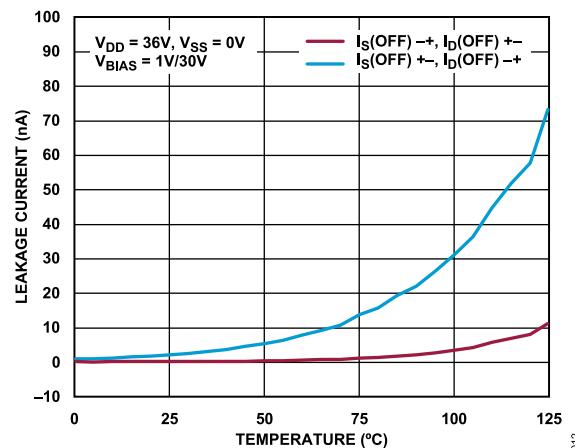
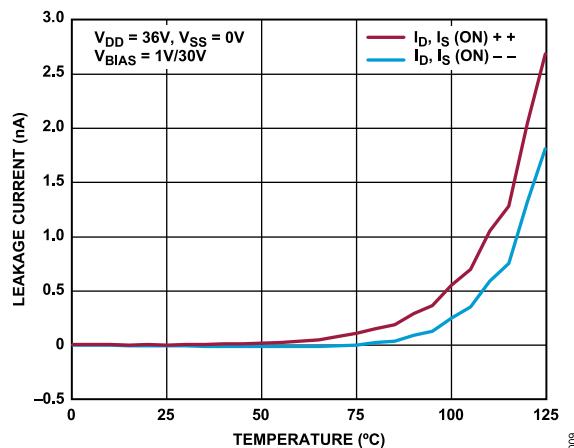
007

Figure 7.  $R_{ON}$  as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, Asymmetric Single Supply



008

## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS

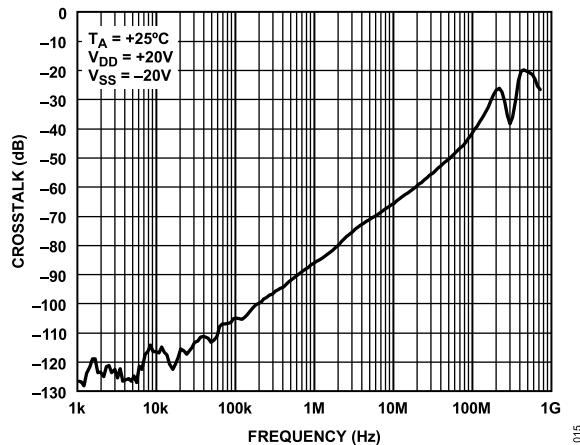
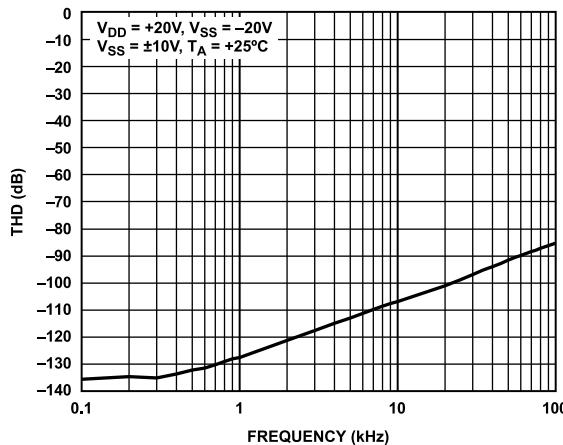
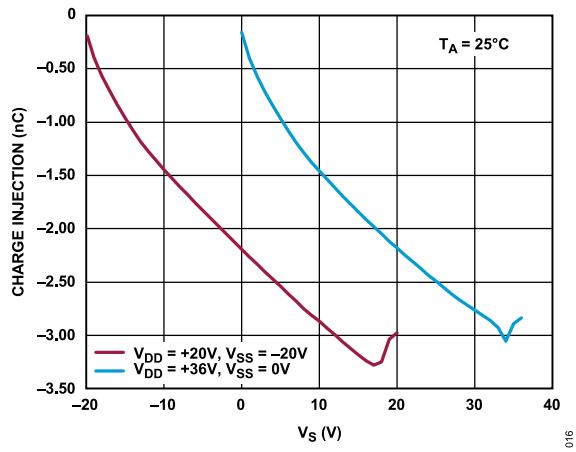
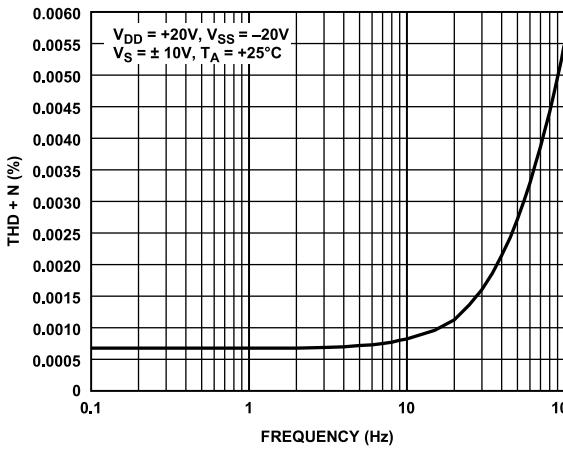
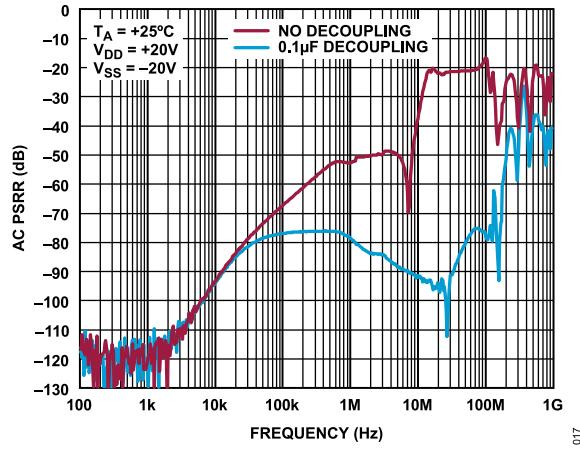
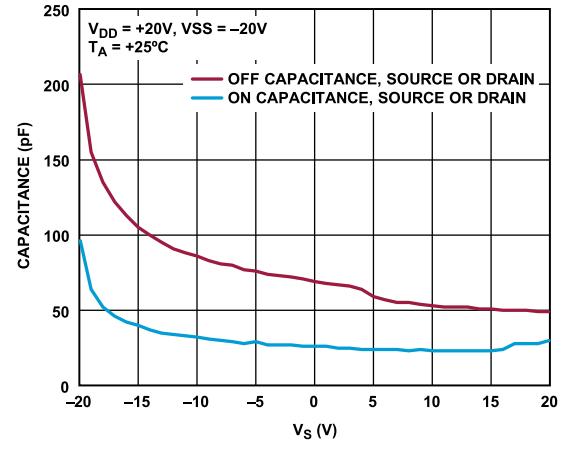
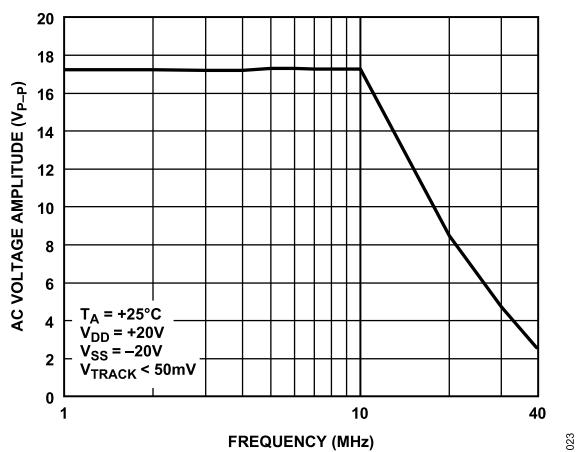
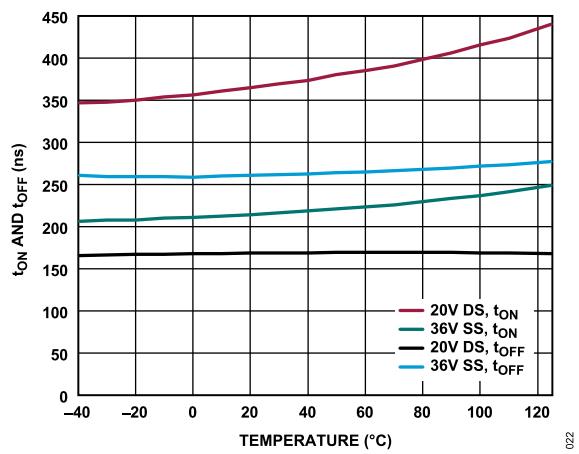
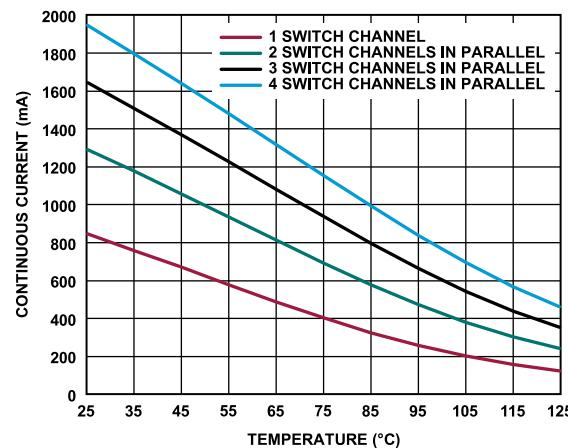
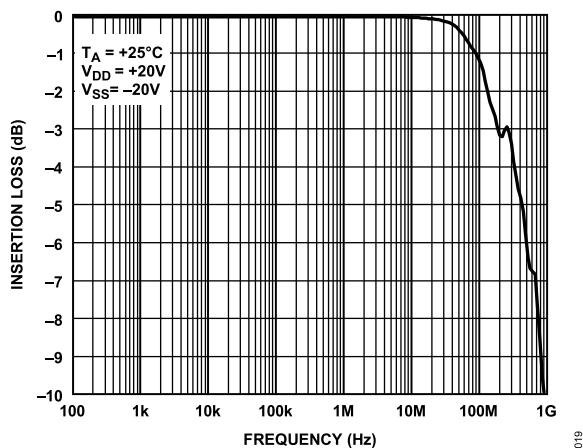
Figure 15. Crosstalk vs. Frequency,  $\pm 20$  V Dual SupplyFigure 18. THD vs. Frequency,  $\pm 20$  V Dual Supply

Figure 16. Charge Injection vs. VS

Figure 19. THD + N vs. Frequency,  $\pm 20$  V Dual SupplyFigure 17. AC PSRR vs. Frequency,  $\pm 20$  V Dual SupplyFigure 20. Capacitance vs. VS,  $\pm 20$  V Dual Supply

## TYPICAL PERFORMANCE CHARACTERISTICS



## TEST CIRCUITS

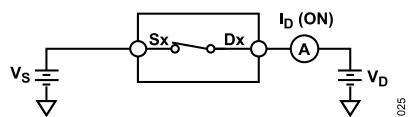


Figure 25. On Leakage

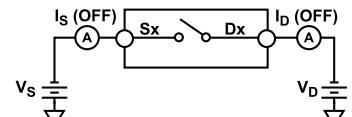


Figure 29. Off Leakage

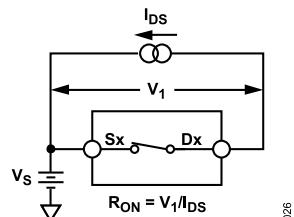


Figure 26. On Resistance

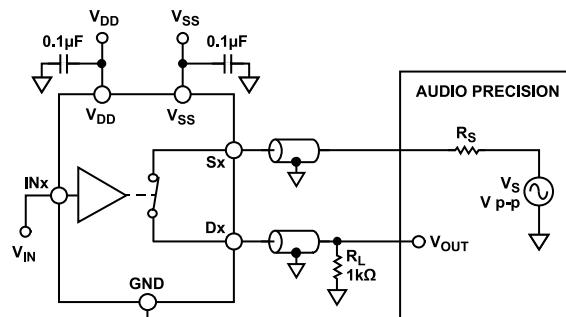
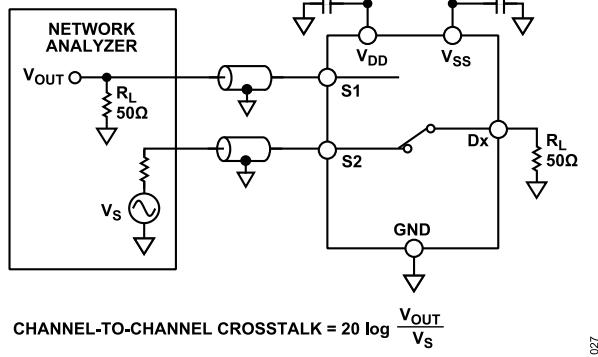


Figure 30. THD + Noise



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 27. Channel-to-Channel Crosstalk

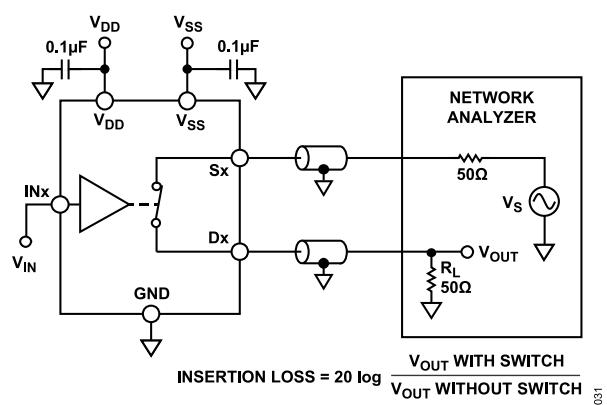


Figure 31. Bandwidth

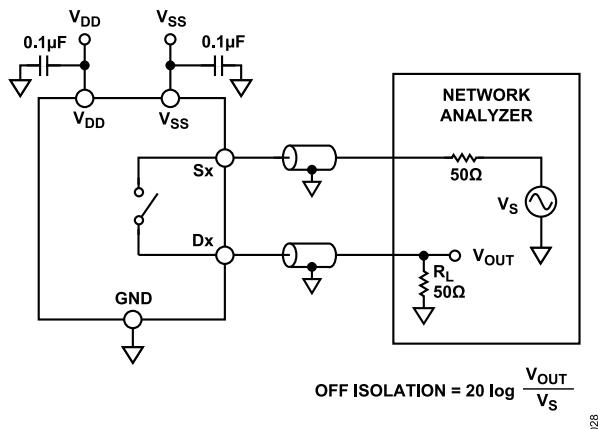


Figure 28. Off Isolation

## TEST CIRCUITS

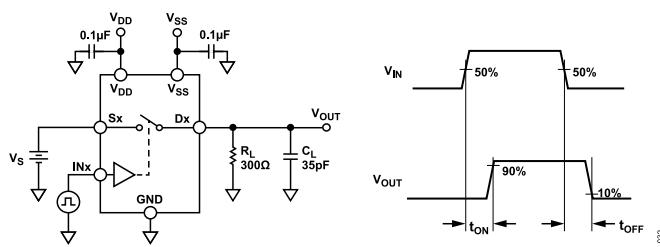


Figure 32. Switching Times

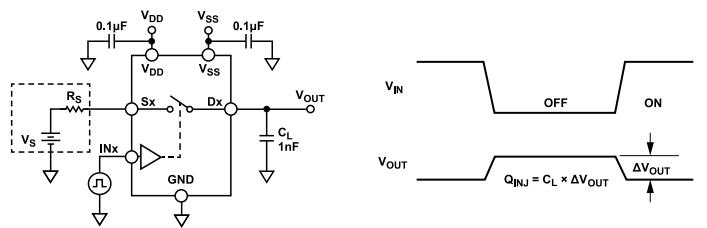


Figure 33. Charge Injection

## TERMINOLOGY

### **I<sub>DD</sub>**

The positive supply current.

### **I<sub>SS</sub>**

The negative supply current.

### **V<sub>D</sub> and V<sub>S</sub>**

The analog voltage on Terminal D and Terminal S, respectively.

### **V<sub>TRACK</sub>**

The difference between V<sub>S</sub> and V<sub>D</sub>.

### **R<sub>ON</sub>**

The ohmic resistance between Terminal D and Terminal S.

### **ΔR<sub>ON</sub>**

The difference between the R<sub>ON</sub> of any two channels.

### **R<sub>FLAT(ON)</sub>**

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### **I<sub>S</sub> (Off)**

The source leakage current with the switch off.

### **I<sub>D</sub> (Off)**

The drain leakage current with the switch off.

### **I<sub>D</sub> (On) and I<sub>S</sub> (On)**

The channel leakage current with the switch on.

### **V<sub>INL</sub>**

The maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

The minimum input voltage for Logic 1.

### **I<sub>INL</sub> and I<sub>INH</sub>**

The input current of the digital input when high or when low.

### **C<sub>S</sub> (Off) and C<sub>D</sub> (Off)**

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

### **C<sub>D</sub> (On) and C<sub>S</sub> (On)**

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

### **C<sub>IN</sub>**

The digital input capacitance.

### **t<sub>ON</sub>**

The delay between applying the digital control input and the output switching on.

### **t<sub>OFF</sub>**

The delay between applying the digital control input and the output switching off.

### **t<sub>D</sub>**

The off-time measured between the 80% point of both switches when switching from one address state to another.

### **Off Isolation**

A measure of unwanted signal coupling through an off switch.

### **Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### **Channel-to-Channel Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### **Bandwidth**

The frequency at which the output is attenuated by 3 dB.

### **On Response**

The frequency response of the on switch.

### **Insertion Loss**

The loss due to the on resistance of the switch.

### **Total Harmonic Distortion + Noise (THD + N)**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### **AC Power Supply Rejection Ratio (AC PSRR)**

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p.

## THEORY OF OPERATIONS

### SWITCH ARCHITECTURE

The ADG6412 contains four independent SPST, N-channel diffused metal-oxide semiconductor (NDMOS) switches, which allows for an excellent  $R_{ON}$  performance. Using an NDMOS only architecture results in a reduction of signal headroom, meaning signals are limited to  $V_{DD} - 2$  V. To achieve the lowest on resistance, on-resistance flatness, and total harmonic distortion, it is recommended the signal stays below  $V_{DD} - 3.5$  V.

To guarantee correct operation of the ADG6412, a minimum of 0.1  $\mu$ F decoupling capacitors are required on both the  $V_{DD}$  and  $V_{SS}$  supply pins.

The ADG6412 is compatible with single-supply systems that have a  $V_{DD}$  of up to 40 V, dual-supply systems of up to  $\pm 22$  V, as well as asymmetric power supplies.

### 1.8 V LOGIC COMPATIBILITY

For ease of use, the ADG6412 does not have a  $V_L$  logic reference voltage. The digital inputs are compatible with 1.8 V logic levels over the full-operating supply range. The limits for 1.8 V logic are:  $V_{INH} = 1.3$  V,  $V_{INL} = 0.8$  V. 1.8 V logic-level inputs enable the ADG6412 to be compatible with processors that have lower supply rails, eliminating the need for an external voltage translator.

If full 1.8 V and 1.2 V JEDEC compliance is required, refer to the Analog Devices, Inc., L range part numbers, such as the [ADG1412L](#).

## APPLICATIONS INFORMATION

## LARGE VOLTAGE, HIGH FREQUENCY SIGNAL TRACKING

Figure 23 shows the voltage range and corresponding frequencies that the ADG6412 can reliably convey. The tracking voltage ( $V_{TRACK}$ ) in the figure shows the source voltage and the drain voltage difference, which is less than 50 mV for a given amplitude and frequency. For large voltage, high frequency signals, the frequency must be kept below 10 MHz. If the required frequency is greater than 10 MHz, decrease the signal range appropriately to ensure signal integrity.

## POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of high performance signal chains.

An example of a bipolar power solution is shown in Figure 34. The LT3463 (a dual switching regulator) generates a positive and negative supply rail for the ADG6412, an amplifier, and/or a precision converter in a typical signal chain. Also, two optional low-dropout regulators (LDOs), the ADP7142 and ADP7182 (positive and negative LDOs, respectively) are shown in Figure 34, which can reduce the output ripple of the LT3463 in ultra-low noise sensitive applications.

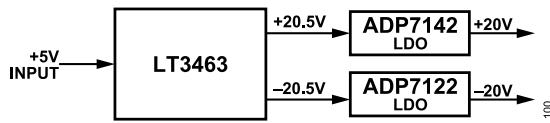


Figure 34. Bipolar Power Solution

Table 13. Recommended Power Management Devices

Product	Description
LT3463	Dual micropower, DC to DC converter with Schottky diodes
ADP7142	40 V, 200 mA, low noise, CMOS, LDO linear regulator
ADP7182	-28 V, -200 mA, low noise, LDO linear regulator

## HIGH-CURRENT DRIVE AND PRECISION CURRENT-SENSE

Figure 35 shows an example application for the ADG6412. In automated test equipment (ATE) and instrumentation applications, when driving a current to a device under test (DUT), there is a requirement to have multiple sense resistors for multiple current ranges to facilitate large current output ranges from micro amps to amps. The low on-resistance of the ADG6412 is ideally suited to switching the force current output path in this application because it allows for high continuous current carrying as seen in Table 4 to Table 7.

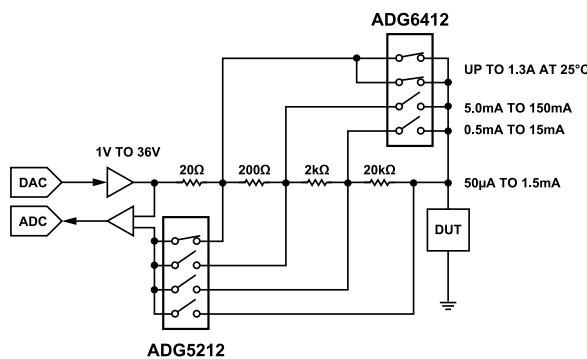


Figure 35. High-Current Drive and Precision Current-Sense Application

## DIGITAL AUDIO CHANNEL TO ULTRA-LOW THD

Figure 36 shows an example application for the ADG6412. For precision audio signal chains, THD is a key specification. The THD performance of a switch is related to the on-resistance flatness, and the ADG6412 has exceptionally low on-resistance flatness of approximately 3 mΩ. Here, the ADG6412 is set up as a gain selection switch for an audio preamplifier to allow flexibility for user to select multiple gain ranges. The THD performance of the ADG6412 maximizes the signal fidelity and the low on-resistance minimizes any gain error in the system.

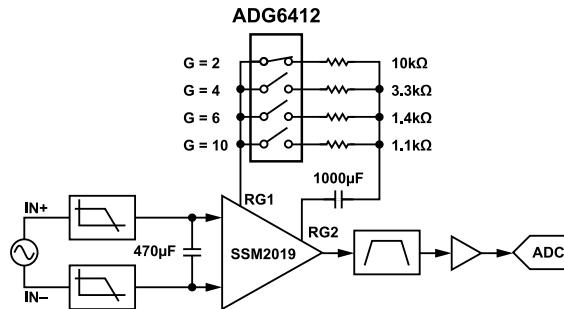
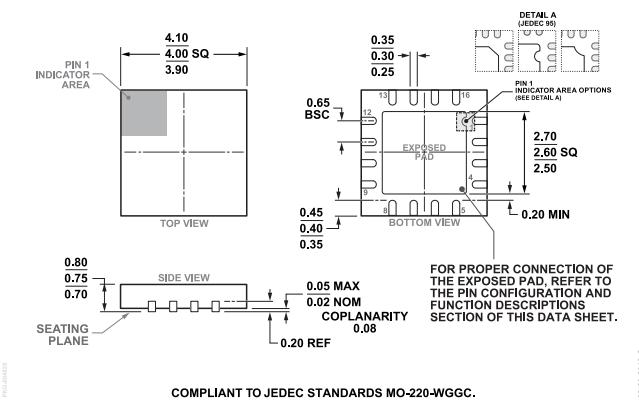


Figure 36. Digital Audio Channel to Ultra-Low THD Application

## OUTLINE DIMENSIONS



**Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP]**  
**4 mm × 4 mm Body and 0.75 mm Package Height**  
**(CP-16-17)**  
*Dimensions shown in millimeters*

Updated: December 20, 2022

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADG6412BCPZ-REEL7	-40°C to +125°C	LFCSP:LEADFRM CHIP SCALE	Reel, 1500	CP-16-17

<sup>1</sup> Z = RoHS-Compliant Part.

## EVALUATION BOARDS

**Table 14. Evaluation Boards**

Model <sup>1</sup>	Description
EVAL-ADG6412EBZ	Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[ADG6412BCPZ-REEL7](#) [EVAL-ADG6412EBZ](#)