4 Ω R_{ON}, 8-Channel iCMOS Multiplexers with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- 4.7 Ω maximum on resistance at 25°C at ±15 V dual supply
- 0.5 Ω typical on-resistance flatness at 25°C at ±15 V dual supply
- Fully specified at ±15 V, +12 V, and ±5 V
- V_L supply for low-logic level compatibility
  - 1.8 V JEDEC standard compliant (JESD8-7A)
  - 1.2 V JEDEC standard compliant (JESD8-12A.01)
- Rail-to-rail operation
- Break-before-make switching action
- 24-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- FPGA and microcontroller systems
- Relay replacement
- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Communication systems

GENERAL DESCRIPTION

The ADG1408L is a monolithic *i*CMOS® eight channel analog multiplexer. The ADG1408L switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. An EN input is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

An external low voltage V_L supply provides flexibility for lower logic control. The ADG1408L is both 1.2 V and 1.8 V JEDEC standard compliant.

FUNCTIONAL BLOCK DIAGRAM

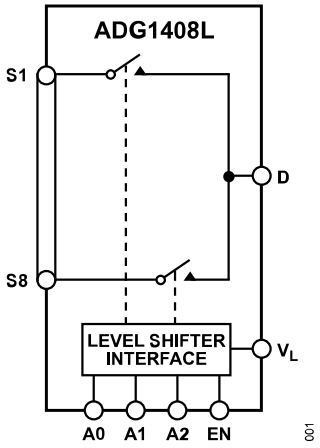

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. 4 Ω typical on resistance at 25°C and at ±15 V dual supply.
2. 0.5 Ω typical on-resistance flatness at 25°C and at ±15 V dual supply.
3. V_L supply for low-logic level compatibility.
4. JEDEC standard compliant for both 1.2 V and 1.8 V logic levels.
5. Guaranteed switch off when digital inputs are floating.
6. 24-lead, 4 mm × 4 mm LFCSP.

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REVISION HISTORY

5/2023—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Parameter	Min	Max	Unit
Dual Supply	±4.5	±16.5	V
Single Supply	5	16.5	V

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 2. ±15 V Dual-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	4			Ω typ	Source voltage (V_S) = ±10 V, source current (I_S) = −10 mA, see Figure 25
	4.7	5.7	6.7	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.2			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.78	0.85	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.5			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.72	0.77	0.92	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.04			nA typ	V_S = ±10 V, drain voltage (V_D) = ∓10 V, see Figure 26
	±0.2	±0.6	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.04			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 26
	±0.45	±2	±30	nA max	
Channel On Leakage, I_D (On), I_D (On)	±0.1			nA typ	V_S = V_D = ±10 V, see Figure 27
	±1.5	±3	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 * V_L	V min	
Input Low Voltage, V_{INL}			0.35 * V_L	V max	
Input High Current, I_{INH}	55			µA typ	Ax voltage (V_{Ax}) = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			µA typ	V_{Ax} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current, I_{INL}	0.2			µA typ	V_{Ax} = 0 V
			0.8	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	160			ns typ	Load resistance (R_L) = 100 Ω, load capacitance (C_L) = 35 pF
	192	223	247	ns max	V_S = 10 V, see Figure 28
Break-Before-Make Time Delay, t_{BBM}	40			ns typ	R_L = 100 Ω, C_L = 35 pF
			28	ns min	S1 voltage (V_{S1}) = S2 voltage (V_{S2}) = 10 V, see Figure 29
Enable Delay On Time, t_{ON} (EN)	117			ns typ	R_L = 100 Ω, C_L = 35 pF
	149	166	184	ns max	V_S = 10 V, see Figure 30
Enable Delay Off Time, t_{OFF} (EN)	139			ns typ	R_L = 100 Ω, C_L = 35 pF
	166	189	207	ns max	V_S = 10 V, see Figure 30

SPECIFICATIONS

Table 2. ±15 V Dual-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Charge Injection	−50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency (f) = 1 MHz, see Figure 32
Channel to Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Total Harmonic Distortion, THD	-101			dB typ	R_L = 10 kΩ, 15 V p-p, f = 20 kHz, see Figure 35
	-88			dB typ	R_L = 10 kΩ, 15 V p-p, f = 100 kHz, see Figure 35
Total Harmonic Distortion Plus Noise, THD + N	0.0013			% typ	R_L = 10 kΩ, 15 V p-p, f = 20 kHz, see Figure 35
	0.0039			% typ	R_L = 10 kΩ, 15 V p-p, f = 100 kHz, see Figure 35
−3 dB Bandwidth	60			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 34
Insertion Loss	0.24			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Source Off Capacitance, C_S (Off)	14			pF typ	V_S = 0 V, f = 1 MHz
Drain Off Capacitance, C_D (Off)	80			pF typ	V_S = 0 V, f = 1 MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	135			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Positive Supply Current, I_{DD}	55			µA typ	V_{Ax} = 0 V or V_L
			95	µA max	
Negative Supply Current, I_{SS}	0.001			µA typ	V_{Ax} = 0 V or V_L
			1	µA max	
Digital Supply Current, I_{VL}	45			µA typ	V_{Ax} = V_L = 1.8 V
			70	µA max	
	30			µA typ	V_{Ax} = V_L = 1.2 V
			55	µA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 3. 12 V Single-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V
Analog Signal Range			0 to V_{DD}	V	
R_{ON}	6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA, see Figure 25
	8	9.5	11.2	Ω max	
ΔR_{ON}	0.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.82	0.85	1.1	Ω max	
$R_{FLAT(ON)}$	1.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	2.4	2.7	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
I_S (Off)	±0.04			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 26
	±0.2	±0.6	±5	nA max	
I_D (Off)	±0.04			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 26
	±0.45	±1	±37	nA max	
I_D (On), I_S (On)	±0.06			nA typ	V_S = V_D = 1 V to 10 V, see Figure 27
	±0.44	±1.3	±32	nA max	
DIGITAL INPUTS					
V_{INH}			0.65 × V_L	V min	
V_{INL}			0.35 × V_L	V max	

SPECIFICATIONS

Table 3. 12 V Single-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_{INH}	55			µA typ	V_{Ax} = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			µA typ	V_{Ax} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
I_{INL}	0.2			µA typ	V_{Ax} = 0 V
			0.8	µA max	
Digital C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
$t_{TRANSITION}$	228			ns typ	R_L = 100 Ω, C_L = 35 pF
	287	333	370	ns max	V_S = 8 V, see Figure 28
t_{BBM}	90			ns typ	R_L = 100 Ω, C_L = 35 pF
			57	ns min	V_{S1} = V_{S2} = 8 V, see Figure 29
t_{ON} (EN)	183			ns typ	R_L = 100 Ω, C_L = 35 pF
	239	274	304	ns max	V_S = 8 V, see Figure 30
t_{OFF} (EN)	161			ns typ	R_L = 100 Ω, C_L = 35 pF
	201	226	247	ns max	V_S = 8 V, see Figure 30
Charge Injection	−12			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 32
Channel to Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
THD	−90			dB typ	R_L = 10 kΩ, 5 V p-p, f = 20 kHz, see Figure 35
	−83			dB typ	R_L = 10 kΩ, 5 V p-p, f = 100 kHz, see Figure 35
THD + N	0.0034			% typ	R_L = 10 kΩ, 5 V p-p, f = 20 kHz, see Figure 35
	0.0068			% typ	R_L = 10 kΩ, 5 V p-p, f = 100 kHz, see Figure 35
−3 dB Bandwidth	36			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 34
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 34
C_S (Off)	20			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	120			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	170			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
I_{DD}	55			µA typ	V_{Ax} = 0 V or V_L
			95	µA max	
I_{VL}	45			µA typ	V_{Ax} = V_L = 1.8 V
			70	µA max	
	30			µA typ	V_{Ax} = V_L = 1.2 V
			55	µA max	

SPECIFICATIONS

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 4. ±5 V Dual-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5 V, V_{SS} = −4.5 V
Analog Signal Range			V_{SS} to V_{DD}	V	
R_{ON}	7			Ω typ	V_S = ±4.5 V, I_S = −10 mA, see Figure 25
	9	10.5	12	Ω max	
ΔR_{ON}	0.3			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.78	0.91	1.1	Ω max	
$R_{FLAT(ON)}$	1.5			Ω typ	V_S = ±4.5 V; I_S = −10 mA
	2.4	2.7	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_S (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, see Figure 26
	±0.2	±0.6	±5	nA max	
I_D (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, see Figure 26
	±0.45	±0.8	±20	nA max	
I_D (On), I_S (On)	±0.04			nA typ	V_S = V_D = ±4.5 V, see Figure 27
	±0.3	±1.1	±22	nA max	
DIGITAL INPUTS					
V_{INH}			0.65 × V_L	V min	
V_{INL}			0.35 × V_L	V max	
I_{INH}	55			μA typ	V_{Ax} = V_L = 1.8 V, see the Theory of Operations section
			90	μA max	
	40			μA typ	V_{Ax} = V_L = 1.2 V, see the Theory of Operations section
			65	μA max	
I_{INL}	0.2			μA typ	V_{Ax} = 0 V
			0.8	μA max	
C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
$t_{TRANSITION}$	314			ns typ	R_L = 100 Ω, C_L = 35 pF
	414	472	517	ns max	V_S = 3 V, see Figure 28
t_{BBM}	90			ns typ	R_L = 100 Ω, C_L = 35 pF
			59	ns min	V_{S1} = V_{S2} = 3 V, see Figure 29
t_{ON} (EN)	265			ns typ	R_L = 100 Ω, C_L = 35 pF
	356	408	445	ns max	V_S = 3 V, see Figure 30
t_{OFF} (EN)	244			ns typ	R_L = 100 Ω, C_L = 35 pF
	316	353	379	ns max	V_S = 3 V, see Figure 30
Charge Injection	−10			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 32
Channel to Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
THD	−94			dB typ	R_L = 10 kΩ, 5 V p-p, f = 20 kHz, see Figure 35
	−82			dB typ	R_L = 10 kΩ, 5 V p-p, f = 100 kHz, see Figure 35
THD + N	0.0024			% typ	R_L = 10 kΩ, 5 V p-p, f = 20 kHz, see Figure 35
	0.0072			% typ	R_L = 10 kΩ, 5 V p-p, f = 100 kHz, see Figure 35
−3 dB Bandwidth	40			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 34
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34

SPECIFICATIONS

Table 4. ±5 V Dual-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_S (Off)	20			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	130			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	180			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	55			µA typ	V_{Ax} = 0 V or V_L
			95	µA max	
I_{SS}	0.001			µA typ	V_{Ax} = 0 V or V_L
			1	µA max	
I_{VL}	45			µA typ	V_{Ax} = V_L = 1.8 V
			70	µA max	
	30			µA typ	V_{Ax} = V_L = 1.2 V
			55	µA max	

CONTINUOUS CURRENT PER CHANNEL, SX OR D

Table 5. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx or D (θ_{JA} = 64.04 °C/W)[1]				
V_{DD} = +15 V, V_{SS} = −15 V	233	89	29	mA max
V_{DD} = +12 V, V_{SS} = 0 V	206	84	29	mA max
V_{DD} = +5 V, V_{SS} = −5 V	198	83	29	mA max

[1] Sx refers to the S1 to S8 pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +2.25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V, or 30 mA, whichever occurs first
Digital Inputs[2]	GND − 0.3 V to 2.25 V, or 30 mA, whichever occurs first
Continuous Current, Sx or D[3]	Data[4] + 15%.
Peak Current, Sx or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	532 mA
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak (RoHS Compliant)	As per JEDEC J-STD-020

1 Overvoltages at the Ax, EN, Sx, or D pins are clamped by the internal diodes. Limit the current to the maximum ratings given.

2 Overvoltages at the Ax and EN digital input pins are clamped by the internal diodes.

3 Sx refers to the S1 to S8.

4 See Table 5

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is the function to the bottom of the case value.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-17[1]	64.04	26.87	°C/W

1 Thermal impedance simulated values are based on the JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADG1408L

Table 8. ADG1408L, 24-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	±2.5	2
FICDM	±1.25	C3

1 For the input and output port to the supplies, for the input and output port to the input and output port, and for all other inputs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

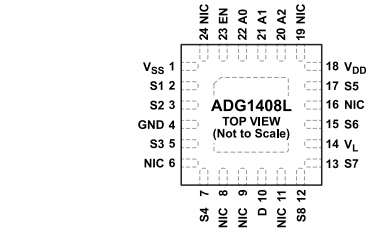


Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, V_{SS} can be connected to ground. Decouple the V_{SS} pin using a 0.1 µF capacitor to GND.
2	S1	Source Terminal 1. S1 can be an input or an output.
3	S2	Source Terminal 2. S2 can be an input or an output.
4	GND	Ground (0 V) Reference.
5	S3	Source Terminal 3. S3 can be an input or an output.
6, 8, 9, 11, 16, 19, 24	NIC	Not Internally Connected.
7	S4	Source Terminal 4. S4 can be an input or an output.
10	D	Drain Terminal. D can be an input or an output.
12	S8	Source Terminal 8. S8 can be an input or an output.
13	S7	Source Terminal 7. S7 can be an input or an output.
14	V_L	Logic Power Supply Potential.
15	S6	Source Terminal 6. S6 can be an input or an output.
17	S5	Source Terminal 5. S5 can be an input or an output.
18	V_{DD}	Most Positive Power Supply Potential. Decouple the V_{DD} pin using a 0.1 µF capacitor to GND.
20	A2	Logic Control Input 2.
21	A1	Logic Control Input 1.
22	A0	Logic Control Input 0.
23	EN	Active High Digital Input. When the EN pin is low, the ADG1408L is disabled and all switches are turned off. When the EN pin is high, the Ax logic inputs determine which switch is on.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, V_{SS}.

Table 10. Truth Table

A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

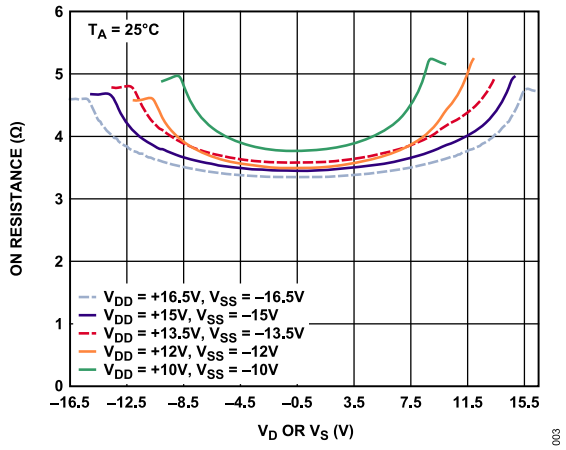


Figure 3. On Resistance vs. V_D or V_S for a Dual Supply

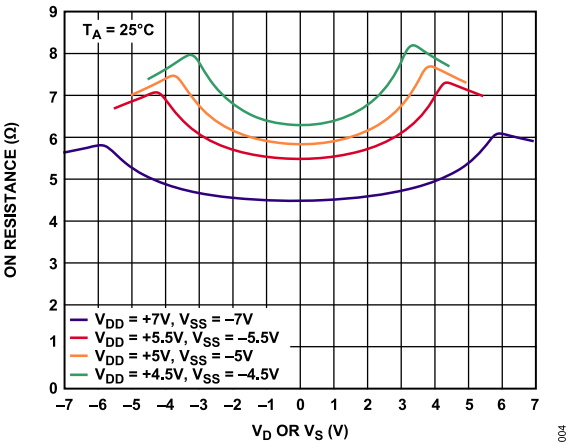


Figure 4. On Resistance vs. V_D or V_S for a Dual Supply

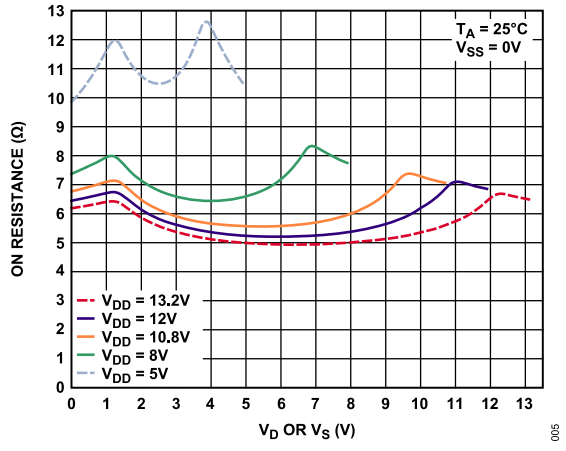


Figure 5. On Resistance vs. V_D or V_S for a Single Supply

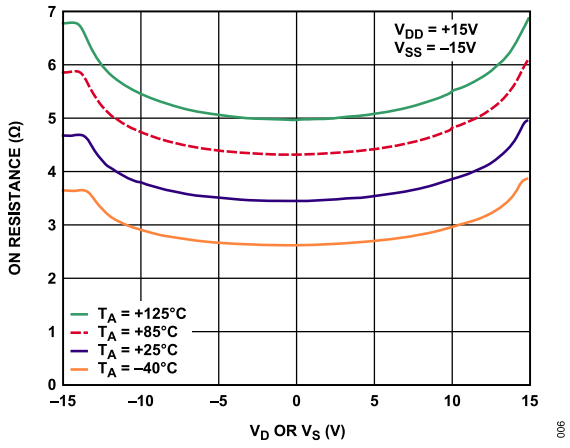


Figure 6. On Resistance vs. V_D or V_S over Temperature for a ±15 V Dual Supply

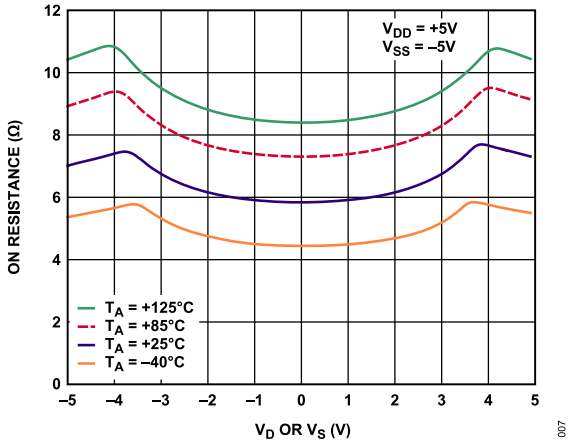


Figure 7. On Resistance vs. V_D or V_S over Temperature for a ±5 V Dual Supply

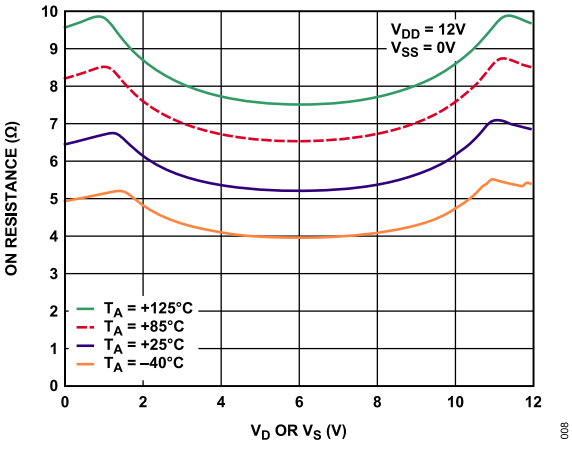


Figure 8. On Resistance vs. V_D or V_S over Temperature for a 12 V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

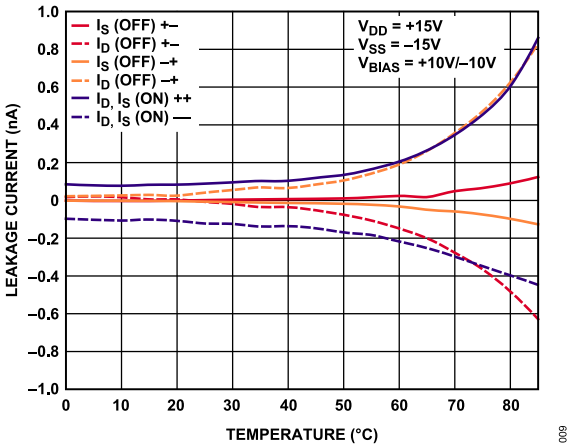


Figure 9. Leakage Current vs. Temperature for a ±15 V Dual Supply

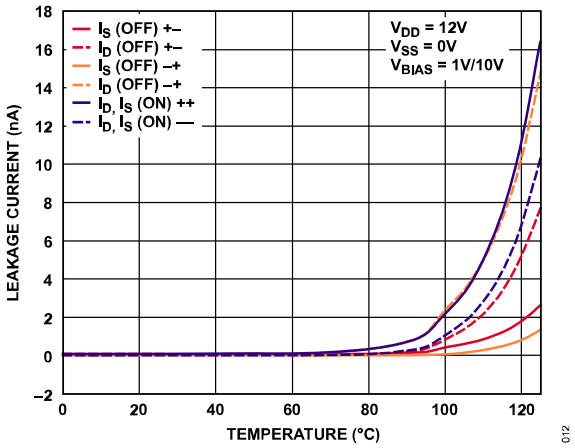


Figure 12. Leakage Current vs. Temperature for a 12 V Single Supply

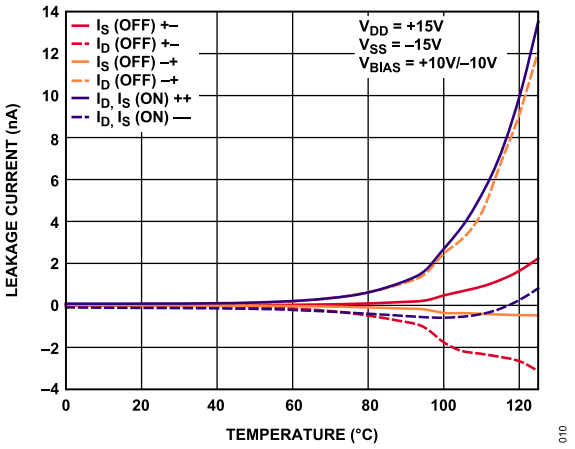


Figure 10. Leakage Current vs. Temperature for a ±15 V Dual Supply

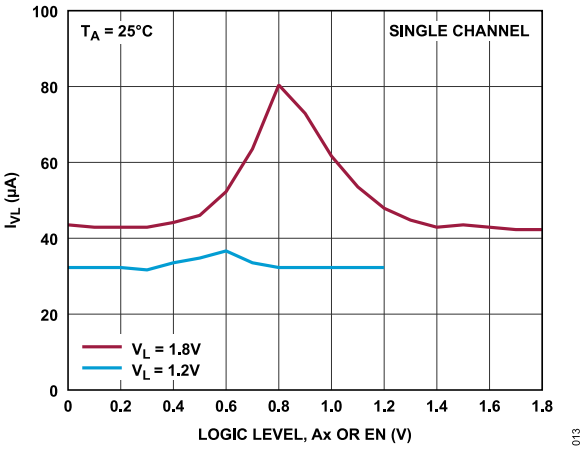


Figure 13. I_{VL} vs. Logic Level, Ax or EN

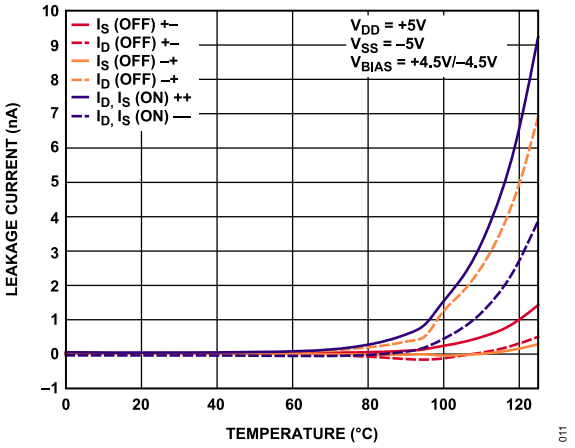


Figure 11. Leakage Current vs. Temperature for a ±5 V Dual Supply

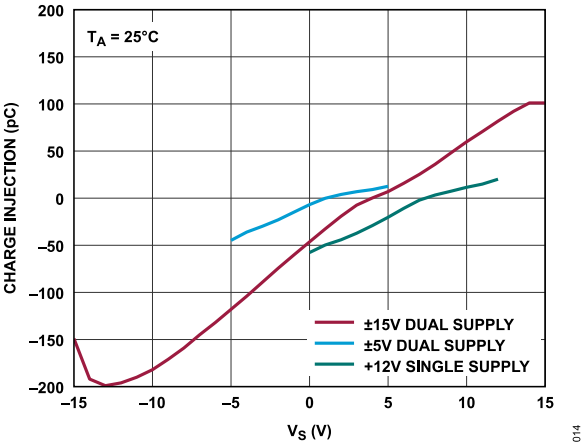


Figure 14. Charge Injection vs. V_S

TYPICAL PERFORMANCE CHARACTERISTICS

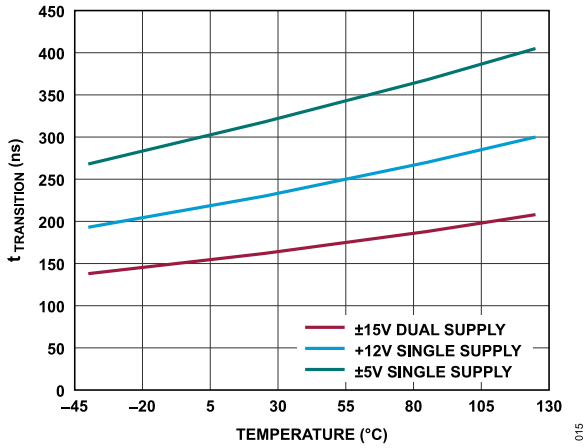


Figure 15. $t_{TRANSITION}$ vs. Temperature

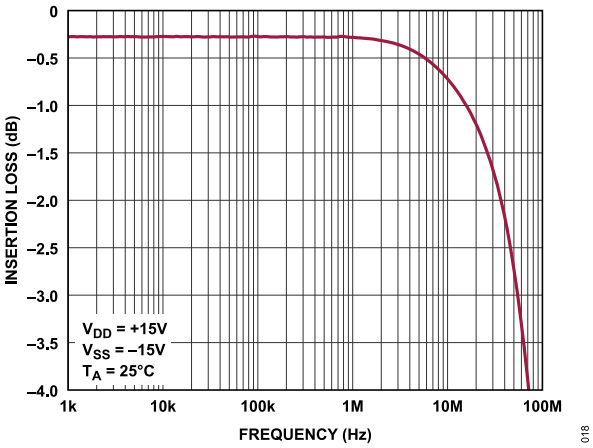


Figure 18. Insertion Loss vs. Frequency

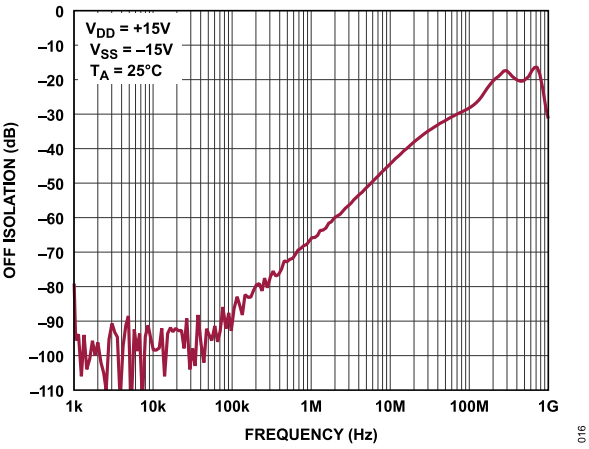


Figure 16. Off Isolation vs. Frequency

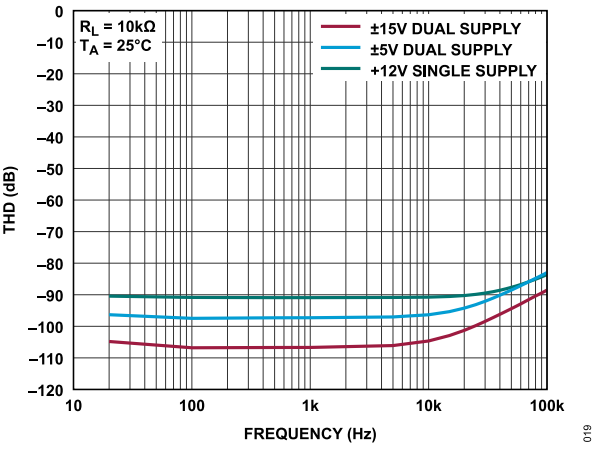


Figure 19. THD vs. Frequency

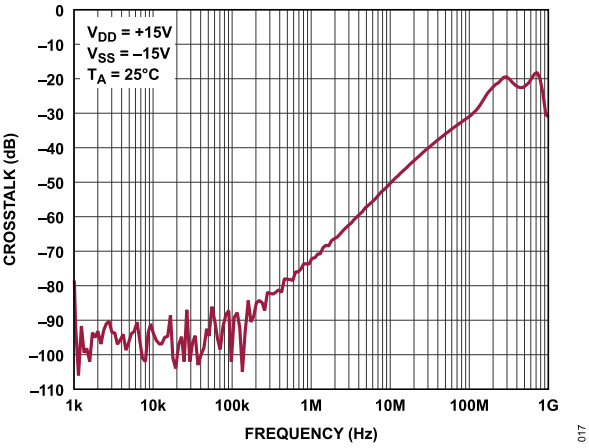


Figure 17. Crosstalk vs. Frequency

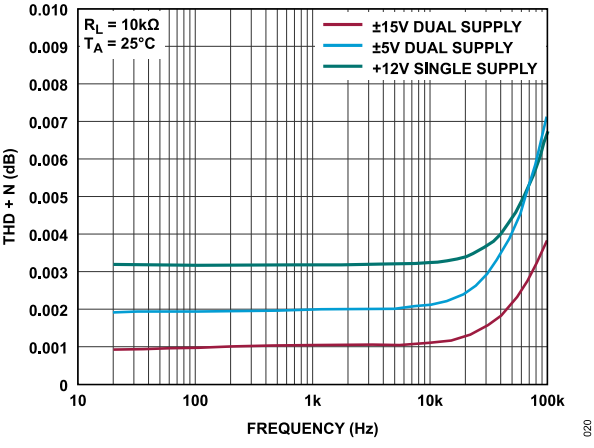


Figure 20. THD + N vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

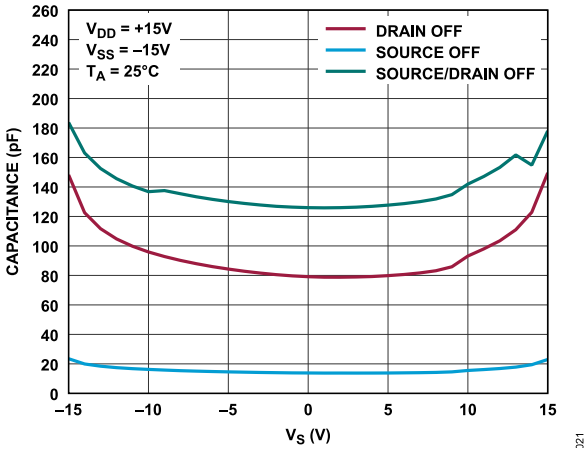


Figure 21. Capacitance vs. V_S for a ±15 V Dual Supply

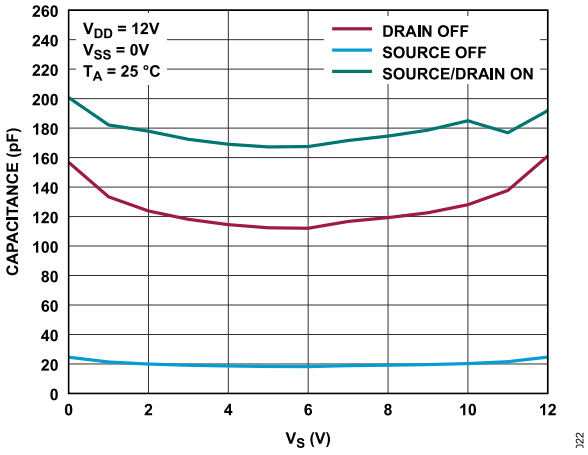


Figure 22. Capacitance vs. V_S for a 12 V Single Supply

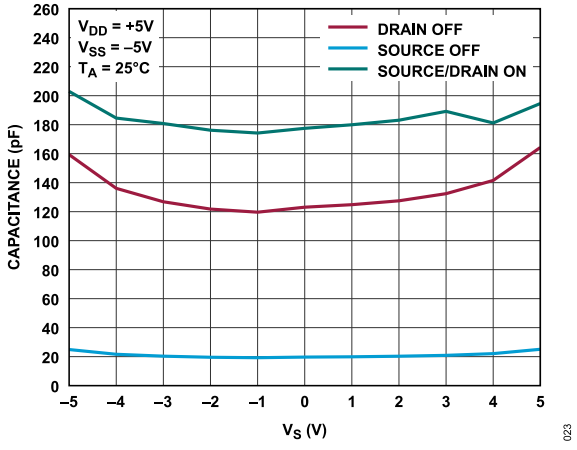


Figure 23. Capacitance vs. V_S for a ±5 V Dual Supply

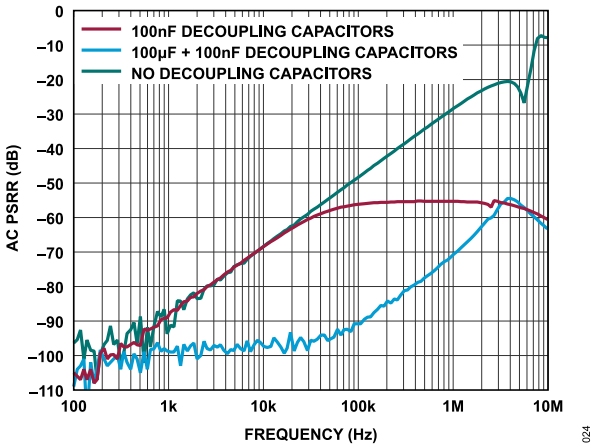


Figure 24. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency

TEST CIRCUITS

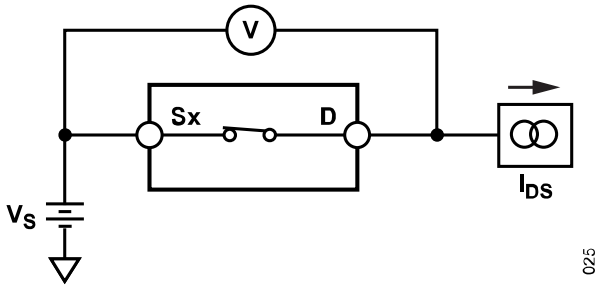


Figure 25. On Resistance

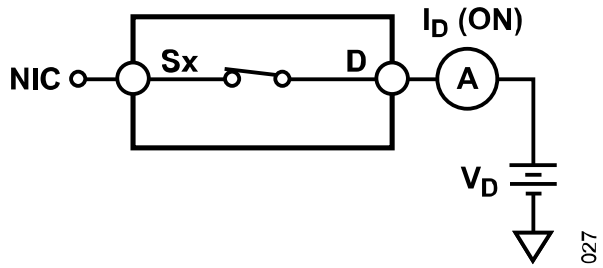


Figure 27. On Leakage

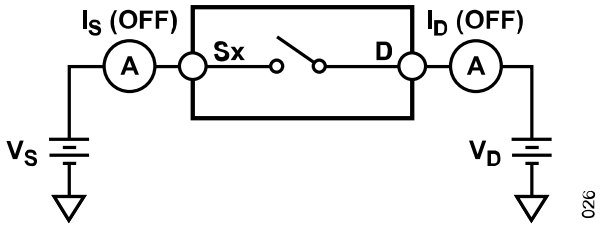


Figure 26. Off Leakage

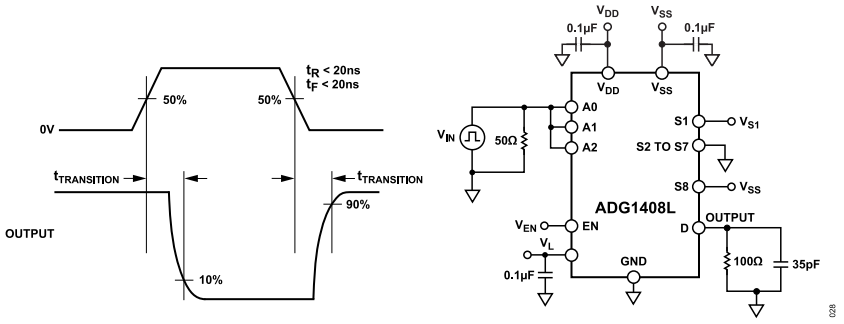


Figure 28. Address to Output Switching Times, $t_{TRANSITION}$

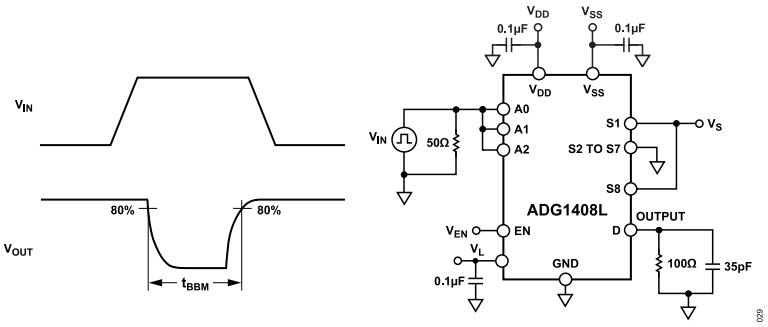


Figure 29. Break-Before-Make Delay, t_{BBM}

TEST CIRCUITS

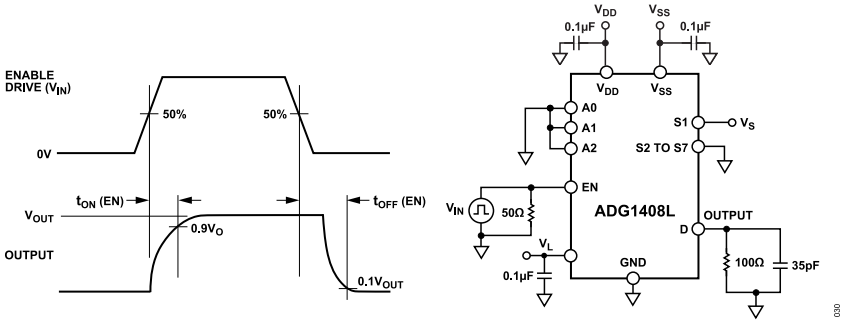


Figure 30. Enable Delay, t_{ON} (EN) and t_{OFF} (EN)

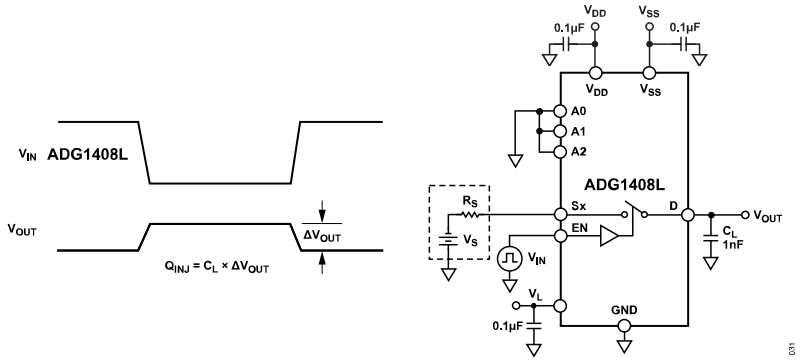


Figure 31. Charge Injection

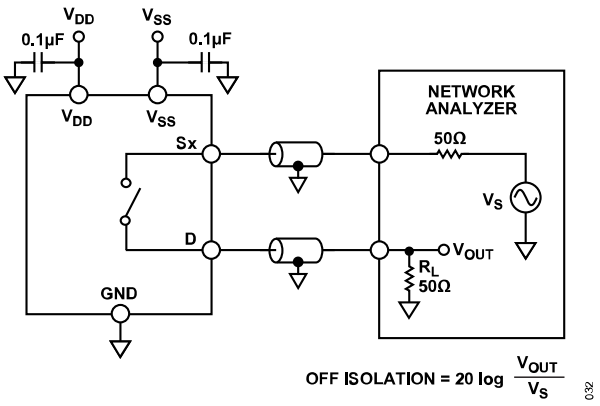


Figure 32. Off Isolation

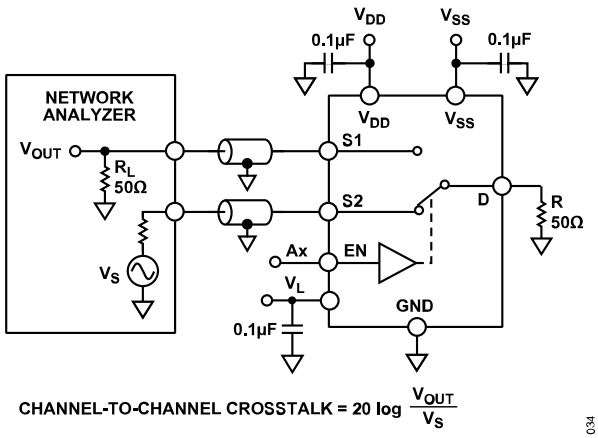


Figure 33. Channel to Channel Crosstalk

TEST CIRCUITS

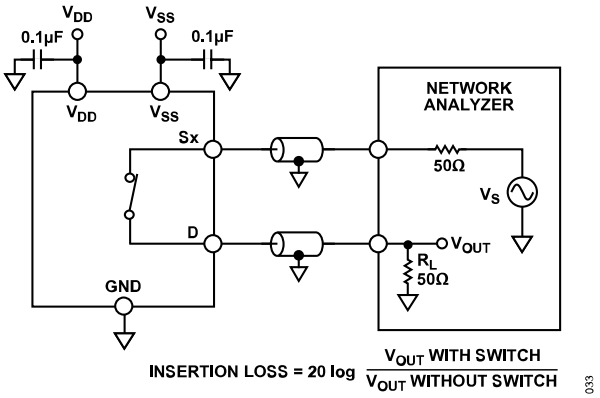


Figure 34. Insertion Loss

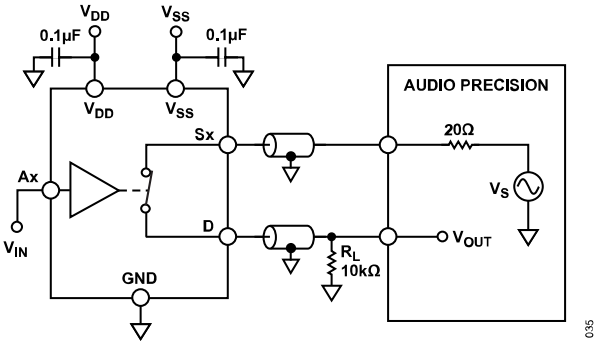


Figure 35. THD + N

TERMINOLOGY

R_{ON}

R_{ON} is the ohmic resistance between D and Sx.

ΔR_{ON}

ΔR_{ON} is the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

$R_{FLAT(ON)}$ is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)

I_S (Off) is the source leakage current when the switch is off.

I_D (Off)

I_D (Off) is the drain leakage current when the switch is off.

I_D (On), I_S (On)

I_D (On) and I_S (On) is the channel leakage current when the switch is on.

V_D (V_S)

V_D (V_S) is the analog voltage on Terminal D and Terminal Sx.

C_S (Off)

C_S (Off) is the channel input capacitance for off condition.

C_D (Off)

C_D (Off) is the channel output capacitance for off condition.

C_D (On), C_S (On)

C_D (On) and C_S (On) is the on switch capacitance.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) is the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

t_{OFF} (EN) is the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

$t_{TRANSITION}$ is the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

Break-Before-Make Time Delay, t_{BBM}

t_{BBM} is the off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL} and V_{INH}

V_{INL} is the maximum input voltage for Logic 0, and V_{INH} is the minimum voltage for Logic 1.

I_{INL} and I_{INH}

I_{INL} is the low input current of the digital input, and I_{INH} is the high input current of the digital input.

I_{DD} and I_{SS}

I_{DD} is the positive supply current, and I_{SS} is the negative supply current.

Off Isolation

Off Isolation is a measure of unwanted signal coupling through an off channel.

Channel to Channel Crosstalk

Channel to channel crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

−3 dB Bandwidth

The −3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion (THD)

THD is the sum of the powers of all harmonic components to the power of the fundamental frequency.

Total Harmonic Distortion Plus Noise (THD + N)

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is a measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the AC PSRR.

THEORY OF OPERATIONS

SWITCH ARCHITECTURE

The ADG1408L is a multiplexer that is compatible with 1.2 V or 1.8 V logic depending on the V_L input.

V_L FLEXIBILITY

An external V_L supply provides logic control flexibility for lower logic levels.

The following V_L conditions must be satisfied for the switch to operate in either 1.2 V or 1.8 V logic operation:

- 1.2 V logic: V_L = 1.1 V to 1.3 V
- 1.8 V logic: V_L = 1.65 V to 1.95 V

1.2 V AND 1.8 V JEDEC COMPLIANCE

The ADG1408L is both 1.2 V and 1.8 V JEDEC standard compliant (normal range) to the digital input threshold.

This compliance with the digital-input threshold ensures the low voltage, complementary metal-oxide semiconductor (CMOS) logic compatibility when operating with a valid logic power supply range.

The following are the switch digital input requirements for both 1.2 V and 1.8 V logic:

- $V_{INH} = 0.65 \times V_L$
- $V_{INL} = 0.35 \times V_L$

INITIALIZATION TIME

The digital section of the ADG1408L goes through an initialization phase during V_{DD}, V_{SS}, and V_L power-up. After V_{DD}, V_{SS}, and V_L power up, ensure that there is a minimum of 50 µs from the time of power-up before any digital input is issued.

Ensure that V_{DD}, V_{SS}, and V_L do not drop out during the 50 µs initialization phase because it may result in an incorrect timing performance of the ADG1408L.

SWITCHES IN A KNOWN STATE

The ADG1408L switches are off when the digital inputs are floating, which prevents unwanted signals passing through the switches. This built-in feature of the ADG1408L eliminates the need for an external pull-down resistor to be installed.

The ADG1408L can pull down floating digital inputs against leakage currents up to half of I_{INH}.

APPLICATIONS INFORMATION

FIELD PROGRAMMABLE GATE ARRAY (FPGA) LOW LOGIC COMPLIANCE

Figure 36 shows a typical application where the ADG1408L is used together with an FPGA or microcontroller. The flexible V_L pin can be tied to the digital supply voltage (V_{CCO}), and the Ax input can be tied directly to the digital IOx ports for ease of use.

The ADG1408L is 1.2 V and 1.8 V JEDEC standard compliant, which ensures that the logic input specifications, V_{INH} and V_{INL}, meet the digital output specifications, minimum V_{OH} and maximum V_{OL}, of the FPGA or microcontroller. Common implementations do not guarantee logic level compatibility, which can introduce implementation risks. The ADG1408L eliminates these risks by complying with the widely accepted 1.2 V and 1.8 V logic level standard.

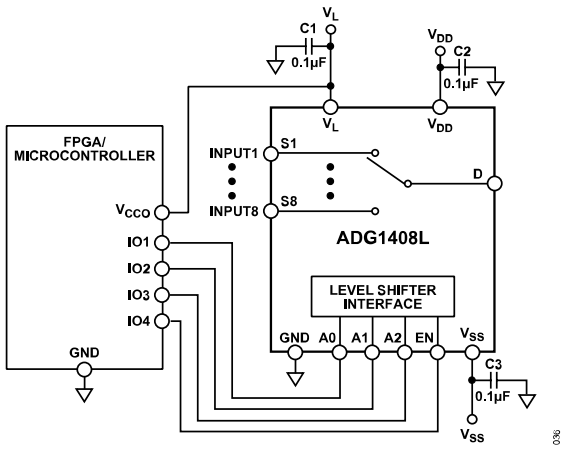


Figure 36. ADG1408L Typical Application Used with an FPGA or Microcontroller

V_{OH} AND V_{OL} AND V_{INH} AND V_{INL} RELATIONSHIP

It is recommended to confirm that the logic output high (V_{OH}) of the FPGA or microcontroller is higher than the input logic high (V_{INH}). In addition, the logic output low (V_{OL}) of the FPGA or microcontroller must be lower than the input logic low (V_{INL}). Figure 37 shows the 1.2 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the Ax inputs of the ADG1408L, V_{INH} and V_{INL}.

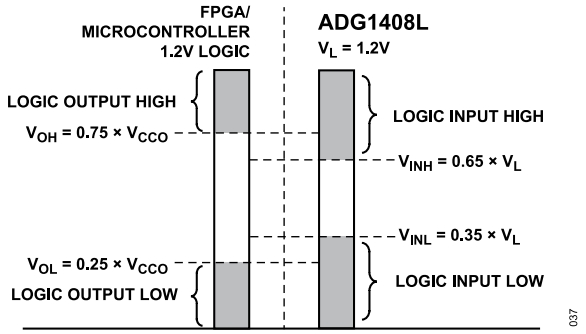


Figure 37. 1.2 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

Figure 38 shows the 1.8 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the Ax inputs of the ADG1408L, V_{INH} and V_{INL}.

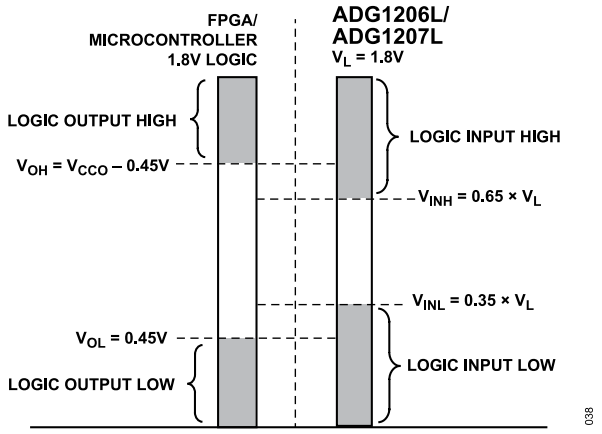


Figure 38. 1.8 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

POWER SUPPLY RAILS

To guarantee correct operation of the ADG1408L, a minimum of 0.1 µF and 10 µF decoupling capacitors are required on the V_{DD}, V_{SS}, and V_L supply pins.

The ADG1408L can operate with V_{DD} and V_{SS} dual supplies between ±4.5 V to ±16.5 V. The ADG1408L can also operate with a V_{DD} single supply between 5 V to 16.5 V and a V_L between 1.1 V to 1.95 V. However, the V_{DD} to V_{SS} range must not exceed 35 V, and the V_L range must not exceed 2.25 V, as stated in the Absolute Maximum Ratings section.

It is possible to operate the ADG1408L with asymmetrical supplies or at other voltage supplies within the ranges listed in Table 1. However, the switch characteristics change. These changes include, but are not limited to, the analog signal range, on resistance, leakage, V_{INH}, V_{INL}, and switching times. The typical performance characteristics can be used as a guide to switch the performance vs. the supply voltage (see the Typical Performance Characteristics section).

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a symmetrical bipolar power solution is shown in Figure 39. The ADP5070 (dual switching regulator) generates the positive and negative supply rail for the ADG1408L. Also shown in Figure 39 are the two optional positive and negative, low dropout (LDO) regulators, the ADP7118 and ADP7182, respectively, that can reduce the output ripple of the ADP5070 in ultralow noise sensitive applications. The ADP160 generates the logic power supply rail of either 1.2 V or 1.8 V.

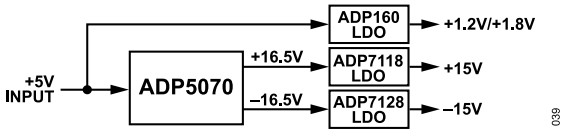
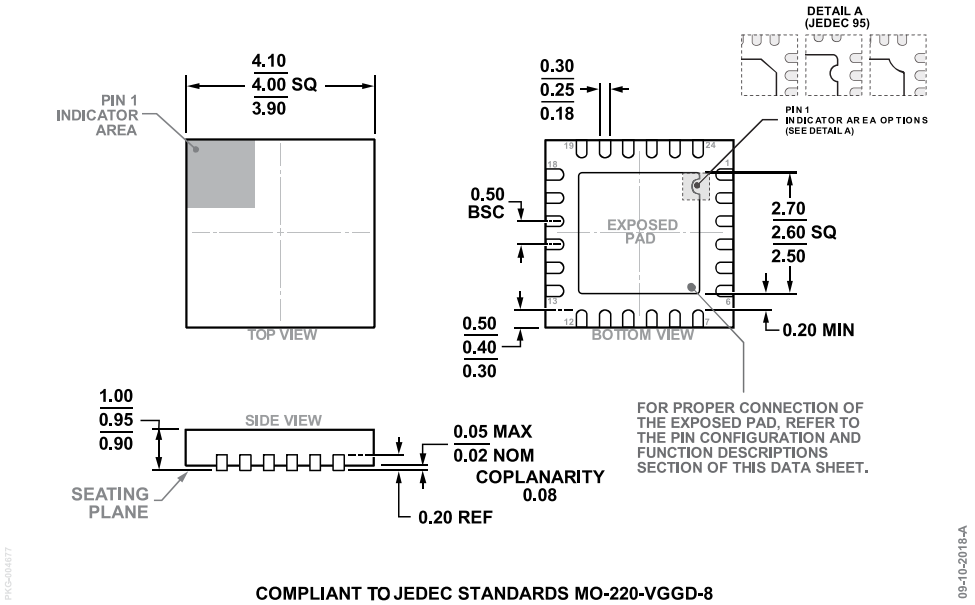


Figure 39. Bipolar Power Solution

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 40. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions shown in millimeters

Updated: May 17, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG1408LYCPZ-REEL7	−40°C to +125°C	24-Lead LFSCP (4 mm × 4 mm × 0.95 mm with EPAD)	Reel, 1500	CP-24-17

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 11. Evaluation Boards

Model[1]	Description
EVAL-ADG1408LEBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

EVAL-ADG1408LEBZ ADG1408LYCPZ-REEL7