Energy Metering IC with Autocalibration

Data Sheet

ADE9153A

FEATURES

- ***m*Sure autocalibration**
  - **Automatic calibration based on a direct measurement of the full signal path**
  - **Calibration procedure not requiring a reference meter**
  - ***m*Sure autocalibration Class 1 meter guaranteed**
- **3 high performance ADCs**
  - **88 dB SNR**
  - **High gain current channel: ±26.04 mV peak, 18.4 mV rms input at highest gain setting**
- **Advanced metrology feature set**
  - **WATT, VAR, VA, Wh, VARh, and VAh**
  - **Supports active energy standards: IEC 62053-21; IEC 62053-22; EN50470-3; OIML R46; and ANSI C12.20**
  - **Supports reactive energy standards: IEC 62053-23 and IEC 62053-24**
  - **Current and voltage rms measurement**
  - **Power quality measurements**
- **Operating temperature, industrial range: −40°C to +85°C**

APPLICATIONS

- **Single-phase energy meters**
- **Energy and power measurement**
- **Street lighting**
- **Smart power distribution system**
- **Machine health**

GENERAL DESCRIPTION

The ADE9153A[1] is a highly accurate, single-phase, energy metering IC with autocalibration. The *m*Sure® autocalibration feature allows a meter to automatically calibrate the current and voltage channels without using an accurate source or an accurate reference meter when a shunt resistor is used as a current sensor. Class 1 and Class 2 meters are supported by *m*Sure autocalibration.

The ADE9153A incorporates three high performance analog-to-digital converters (ADCs), providing an 88 dB signal-to-noise ratio (SNR). The ADE9153A offers an advanced metrology feature set of measurements like line voltage and current, active energy, fundamental reactive energy, and apparent energy calculations, and current and voltage rms calculations. ADE9153A includes power quality measurements such as zero crossing detection, line period calculation, angle measurement, dip and swell, peak and overcurrent detection, and power factor measurements. Each input channel supports independent and flexible gain stages. Current Channel A is ideal for shunts, having a flexible gain stage and providing full-scale input ranges from 62.5 mV peak down to 26.04 mV peak. Current Channel B has gain stages of 1×, 2×, and 4× for use with current transformers (CTs). A high speed, 10 MHz, serial peripheral interface (SPI) port allows access to the ADE9153A registers.

Note that throughout this data sheet, multifunction pins, such as ZX/DREADY/CF2, are referred to either by the entire pin name or by a single function of the pin, for example, CF2, when only that function is relevant.

The ADE9153A operates from a 3.3 V supply and is available in a 32-lead LFCSP package.

TYPICAL APPLICATIONS CIRCUIT

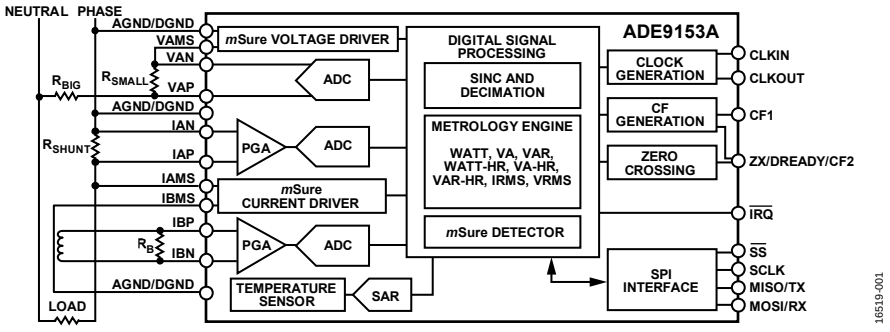

Figure 1.

[1] Protected by U.S. Patents 8,350,558; 8,010,304; WO2013038176 A3; 0113507 A1; 0253102 A1; 0354266 A1; and 0154029 A1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

2/2018—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.97 V to 3.63 V, AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, and T_A = 25°C (typical), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY (MEASUREMENT ERROR PER PHASE)					Percentage of the typical value derived from comparing the actual value with the typical-based expected values when a 10:1 signal is applied
Total Active Energy		0.1		%	Over a dynamic range of 3000 to 1, 10 sec accumulation programmable gain amplifier (PGA), AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 10,000 to 1, 30 sec accumulation; AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 3000 to 1, 10 sec accumulation; AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 10,000 to 1, 30 sec accumulation AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 1 sec accumulation; AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 3000 to 1, 10 sec accumulation AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
RMS Current (I_{RMS}) and Apparent Power (VA)		0.1		%	Over a dynamic range of 1000 to 1, 1 sec (averaging) AI_PGAGAIN = 16×, BI_PGAGAIN = 1×
		0.2		%	Over a dynamic range of 1000 to 1, 1 sec (averaging), AI_PGAGAIN = 38.4×
		0.3		%	Over a dynamic range of 3000 to 1, 1 sec (averaging), AI_PGAGAIN = 16×, BI_PGAGAIN = 1×
		0.6		%	Over a dynamic range of 3000 to 1, 1 sec (averaging), AI_PGAGAIN = 38.4×
RMS Voltage (V_{RMS})		0.2		%	Over a dynamic range of 1000 to 1, 1 sec (averaging)
Active Power (WATT), Fundamental Reactive Power (VAR)		0.25		%	Over a dynamic range of 3000 to 1, 1 sec, AI_PGAGAIN = 16×
		0.5		%	Over a dynamic range of 3000 to 1, 1 sec, AI_PGAGAIN = 38.4×
One Cycle RMS Current and Voltage Refreshed Each Half Cycle		0.5		%	Over a dynamic range of 500 to 1 on current and 250 to 1 on voltage
		1		%	Over a dynamic range of 1000 to 1 on current and 500 to 1 on voltage
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Voltage to Current Angle Measurement		0.036		Degrees	Resolution at 50 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
PGA Gain Settings (xI_PGAGAIN)					
Current Channel A (Phase Shunt)		16, 24, 32, 38.4		V/V	PGA gain setting is referred to as gain
Current Channel B (Neutral CT)		1, 2, 4		V/V	PGA gain setting is referred to as gain
Pseudo Differential Input Voltage Range					
(IAP − IAN)	−1/gain		+1/gain	V	44.19 mV rms on Current Channel A, AI_PGAGAIN = 16×
(VAP − VAN)	−0.5		+0.5	V	353.6 mV rms on voltage channel
Differential Input Voltage Range					
(IBP − IBN)	−1/gain		+1/gain	V	707 mV rms on Current Channel B
Maximum Operating Voltage on the Analog Input Pins					
VAP	0		1.35	V	Voltage on the pin with respect to ground
IAP, IAN	−0.1125		+0.1125	V	Voltage on the IAx pin with respect to ground
IBP, IBN	0.35		1.45	V	Voltage on the IBx pin with respect to ground; internal common-mode voltage at IBx pin = 0.9 V
SNR					
Current Channel A					
AI_PGAGAIN = 16×		90		dB	V_{IN} is a full-scale signal
AI_PGAGAIN = 38.4×		88		dB	V_{IN} is a full-scale signal
Current Channel B					
BI_PGAGAIN = 1x		90		dB	V_{IN} is a full-scale signal
BI_PGAGAIN = 4x		78		dB	V_{IN} is a full-scale signal
Voltage Channel		87		dB	V_{IN} is a full-scale signal
ADC Output Pass Band (0.1 dB)		0.672		kHz	
ADC Output Bandwidth (−3 dB)		1.6		kHz	
Crosstalk		−120		dB	At 50 Hz or 60 Hz; see the Terminology section
AC Power Supply Rejection Ratio (AC PSRR)					At 50 Hz; see the Terminology section
Current Channel A		−115		dB	
Current Channel B		−100		dB	
Voltage Channel		−100		dB	
AC Common-Mode Rejection Ratio (AC CMRR)		−120		dB	At 50 Hz
ADC Gain Error					Percentage of error from the ideal value; see the Terminology section
Current Channel A		±0.2	±1.5	%	
Current Channel B		−2.0	±3.5	%	
Voltage Channel		−0.8	±3.0	%	
ADC Offset					
Current Channel A					See the Terminology section
AI_PGAGAIN = 16×		+0.04	±0.1	mV	
AI_PGAGAIN = 38.4×		−0.02	±0.05	mV	
Current Channel B		−0.26	±0.37	mV	
Voltage Channel		+0.35	±0.75	mV	
ADC Offset Drift		±0.5	±5	µV/°C	See the Terminology section

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel Drift (PGA, ADC, Internal Voltage Reference)					See the Terminology section
Current Channel A		±5	±30	ppm/°C	
Current Channel B		±20	±50	ppm/°C	
Voltage Channel		±20	±50	ppm/°C	
Differential Input Impedance (DC)					See the Terminology section
Current Channel A	5000	7800		kΩ	
Current Channel B	100	113		kΩ	
Voltage Channel	240	256		kΩ	
INTERNAL VOLTAGE REFERENCE					Nominal = 1.25 V ± 1 mV
Voltage Reference		1.25		V	T_A = 25°C at REFIN
Temperature Coefficient		±5	±30	ppm/°C	T_A = −40°C to +85°C; tested during device characterization
TEMPERATURE SENSOR					
Temperature Accuracy		±5		°C	−40°C to +85°C
Temperature Readout Step Size			0.3	°C	
CRYSTAL OSCILLATOR					All specifications at CLKIN = 12.288 MHz; the crystal oscillator is designed to interface with 100 µW crystals
Input Clock Frequency	12.287	12.288	12.289	MHz	±100 ppm
Internal Capacitance on CLKIN, CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.58		MΩ	
Transconductance (g_m)	5	8.7		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency, CLKIN	12.287	12.288	12.289	MHz	±100 ppm
Duty Cycle	45:55	50:50	55:45		
CLKIN Logic Input Voltage					3.3 V tolerant
High, V_{INH}	1.2			V	
Low, V_{INL}			0.5	V	
LOGIC INPUTS—MOSI/RX, SCLK					
Input Voltage					
High, V_{INH}	2.4			V	
Low, V_{INL}			0.8	V	
Input Current, I_{IN}			11	µA	V_{IN} = 0 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
MISO/TX, $\overline{IRQ}$					
Output Voltage					
High, V_{OH}	2.5			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.4	V	I_{SINK} = 3 mA
Internal Capacitance, C_{IN}			10	pF	
CF1, CF2					
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 6 mA
Low, V_{OL}			0.8	V	I_{SINK} = 6 mA
Internal Capacitance, C_{IN}			10	pF	
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	
DVDD		1.7		V	
VDD2P5		2.5		V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
VDD Pin Current, I_{DD}		9.3	12	mA	Consumption in operation, without *m*Sure running
		8.5		µA	When the ADE9153A is held in reset

AUTOCALIBRATION

VDD = 3.3 V, AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz, T_A = 25°C (typical), I_{MAX} = 60 A rms, V_{NOM} = 230 V, R_{SHUNT_PHASE} = 200 µΩ, turns ratio on $CT_{NEUTRAL}$ = 2500:1, burden on $CT_{NEUTRAL}$ = 16.4 Ω, and $CT_{NEUTRAL}$ voltage potential divider of 1000:1 (990 kΩ and 1 kΩ resistors), unless otherwise noted. The values in Table 2 are specified for the system described; if the shunt or voltage potential divider is changed, the values in Table 2 change as well. For example, increasing the shunt value decreases the calibration time required for the phase current channel; conversely, decreasing the shunt value increases the calibration time.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUTOCALIBRATION					T_A = 25°C ±5 °C
Current Channel A (Phase Shunt)					
Calibration Time					
Turbo Mode					For more information on the power modes and calibration times, see the *m*Sure Autocalibration Feature section
0.353% Accuracy Target		16		sec	
0.25% Accuracy Target		45		sec	
Normal Mode					
0.353% Accuracy Target		40		sec	
0.25% Accuracy Target		115		sec	
Current Consumption					Additional consumption from 3.3 V supply
Turbo Mode		16		mA rms	With peak consumption of 33 mA
Normal Mode		9.3		mA rms	With peak consumption of 19 mA
Current Channel (Neutral CT)					
Calibration Time					For more information, see the *m*Sure Autocalibration Feature section
0.5 % Accuracy Target,					
Turbo Mode		12		sec	
Normal Mode		20		sec	
Current Consumption					Additional consumption from 3.3 V supply
Turbo Mode		16		mA rms	With peak consumption of 33 mA
Normal Mode		9.3		mA rms	With peak consumption of 19 mA
Voltage Channel					
Calibration Time					For more information, see the *m*Sure Autocalibration Feature section
0.353% Accuracy Target		25		sec	
0.25% Accuracy Target		85		sec	
Current Consumption		<1		mA rms	Additional consumption from 3.3 V supply

SPI TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency	f_{SCLK}			10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

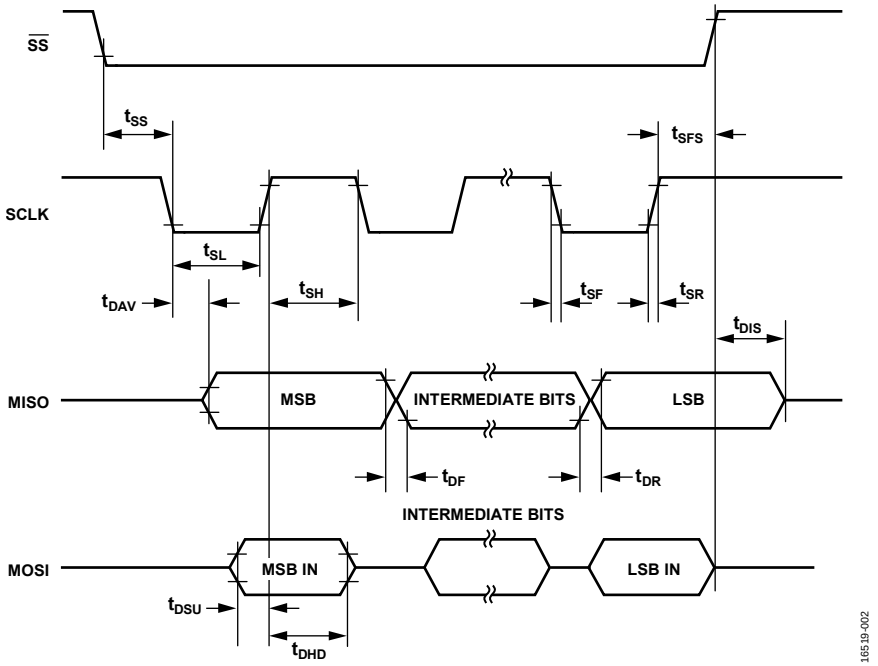


Figure 2. SPI Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VDD to AGND/DGND	−0.3 V to +3.96 V
Analog Input Voltage to AGND/DGND, IAP, IAN, IBP, IBN, VP, VN[1]	−0.75 V to +2.2 V
Reference Input Voltage to AGND/DGND	−0.3 V to +2.2 V
Digital Input Voltage to AGND/DGND	−0.3 V to +3.96 V
Digital Output Voltage to AGND/DGND	−0.3 V to +3.96 V
Operating Temperature	
Industrial Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	260°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	4 kV
Machine Model (MM)	200 V
Field Induced Charged Device Model (FICDM)	1.25 kV

[1] The rating of −0.75 V on the analog input pins is limited by protection diodes inside the ADE9153A. These pins were tested with 7.5 mA going to the pin to simulate a 30× overcurrent condition on the channel, based on the test circuit antialiasing resistor of 150 Ω.
[2] Analog Devices, Inc., recommends that reflow profiles used in soldering RoHS-compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-12[3]	27.83	2.10	°C/W

[1] The θ_{JA} measurement uses a 2S2P JEDEC test board.
[2] The θ_{JC} measurement uses a 1S0P JEDEC test board.
[3] All thermal measurements comply with JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

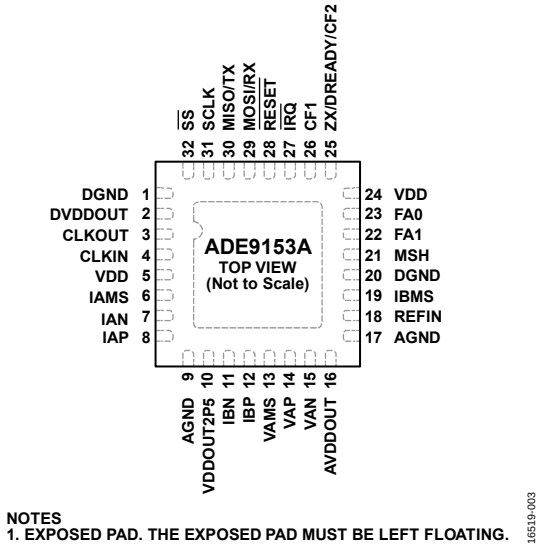


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 20	DGND	Digital Ground. These pins provide the ground reference for the digital circuitry in the ADE9153A and form the return path for the Current Channel A and Current Channel B *m*Sure currents.
2	DVDDOUT	1.7 V Output of the Digital LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 1 (DGND). Do not connect external load circuitry to this pin.
3	CLKOUT	Clock Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. An external buffer is required to drive other circuits from CLKOUT.
4	CLKIN	Master Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. See the ADE9153A Technical Reference Manual for details on choosing a suitable crystal. Alternatively, an external clock can be provided at the logic input.
5, 24	VDD	Supply Voltage. These pins provide the supply voltage for the ADE9153A. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple these pins to AGND or DGND with a 4.7 µF capacitor in parallel with a ceramic 0.1 µF capacitor.
6	IAMS	Output for the *m*Sure Current Driver on Current Channel A (Phase Current Channel). IAMS is connected to the positive end of the shunt on the phase (to the side of the shunt closest to the load, on the same side as IAP).
7, 8	IAN, IAP	Analog Inputs for Current Channel A (Phase Current Channel). The IAP and IAN current channel is ideal for use with shunts. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±125 mV. These channels have an internal PGA gain of 16, 24, 32, and 38.4. Use these pins with the related input circuitry, as shown in Figure 37.
9, 17	AGND	Ground Reference for the Analog Circuitry. See Figure 37 for information on how to connect these ground pins.
10	VDDOUT2P5	2.5 V Output of the Analog LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 9 (AGND). Do not connect external load circuitry to this pin.
11, 12	IBN, IBP	Analog Inputs for Current Channel B (Neutral Current Channel). The IBP and IBN current channel is ideal for use with CTs. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1000 mV. These channels have an internal PGA gain of 1, 2, or 4. Use these pins with the related input circuitry, as shown in Figure 37.
13	VAMS	Path for *m*Sure on the Voltage Channel. VAMS is connected to the bottom end of the resistor divider, which is typically connected to the phase, as shown in Figure 1.
14, 15	VAP, VAN	Analog Inputs for the Voltage Channels. The VAP (positive) and VAN (negative) inputs are fully differential with an input level of 0.1 V to 1.7 V. Use these pins with the related input circuitry, as shown in Figure 37.
16	AVDDOUT	1.9 V Output of the Analog LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 17 (AGND). Do not connect external load circuitry to this pin.

Pin No.	Mnemonic	Description
18	REFIN	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. Decouple this pin to Pin 17 (AGND) with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. After reset, the on-chip reference is enabled. An external reference source with 1.25 V ± 0.01% can also be connected at this pin.
19	IBMS	Output for the *m*Sure Current Driver on Current Channel B (Neutral Current Channel). IBMS is connected to a wire leading through the primary winding of the CT and back to Pin 20 (DGND).
21	MSH	External Capacitor Pin for the *m*Sure Current Driver. Connect an external 0.47 µF ceramic capacitor between the MSH pin and Pin 20 (DGND).
22	FA1	*m*Sure Capacitor, Positive Terminal. Connect an external capacitor of value 0.47 µF between FA0 and FA1.
23	FA0	*m*Sure Capacitor, Negative Terminal. Connect an external capacitor of value 0.47 µF between FA0 and FA1.
25	ZX/DREADY/CF2	Voltage Channel Zero-Crossing Output Pin. See the Voltage Channel section. This pin can be configured to output CF2 if necessary. See the description for CF1.
26	CF1	Calibration Frequency (CF) Logic Outputs. The CF1 and CF2 outputs provide proportional power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers, respectively.
27	$\overline{\text{IRQ}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
28	$\overline{\text{RESET}}$	Active Low Reset Input. To initiate a hardware reset, this pin must be brought low for a minimum of 10 µs.
29	MOSI/RX	Data Input for the SPI Port (MOSI) and Receive Pin for the UART (RX).
30	MISO/TX	Data Output for the SPI Port (MISO) and Transmit Pin for the UART (TX).
31	SCLK	Serial Clock Input for the SPI Port. All serial data transfers are synchronized to this clock. The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time (for example, transitioning to opto-isolator outputs).
32	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EPAD	Exposed Pad. The exposed pad must be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Energy characteristics obtained from a 50% of full scale, sinusoidal, 50 Hz voltage signal; the sinusoidal, 50 Hz, swept amplitude current signal is from 100% of full scale to 0.01% of full scale.

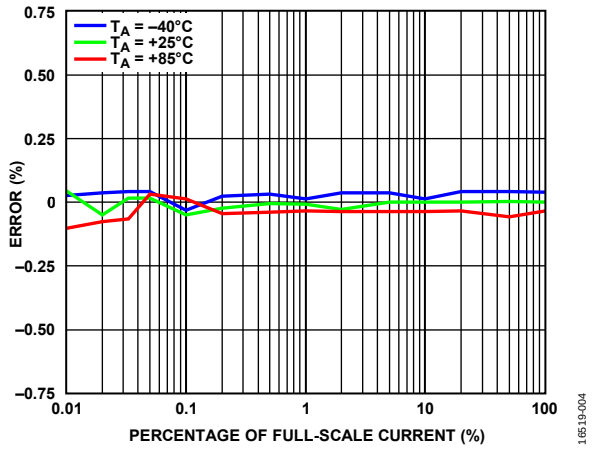


Figure 4. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, Current Channel A (AI) PGA Gain = 16×

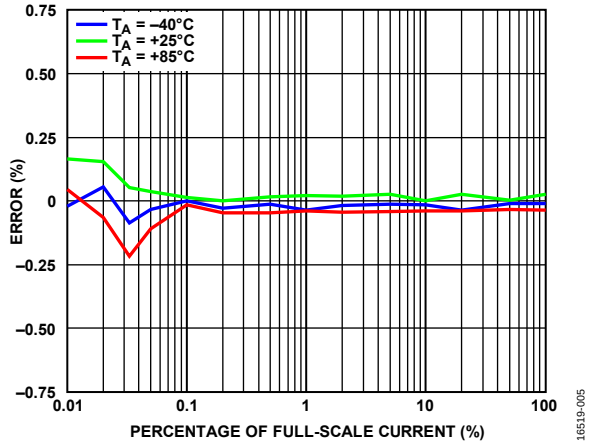


Figure 5. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 38.4×

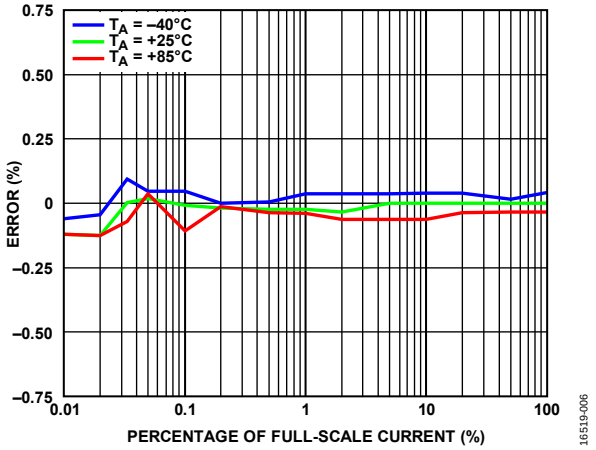


Figure 6. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0, AI PGA Gain = 16×

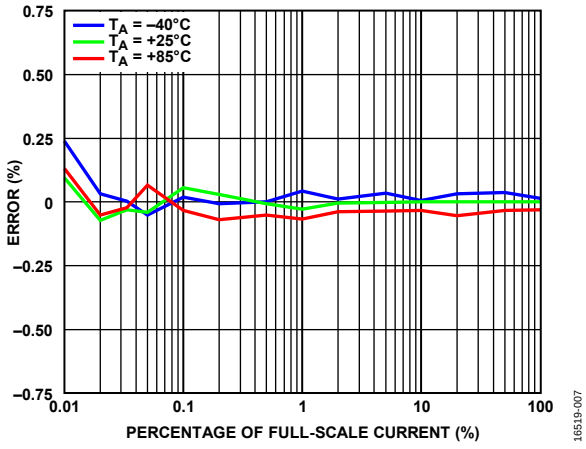


Figure 7. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0, AI PGA Gain = 38.4×

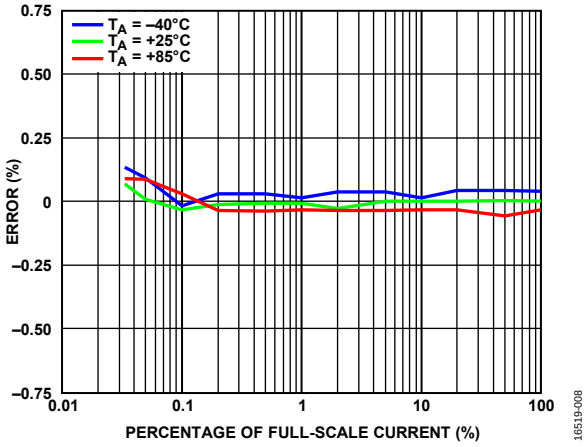


Figure 8. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 16×

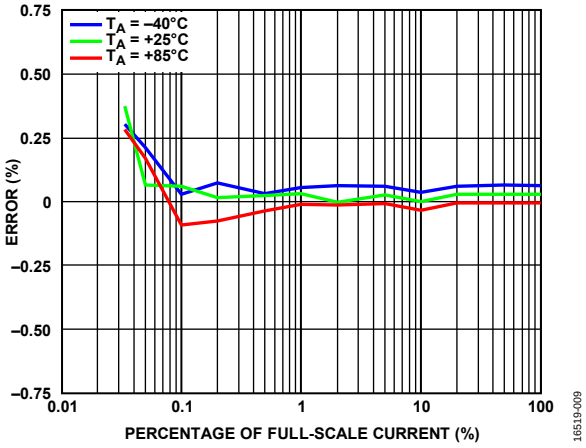


Figure 9. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 38.4×

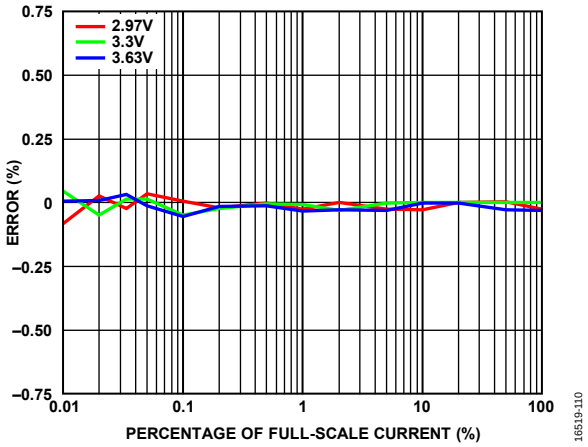


Figure 10. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 16×

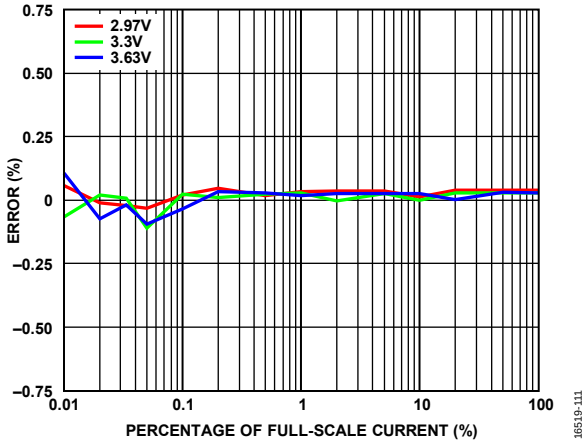


Figure 11. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 38.4×

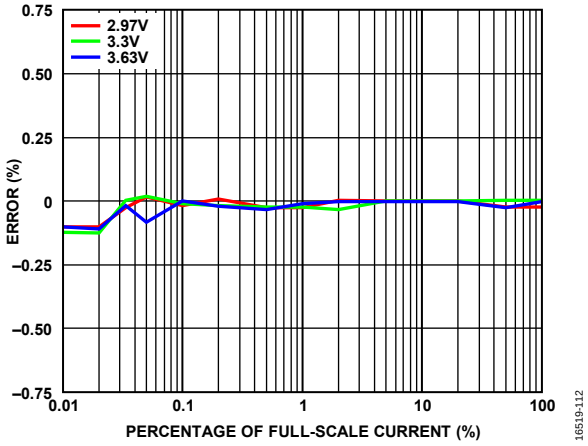


Figure 12. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C, AI PGA Gain = 16×

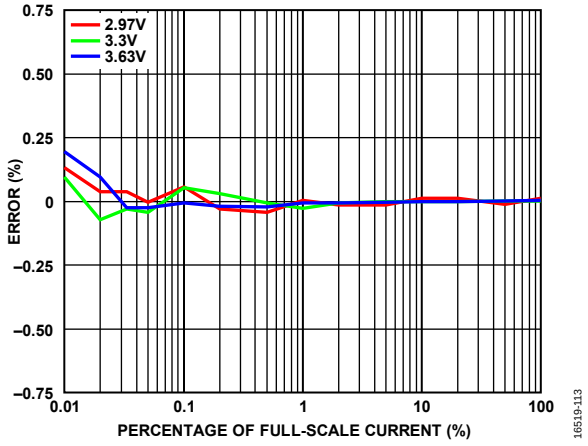


Figure 13. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C, AI PGA Gain = 38.4×

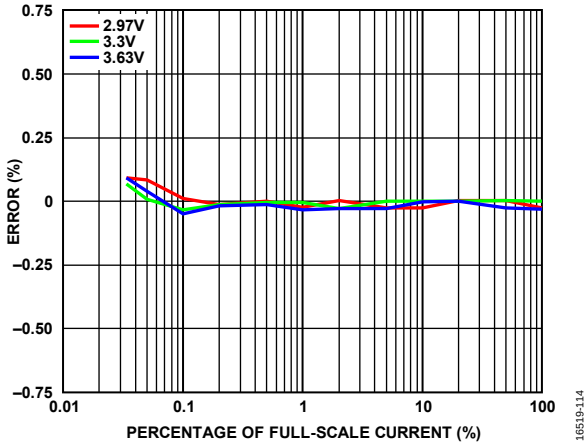


Figure 14. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 16×

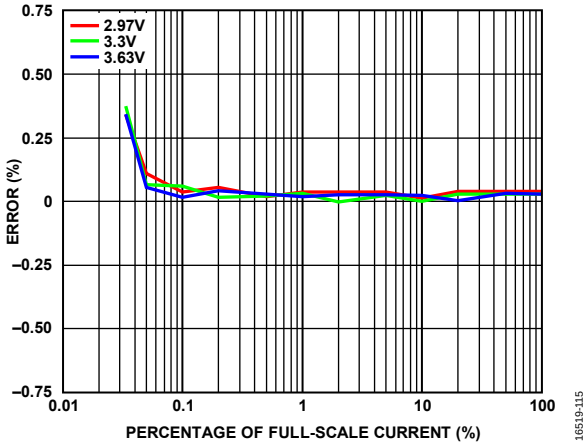


Figure 15. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 38.4×

ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Energy characteristics obtained from a 50% of full scale, sinusoidal, 50 Hz voltage signal and a 10% of full scale, sinusoidal, 50 Hz, current signal over a variable frequency between 45 Hz and 65 Hz.

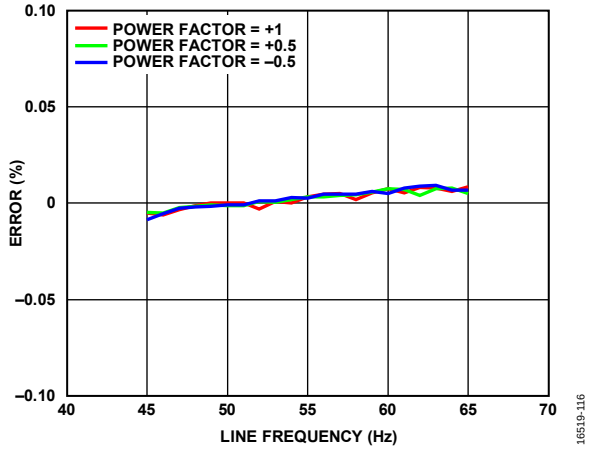


Figure 16. Total Active Energy Error vs. Line Frequency, Power Factor = −0.5, +0.5, and +1, AI PGA Gain = 38.4×

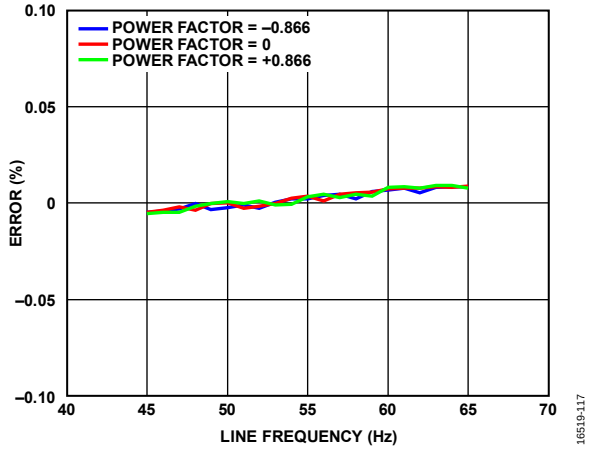


Figure 17. Fundamental Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, +0.866, and 0, AI PGA Gain = 38.4×

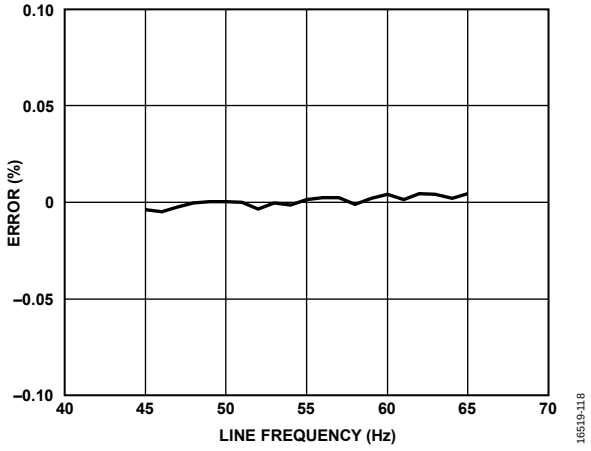


Figure 18. Total Apparent Energy Error vs. Line Frequency, AI PGA Gain = 38.4×

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained with a sinusoidal, 50 Hz current and voltage signals with a swept amplitude from 100% of full scale to 0.033% of full scale.

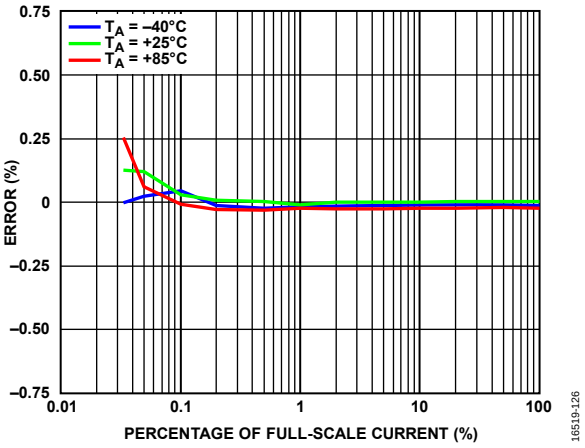


Figure 19. Current Channel A RMS Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 16×

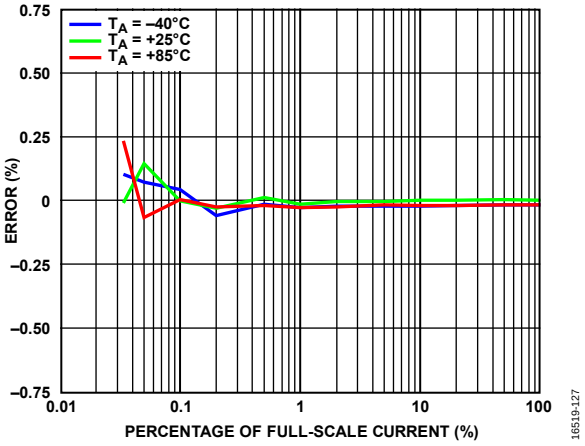


Figure 20. Current Channel A RMS Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 38.4×

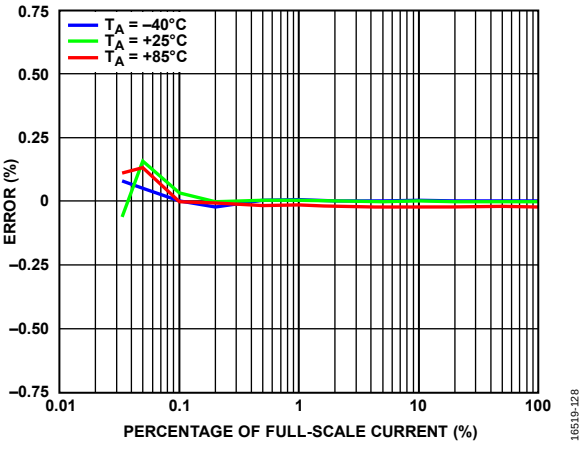


Figure 21. Current Channel B RMS Error as a Percentage of Full-Scale Current over Temperature

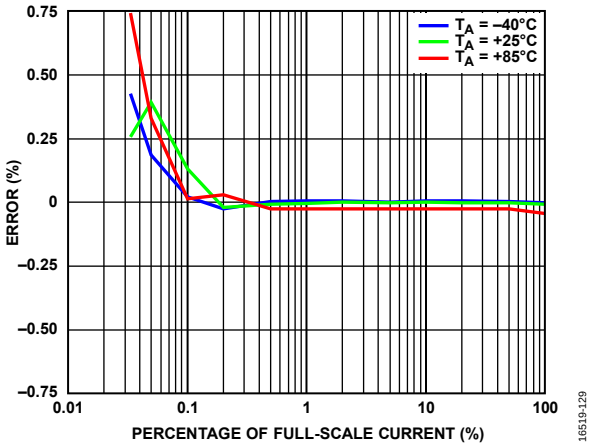


Figure 22. Voltage Channel RMS Error as a Percentage of Full-Scale Current over Temperature

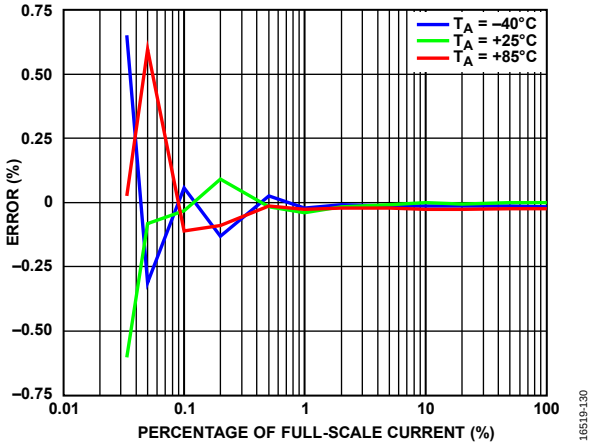


Figure 23. Current Channel A RMS Offset Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 16×

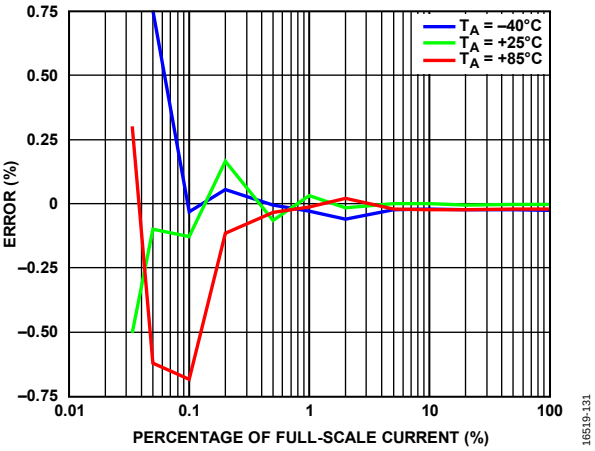


Figure 24. Current Channel A RMS Offset Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 38.4×

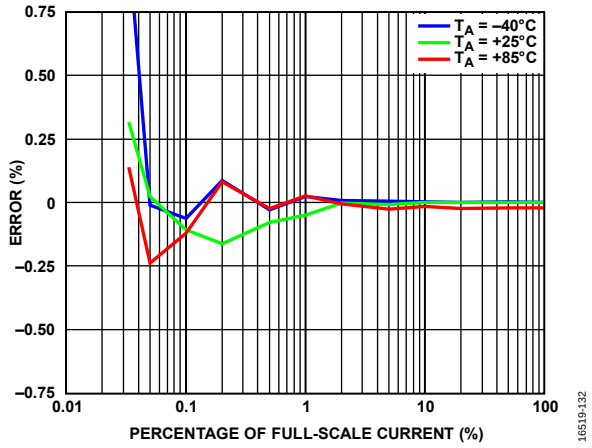


Figure 25. Current Channel B RMS Offset Error as a Percentage of Full-Scale Current over Temperature

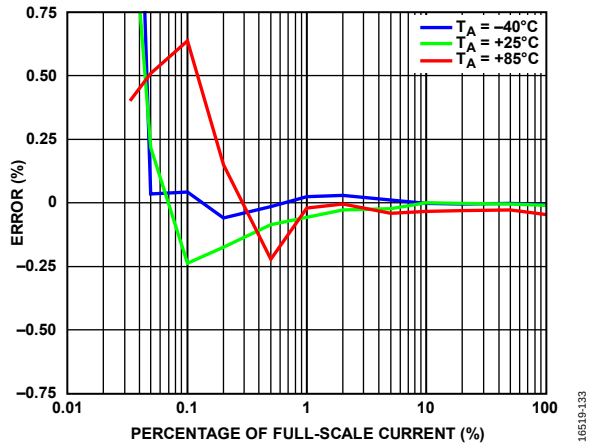


Figure 26. Voltage Channel RMS Offset Error as a Percentage of Full-Scale Current over Temperature

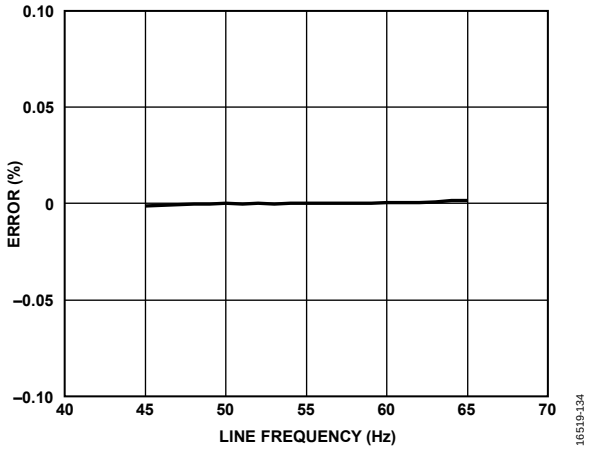


Figure 27. Current Channel A RMS Error vs. Line Frequency

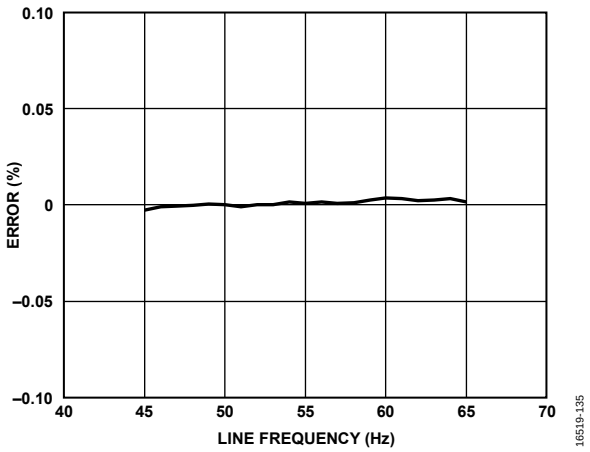


Figure 28. Current Channel B RMS Error vs. Line Frequency

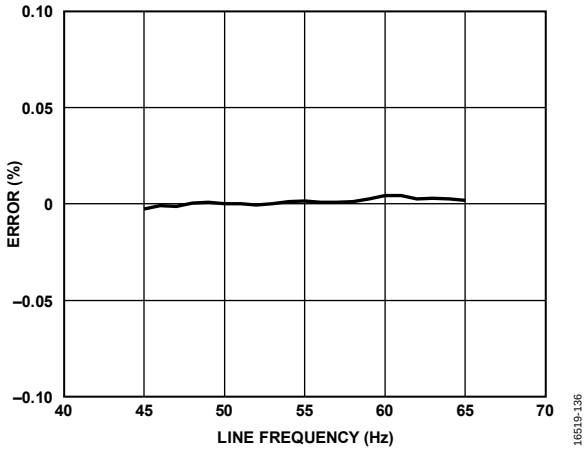


Figure 29. Voltage Channel RMS Error vs. Line Frequency

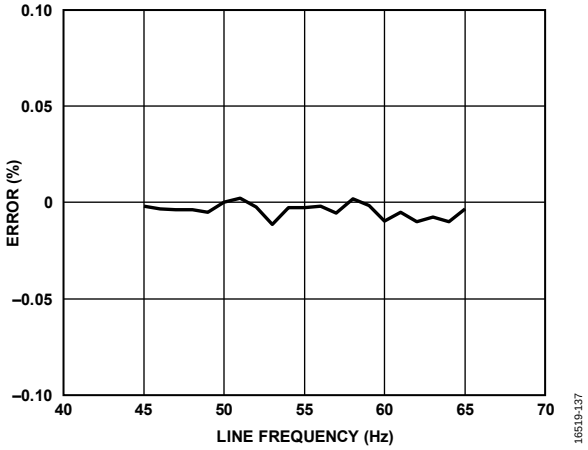


Figure 30. Current Channel A RMS Overcurrent Error vs. Line Frequency

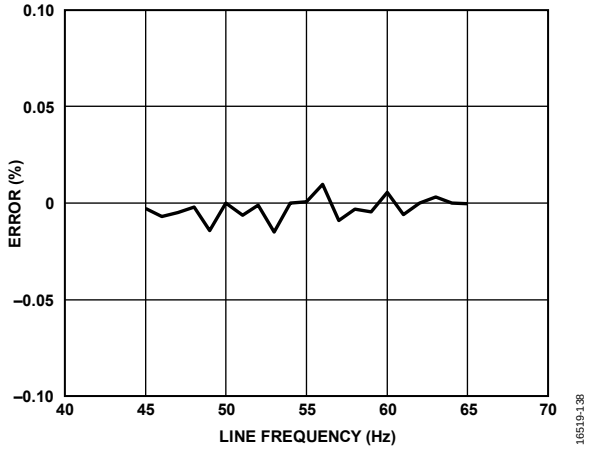


Figure 31. Current Channel B RMS Overcurrent Error vs. Line Frequency

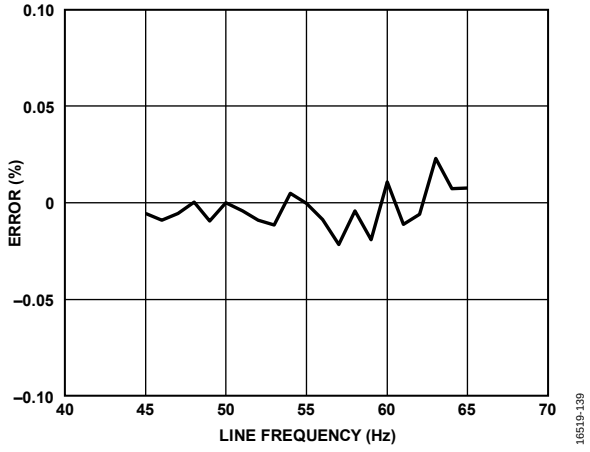


Figure 32. Voltage Channel RMS Overcurrent Error vs. Line Frequency

SIGNAL-TO-NOISE RATIO (SNR) PERFORMANCE OVER DYNAMIC RANGE

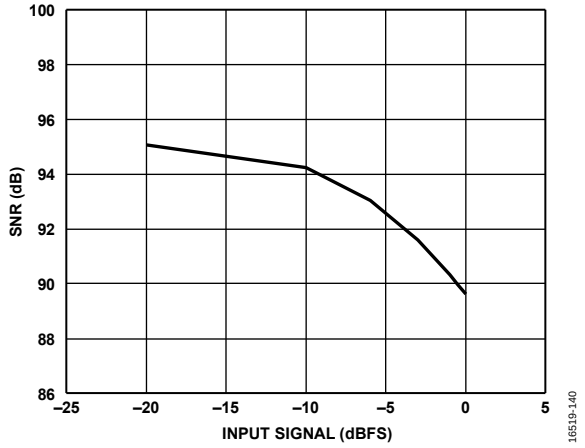


Figure 33. Current Channel A SNR with Respect to Full Scale, AI PGA Gain = 16×

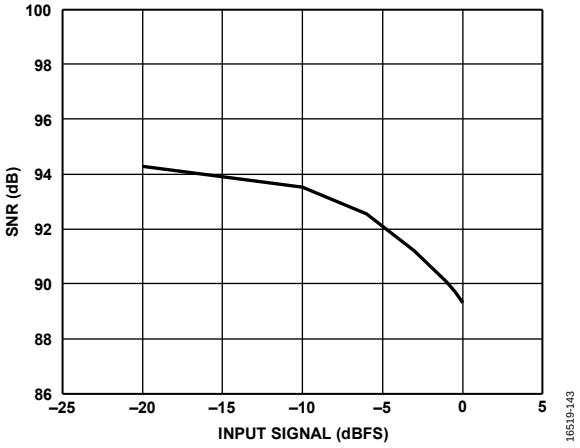


Figure 35. Current Channel B SNR with Respect to Full Scale

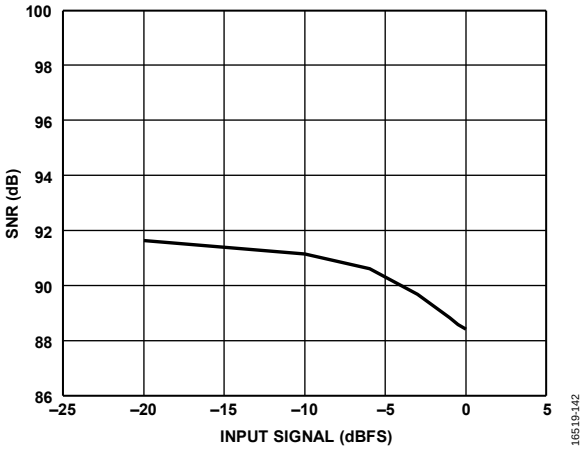


Figure 34. Current Channel A SNR with Respect to Full Scale, AI PGA Gain = 38.4×

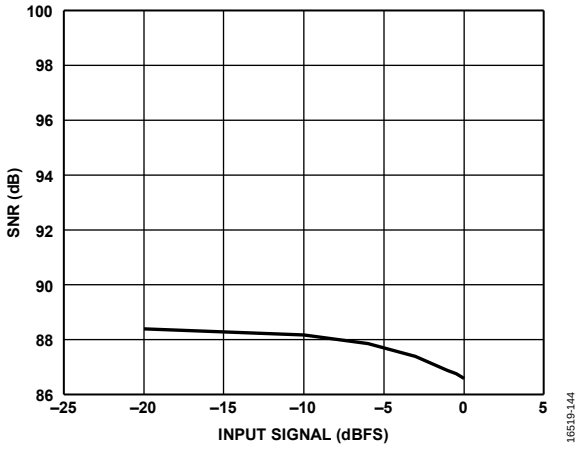


Figure 36. Voltage Channel SNR with Respect to Full Scale

TEST CIRCUIT

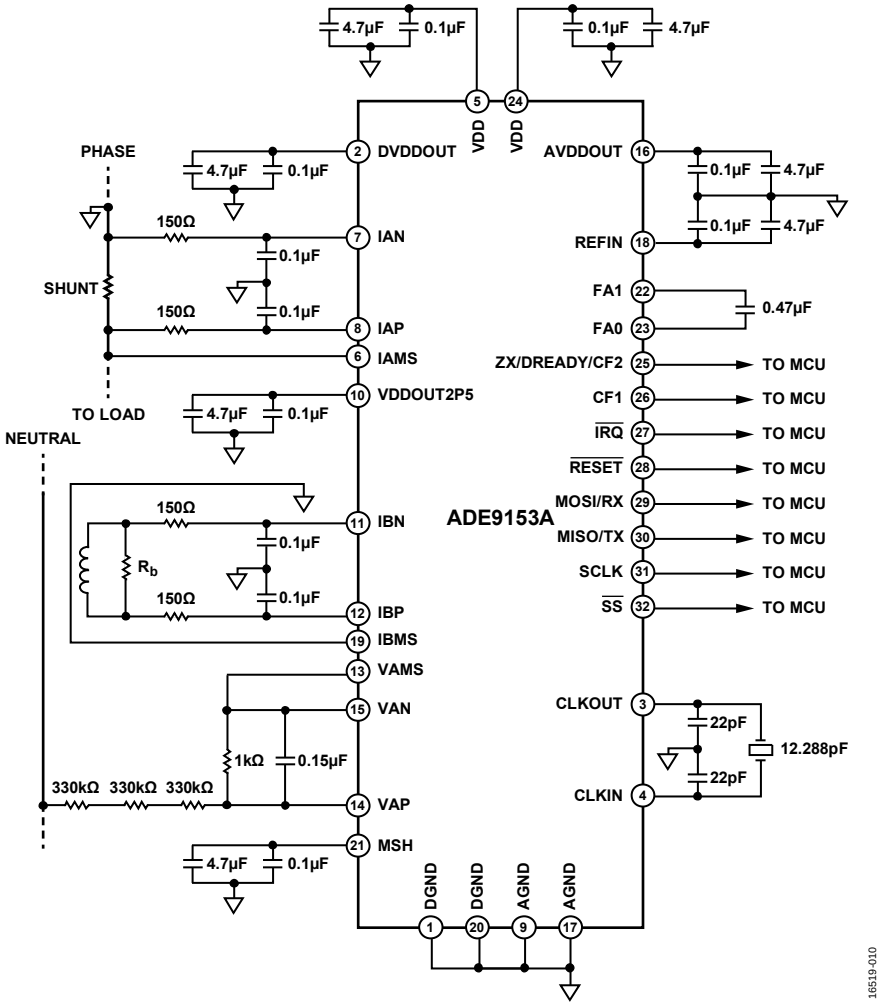


Figure 37. Test Circuit

TERMINOLOGY

Crosstalk
Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 70 Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 200 sec. Crosstalk is expressed in decibels.

Differential Input Impedance (DC)
The differential input impedance represents the impedance between the IAP and IAN pair, the IBP and IBN pair, or the VAP and VAN pair.

ADC Offset
ADC offset is the difference between the average measured ADC output code with both inputs connected to ground and the ideal ADC output code of zero. ADC offset is expressed in mV.

ADC Offset Drift over Temperature
The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. Calculate the offset drift over temperature as follows:

$$Drift = \max\left(\left|\frac{Offset(-40°C) - Offset(+25°C)}{(-40°C - (+25°C))}\right|, \left|\frac{Offset(+85°C) - Offset(+25°C)}{(+85°C - (+25°C))}\right|\right)$$

Offset drift is expressed in µV/°C.

Channel Drift over Temperature
The channel drift over temperature coefficient includes the temperature variation of the PGA and ADC gain when using the internal voltage reference. This coefficient represents the overall temperature coefficient of one channel. With the internal voltage reference, the ADC gain is measured at −40°C, +25°C, and +85°C. Then, the temperature coefficient is calculated as follows:

$$Drift = \max\left(\left|\frac{Gain(-40°C) - Gain(+25°C)}{Gain(+25°C) \times (-40°C - +25°C)}\right|, \left|\frac{Gain(+85°C) - Gain(+25°C)}{Gain(+25°C) \times (+85°C - +25°C)}\right|\right)$$

Gain drift is measured in ppm/°C.

ADC Gain Error
The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.25 V is used. The difference is expressed as a percentage of the ideal code and represents the overall gain error of one channel.

AC Power Supply Rejection (AC PSRR)
AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is V_{NOM} and modulated with ac and the inputs are grounded. For the ac PSRR measurement, 100 sec of samples are captured with nominal supplies (3.3 V) and a second set is captured with an additional ac signal (233 mV rms at 100 Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = $20 \log_{10}(V_{RIPPLE}/V_{NOMINAL})$.

Signal-to-Noise Ratio (SNR)
SNR is calculated by inputting a 50 Hz signal, and acquiring samples over 10 sec. The amplitudes for each frequency, up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB), are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

ADC Output Pass Band
The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 filter and sinc4 filter + infinite impulse response (IIR), low-pass filter (LPF).

ADC Output Bandwidth
The ADC output bandwidth is the bandwidth within −3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

Speed of Convergence
The speed of convergence is the time it takes for *m*Sure to reach a certain level of accuracy. This speed, or time required, is logarithmically proportional to the required accuracy. In other words, if a greater accuracy is required in *m*Sure autocalibration, the time required increases logarithmically.

Similarly, the speed is related to the power mode in which *m*Sure is being run: the lower the power mode, the slower the speed of convergence. This relationship is shown in Table 2 for the specified system. The speed of convergence determines the time it takes to complete the autocalibration process and to reach a certain specified accuracy.

Absolute Accuracy
Absolute accuracy takes into account the accuracy of the *m*Sure reference. The speed of convergence to reach this accuracy depends on the time of an *m*Sure autocalibration run. The longer the time of an *m*Sure autocalibration run, the greater the accuracy.

Certainty of Estimation
The certainty of the *m*Sure estimation, which is also referred to as simply certainty (CERT), is a metric of the precision of the *m*Sure measurement. This certainty is displayed as a percentage; the lower the value, the more confidence there is in the estimation value.

Conversion Constant
In this data sheet, the conversion constant (CC) is the value that *m*Sure returns when estimating the transfer function of the sensor and front end. This value is in units of A/code or V/code, depending on which channel the estimation occurs.

THEORY OF OPERATION

*m*SURE AUTOCALIBRATION FEATURE

The ADE9153A offers *m*Sure autocalibration technology, enabling the automatic calibration of the current and voltage channel accurate, automatic calibration. Autocalibration features have two main components: absolute accuracy and the speed of convergence (see the Terminology section for more details).

When performing autocalibration, the current channels, AI and BI, can be run in two power modes: turbo mode and normal mode. The power mode is a trade-off between the speed of convergence and current consumption. In turbo mode, the speed of convergence is 4× faster and the current consumption is only 2× higher when compared to normal mode, which means that the average consumption over a full run is less than in low power mode, but the instantaneous consumption is higher, as shown in Figure 38.

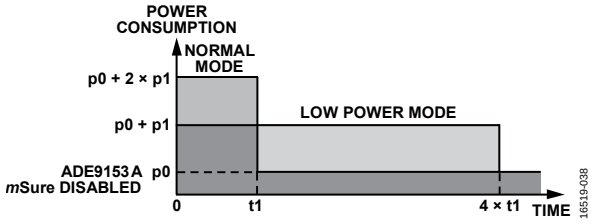


Figure 38. mSure Autocalibration Power Modes to Same Certainty

The ADE9153A can perform the autocalibration of a meter without requiring an accurate source or reference meter. By powering up the meter, the CC of each channel can be measured, and that requirement alone is enough to perform the autocalibration.

After the meter is powered, the autocalibration feature can be run on each channel, one at a time, by using the MS_ACAL_CFG register. Each channel has a set amount of run time. After each channel finishes a run, the certainty of the measurements are confirmed with the MS_ACAL_xCERT registers. Then, the MS_ACAL_xCC register can be used to calculate a gain value that calibrates the meter.

*m*Sure System Warning Interrupts

A set of interrupts in the ADE9153A are dedicated to alerting the user regarding any issues during an *m*Sure autocalibration. These alerts are all indicated as a bit in the MS_STATUS_IRQ register, which is a Tier 2 status register as described in the Interrupts/Events section.

The MS_CONFERR bit is set if a run of *m*Sure is incorrectly set up with the MS_ACAL_CFG register. Clear these registers to 0 and check the settings being written before starting another run.

The MS_ABSENT bit is set if the *m*Sure signal is not detected. If this bit is triggered, wiring in the meter may be incorrect or broken.

The MS_TIMEOUT bit is set if autocalibration is left to run for more than the 600 sec limit of the system. If this interrupt is triggered, ensure that the runs of *m*Sure are being correctly handled in terms of enabling and disabling *m*Sure when appropriate.

The MS_SHIFT bit is set when there is a shift in the CC value that occurs in the middle of a run. This setting means that an event at the meter level changed the CC before the run finished and another run must be performed to achieve a more accurate value. The certainty in this case is high, >50,000 ppm.

Figure 39 to Figure 41 show the speed of convergence of the *m*Sure result (the CC value). As the value of the shunt increases, or as the gain of the PGA increases, the speed of convergence also increases due to the signal size being larger. These are both parameters that must be set based on the overall system, taking into account factors such as the maximum current being measured. Figure 39 to Figure 41 show how the speed of convergence is influenced from factors in a system.

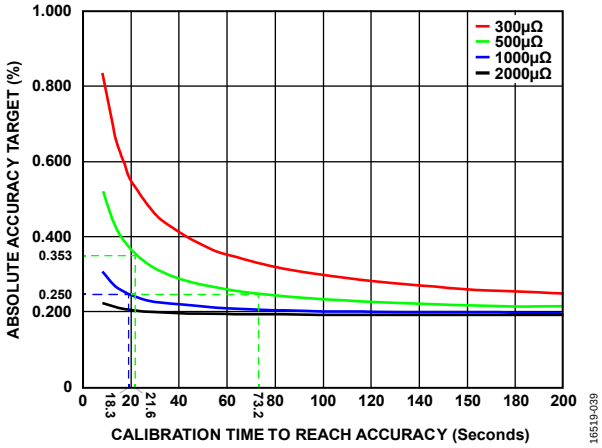


Figure 39. Speed of Convergence for Autocalibration (Shunt Channel, Normal Mode) Based on Shunt Value

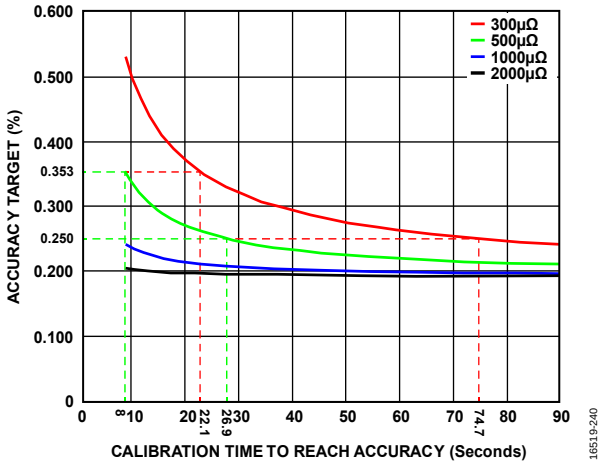


Figure 40. Speed of Convergence for Autocalibration (Shunt Channel, Turbo Mode) Based on Shunt Value

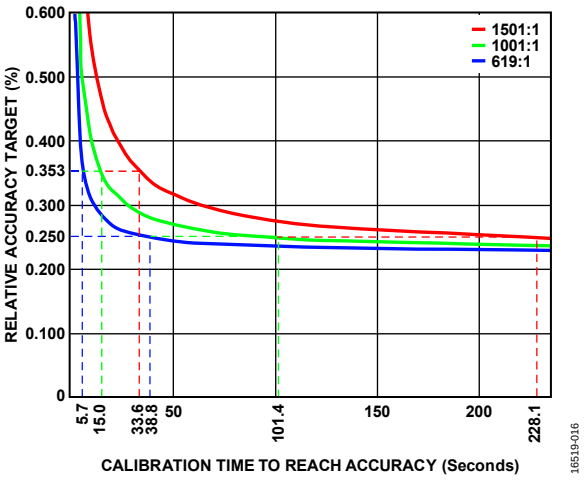


Figure 41. Speed of Convergence for Autocalibration (Voltage Channel) Based on the Potential Divider Ratio

MEASUREMENTS

Current Channel

The ADE9153A has two current channels. Channel A is optimized for use with a shunt, and Channel B is for use with a current transformer. The current channel datapaths for Channel A and Channel B are shown in Figure 42 and Figure 43, respectively.

Current Channel Gain, xIGAIN

The ADE9153A provides current gain calibration registers, AIGAIN and BIGAIN, with one register for each channel.

The current channel gain varies with xIGAIN, as shown in the following equation:

$$Current\ Channel\ Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right)$$

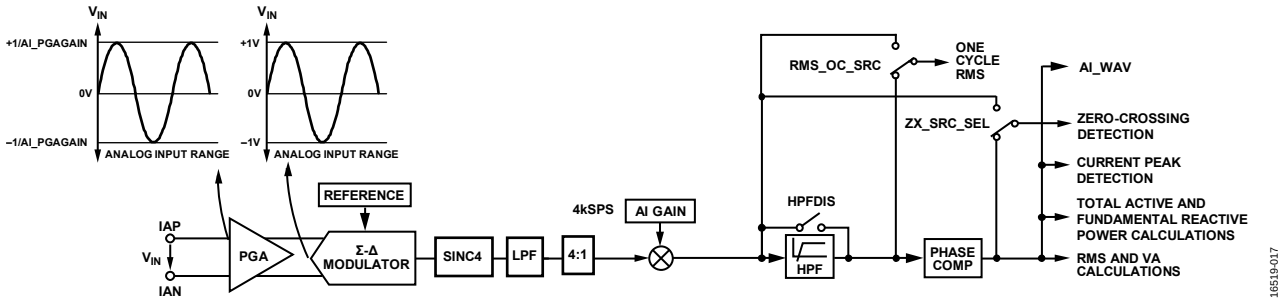


Figure 42. ADE9153A Current Channel A Datapath

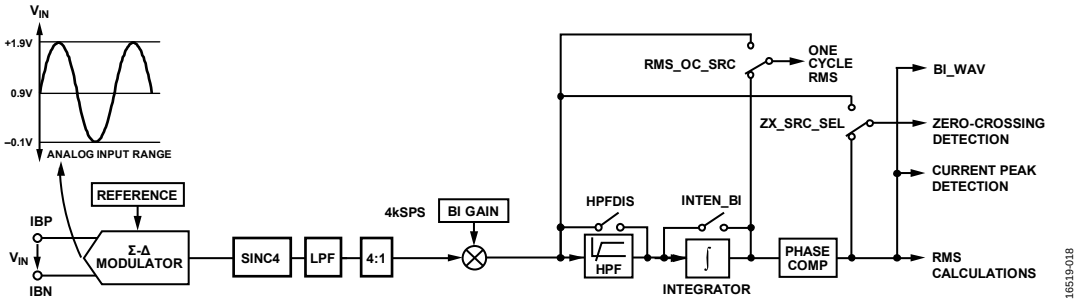


Figure 43. ADE9153A Current Channel B Datapath

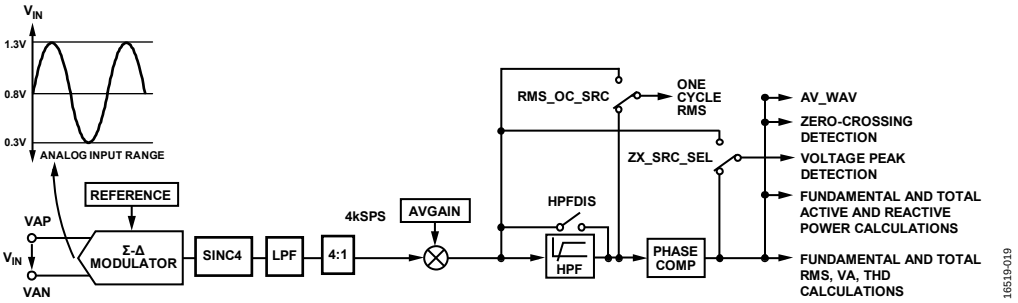


Figure 44. ADE9153A Voltage Channel Datapath

High-Pass Filter

A high-pass filter removes dc offsets for accurate rms and energy measurements. This filter is enabled by default and features a corner frequency of 1.25 Hz.

To disable the high-pass filter on all current and voltage channels, set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF_CRN bits in the CONFIG2 register.

Digital Integrator

A digital integrator is included on Current Channel B for the possibility of interfacing with a di/dt current sensor, also known as Rogowski coils. It is important to take note that the integrator cannot be used with any of the *m*Sure functions. To configure the digital integrator, use the INTEN_BI bits in the CONFIG0 register. The digital integrator is disabled by default.

Phase Compensation

The ADE9153A provides a phase compensation register for each current channel: APHASECAL and BPHASECAL. The phase calibration range is −15° to +2.25° at 50 Hz and −15° to +2.7° at 60 Hz.

Use the following equation to calculate the xPHASECAL value for a given phase correction (φ)° angle. Phase correction (φ)° is positive to correct a current that lags the voltage, and negative to correct a current that leads the voltage, as seen in a current transformer.

$$xPHASECAL = \left(\frac{\sin((\varphi - \omega) + \sin\omega}{\sin(2\omega - \varphi)} \right) \times 2^{27}$$

$$\omega = 2\pi \times f_{LINE}/f_{DSP}$$

where:
f_{LINE} is the line frequency.
f_{DSP} = 4 kHz.

Voltage Channel

The ADE9153A has a single voltage channel with the datapath shown in Figure 44. The AVGAIN register calibrates the voltage channel and has the same scaling as the xIGAIN registers.

RMS and Power Measurements

The ADE9153A calculates total values of rms current, rms voltage, active power, fundamental reactive power, and apparent power. The algorithm for computing the fundamental reactive power requires initialization of the network frequency using the SELFREQ bit in the ACCMODE register and the nominal voltage in the VLEVEL register.

Calculate the VLEVEL value according to the following equation:

$$VLEVEL = x \times 1{,}444{,}084$$

where x is the dynamic range of the nominal voltage input signal with respect to full scale.

For example, if the signal is at ½ of full scale, x = 2. Therefore,

$$VLEVEL = 2 \times 1{,}444{,}084$$

Total RMS

The ADE9153A offers total current and voltage rms measurements on all channels. Figure 45 shows the datapath of the rms measurements.

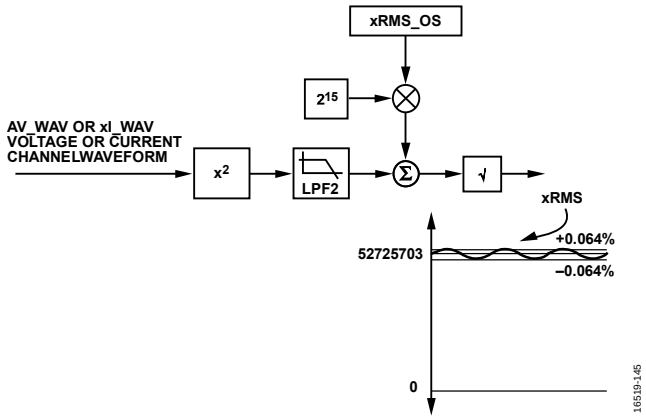


Figure 45. Filter-Based Total RMS Datapath

The total rms calculations, one for each channel (AIRMS, BIRMS, and AVRMS), are updated every 4 kSPS. The xIRMS value at full scale is 52,725,703 codes. The xVRMS value at full scale is 26,362,852 codes. The total rms measurements can be calibrated for gain and offset. Perform gain calibration on the respective Current A voltage channel datapath with the xGAIN registers. The following equation indicates how the offset calibration registers modify the result in the corresponding rms registers:

$$xRMS = \sqrt{xRMS_0^2 + 2^{15} \times xRMOS\_OS}$$

where $xRMS_0$ is the initial xRMS register value before offset calibration.

Total Active Power

The ADE9153A offers a total active power measurement. The datapath for the total active power measurement is shown in Figure 46.

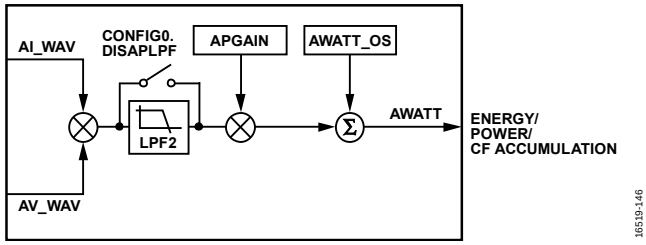


Figure 46. Total Active Power (AWATT) Datapath

The total active power calculation, AWATT, is updated every 4 kSPS. With full-scale inputs, the AWATT value is 10,356,306 codes.

The low-pass filter, LPF2, is enabled by default (DISAPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISAPLPF bit in the CONFIG0 register.

The following equation indicates how the gain and offset calibration registers modify the results in the power register:

$$AWATT = \left(1 + \frac{APGAIN}{2^{27}}\right) AWATT_0 + AWATT\_OS$$

APGAIN is a common gain for all power measurements: active, reactive, and apparent power measurements.

Fundamental Reactive Power

The ADE9153A offers a fundamental reactive power measurement. Figure 47 shows the datapath for the fundamental reactive power calculation.

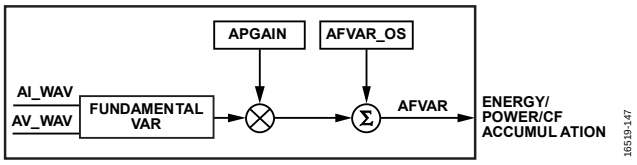


Figure 47. Fundamental Reactive Power (AFVAR) Datapath

The fundamental reactive power calculation, AFVAR, is updated every 4 kSPS. With full-scale inputs, the AFVAR value is 10,356,306 codes.

LPF2 is enabled by default (DISRPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISRPLPF bit in the CONFIG0 register.

The following equation indicates how the gain and offset calibration registers modify the results in the power register:

$$AFVAR = \left(1 + \frac{APGAIN}{2^{27}}\right) AFVAR_0 + AFVAR\_OS$$

Total Apparent Power

The ADE9153A offers a total apparent power measurement. The datapath for the total apparent power calculation is shown in Figure 48.

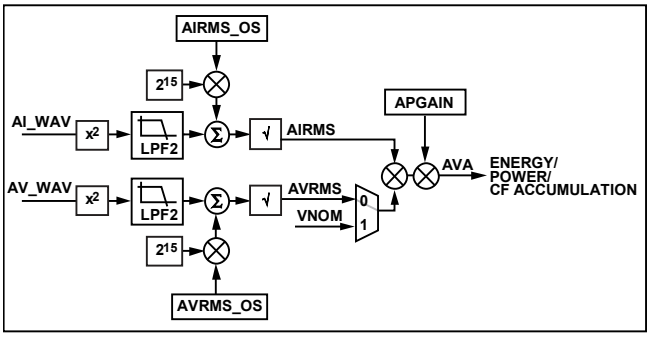


Figure 48. Total Apparent Power (AVA) Datapath

The total apparent power calculation, AVA, is updated every 4 kSPS. With full-scale inputs, the AVA value is 10,356,306 codes.

LPF2 is enabled by default (DISRPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISRPLPF bit in the CONFIG0 register.

The ADE9153A offers a register, VNOM, to calculate the total apparent power when the voltage is missing. This register is set to correspond to a desired voltage rms value. If the VNOMA_EN bit in the CONFIG0 register is set, the VNOM value is used instead of AVRMS.

Energy Accumulation, Power Accumulation, and No Load Detection Features

The ADE9153A calculates total active, fundamental reactive, and total apparent energy. By default, the accumulation mode is signed accumulation but can be changed to absolute, positive only, or negative only for active and reactive energies using the WATTACC and VARACC bits in the ACCMODE register.

Energy Accumulation

The energy is accumulated into a 42-bit signed internal energy accumulator at 4 kSPS. The user readable energy register is signed and 45 bits wide, split between two 32-bit registers as shown in Figure 49. With full-scale inputs, the user energy register overflows in 106.3 sec.

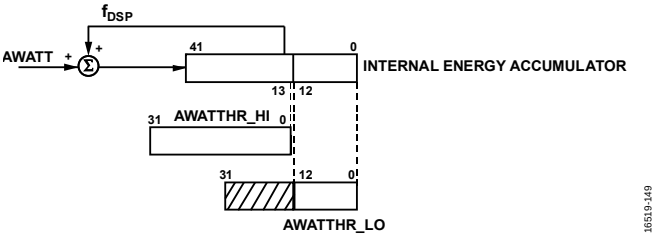


Figure 49. Internal Energy Accumulator to AWATTHR_HI and AWATTHR_LO

Energy Accumulation Modes

The energy registers can accumulate a user defined number of samples or half line cycles configured by the EGY_TMR_MODE bit in the EP_CFG register. Half line cycle accumulation uses the voltage channel zero crossings. The number of samples or half line cycles is set in the EGY_TIME register. The maximum value of EGY_TIME is 8191 decimal. With full-scale inputs, the internal register overflows in 13.3 sec. For a 50 Hz signal, EGY_TIME must be lower than 1329 decimal to prevent overflow during half line cycle accumulation.

After EGY_TIME + 1 samples or half line cycles, the EGYRDY bit is set in the status register and the energy register is updated. The data from the internal energy register is added or latched to the user energy register, depending on the EGY_LD_ACCUM bit setting in the EP_CFG register.

Reset Energy Register on Read

The user can reset the energy register on a read using the RD_RST_EN bit in the EP_CFG register. In this way, the value in the user energy register is reset when it is read.

Power Accumulation

The ADE9153A accumulates the total active, fundamental reactive, and total apparent powers into the AWATT_ACC, AFVAR_ACC, and AVA_ACC 32-bit signed registers, respectively. This accumulation can be used as an averaged power reading.

The number of samples accumulated is set using the PWR_TIME register. The PWRRDY bit in the status register is set after PWR_TIME + 1 samples accumulate at 4 kSPS. The maximum value of the PWR_TIME register is 8191 decimal, and the maximum power accumulation time is 1.024 sec.

The CFxSIGN, AVARSIGN, and AWSIGN bits in the PHSIGN register indicate the sign of accumulated powers over the PWR_TIME interval. When the sign of the accumulated power changes, the corresponding REVx bits in the status register are set and $\overline{\text{IRQ}}$ generates an interrupt.

The ADE9153A allows the user to accumulate total active power and fundamental reactive power into separate positive and negative accumulation registers: PWATT_ACC, NWATT_ACC, PFVAR_ACC, and NFVAR_ACC. A new accumulation from zero begins when the power update interval set in PWR_TIME elapses.

No Load Detection Feature

The ADE9153A features no load detection for each energy to prevent energy accumulation due to noise. If the accumulated energy over the user defined time period is below the user defined threshold, zero energy is accumulated into the energy register. The NOLOAD_TMR bits in the EP_CFG register determine the no load time period, and the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers contain the user defined no load threshold. The no load status is available in the PHNOLOAD register and the status register, which can be driven to the $\overline{\text{IRQ}}$ interrupt pin.

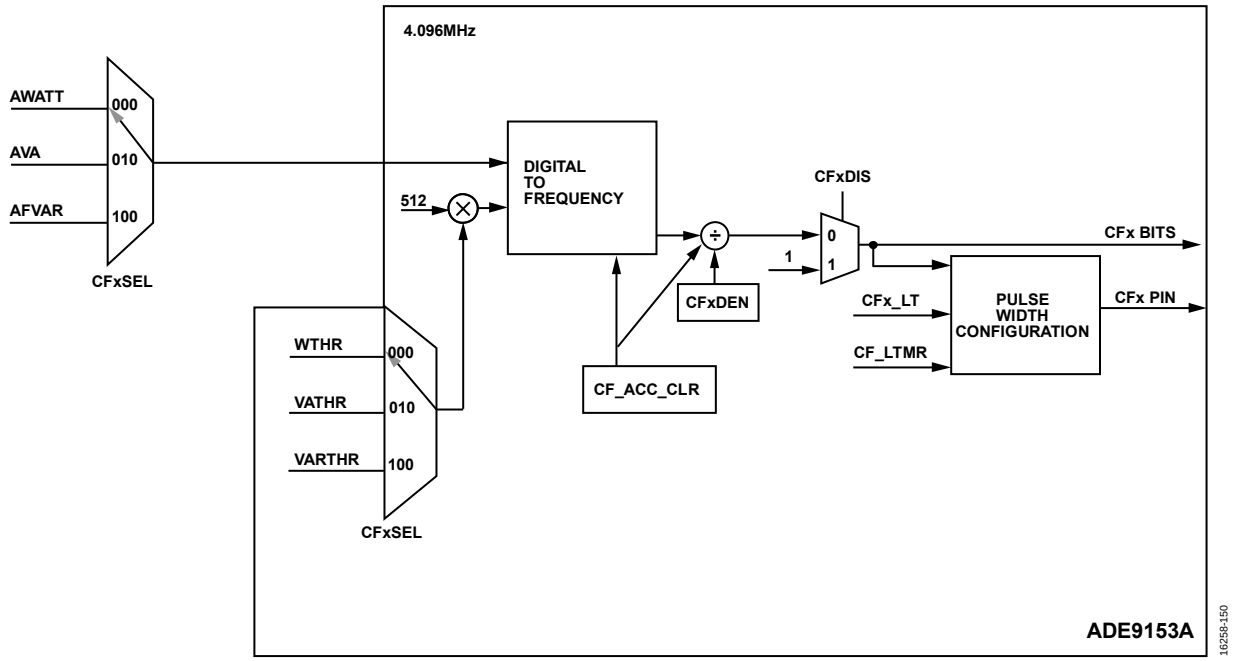


Figure 50. Digital to Frequency Conversion for CFx

Digital to Frequency Conversion—CFx Output

The ADE9153A includes two pulse outputs on the CF1 and CF2 output pins that are proportional to the energy accumulation. The block diagram of the CFx pulse generation is shown in Figure 50. CF2 is multiplexed with ZX and DREADY.

Calibration Frequency (CF) Energy Selection

The CFxSEL bits in the CFMODE register select which type of energy to output on the CFx pins. For example, with CF1SEL = 000b and CF2SEL = 100b, CF1 indicates the total active energy, and CF2 indicates the fundamental reactive energy.

Configuring the CFx Pulse Width

The values of the CFx_LT and the CF_LTMR bits in the CF_LCFG register determine the pulse width.

The maximum CFx with threshold (xTHR) = 0x00100000 and CFxDEN = 2 is 78.9 kHz. It is recommended to leave xTHR at the default value of 0x00100000.

CFx Pulse Sign

The CFxSIGN bits in the PHSIGN register indicate whether the energy in the most recent CFx pulse is positive or negative. The REVPCFx bits in the status register indicate if the CFx polarity changed sign. This feature generates an interrupt on the $\overline{\text{IRQ}}$ pin.

Clearing the CFx Accumulator

To clear the accumulation in the digital to frequency converter and CFDEN counter, write 1 to the CF_ACC_CLR bit in the CONFIG1 register. The CF_ACC_CLR bit automatically clears itself.

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE9153A offers zero-crossing detection on the voltage and both current channels. The current and voltage channel datapaths preceding the zero-crossing detection are shown in Figure 51 and Figure 52.

Use the ZX_SRC_SEL bit in the CONFIG0 register to select data before the high-pass filter or after phase compensation to configure the inputs to zero-crossing detection. ZX_SRC_SEL = 0 by default after reset.

To provide protection from noise, voltage channel zero-crossing events (ZXAV) do not generate if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel zero-crossing detection outputs, ZXAI and ZXBI, are active for all input signals levels.

Calculate the zero-crossing threshold, ZXTHRSH, from the following equation:

$$ZXTHRSH = \frac{(V\_WAV\ at\ Full\ Scale) \times (LPF1\ Attenuation)}{x \times 32 \times 2^8}$$

where
V_WAV at Full Scale is ±37,282,702 decimal.
LPF1 Attenuation is 0.86 at 50 Hz, and 0.81 at 60 Hz.
x is the dynamic range below which the voltage channel zero crossing must be blocked.

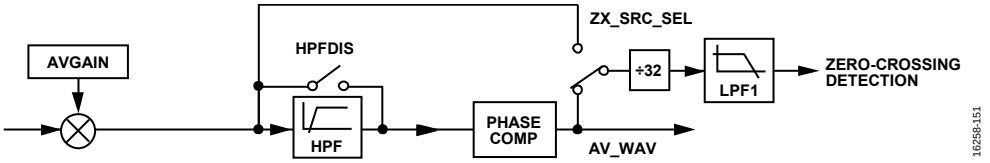


Figure 51. Voltage Channel Signal Path Preceding Zero-Crossing Detection

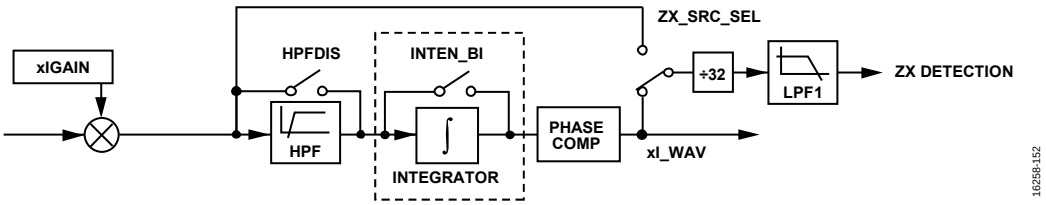


Figure 52. Current Channel Signal Path Preceding Zero-Crossing Detection

The zero-crossing detection circuits have two different output rates: 4 kSPS and 512 kSPS. The 4 kSPS zero-crossing signal calculates the line period, updates the ZXx bits in the status register, and monitors the zero-crossing timeout and energy accumulation functions. The 512 kSPS zero-crossing signal calculates the angle and updates the zero-crossing output on the CF2/ZX/DREADY pin.

CF1/ZX/DREADY

The CF1/ZX/DREADY pin can output zero crossings using the ZX_OUT_OE bit in the CONFIG1 register. The CF1/ZX/DREADY output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs.

Zero-Crossing Timeout

If a zero crossing is not received after (ZXTOUT + 1)/4000 sec, the ZXTOAV bit in the status register is set and generates an interrupt on the $\overline{\text{IRQ}}$ pin.

Line Period Calculation

The ADE9153A calculates the line period on the voltage with the result available in the APERIOD register. Calculate the line period, t_L, from the APERIOD register according to the following equation:

$$t_L = \frac{APERIOD + 1}{4000 \times 2^{16}} (\text{sec})$$

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if zero crossings are not detected, the APERIOD register is coerced to correspond to 50 Hz or 60 Hz, depending on the SELFREQ bit in the ACCMODE register.

Angle Measurement

The ADE9153A provides two angle measurements: ANGL_AV_AI for the angle between current Channel A and the voltage channel, and ANGL_AI_BI for the angle between Current Channel A and Current Channel B. To convert angle register readings to degrees, use the following equations.

For a 50 Hz system,

Angle (Degrees) = *ANGL_x_y* × 0.017578125

For a 60 Hz system,

Angle (Degrees) = *ANGL_x_y* × 0.02109375

One Cycle RMS Measurement

RMS½ is an rms measurement performed over one line cycle, updated every half cycle. This measurement is provided on all three channels for voltage and current. All the half cycle rms measurements are performed over the same time interval and update at the same time, as indicated by the RMS_OC_RDY bit in the status register. The results are stored in the AIRMS_OC, AVRMS_OC, and BIRMS_OC registers. The xIRMS_OC and AVRMS_OC register reading with full-scale inputs is 52,725,703 codes and 26,362,852, respectively.

It is recommended to select the data before the high-pass filter for the fast rms measurement by setting the RMS_OC_SRC bit in the CONFIG0 register.

The voltage channel is used for the timing of the rms½ measurement. Alternatively, set the UPERIOD_SEL bit in the CONFIG2 register to set desired period in the USER_PERIOD register for line period measurement. An offset correction register, xRMS_OC_OS, is available for improved performance with small input signal levels. The datapath is shown in Figure 53.

Dip and Swell Indication

The ADE9153A monitors the rms½ value on the voltage channel to determine a dip and swell event. If the voltage goes below a threshold specified in the DIP_LVL register for a user configured number of half cycles in the DIP_CYC register, the DIPA bit is set in the EVENT_STATUS register. The minimum rms½ value measured during the dip is stored in the DIPA register.

Similarly, if the voltage goes above a threshold specified in the SWELL_LVL register for a user configured number of half cycles in the SWELL_CYC register, the SWELLA bit is set in the EVENT_STATUS register. The maximum rms½ value measured during the swell is stored in the SWELLA register.

The dip and swell event generates an interrupt on the $\overline{\text{IRQ}}$ pin.

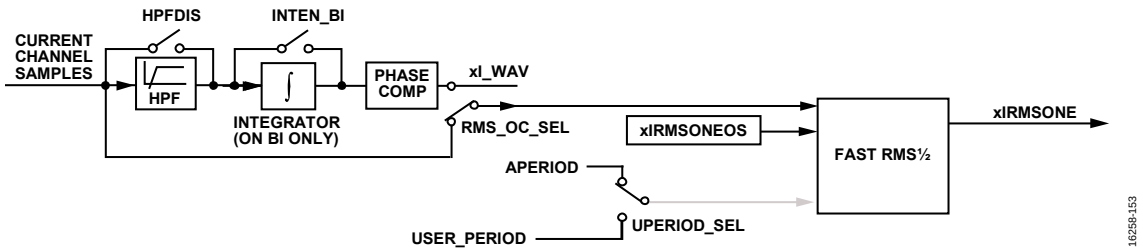


Figure 53. RMS½, RMS Measurements

Overcurrent Indication

The ADE9153A monitors the rms½ value on current channels to determine overcurrent events. If an rms½ current is greater than the user configured threshold in the OI_LVL register, the OIx bit in the EVENT_STATUS register is set. The overcurrent event generates an interrupt on the $\overline{\text{IRQ}}$ pin.

The OIx_EN bits in the CONFIG3 register select the current channel to monitor for overcurrent events. The OIx bits in the EVENT_STATUS register indicate which current channel exceeded the threshold. The overcurrent value is stored in the OIA and OIB registers.

Peak Detection

The ADE9153A records the peak value measured on all three channels from the AI_WAV, AV_WAV, and BI_WAV waveforms. The PEAK_SEL bits in the CONFIG3 register allow the user to select which channel to monitor.

The IPEAK register stores the peak current value in the IPEAKVAL bits and indicates which phase currents reached the value in the IPPHASE bits. IPEAKVAL is equal to xI_WAV/2^5.

Similarly, VPEAK stores the peak voltage value in the VPEAKVAL bits. VPEAKVAL is equal to AV_WAV/2^5. After a read, the VPEAK and IPEAK registers reset.

Power Factor

The power factor calculation, APF, is updated every 1.024 sec. The sign of the APF calculation follows the sign of AWATT. To determine if power factor is leading or lagging, refer to the sign of the total or fundamental reactive energy and the sign of the APF or AWATT value, as shown in Figure 54.

The power factor result is stored in 5.27 format. The highest power factor value is 0x07FF FFFF, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800 0000. To determine the power factor from the APF register value, use the following equation:

$$Power\ Factor = APF \times 2^{-27}$$

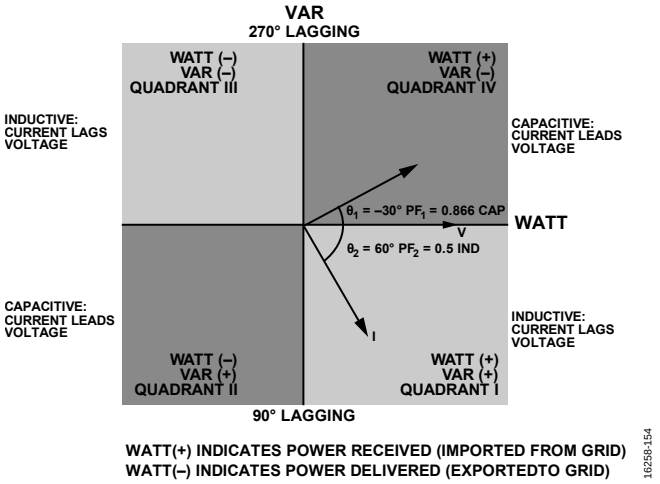


Figure 54. WATT and VAR Power Sign for Capacitive and Inductive Loads

Temperature

The temperature reading is available in the TEMP_RSLT register. To convert the temperature range into Celsius, use the following equation:

$$Temperature\ (°C) = TEMP\_RSLT \times (-TEMP\_GAIN/2^{17}) + (TEMP\_OFFSET/2^5)$$

During the manufacturing of each device, the TEMP_GAIN and TEMP_OFFSET bits of Register TEMP_TRIM are programed. To configure the temperature sensor, program the TEMP_CFG register.

APPLICATIONS INFORMATION

INTERRUPTS/EVENTS

The ADE9153A has two pins, $\overline{\text{IRQ}}$ and ZX/DREADY/CF2, that can be used as interrupts to the host processor.

$\overline{\text{IRQ}}$ PIN INTERRUPTS

The $\overline{\text{IRQ}}$ pin goes low when an enabled interrupts occurs and stays low until the event is acknowledged by setting the corresponding status bit in the status register. The bits in the mask register configure the respective interrupts.

SERVICING INTERRUPTS

Interrupts in the ADE9153A are in a tiered system where it never takes more than two communications to clear an interrupt. The status register is a Tier 1 interrupt register and CHIP_STATUS, EVENT_STATUS, and MS_STATUS_IRQ are Tier 2 interrupt registers, which correspond to the status bits, CHIP_STAT, EVENT_STAT, and MS_STAT.

For the Tier 1 status register bits, Bits[25:0],

1. Read the status register to see which bit is set.
2. Write a 1 to the status bits that must be cleared.

For the Tier 2 status register bits, Bits[31:29],

1. Read the status register to see which Tier 2 register is set.
2. Read the Tier 2 register (CHIP_STATUS, EVENT_STATUS, or MS_STATUS_IRQ); the register is cleared on a read.

CF2/ZX/DREADY EVENT PIN

The CF2 pin is multiplexed with the ZX and DREADY functions that track the state of zero crossings and when new data is available, respectively. The ZX pin functionality goes high with negative to positive zero crossings and goes low with positive negative zero crossings. The DREADY pin functionality outputs a 1 ms pulse when new data is ready.

ACCESSING ON-CHIP DATA

The ADE9153A has two communication protocols for accessing on-chip data, a fast 10 MHz SPI and a slower 4800 Baud/115,200 Baud universal asynchronous receiver/transmitter (UART).

After power-on or reset, to select the SPI interface, the $\overline{SS}$ pin must be low and the SCLK pin must be high. To select the UART interface, the $\overline{SS}$ pin must be high and the SCLK pin must be low. When the ADE9153A is powered, the communication is set, and it is locked in until the next ADE9153A reset.

SPI PROTOCOL OVERVIEW

The ADE9153A has an SPI-compatible interface consisting of four pins: SCLK, MOSI/RX, MISO/TX, and $\overline{SS}$. The ADE9153A is always an SPI slave; it never initiates a SPI communication. The SPI interface is compatible with 16-bit and 32-bit read/write operations. The maximum serial clock frequency supported by this interface is 10 MHz.

The ADE9153A provides SPI burst read functionality on certain registers, allowing multiple register to be read after sending one command header, CMD_HDR.

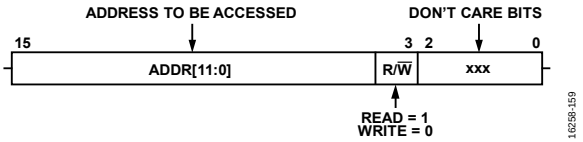


Figure 55. Command Header, CMD_HDR

The ADE9153A SPI port calculates a 16-bit cyclic redundancy check (CRC-16) of the data sent out on the MOSI/RX pin so that the integrity of the data received by the master can be checked. The CRC of the data sent out on the MOSI/RX pin during the last register read is offered in a 16-bit register, CRC_SPI, and can be appended to the SPI read data as part of the SPI transaction.

UART INTERFACE

The ADE9153A has a UART interface consisting of two pins: RX and TX. This UART interface allows an isolated communication interface to be achieved using only two low cost opto-isolators. The UART interface is compatible with 16-bit and 32-bit read/write operations. When the UART is selected, the Baud rate is 4800 Baud; however, a faster communication rate of 115,200 Baud can also be selected. The ADE9153A Baud rates are shown in Table 7.

Table 7. UART Baud Rate

Ideal Rate (Baud)	ADE9153A Actual Rate (Baud) (CLKIN = 12.288 MHz)	Error
4800	CLKIN/2560 = 4800	0.00%
115,200	CLKIN/104 = 118153.8	2.56%

If the UART is to be used at 4800 Baud, no action is required when the UART interface is chosen after a reset. The 115,200 Baud rate is chosen with a single write of 0x0052 to the UART_BAUD_SWITCH register. The Baud rate can be switched back to 4800 Baud by writing 0x000 to the UART_BAUD_SWITCH register. UART_BAUD_SWITCH is a write only register.

The UART communication is comprised of 11-bit frames with one start bit, eight data bits, one odd parity bit, and one stop bit.

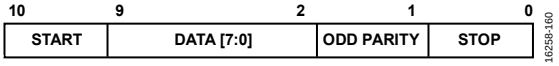


Figure 56. Frame Bits

Every UART communication starts with two command frames that contain the ADE9153A address being accessed, a read or write bit, a bit indicating whether to include the checksum, and then 00b as the lower two bits (see Figure 57).

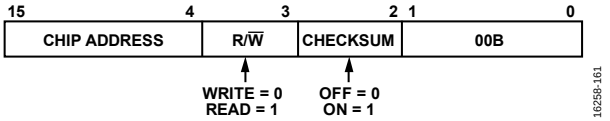


Figure 57. Command Header (CMD)

The frames are then organized with the two command header frames, followed by the data frames, and finally an optional checksum that is enabled in the command frames.

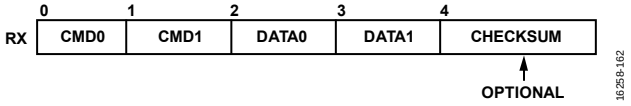


Figure 58. UART 16-Bit Write

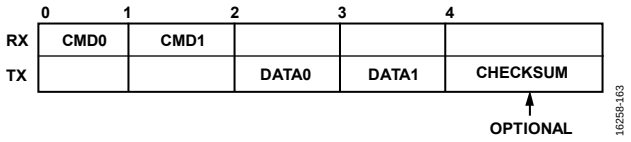


Figure 59. UART 16-Bit Read

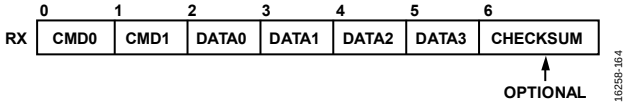


Figure 60. UART 32-Bit Write

COMMUNICATION VERIFICATION REGISTERS

The ADE9153A includes three register that allow SPI operation verification. The LAST_CMD (Address 0x4AE), LAST_DATA_16 (Address 0x4AC), and LAST_DATA_32 (Address 0x423) registers record the received CMD_HDR and the last read or transmitted data.

CRC OF CONFIGURATION REGISTERS

The configuration register CRC feature in the ADE9153A monitors certain user and private register values. The results are stored in the CRC_RSLT register. When enabled, the ADE9153A generates an interrupt on $\overline{\text{IRQ}}$ if any of the monitored registers change the value of the CRC_RSLT register.

CONFIGURATION LOCK

The configuration lock feature prevents changes to the ADE9153A configuration. To enable this feature, write 0x3C64 to the WR_LOCK register. To disable the feature, write 0x4AD1.

To determine whether this feature is active, read the WR_LOCK register, which reads as 1 if the protection is enabled and 0 if it is disabled.

When this feature is enabled, it prevents writing to addresses from Address 0x000 to Address 0x073 and Address 0x400 to Address 0x4FE.

REGISTER INFORMATION

REGISTER SUMMARY

Table 8. Register Summary

Address	Name	Description	Length (Bits)	Reset	Access
0x000	AIGAIN	Phase A current gain adjust.	32	0x00000000	R/W
0x001	APHASECAL	Phase A phase correction factor.	32	0x00000000	R/W
0x002	AVGAIN	Phase A voltage gain adjust.	32	0x00000000	R/W
0x003	AIRMS_OS	Phase A current rms offset for filter-based AIRMS calculation.	32	0x00000000	R/W
0x004	AVRMS_OS	Phase A voltage rms offset for filter-based AVRMS calculation.	32	0x00000000	R/W
0x005	APGAIN	Phase A power gain adjust for AWATT, AVA, and AFVAR calculations.	32	0x00000000	R/W
0x006	AWATT_OS	Phase A total active power offset correction for AWATT calculation.	32	0x00000000	R/W
0x007	AFVAR_OS	Phase A fundamental reactive power offset correction for AFVAR calculation.	32	0x00000000	R/W
0x008	AVRMS_OC_OS	Phase A voltage rms offset for fast rms, AVRMS_OC calculation.	32	0x00000000	R/W
0x009	AIRMS_OC_OS	Phase A current rms offset for fast rms, AIRMS_OC calculation.	32	0x00000000	R/W
0x010	BIGAIN	Phase B current gain adjust.	32	0x00000000	R/W
0x011	BPHASECAL	Phase B correction factor.	32	0x00000000	R/W
0x013	BIRMS_OS	Phase B current rms offset for filter-based BIRMS calculation.	32	0x00000000	R/W
0x019	BIRMS_OC_OS	Phase B current rms offset for fast rms, BIRMS_OC calculation.	32	0x00000000	R/W
0x020	CONFIG0	DSP configuration register.	32	0x00000000	R/W
0x021	VNOM	Nominal phase voltage rms used in the calculation of apparent power, AVA, when the VNOMA_EN bit is set in the CONFIG0 register.	32	0x00000000	R/W
0x022	DICOEFF	Value used in the digital integrator algorithm. If the integrator is turned on, with INTEN_BI equal to 1 in the CONFIG0 register, it is recommended to leave this register at the default value.	32	0x00000000	R/W
0x023	BI_PGAGAIN	PGA gain for Current Channel B ADC.	32	0x00000000	R/W
0x030	MS_ACAL_CFG	*m*Sure autocalibration configuration register.	32	0x00000000	R/W
0x045	MS_AICC_USER	User input Current Channel A CC value for *m*Sure initialization and threshold calculation.	32	0x00000000	R/W
0x046	MS_BICC_USER	User input Current Channel B CC value for *m*Sure initialization and threshold calculation.	32	0x00000000	R/W
0x047	MS_AVCC_USER	User input Voltage Channel CC value for *m*Sure initialization and threshold calculation.	32	0x00000000	R/W
0x049	CT_PHASE_DELAY	Phase delay of the CT used on Current Channel B. This register is in 5.27 format and expressed in degrees.	32	0x00000000	R/W
0x04A	CT_CORNER	Corner frequency of the CT. This value is calculated from the CT_PHASE_DELAY value.	32	0x00000000	R/W
0x04C	VDIV_RSMALL	This register holds the resistance value, in Ω, of the small resistor in the resistor divider.	32	0x00000000	R/W
0x200	AI_WAV	Instantaneous Current Channel A waveform processed by the DSP at 4 kSPS.	32	0x00000000	R
0x201	AV_WAV	Instantaneous voltage channel waveform processed by the DSP at 4 kSPS.	32	0x00000000	R
0x202	AIRMS	Phase A filter-based current rms value updated at 4 kSPS.	32	0x00000000	R
0x203	AVRMS	Phase A filter-based voltage rms value updated at 4 kSPS.	32	0x00000000	R
0x204	AWATT	Phase A low-pass filtered total active power updated at 4 kSPS.	32	0x00000000	R
0x206	AVA	Phase A total apparent power updated at 4 kSPS.	32	0x00000000	R
0x207	AFVAR	Phase A fundamental reactive power updated at 4 kSPS.	32	0x00000000	R
0x208	APF	Phase A power factor updated at 1.024 sec.	32	0x00000000	R
0x209	AIRMS_OC	Phase A current fast rms calculation; one cycle rms updated every half cycle.	32	0x00000000	R
0x20A	AVRMS_OC	Phase A voltage fast rms calculation; one cycle rms updated every half cycle.	32	0x00000000	R

Address	Name	Description	Length (Bits)	Reset	Access
0x210	BI_WAV	Instantaneous Phase B Current Channel waveform processed by the DSP at 4 kSPS.	32	0x00000000	R
0x212	BIRMS	Phase B filter-based current rms value updated at 4 kSPS.	32	0x00000000	R
0x219	BIRMS_OC	Phase B Current fast rms calculation; one cycle rms updated every half cycle.	32	0x00000000	R
0x220	MS_ACAL_AICC	Current Channel A *m*Sure CC estimation from autocalibration.	32	0x00000000	R
0x221	MS_ACAL_AICERT	Current Channel A *m*Sure certainty of autocalibration.	32	0x00000000	R
0x222	MS_ACAL_BICC	Current Channel B *m*Sure CC estimation from autocalibration.	32	0x00000000	R
0x223	MS_ACAL_BICERT	Current Channel B *m*Sure certainty of autocalibration.	32	0x00000000	R
0x224	MS_ACAL_AVCC	Voltage channel *m*Sure CC estimation from autocalibration.	32	0x00000000	R
0x225	MS_ACAL_AVCERT	Voltage channel *m*Sure certainty of autocalibration.	32	0x00000000	R
0x240	MS_STATUS_CURRENT	The MS_STATUS_CURRENT register contains bits that reflect the present state of the *m*Sure system.	32	0x00000000	R
0x241	VERSION_DSP	This register indicates the version of the ADE9153B DSP after the user writes run = 1 to start measurements.	32	0x00000000	R
0x242	VERSION_PRODUCT	This register indicates the version of the product being used.	32	0x0009153A	R
0x39D	AWATT_ACC	Phase A accumulated total active power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x39E	AWATTHR_LO	Phase A accumulated total active energy, least significant bits (LSBs). Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x39F	AWATTHR_HI	Phase A accumulated total active energy, most significant bits (MSBs). Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x3B1	AVA_ACC	Phase A accumulated total apparent power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3B2	AVAHR_LO	Phase A accumulated total apparent energy, LSBs. Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x3B3	AVAHR_HI	Phase A accumulated total apparent energy, MSBs. Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x3BB	AFVAR_ACC	Phase A accumulated fundamental reactive power. Updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3BC	AFVARHR_LO	Phase A accumulated fundamental reactive energy, LSBs. Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x3BD	AFVARHR_HI	Phase A accumulated fundamental reactive energy, MSBs. Updated according to the settings in the EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x3EB	PWATT_ACC	Accumulated positive total active power from the AWATT register; updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3EF	NWATT_ACC	Accumulated negative total active power from the AWATT register; updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3F3	PFVAR_ACC	Accumulated positive fundamental reactive power from the AFVAR register, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3F7	NFVAR_ACC	Accumulated negative fundamental reactive power from the AFVAR register, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x400	IPEAK	Current peak register.	32	0x00000000	R
0x401	VPEAK	Voltage peak register.	32	0x00000000	R
0x402	Status	Tier 1 interrupt status register.	32	0x00000000	R/W
0x405	Mask	Tier 1 interrupt enable register.	32	0x00000000	R/W
0x409	OI_LVL	Overcurrent RMS_OC detection threshold level.	32	0x00FFFFFF	R/W
0x40A	OIA	Phase A overcurrent RMS_OC value. If overcurrent detection on this channel is enabled with OIA_EN in the CONFIG3 register and AIRMS_OC is greater than the OILVL threshold, this value is updated.	32	0x00000000	R
0x40B	OIB	Phase B overcurrent RMS_OC value. See the OIA description.	32	0x00000000	R
0x40E	USER_PERIOD	User configured line period value used for RMS_OC when the UPERIOD_SEL bit in the CONFIG2 register is set.	32	0x00500000	R/W

Address	Name	Description	Length (Bits)	Reset	Access
0x40F	VLEVEL	Register used in the algorithm that computes the fundamental reactive power.	32	0x0045D450	R/W
0x410	DIP_LVL	Voltage RMS_OC dip detection threshold level.	32	0x00000000	R/W
0x411	DIPA	Phase A voltage RMS_OC value during a dip condition.	32	0x007FFFFF	R
0x414	SWELL_LVL	Voltage RMS_OC swell detection threshold level.	32	0x00FFFFFF	R/W
0x415	SWELLA	Phase A voltage RMS_OC value during a swell condition.	32	0x00000000	R
0x418	APERIOD	Line period on the Phase A voltage.	32	0x00500000	R
0x41C	ACT_NL_LVL	No load threshold in the total active power datapath.	32	0x00008225	R/W
0x41D	REACT_NL_LVL	No load threshold in the fundamental reactive power datapath.	32	0x00008225	R/W
0x41E	APP_NL_LVL	No load threshold in the total apparent power datapath.	32	0x00008225	R/W
0x41F	PHNOLOAD	Phase no load register.	32	0x00000000	R
0x420	WTHR	Sets the maximum output rate from the digital to frequency converter of the total active power for the CF calibration pulse output. It is recommended to leave this at WTHR = 0x00100000.	32	0x00100000	R/W
0x421	VARTHR	See WTHR. It is recommended to leave this at VARTHR = 0x00100000.	32	0x00100000	R/W
0x422	VATHR	See WTHR. It is recommended to leave this value at VATHR = 0x00100000.	32	0x00100000	R/W
0x423	LAST_DATA_32	This register holds the data read or written during the last 32-bit transaction on the SPI port.	32	0x00000000	R
0x424	CT_PHASE_MEAS	Set to 0xE5 for CT_PHASE_DELAY measurement; otherwise, the value must be 0xE4.	32	0x000000E4	R/W
0x425	CF_LCFG	CF calibration pulse width configuration register.	32	0x00000000	R/W
0x471	TEMP_TRIM	Temperature sensor gain and offset, calculated during the manufacturing process.	32	0x00000000	R
0x472	CHIP_ID_HI	Chip identification, 32 MSBs.	32	0x00000000	R
0x473	CHIP_ID_LO	Chip identification, 32 LSBs.	32	0x00000000	R
0x480	Run	Write this register to 1 to start the measurements.	16	0x0000	R/W
0x481	CONFIG1	Configuration Register 1.	16	0x0300	R/W
0x485	ANGL_AV_AI	Time between positive to negative zero crossings on Phase A voltage and current.	16	0x0000	R
0x488	ANGL_AI_BI	Time between positive to negative zero crossings on Phase A and Phase B currents.	16	0x0000	R
0x48B	DIP_CYC	Voltage RMS_OC dip detection cycle configuration.	16	0xFFFF	R/W
0x48C	SWELL_CYC	Voltage RMS_OC swell detection cycle configuration.	16	0xFFFF	R/W
0x490	CFMODE	CFx configuration register.	16	0x0000	R/W
0x491	COMPMODE	Computation mode register. Set this register to 0x0005.	16	0x0000	R/W
0x492	ACCMODE	Accumulation mode register.	16	0x0000	R/W
0x493	CONFIG3	Configuration Register 3 for configuration of power quality settings.	16	0x0000	R/W
0x494	CF1DEN	CF1 denominator register.	16	0xFFFF	R/W
0x495	CF2DEN	CF2 denominator register.	16	0xFFFF	R/W
0x498	ZXTOUT	Zero-crossing timeout configuration register.	16	0xFFFF	R/W
0x499	ZXTHRSH	Voltage channel zero-crossing threshold register.	16	0x0009	R/W
0x49A	ZX_CFG	Zero-crossing detection configuration register.	16	0x0000	R/W
0x49D	PHSIGN	Power sign register.	16	0x0000	R
0x4A8	CRC_RSLT	This register holds the CRC of the configuration registers.	16	0x0000	R
0x4A9	CRC_SPI	The register holds the 16-bit CRC of the data sent out on the MOSI/RX pin during the last SPI register read.	16	0x0000	R
0x4AC	LAST_DATA_16	This register holds the data read or written during the last 16-bit transaction on the SPI port. When using UART, this register holds the lower 16 bits of the last data read or write.	16	0x0000	R
0x4AE	LAST_CMD	This register holds the address and the read/write operation request (CMD_HDR) for the last transaction on the SPI port.	16	0x0000	R
0x4AF	CONFIG2	Configuration Register 2. This register controls the high-pass filter (HPF) corner and the user period selection.	16	0x0C00	R/W

Address	Name	Description	Length (Bits)	Reset	Access
0x4B0	EP_CFG	Energy and power accumulation configuration.	16	0x0000	R/W
0x4B1	PWR_TIME	Power update time configuration.	16	0x00FF	R/W
0x4B2	EGY_TIME	Energy accumulation update time configuration.	16	0x00FF	R/W
0x4B4	CRC_FORCE	This register forces an update of the CRC of configuration registers.	16	0x0000	W
0x4B6	TEMP_CFG	Temperature sensor configuration register.	16	0x0000	R/W
0x4B7	TEMP_RSLT	Temperature measurement result.	16	0x0000	R
0x4B9	AI_PGAGAIN	This register configures the PGA gain for Current Channel A.	16	0x0000	R/W
0x4BF	WR_LOCK	This register enables the configuration lock feature.	16	0x0000	R/W
0x4C0	MS_STATUS_IRQ	The Tier 2 status register for the autocalibration *m*Sure system related interrupts. Any bit set in this register causes the corresponding bit in the status register to be set. This register is cleared on a read and all bits are reset. If a new status bit arrives on the same clock on which the read occurs, the new status bit remains set; in this way, no status bit is missed.	16	0x0000	R
0x4C1	EVENT_STATUS	Tier 2 status register for power quality event related interrupts. See the MS_STATUS_IRQ description.	16	0x0000	R
0x4C2	CHIP_STATUS	Tier 2 status register for chip error related interrupts. See the MS_STATUS_IRQ description.	16	0x0000	R
0x4DC	UART_BAUD_SWITCH	This register switches the UART Baud rate between 4800 Baud and 115,200 Baud. Writing a value of 0x0052 sets the Baud rate to 115,200 Baud; any other value maintains a Baud rate of 4800.	16	0x0000	W
0x4FE	Version	Version of the ADE9153B IC.	16	0x0000	R
0x600	AI_WAV_1	SPI burst read accessible registers organized functionally. See AI_WAV.	32	0x00000000	R
0x601	AV_WAV_1	SPI burst read accessible registers organized functionally. See AV_WAV.	32	0x00000000	R
0x602	BI_WAV_1	SPI burst read accessible registers organized functionally. See BI_WAV.	32	0x00000000	R
0x604	AIRMS_1	SPI burst read accessible registers organized functionally. See AIRMS.	32	0x00000000	R
0x605	BIRMS_1	SPI burst read accessible registers organized functionally. See BIRMS.	32	0x00000000	R
0x606	AVRMS_1	SPI burst read accessible registers organized functionally. See AVRMS.	32	0x00000000	R
0x608	AWATT_1	SPI burst read accessible registers organized functionally. See AWATT.	32	0x00000000	R
0x60A	AFVAR_1	SPI burst read accessible registers organized functionally. See AFVAR.	32	0x00000000	R
0x60C	AVA_1	SPI burst read accessible registers organized functionally. See AVA.	32	0x00000000	R
0x60E	APF_1	SPI burst read accessible registers organized functionally. See APF.	32	0x00000000	R
0x610	AI_WAV_2	SPI burst read accessible registers organized by phase. See AI_WAV.	32	0x00000000	R
0x611	AV_WAV_2	SPI burst read accessible registers organized by phase. See AV_WAV.	32	0x00000000	R
0x612	AIRMS_2	SPI burst read accessible registers organized by phase. See AIRMS.	32	0x00000000	R
0x613	AVRMS_2	SPI burst read accessible registers organized by phase. See AVRMS.	32	0x00000000	R
0x614	AWATT_2	SPI burst read accessible registers organized by phase. See AWATT.	32	0x00000000	R
0x615	AVA_2	SPI burst read accessible registers organized by phase. See AVA.	32	0x00000000	R
0x616	AFVAR_2	SPI burst read accessible registers organized by phase. See AFVAR.	32	0x00000000	R
0x617	APF_2	SPI burst read accessible registers organized by phase. See APF.	32	0x00000000	R
0x618	BI_WAV_2	SPI burst read accessible registers organized by phase. See BI_WAV.	32	0x00000000	R
0x61A	BIRMS_2	SPI burst read accessible registers organized by phase. See BIRMS.	32	0x00000000	R

REGISTER DETAILS

Table 9. Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x020	CONFIG0	[31:10]	Reserved		Reserved.	0x0	R
		9	Reserved		Reserved.		
		8	DISRPLPF		Set this bit to disable the low-pass filter in the fundamental reactive power datapath.	0x0	R/W
		7	DISAPLPF		Set this bit to disable the low-pass filter in the total active power datapath.	0x0	R/W
		6	Reserved		Reserved.	0x0	R
		5	VNOMA_EN		Set this bit to use the nominal phase voltage rms, VNOM, in the computation of the Phase A total apparent power, AVA.	0x0	R
		4	RMS_OC_SRC		This bit selects the samples used for the RMS_OC calculation.	0x0	R
				0	x_WAV waveforms after the high-pass filter and phase compensation.		
				1	ADC samples, before the high-pass filter.		
		3	ZX_SRC_SEL		This bit selects whether data going into the zero-crossing detection circuit comes before the high-pass filter and phase compensation, or afterwards.	0x0	R
				0	After the high-pass filter and phase compensation.		
				1	Before the high-pass filter and phase compensation.		
		2	INTEN_BI		Set this bit to enable the integrator on Current Channel B.	0x0	R/W
		1	RESERVED		Reserved.	0x0	R/W
		0	HPFDIS		Set this bit to disable high-pass filters in all current and voltage channels.	0x0	R
0x023	BI_PGAGAIN	[31:0]	BI_GAIN		PGA gain for Current Channel B.	0x0	R/W
				0	Gain = 1.		
				1	Gain = 2.		
				10	Gain = 4.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x030	MS_ACAL_CFG	[31:7]	Reserved		Reserved.	0x0	R
		6	AUTOCAL_AV		Enable autocalibration on the voltage channel.	0x0	R/W
		5	AUTOCAL_BI		Enable autocalibration on Current Channel B.	0x0	R/W
		4	AUTOCAL_AI		Enable autocalibration on Current Channel A.	0x0	R/W
		3	ACALMODE_BI		Current Channel B autocalibration power mode.	0x0	R/W
				0	Normal mode.		
				1	Turbo mode.		
		2	ACALMODE_AI		Current Channel A autocalibration power mode.	0x0	R/W
				0	Normal mode.		
				1	Turbo mode.		
		1	ACAL_RUN		Runs autocalibration as configured in Bits[6:2]. The ACAL_MODE bit must also be set while running autocalibration.	0x0	R/W
		0	ACAL_MODE		This bit must be set when running auto-calibration; otherwise, autocalibration does not run. All registers, except for the auto-calibration result registers, are disabled when this bit is set.	0x0	R/W
0x240	MS_STATUS_CURRENT	[31:1]	Reserved		Reserved.	0x0	R
		0	MS_SYSRDYP		When this bit is set, the *m*Sure system is ready for a run of autocalibration.	0x0	R
0x400	IPEAK	[31:27]	Reserved		Reserved.	0x0	R
		[26:24]	IPPHASE		These bits indicate which current channels generate the IPEAKVAL value. Note that the PEAKSEL[1:0] bits in the CONFIG3 register determine on which current channel to monitor the peak value. When IPPHASE, Bit 0 is set to 1, Current Channel A generates the IPEAKVAL (Bits[23:0]) value. Similarly, IPPHASE (Bit 1) indicates that Current Channel B generates the peak value.	0x0	R
		[23:0]	IPEAKVAL		The IPEAK register stores the absolute value of the peak current. IPEAK is equal to xI_WAV/2^5.	0x0	R
0x401	VPEAK	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	VPEAKVAL		The VPEAK register stores the absolute value of the peak voltage. VPEAK is equal to AV_WAV/2^5.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x402	Status	31	CHIP_STAT		When set, this indicates a bit in the CHIP_STATUS register is set. This bit is cleared when CHIP_STATUS is read.	0x0	R
		30	EVENT_STAT		When set, this indicates a bit in the EVENT_STATUS register is set. This bit is cleared when EVENT_STATUS is read.	0x0	R
		29	MS_STAT		When set, this indicates a bit in the MS_STATUS_IRQ register is set. This bit is cleared when MS_STATUS_ IRQ is read.	0x0	R
		[28:26]	Reserved		Reserved.	0x0	R
		25	PF_RDY		This bit goes high to indicate when the power factor measurements are updated, every 1.024 sec.	0x0	R/W1
		24	CRC_CHG		This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W1
		23	CRC_DONE		This bit is set to indicate when the configuration register CRC calculation is complete, after being initiated by writing to the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W1
		22	Reserved		Reserved.	0x0	R
		21	ZXTOAV		This bit is set to indicate a zero-crossing timeout on the voltage channel; this means that a zero crossing on the voltage channel is missing.	0x0	R/W1
		20	ZXBI		This bit is set to 1 to indicate that a zero crossing is detected on Current Channel B.	0x0	R/W1
		19	ZXAI		This bit is set to 1 to indicate that a zero crossing is detected on Current Channel A.	0x0	R/W1
		18	Reserved		Reserved.	0x0	R
		17	ZXAV		This bit is set to 1 to indicate that a zero crossing is detected on Voltage Channel.	0x0	R/W1
		16	RSTDONE		This bit is set to indicate that the IC finished the power-up sequence after a reset, which means that the user can configure the IC via the SPI port or UART.	0x0	R/W1

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		15	FVARNL		This bit is set when fundamental reactive energy enters or exits the no load condition.	0x0	R/W1
		14	VANL		This bit is set when total apparent energy enters or exits the no load condition.	0x0	R/W1
		13	WATTNL		This bit is set when total active energy enters or exits the no load condition.	0x0	R/W1
		12	TEMP_RDY		This bit is set when there is a new temperature reading ready from the temperature sensor.	0x0	R/W1
		11	RMS_OC_RDY		This bit is set when the RMS_OC values update.	0x0	R/W1
		10	PWRRDY		This bit is set when the power values in the AWATT_ACC, AVA_ACC, and AFVAR_ACC registers update, after PWR_TIME 4 kSPS samples.	0x0	R/W1
		9	DREADY		This bit is set when new waveform samples are ready.	0x0	R/W1
		8	EGYRDY		This bit is set when the power values in the AWATTHR_x, AVAHR, and AFVARHR registers update, after EGY_TIME 4 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W1
		7	CF2		This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W1
		6	CF1		This bit is set when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W1
		5	REVPCF2		This bit is set to indicate if the CF2 polarity changed sign. For example, if the last CF2 pulse was positive active energy and the next CF2 pulse is negative active energy, the REVPCF2 bit is set. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R/W1
		4	REVPCF1		This bit is set to indicate if the CF1 polarity changed sign. See the REVPCF2 description.	0x0	R/W1
		3	Reserved		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	REVRPA		This bit indicates if the Phase A fundamental reactive power changed sign. This bit is updated when the power value in the AFVAR_ACC register updates, after PWR_TIME 4 kSPS samples.	0x0	R/W1
		1	Reserved		Reserved.	0x0	R
		0	REVAPA		This bit indicates if the Phase A total active power changes sign. See the REVRPA description.	0x0	R/W1
0x405	Mask	31	CHIP_STAT		Set this bit to enable an interrupt when any bit in the CHIP_STATUS register is set.	0x0	R
		30	EVENT_STAT		Set this bit to enable an interrupt when any bit in the EVENT_STATUS register is set.	0x0	R/W
		29	MS_STAT		Set this bit to enable an interrupt when any bit in the MSURE_STATUS_IRQ register is set.	0x0	R/W
		[28:26]	Reserved		Reserved.	0x0	R
		25	PF_RDY		Set this bit to enable an interrupt when the power factor measurements update, every 1.024 sec.	0x0	R/W
		24	CRC_CHG		Set this bit to enable an interrupt if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		23	CRC_DONE		Set this bit to enable an interrupt when the configuration register CRC calculation is complete, after being initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		22	Reserved		Reserved.	0x0	R
		21	ZXTOAV		Set this bit to enable an interrupt when there is a zero-crossing timeout on the voltage channel; this means that a zero crossing on the voltage channel is missing.	0x0	R/W
		20	ZXBI		Set this bit to enable an interrupt when a zero crossing is detected on Current Channel B.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		19	ZXAI		Set this bit to enable an interrupt when a zero crossing is detected on Current Channel A.	0x0	R/W
		18	Reserved		Reserved.	0x0	R
		17	ZXAV		Set this bit to enable an interrupt when a zero crossing is detected on the voltage channel.	0x0	R/W
		16	Reserved		Reserved.	0x0	R
		15	FVARNL		Set this bit to enable an interrupt when fundamental reactive energy enters or exits the no load condition.	0x0	R/W
		14	VANL		Set this bit to enable an interrupt when total apparent energy enters or exits the no load condition.	0x0	R/W
		13	WATTNL		Set this bit to enable an interrupt when the total active energy enters or exits the no load condition.	0x0	R/W
		12	TEMP_RDY		Set this bit to enable an interrupt when there is a new temperature reading ready from the temperature sensor.	0x0	R/W
		11	RMS_OC_RDY		Set this bit to enable an interrupt when the RMS_OC values update.	0x0	R/W
		10	PWRRDY		Set this bit to enable an interrupt when the power value in the AWATT_ACC, AVA_ACC, and AFVAR_ACC registers update after PWR_TIME 4 kSPS samples.	0x0	R/W
		9	DREADY		Set this bit to enable an interrupt when new waveform samples are ready.	0x0	R/W
		8	EGYRDY		Set this bit to enable an interrupt when the power values in the AWATTHR, AVAHR, and AFVARHR registers update, after EGY_TIME 4 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
		7	CF2		Set this bit to enable and interrupt when the CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		6	CF1		Set this bit to enable and interrupt when the CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		5	REVPCF2		Set this bit to enabled an interrupt when the CF2 polarity changed sign.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	REVPCF1		Set this bit to enabled an interrupt when the CF1 polarity changed sign.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	REVRPA		Set this bit to enable an interrupt when the Phase A fundamental reactive power has changed sign.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	REVAPA		Set this bit to enable an interrupt when the Phase A total active power changes sign.	0x0	R/W
0x409	OI_LVL	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	OILVL_VAL		Overcurrent detection threshold level.	0xFFFFFF	R/W
0x40A	OIA	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	OIA_VAL		Current Channel A overcurrent RMS_OC value. If this phase is enabled with the OIA_EN bit set in the CONFIG3 register and AIRMS_OC is greater than the OILVL threshold, this value updates.	0x0	R
0x40B	OIB	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	OIB_VAL		Current Channel B overcurrent RMS_OC value. If this phase is enabled with the OIB_EN bit set in the CONFIG3 register and BIRMS_OC is greater than the OILVL threshold, this value updates.	0x0	R
0x40F	VLEVEL	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	VLEVEL_VAL		This register is used in the algorithm that computes the fundamental reactive power.	0x45D450	R/W
0x411	DIPA	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	DIPA_VAL		Voltage channel RMS_OC value during a dip condition.	0x7FFFFF	R
0x415	SWELLA	[31:24]	Reserved		Reserved.	0x0	R
		[23:0]	SWELLA_VAL		Voltage channel RMS_OC value during a swell condition.	0x0	R
0x41F	PHNOLOAD	[31:3]	Reserved		Reserved.	0x0	R
		2	AFVARNL		This bit is set if the Phase A fundamental reactive energy is in no load.	0x0	R/W
		1	AVANL		This bit is set if the Phase A total apparent energy is in no load.	0x0	R/W
		0	AWATTNL		This bit is set if the Phase A total active energy is in no load.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x425	CF_LCFG	[31:21]	Reserved		Reserved.	0x0	R
		20	CF2_LT		If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set as 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		19	CF1_LT		If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. See the CF2_LT description.	0x0	R/W
		[18:0]	CF_LTMR		If the CFx_LT bit in the CF_LCFG register is set, this value determines the active low pulse width of the CFx pulse.	0x0	R/W
0x471	TEMP_TRIM	[31:16]	TEMP_OFFSET		Offset of temperature sensor, calculated during the manufacturing process.	0x0	R
		[15:0]	TEMP_GAIN		Gain of temperature sensor, calculated during the manufacturing process.	0x0	R
0x481	CONFIG1	15	EXT_REF		Set this bit if using an external voltage reference.	0x0	R/W
		14	DIP_SWELL_IRQ_MODE		This bit sets the interrupt mode for dip/swell.	0x0	R/W
				0	Receive continuous interrupts after every DIP_CYC/SWELL_CYC cycles.		
				1	Receive one interrupt when entering dip/swell condition and another interrupt when exiting dip/swell condition.		
		[13:12]	Reserved		Reserved.	0x0	R
		11	BURST_EN		Set this bit to enable burst read functionality on the registers. Note that this bit disables the CRC being appended to SPI register reads.	0x0	R/W
		10	Reserved		Reserved.	0x0	R
		[9:8]	PWR_SETTLE		These bits configure the time for the power and filter-based rms measurements to settle before starting the power, energy, and CF accumulations.	0x3	R/W
				0	64 ms.		
				1	128 ms.		
				10	256 ms.		
				11	0 ms.		
		[7:6]	Reserved		Reserved.	0x0	R
		5	CF_ACC_CLR		Set this bit to clear the accumulation in the digital to frequency converter and the CFDEN counter. This bit automatically clears itself.	0x0	W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:3]	Reserved		Reserved.	0x0	R
		2	ZX_OUT_OE		When this bit is set, ZX is driven to the CF2 pin.	0x0	R/W
		1	DREADY_OE		When this bit is set, DREADY is driven to the CF2 pin.	0x0	R/W
		0	SWRST		Set this bit to initiate a software reset. This bit is self clearing.	0x0	W1
0x490	CFMODE	[15:8]	Reserved		Reserved.	0x0	R
		7	CF2DIS		CF2 output disable. Set this bit to disable the CF2 output and bring the pin high. Note that when this bit is set, the CFx bit in the status register is not set when a CF pulse is accumulated in the digital to frequency converter.	0x0	R/W
		6	CF1DIS		CF1 output disable. See the CF2DIS description.	0x0	R/W
		[5:3]	CF2SEL		Type of energy output on the CF2 pin.	0x0	R/W
				0	Total active power.		
				10	Total apparent power.		
				100	Fundamental reactive power.		
		[2:0]	CF1SEL		Selects type of energy output on the CF1 pin. See the CF2SEL description.	0x0	R/W
0x492	ACCMODE	[15:5]	Reserved		Reserved.	0x0	R
		4	SELFREQ		System frequency select bit.	0x0	R/W
				0	50 Hz system.		
				1	60 Hz system.		
		[3:2]	VARACC		Fundamental reactive power accumulation mode for energy registers and CFx pulses.	0x0	R/W
				0	Signed accumulation mode.		
				1	Absolute value accumulation mode.		
				10	Positive accumulation mode.		
				11	Negative accumulation mode.		
		[1:0]	WATTACC		Total active power accumulation mode for energy registers and CFx pulses. See the VARACC description.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x493	CONFIG3	[15:4]	Reserved		Reserved.	0x0	R
		[3:2]	PEAK_SEL		Peak detection phase selection.	0x0	R/W
				0	Phase A and Phase B disabled from voltage and current peak detection.		
				1	Phase A Voltage and current peak detection enabled, Phase B current peak detection disabled.		
				10	Phase A voltage and current peak detection disabled, Phase B current peak detection enabled.		
				11	Phase A and Phase B enabled for voltage and current peak detection.		
		1	OIB_EN		Overcurrent detection enable for Current Channel B.	0x0	R/W
		0	OIA_EN		Overcurrent detection enable for Current Channel A.	0x0	R/W
0x49A	ZX_CFG	[15:1]	Reserved		Reserved.	0x0	R
		0	DISZXLPF		Zero-crossing low-pass filter disable.	0x0	R/W
0x49D	PHSIGN	[15:8]	Reserved		Reserved.	0x0	R
		7	CF2SIGN		Sign of the power in the CF2 datapath. The CF2 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		6	CF1SIGN		Sign of the power in the CF1 datapath. See the CF2SIGN description.	0x0	R
		[5:2]	Reserved		Reserved.	0x0	R
		1	AVARSIGN		Phase A fundamental reactive power sign bit. The fundamental reactive power is positive if this bit is clear and negative if this bit is set.	0x0	R
		0	AWSIGN		Phase A active power sign bit. The active power is positive if this bit is clear and negative if this bit is set.	0x0	R

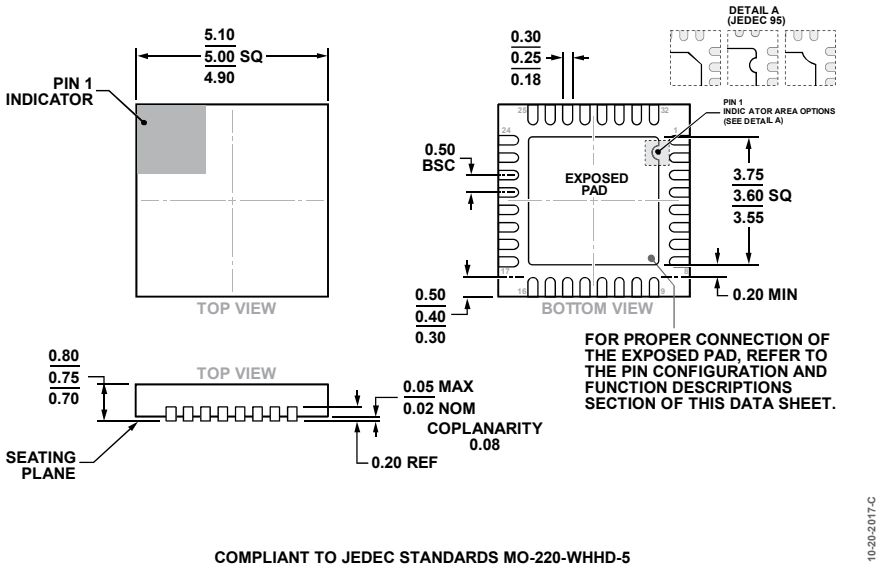
Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x4AF	CONFIG2	[15:13]	Reserved		Reserved.	0x0	R
		12	UPERIOD_SEL		Set this bit to use a user configured line period, in USER_PERIOD, for RMS_OC calculation. If this bit is clear, the voltage line period is used.	0x0	R/W
		[11:9]	HPF_CRN		High-pass filter corner ($f_{3\ dB}$) enabled when the HPFDIS bit in the CONFIG0 register is equal to zero.	0x6	R/W
				0	38.695 Hz.		
				1	19.6375 Hz.		
				10	9.895 Hz.		
				11	4.9675 Hz.		
				100	2.49 Hz.		
				101	1.2475 Hz.		
				110	0.625 Hz.		
				111	0.3125 Hz.		
		[8:0]	Reserved		Reserved.	0x0	R
0x4B0	EP_CFG	[15:8]	Reserved		Reserved.	0x0	R
		[7:5]	NOLOAD_TMR		This register configures how many 4 kSPS samples over which to evaluate the no load condition.	0x0	R/W
				0	64 samples.		
				1	128 samples.		
				10	256 samples.		
				11	512 samples.		
				100	1024 samples.		
				101	2048 samples.		
				110	4096 samples.		
				111	Disable no load threshold.		
		4	Reserved		Reserved.	0x0	R
		3	RD_RST_EN		Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the AWATTHR_x, AFVARHR, or AVAHR registers are read, it is reset and begins accumulating energy from zero.	0x0	R/W
		2	EGY_LD_ACCUM		If this bit is equal to zero, the internal energy register is added to the user accessible energy register. If this bit is set, the internal energy register overwrites the user accessible energy register when the EGYRDY event occurs.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	EGY_TMR_MODE		This bit determines whether energy is accumulated based on the number of 4 kSPS samples or zero-crossing events configured in the EGY_TIME register.	0x0	R/W
				0	Accumulate energy based on 4 kSPS samples.		
				1	Accumulate energy based on the zero-crossing events.		
		0	EGY_PWR_EN		Set this bit to enable the energy and power accumulator when the run bit is also set.	0x0	R/W
0x4B4	CRC_FORCE	[15:1]	Reserved		Reserved.	0x0	R
		0	FORCE_CRC_UPDATE		Write this bit to force the configuration register CRC calculation to start. When the calculation is complete, the CRC_DONE bit is set in the status register.	0x0	W1
0x4B6	TEMP_CFG	[15:4]	Reserved		Reserved.	0x0	R
		3	TEMP_START		Set this bit to manually request a new temperature sensor reading. The new temperature reading is available in 1 ms, indicated by the TEMP_RDY bit in the status register. Note that this bit is self clearing.	0x0	W1
		2	TEMP_EN		Set this bit to enable the temperature sensor.	0x0	R/W
		[1:0]	TEMP_TIME		These bits select the number of temperature readings to average.	0x0	R/W
				0	1 sample. New temperature measurement every 1ms.		
				1	256 samples. New temperature measurement every 256 ms.		
				10	512 samples. New temperature measurement every 512 ms.		
				11	1024 samples. New temperature measurement every 1 sec.		
0x4B7	TEMP_RSLT	[15:12]	Reserved		Reserved.	0x0	R
		[11:0]	TEMP_RESULT		12-bit temperature sensor result	0x0	R
0x4B9	AI_PGAGAIN	[15:5]	Reserved		Reserved.	0x0	R
		4	AI_SWAP		This bit sets the signal side of the PGA, meaning that the IAP and IAN pins can be swapped by setting this bit. This bit must be set to 1 for proper operation, only set to 0 if sensor is connected in reverse.	0x0	R/W
				0	Signal on IAN.		
				1	Signal on IAP.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	Reserved		Reserved.	0x0	R
		[2:0]	AI_GAIN		PGA gain for Current Channel A.	0x0	R/W
				10	Gain = 16.		
				11	Gain = 24.		
				100	Gain = 32.		
				101	Gain = 38.4.		
0x4C0	MS_STATUS_IRQ	15	Reserved		Reserved.	0x0	R
		14	MS_SYSRDY		This bit is set when a new run of *m*Sure is ready to be enabled after a run of *m*Sure is disabled. A new run is ready less than 1 sec after disabling the previous run.	0x0	R
		13	MS_CONFERR		This bit is set if there is an invalid configuration of *m*Sure autocalibration. Fix the configuration error and try it running again.	0x0	R
		12	MS_ABSENT		When this bit is set, *m*Sure is not detected on the channel that was last enabled.	0x0	R
		11	Reserved		Reserved.	0x0	R
		10	Reserved		Reserved.	0x0	R
		9	Reserved		Reserved.	0x0	R
		8	Reserved		Reserved.	0x0	R
		7	Reserved		Reserved.	0x0	R
		6	Reserved		Reserved.	0x0	R
		5	Reserved		Reserved.	0x0	R
		4	Reserved		Reserved.	0x0	R
		3	MS_TIMEOUT		This bit is set when *m*Sure times out after 600 sec.	0x0	R
		2	Reserved		Reserved.	0x0	R
		1	MS_READY		This bit is set when the *m*Sure result registers first start to be populated (after the 8 sec block). Then, this bit is set every second for when the value is updated until *m*Sure is stopped.	0x0	R
		0	MS_SHIFT		This bit is set when there is a shift in the *m*Sure CC value in the middle of a run, meaning that the value found for the xCC shifted and another run of *m*Sure with the same settings must be performed to verify the shift.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x4C1	EVENT_STATUS	[15:6]	Reserved		Reserved.	0x0	R
		5	OIB		This bit is set when Current Channel B is in an overcurrent condition and is zero when it is not in an overcurrent condition.	0x0	R
		4	OIA		This bit is set when Current Channel A is in an overcurrent condition and is zero when it is not in an overcurrent condition.	0x0	R
		3	Reserved		Reserved.	0x0	R
		2	SWELLA		This bit is set when the voltage channel is in a swell condition and is zero when it is not in a swell condition.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DIPA		This bit is set when the voltage channel is in the dip condition and is zero when it is not in a dip condition.	0x0	R
0x4C2	CHIP_STATUS	[15:8]	Reserved		Reserved.	0x0	R
		7	UART_RESET		When this bit is set, a UART interface reset is detected.	0x0	R
		6	UART_ERROR2		Reset the UART interface to clear this error.	0x0	R
		5	UART_ERROR1		Reset the UART interface to clear this error.	0x0	R
		4	UART_ERROR0		Reset the UART interface to clear this error.	0x0	R
		3	ERROR3		Issue a software reset or hardware reset to clear this error.	0x0	R
		2	ERROR2		Issue a software reset or hardware reset to clear this error.	0x0	R
		1	ERROR1		Issue a software reset or hardware reset to clear this error.	0x0	R
		0	ERROR0		Issue a software reset or hardware reset to clear this error.	0x0	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 61. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE9153AACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADE9153AACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], 13″Tape and Reel	CP-32-12
EV-ADE9153ASHIELDZ		Arduino Shield Evaluation Board	

[1] Z = RoHS Compliant Part.

D16519-0-2/18(0)

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