Data Sheet

ADE9103/ADE9112/ADE9113

Isolated, Sigma-Delta ADCs with SPI

FEATURES

- 2 (ADE9112) or 3 (ADE9113) channel isolated, simultaneously sampling Σ-Δ ADCs, with integrated *iso*Power, isolated dc-to-dc converters
- 3 (ADE9103) channel nonisolated, simultaneously sampling Σ-Δ ADCs
- Synchronization of multiple ADE9103/ADE9112/ADE9113 devices
- 4-wire SPI with bidirectional CRC and daisy-chain functionality
- Unique SPI readable part ID registers
- Up to 4 ADE9103/ADE9112/ADE9113 devices clocked from a single crystal or an external clock
- $\overline{\text{IRQ}}$ hardware pin and registers for fault detection and robustness
- Sample rate up to 32 kSPS
- SNR up to 95 dB
- ±31.25 mV peak analog input voltage range for current channel
- ±500 mV peak single-ended analog input voltage range for voltage channels
- Internal voltage reference temperature coefficient: <13 ppm/°C typical
- ADC offset drift: <2 nV/°C typical
- Ideal for both AC and DC measurement systems
- Single 3.3 V supply for isolated and nonisolated measurements
- Compact 28-lead, wide-body with finer pitch SOIC package with 8.3 mm creepage
- Temperature range: −40°C to +125°C
- Passes CISPR 32 Class B RF Emissions
- ADE9112 and ADE9113 safety and regulatory approvals
  - IEC 60747-17 certificate of conformity expected
  - 5000 V RMS for 1 minute per UL 1577
  - IEC 61010-1 and IEC 62368-1

APPLICATIONS

- Shunt-based polyphase meters
- Electric vehicle supply equipment
- DC meters
- Power quality monitoring
- Solar inverters
- Process monitoring
- Protective devices
- Isolated sensor interfaces

GENERAL DESCRIPTION

The ADE9103/ADE9112/ADE9113 are precision simultaneously sampling Σ-Δ analog-to-digital converters (ADCs) for both DC and polyphase shunt-based energy metering applications. The ADE9113[1] integrates safety certified signal and power galvanic isolation with three simultaneously sampling fully differential 24-bit Σ-Δ ADC channels. The ADE9112 features two fully differential Σ-Δ ADC channels for isolated applications where only a single voltage channel is required. The ADE9103 is a nonisolated, 3-channel Σ-Δ ADC for use in applications where isolation is not required, such as for neutral measurement. The ADE9103/ADE9112/ADE9113 all include a high-gain, current channel well suited for use with a shunt resistor as the current sensor. Multiple ADE9103/ADE9112/ADE9113 devices can be synchronized to sample simultaneously and provide coherent outputs.

The current channel ADC provides an 86 dBFS signal-to-noise ratio (SNR), at a sample rate of 4 kSPS, over a 1.65 kHz signal bandwidth and a typical gain drift of 13 ppm/°C, which enables down to Class 0.2 accuracy. The voltage ADCs provide an SNR of 91 dBFS over the same sample rate and bandwidth. The high gain on the current channel (IP and IM) aids the use of lower resistance shunts for reduced losses due to heat. The low offset drift of 2 nV/°C offers the performance required for DC metering.

The ADE9103/ADE9112/ADE9113 delivers system cost savings and increased robustness. The main ADE9103/ADE9112/ADE9113 can drive clocks of up to three additional ADE9103/ADE9112/ADE9113 with a single crystal. The bidirectional, serial port interface (SPI) supports a daisy-chain capability, allowing access to all registers while reducing the required microcontroller pin count. The 28-lead SOIC_W_FP allows more compact layouts. Valid data transfers are ensured with bidirectional, cyclic redundancy check (CRC) and $\overline{\text{IRQ}}$ pin alerts the system of critical faults. The ADE9112 and ADE9113 pass CISPR 32 Class B emissions on a 2-layer printed circuit board (PCB) with the addition of a high voltage capacitor and on a 4-layer PCB with an internal stitching capacitor.

Table 1. ADE9103/ADE9112/ADE9113 Product Comparison

Model	24-Bit Current Measurement Channel	24-Bit Voltage Measurement Channel	Integrated Safety Isolation
ADE9103	Yes	2	No
ADE9112	Yes	1	Yes
ADE9113	Yes	2	Yes

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; 7,558,080; 8,892,933; and 11,533,027. Other patents are pending.

Rev. A

TABLE OF CONTENTS

REVISION HISTORY

4/2025—Rev. 0 to Rev. A

Changes to Features Section ... 1
Added Note 1, Table 1 ... 6
Changes to Internal Capacitance on XTALIN and XTALOUT to DGND, C_{IN1}, C_{IN2} Parameter, Table 1 ... 6
Added Note 1, Table 3 ... 10
Changes to Figure 5 Caption ... 10
Changes to Table 4 ... 11
Changes to Table 5 ... 12
Changes to Table 6 and Table 7 ... 13
Changes to Table 11 ... 14
Changes to Table 12 ... 16
Changes to Figure 27 ... 21
Changes to ADC Transfer Function Section ... 25
Changes to CRC of Configuration Registers Section ... 27
Added Zero Crossing Section ... 27
Changes to Interrupts Section ... 27
Changes to Figure 37 ... 29
Changed Clock Section to Crystal Oscillator/External Clock Section ... 32
Changes to Crystal Oscillator/External Clock Section ... 32
Added Crystal Selection Section ... 33
Added Load Capacitor Calculation Section ... 33

TABLE OF CONTENTS

11/2023—Revision 0: Initial Version

TYPICAL APPLICATIONS CIRCUIT

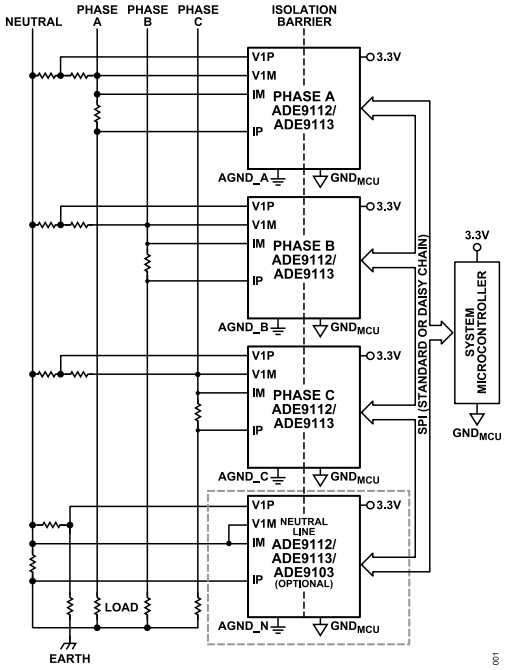

Figure 1. Typical Applications Circuit with isolation between Phase A, Phase B, Phase C and MCU Domains

FUNCTIONAL BLOCK DIAGRAMS

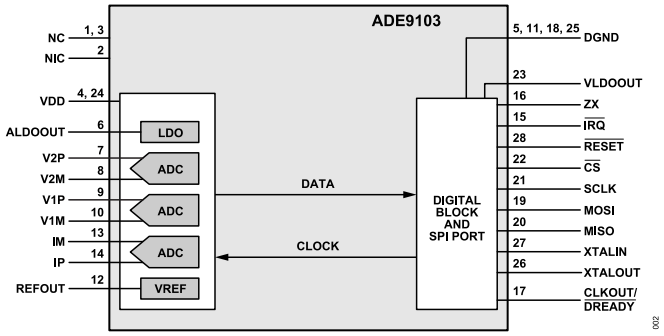

Figure 2. ADE9103 Functional Block Diagram

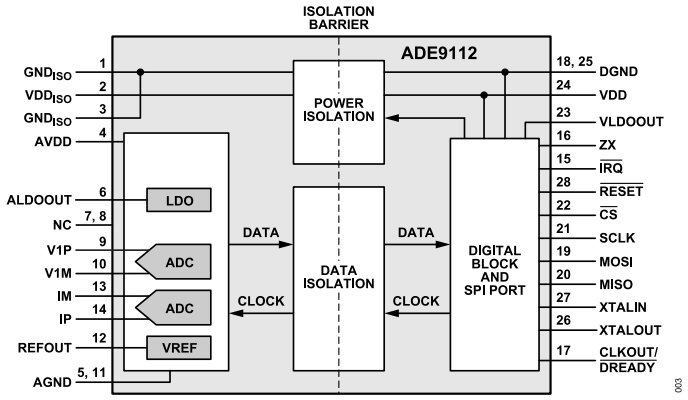

Figure 3. ADE9112 Functional Block Diagram

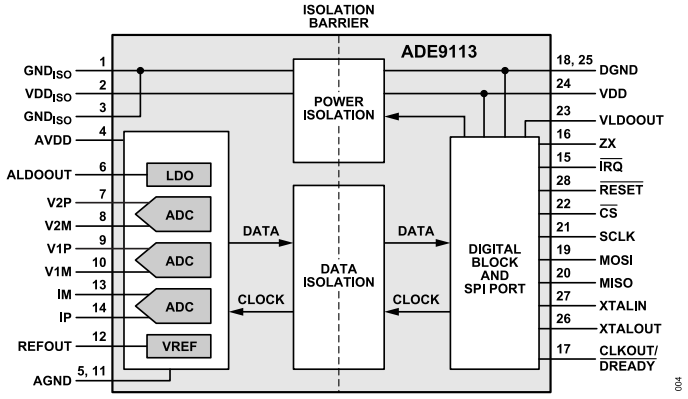

Figure 4. ADE9113 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = 0 V, DGND = 0 V, on-chip reference, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +125°C, and T_A = 25°C (typical), unless otherwise noted.

Table 2. Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
ADE9112/ADE9113					
Normal Operation		8	13	mA	
Hold Reset Operation		9.5	12.5	µA	$\overline{\text{RESET}}$ pin held low
ADE9103					
Normal Operation		3.4	4.1	mA	
Hold Reset Operation		1.0	1.3	mA	$\overline{\text{RESET}}$ pin held low
VDD_{ISO} Pin for ADE9112/ADE9113 Only		2.05		V	Referenced to the GND_{ISO} pin
INTERNAL VOLTAGE REFERENCE					
Voltage Reference (VREF)		1.25		V	REFOUT pin
Temperature Coefficient					T_A = −40°C to +125°C
ADE9112/ADE9113		12	23	ppm/°C	
ADE9103		13	28	ppm/°C	
LOW DROPOUT (LDO) REGULATOR					Generated internally, and external decoupling only
Analog LDO		1.8		V	±5%, ALDOOUT pin
Digital LDO		1.8		V	±5%, VLDOOUT pin
ZERO-CROSSING OUTPUT					
Latency		80		µs	
Jitter		30		µs	
TEMPERATURE RANGE					
Specified Performance	−40		+125	°C	
ANALOG INPUTS					
Differential Voltage Range					
IP and IM Pins	−31.25		+31.25	mV	
Differential Voltage Range					
V1P and V1M Pins	−1000		+1000	mV	
V2P and V2M Pins	−1000		+1000	mV	
Single-Ended Voltage Range[1]					
V1P and V1M Pins	−500		+500	mV	
V2P and V2M Pins	−500		+500	mV	
Maximum Voltage[1] with Reference to DGND[2] or AGND[3]					
IP and IM Pins	−40.625		+40.625	mV	
V1P, V2P, V1M, and V2M Pins	−600		+600	mV	
Crosstalk[4]					Aggressor channels at full scale. See Crosstalk section
V1 and V2 to I		−125		dB	
V1 and I to V2		−125		dB	
V2 and I to V1		−125		dB	
Differential Input Impedance (DC)					
IP and IM	2700	3900		kΩ	
V1P, V1M, V2P, and V2M	300	370		kΩ	
ADC Offset					See ADC Offset section
IP and IM		0.3	±10	µV	
V1P, V1M, V2P, and V2M		−43	±160	µV	
ADC Offset Drift					See ADC Offset Drift over Temperature section
IP and IM		2	41	nV/°C	

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V1P and V1M					
ADE9112/ADE9113		87	212	nV/°C	
ADE9103		100	268	nV/°C	
V2P and V2M					
ADE9112/ADE9113		115	245	nV/°C	
ADE9103		121	290	nV/°C	
Gain Error					
All Channels		±0.1	±0.5	%	Not including anti-aliasing filter
Gain Drift (Gain Amplifier, ADC, and Internal Voltage Reference)					See Gain Drift over Temperature section
IP, −40°C to +125°C					
ADE9112/ADE9113		12	24	ppm/°C	
ADE9103		15	31	ppm/°C	
V1P and V2P, −40°C to +125°C					
ADE9112/ADE9113		13	24	ppm/°C	
ADE9103		15	30	ppm/°C	
POWER SUPPLY REJECTION (PSR)/COMMON-MODE REJECTION RATIO (CMRR)					See the Power Supply Rejection (PSR) section
AC PSR					VDD = 3.3 V + 120 mV RMS (100 Hz), IP = V1P = V2P = AGND
IP and IM		−120		dB	
V1P, V1M, V2P, and V2M		−105		dB	
DC PSR					VDD = 3.3 V ± 330 mV DC, IP = 3.125 mV peak, V1P = V2P = 100 mV peak
IP and IM		−120		dB	
V1P, V1M, V2P, and V2M		−105		dB	
AC CMRR					At 50 Hz and 60 Hz
IP and IM		−114		dB	
V1P, V1M, V2P, and V2M		−111		dB	
Pass-Band Flatness (−0.1 dB)					
32 kSPS Output		1.5		kHz	
		2.86		kHz	Compensation enabled, LPF_BW = 0
		2.43		kHz	Compensation enabled, LPF_BW = 1
8 kSPS Output		1.5		kHz	
		2.87		kHz	Compensation enabled, LPF_BW = 0
		2.44		kHz	Compensation enabled, LPF_BW = 1
4 kSPS Output		0.77		kHz	
2 kSPS Output		0.38		kHz	
1 kSPS Output		0.20		kHz	
Output Bandwidth (−3 dB)[1]					DATAPATH_CONFIG = 000 has no LPF and, therefore, bandwidth is not specified
32 kSPS and 8 kSPS		3.3		kHz	LPF_BW = 0
		2.7		kHz	LPF_BW = 1
4 kSPS		1.65		kHz	LPF_BW = 0
		1.35		kHz	LPF_BW = 1
2 kSPS		0.825		kHz	LPF_BW = 0
		0.675		kHz	LPF_BW = 1
1 kSPS		0.413		kHz	LPF_BW = 0
		0.338		kHz	LPF_BW = 1

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT CHANNEL					
Signal-to-Noise Ratio (SNR)					At full-scale input, and see the Signal-to-Noise Ratio (SNR) section
All 32 kSPS and 8 kSPS Outputs		83		dBFS	
4 kSPS Output		86		dBFS	
2 kSPS Output		89		dBFS	
1 kSPS Output		91		dBFS	
Signal-to-Noise-and-Distortion Ratio (SINAD)					At full-scale input, and see the Signal-to-Noise-and-Distortion (SINAD) Ratio section
All 32 kSPS and 8 kSPS Outputs		83		dBFS	
4 kSPS Output		86		dBFS	
2 kSPS Output		89		dBFS	
1 kSPS Output		90		dBFS	
Total Harmonic Distortion (THD)					At full-scale input, and see the Total Harmonic Distortion (THD) section
All Outputs		−96		dBFS	
Spurious-Free Dynamic Range (SFDR)					At full-scale input, and see the Spurious-Free Dynamic Range (SFDR) section
All Outputs		−96		dBFS	
VOLTAGE CHANNEL					
Signal-to-Noise Ratio (SNR)					At full-scale input, and see the Signal-to-Noise Ratio (SNR) section
All 32 kSPS and 8 kSPS Outputs		91		dBFS	
4 kSPS Output		93		dBFS	
2 kSPS Output		94		dBFS	
1 kSPS Output		95		dBFS	
Signal-to-Noise-and-Distortion Ratio (SINAD)					At full-scale input, and see the Signal-to-Noise-and-Distortion (SINAD) Ratio section
All 32 kSPS and 8 kSPS Outputs		88		dBFS	
4 kSPS Output		90		dBFS	
2 kSPS Output		91		dBFS	
1 kSPS Output		91		dBFS	
Total Harmonic Distortion (THD)					At full-scale input, and see the Total Harmonic Distortion (THD) section
±0.5 V_{PEAK} Differential		−101		dBFS	
±1.0 V_{PEAK} Differential		−92		dBFS	
Spurious-Free Dynamic Range (SFDR)					At full-scale input, and see the Spurious-Free Dynamic Range (SFDR) section
±0.5 V_{PEAK} Differential		100		dBFS	
±1.0 V_{PEAK} Differential		94		dBFS	
XTALIN					
Input Clock Frequency, XTALIN	15.84	16.384	16.547	MHz	
XTALIN Duty Cycle	45		55	%	
Using XTALOUT to Other Devices	47.5		52.5	%	
XTALIN Logic Inputs					
Input High Voltage, VINH	1.2			V	
Input Low Voltage, VINL			0.5	V	
Internal Capacitance on XTALIN and XTALOUT to DGND, C_{IN1}, C_{IN2}		4		pF	

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Internal Feedback Resistance Between XTALIN and XTALOUT		2.7		MΩ	
Transconductance (g_m)	6	10		mA/V	
CLKOUT Delay			15	ns	
LOGIC INPUTS—MOSI, SCLK, and $\overline{CS}$					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			8.5	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—CLKOUT/$\overline{DREADY}$ AND MISO					
Output High Voltage, V_{OH}	2.4			V	Source current (I_{SOURCE}) = 3.5 mA
Output Low Voltage, V_{OL}			0.4	V	Sink current (I_{SINK}) = 3.5 mA

[1] Guaranteed by design and not subject to production test.

[2] For the ADE9103 only.

[3] For the ADE9112/ADE9113 only.

[4] V1 refers to V1 voltage channel (V1P and V1M pins), V2 refers to V2 voltage channel (V2P and V2M pins), and I refers to current channel (IP and IM pins).

SPECIFICATIONS

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = 0 V, DGND = 0 V, on-chip reference, XTALIN = 16.384 MHz, and T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 3. SPI Interface Timing Parameters

Parameter[1]	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	10		ns
SCLK Frequency	f_{SCLK}	40	20,000	kHz
SCLK Low Pulse Width	t_{SL}	20		ns
SCLK High Pulse Width	t_{SH}	20		ns
Data Output Valid After $\overline{CS}$ Edge	t_{DAVFB}		20	ns
Subsequent Data Output Valid After SCLK Edge	t_{DAVSB}		20	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10		ns
Data Output Fall Time	t_{DF}		10	ns
Data Output Rise Time	t_{DR}		10	ns
SCLK Rise Time	t_{SR}		5	ns
SCLK Fall Time	t_{SF}		5	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}		20	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}		10	ns
$\overline{CS}$ High Time Between SPI Transactions	t_{CH}			
Nonisolated (NONISO) Side		400		ns
Isolated (ISO) Side		10,000		ns

[1] Specifications guaranteed by design and characterization and not subject to production test.

Timing Diagrams

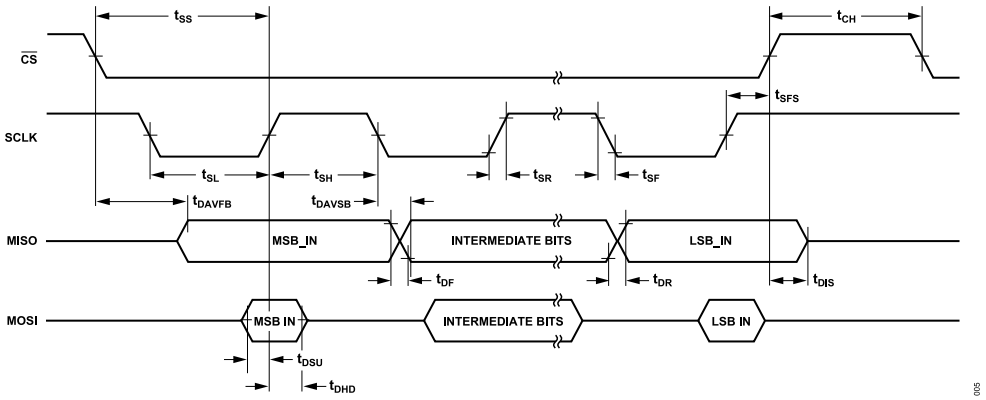

Figure 5. SPI Timing, CPOL = 1 and CHPA = 1

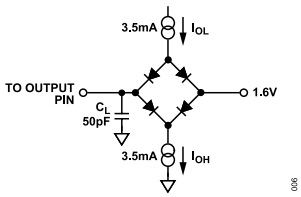

Figure 6. Load Circuit for Timing Specifications

SPECIFICATIONS

INSULATION CHARACTERISTICS

The ADE9112 and ADE9113 are suitable for reinforced electrical insulation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 4. ADE9112 and ADE9113 Isolation Characteristics

Parameter	Symbol	Conditions	Value	Unit
CLASSIFICATIONS				
Overvoltage Category per IEC 60664-1		For Rated Mains Voltage ≤ 150 V_{RMS}	I to IV	
		For Rated Mains Voltage ≤ 300 V_{RMS}	I to IV	
		For Rated Mains Voltage ≤ V_{IOWM}	I to III	
Climatic Classification			40/125/21	
Pollution Degree		Per DIN VDE 0110, Table 1	2	
IEC 60747-17 HIGH VOLTAGE RATINGS				
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage	405	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}	Repetitive peak voltage	573	V_{PEAK}
Maximum Transient Isolation Voltage	V_{IOTM}	Nonrepetitive transient voltages	7071	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{ISO}	Maximum isolation withstanding AC RMS voltage for one minute	5000	V_{RMS}
Maximum Surge Isolation Voltage, Reinforced	V_{IOSM}	Tested in oil, 1.2 µs/50 µs waveform per IEC 61000-4-5, V_{TEST} = 1.3 × V_{IOSM} = 10,400 V_{PEAK}	8000	V_{PEAK}
Maximum Impulse Voltage	V_{IMP}	Tested in air, 1.2 µs/50 µs waveform per IEC 61000-4-5	7071	V_{PEAK}
Input to Output Test Voltage	V_{PR}		1125	V_{PEAK}
Apparent Charge	q_{pd}	Test method B1, V_{PR} = 1.875 × V_{IORM}, t = 1 sec	5	pC
PACKAGE CHARACTERISITICS				
External Clearance	CLR	Measured from input terminals to output terminals, shortest distance through air	8.3	mm
External Creepage	CPG	Measured from input terminals to output terminals, shortest distance along body	8.3	mm
Internal Clearance	DTI	Distance through thin film insulation	21.5	µm
Comparative Tracking Index	CTI		>400	V
Material Group			II	
Resistance (Input to Output)[1]	R_{IO}	V_{IO} = 500 V, T_A = 25°C	10^{12}	Ω
	R_{IO_S}	V_{IO} = 500 V, T_A = T_S	10^9	Ω
Capacitance (Input to Output)[1]	C_{IO}	f_{TEST} = 1 MHz	1.3	pF
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S		150	°C
Maximum Input Power Dissipation	P_S	Total Power Dissipation at 25°C	1.90	W

[1] Device is measured as a 2-terminal device.

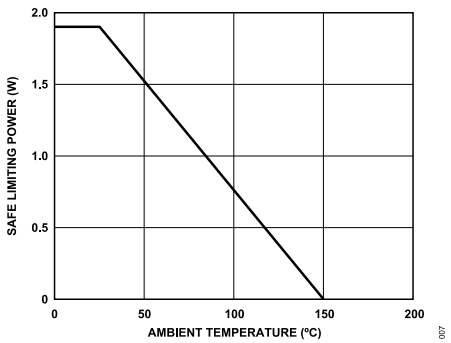

Figure 7. Thermal Derating Curve, Dependence of Safety Limiting Values, per IEC 60747-17

SPECIFICATIONS

REGULATORY APPROVALS

The ADE9112 and ADE9113 are approved by the organizations listed in Table 5. Certifications available on the Safety and Regulatory Certification for Digital Isolation web page.

Refer to Table 5 for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5. ADE9112 and ADE9113 Regulatory Approvals

Regulatory Agency	Standard Certification/Approval	File
VDE	Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10 and EN IEC 60747-17:2020+AC:2021 Reinforced insulation, see Table 4 for characteristics	(Pending)
UL	Recognized under the UL1577 Component Recognition Program Single protection, 5000 V RMS isolation voltage	E214100
TUV Sud	EN IEC 62368-1:2020/A11:2020 Basic insulation at 830 V RMS Reinforced insulation at 415 V RMS	B 056232 0034
	EN 61010-1:2020/A1:2019 Basic insulation at 600 V RMS mains Reinforced insulation at 300 V RMS mains	B 056232 0035

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6. ADE9103 Absolute Maximum Ratings

Parameter	Rating
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage	
IP and IM to DGND	−1.4 V to +1.4 V
V1P and V1M, to DGND	−2.0 V to +2.0 V
V2P and V2M to DGND	−1 V to +1 V
Digital Input Voltage	
MOSI, SCLK, $\overline{CS}$, $\overline{RESET}$, and XTALIN to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage	
$\overline{IRQ}$, ZX, CLKOUT, MISO, SCLK, and XTALOUT to DGND	−0.3 V to VDD + 0.3 V
Temperature	
Operating	−40°C to +125°C
Storage Range	−65°C to +150°C
Lead (Soldering, 10 sec)[1]	260°C
Moisture Sensitivity Level	MSL3

[1] Analog Devices recommends that reflow profiles used in soldering RoHS-compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Table 7. ADE9112/ADE9113 Absolute Maximum Ratings

Parameter	Rating
VDD to DGND and AVDD to AGND	−0.3 V to +3.7 V
Analog Input Voltage	
IP and IM to AGND	−1.4 V to +1.4 V
V1P and V1M to AGND	−2.0 V to +2.0 V
V2P and V2M to AGND	−1 V to +1 V
Digital Input Voltage	
MOSI, SCLK, $\overline{CS}$, $\overline{RESET}$, and XTALIN to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage	
$\overline{IRQ}$, ZX, CLKOUT, MISO, SCLK, and XTALOUT to DGND	−0.3 V to VDD + 0.3 V
Common-Mode Transients[1]	−150 kV/µs to +150 kV/µs
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Lead (Soldering, 10 sec)[2]	260°C
Moisture Sensitivity Level	MSL3

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

[2] Analog Devices recommends that reflow profiles used in soldering RoHS-compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction-to-case thermal resistance.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RN-28-1	65.69	36.19	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADE9103

Table 9. ADE9103, 28-Lead SOIC_W_FP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
CDM	±1250	C3

ESD Ratings for ADE9112 and ADE9113

Table 10. ADE9112 and ADE9113, 28-Lead SOIC_W_FP

ESD Model[1]	Withstand Threshold (V)	Class
HBM	±4000	3A
CDM	±1250	C3

[1] With respect to local VDD and AGND, and DGND and GND_{ISO} pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

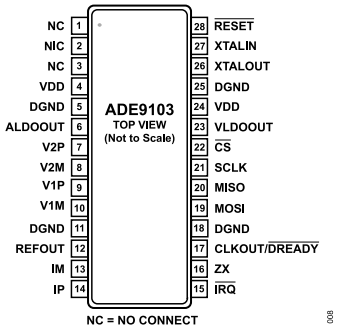

Figure 8. ADE9103 Pin Configuration

Table 11. ADE9103 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3	NC	No Connect. Pin 1 and Pin 3 are connected together internally. These NC pins have no internal connection.
2	NIC	Not Connected Internally. The NIC pin has no internal connection.
4, 24	VDD	Primary Supply Voltage. The VDD pins provide the supply voltage for the ADE9103. Maintain the supply voltage at 3.3 V ± 10% for the specified operation. Decouple the VDD pins to the closest DGND pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
5, 11, 18, 25	DGND	Ground Reference.
6	ALDOOUT	1.8 V Output of Analog LDO Regulator. Decouple the ALDOOUT pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to DGND, Pin 5. Do not connect the external load circuitry to the ALDOOUT pin.
7	V2P	Positive Analog Input for the V2 Voltage Channel. V2P and V2M are differential voltage inputs with a maximum single-ended signal level of ±500 mV with respect to the VxM pins for specified operation. Use the V2P and V1P pins with the related input circuitry, as shown in Figure 27. If the V2 voltage channel is not used, connect the V2P pin to the V2M pin.
8	V2M	Negative Analog Input for the V2 Voltage Channel.
9	V1P	Positive Analog Inputs for the V1 Voltage Channel. The voltage channels are used with the voltage transducers. V1P and V1M are differential voltage inputs with a maximum single-ended signal level of ±500 mV with respect to the VxM pins for specified operation. Use the V1P and V2P pins with the related input circuitry, as shown in Figure 27. If the V1 voltage channel is not used, connect the V1P pin to the V1M pin.
10	V1M	Negative Analog Input for the V1 Voltage Channel.
12	REFOUT	Voltage Reference Output. The REFOUT pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. Decouple the REFOUT pin to DGND, Pin 11, with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. Do not connect external load circuitry to the REFOUT pin.
13	IM	Negative Analog Input for the Current Channel. The current channel is used with shunts. IM and IP are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use the IM and IP pins with the related input circuitry, as shown in Figure 27.
14	IP	Positive Analog Input for the Current Channel.
15	$\overline{\text{IRQ}}$	Interrupt Request Output. The $\overline{\text{IRQ}}$ pin is an active low logic open drain outputwith weak internal pull-up resistor.
16	ZX	Zero-Crossing Output Pin. The ZX pin must float when unused.
17	CLKOUT/$\overline{\text{DREADY}}$	Clock Output (CLKOUT). When CLKOUT functionality is selected (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details), the ADE9103 generates a digital signal synchronous to the main clock at the XTALIN pin. Use CLKOUT to provide a clock to other ADE9103/ADE9112/ADE9113 devices. Data Ready, Active Low ($\overline{\text{DREADY}}$). When $\overline{\text{DREADY}}$ functionality is selected (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details), the ADE9103 generates an active low signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE9103.
19	MOSI	Data Input for the SPI Port.
20	MISO	Data Output for the SPI Port. Attach a 10 kΩ pull-up resistor to the VDD supply voltage for increased electromagnetic compatibility (EMC) robustness.
21	SCLK	Serial Clock Input for the SPI Port. All serial data transfers are synchronized to this clock (see Table 3 for SPI interface timing parameters and SPI Compatible Communication section for additional SPI port details).
22	$\overline{\text{CS}}$	Chip Select for the SPI Port (Active Low).

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 11. ADE9103 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
23	VLDOOUT	1.8 V Output of Digital LDO Regulator. Decouple the VLDOOUT pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to DGND, Pin 25. Do not connect the external load circuitry to the VLDOOUT pin.
26	XTALOUT	Crystal Output. A crystal must be chosen based on the transconductance (g_m) in Table 2. The crystal is connected across the XTALIN and XTALOUT pins to provide a clock source for the ADE9103. The XTALOUT pin must float when unused.
27	XTALIN	Main Clock Input. An external clock can be provided at this logic input. The CLKOUT signal of another appropriately configured ADE9103/ADE9112/ADE9113 (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details) can be provided at the XTALIN pin. Alternatively, a crystal can be connected across XTALIN and XTALOUT to provide a clock source for the ADE9103. See the Crystal Oscillator/External Clock section for more details.
28	$\overline{\text{RESET}}$	Active Low Reset Input. To initiate a hardware reset, this pin must be brought low for a minimum of 1.5 µs.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

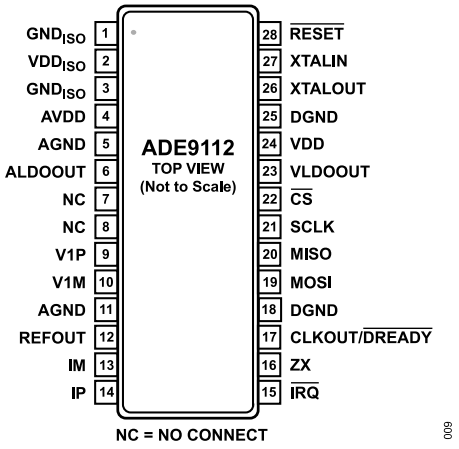

Figure 9. ADE9112 Pin Configuration

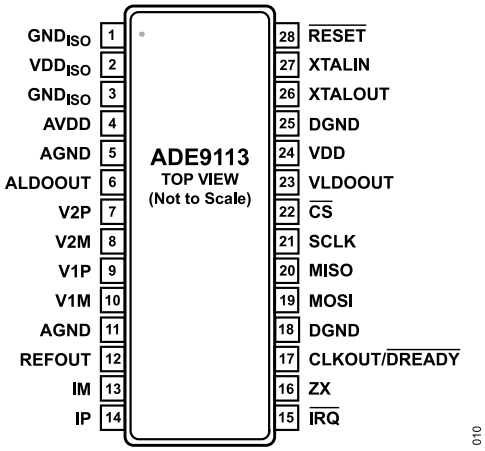

Figure 10. ADE9113 Pin Configuration

Table 12. ADE9112 and ADE9113 Pin Function Descriptions

Pin No.			
ADE9112	**ADE9113**	**Mnemonic**	**Description**
1, 3	1, 3	GND_{ISO}	Ground for the Isolated DC-to-DC Converter, Connected to the GND_{ISO} Paddle.
2	2	VDD_{ISO}	DC-to-DC Converter Voltage Output. VDD_{ISO} requires a low ESR 100 nF bypass capacitor connected to GND_{ISO}.
4	4	AVDD	Power Supply for the Isolated Side. AVDD requires 4.7 µF and 100 nF bypass capacitor to AGND.
5, 11	5, 11	AGND	Ground Reference.
6	6	ALDOOUT	1.8 V Output of Analog LDO Regulator. Decouple the ALDOOUT pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to AGND, Pin 5. Do not connect the external load circuitry to the ALDOOUT pin.
7		NC	No Connect. The NC pin has an internal connection. Leave the NC pin floating or tie it to Pin 8.
8		NC	No Connect. The NC pin has an internal connection. Leave the NC pin floating or tie it to Pin 7.
	7	V2P	Positive Analog Input for the V2 Voltage Channel. The voltage channels are used with the voltage transducers. V2Pand V2M are differential voltage inputs with a maximum single-ended signal level of ±500 mV with respect to the VxM pins for specified operation. Use the V2P and V1P pins with the related input circuitry, as shown in Figure 27. If the V2 voltage channel is not used, connect the V2P pin to the V2M pin.
	8	V2M	Negative Analog Input for the V2 Voltage Channel.
9	9	V1P	Positive Analog Inputs for the V1 Voltage Channel. V1P and V1M are differential voltage inputs with a maximum single-ended signal level of ±500 mV with respect to the VxM pins for specified operation. Use the V1P and V2P pins with the related input circuitry, as shown in Figure 27. If the V1 voltage channel is not used, connect the V1P pin to the V1M pin.
10	10	V1M	Negative Analog Input for the V2 Voltage Channel.
12	12	REFOUT	Voltage Reference Output. The REFOUT pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. Decouple the REFOUT pin to AGND, Pin 11, with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. Do not connect external load circuitry to the REFOUT pin.
13	13	IM	Negative Analog Input for the Current Channel. The current channel is used with shunts. IM and IP are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use the IM and IP pins with the related input circuitry, as shown in Figure 27.
14	14	IP	Positive Analog Input for the Current Channel.
15	15	$\overline{IRQ}$	Interrupt Request Output. The $\overline{IRQ}$ pin is an active low logic open drain output with weak internal pull-up resistor.
16	16	ZX	Zero-Crossing Output Pin. The ZX pin must float when unused.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 12. ADE9112 and ADE9113 Pin Function Descriptions (Continued)

Pin No.			
ADE9112	ADE9113	Mnemonic	Description
17	17	CLKOUT/$\overline{\text{DREADY}}$	Clock Output (CLKOUT). When CLKOUT functionality is selected (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details), the ADE9112 and ADE9113 generate a digital signal synchronous to the main clock at the XTALIN pin. Use CLKOUT to provide a clock to the other ADE9112 and ADE9113 devices on the board. Data Ready, Active Low ($\overline{\text{DREADY}}$). When $\overline{\text{DREADY}}$ functionality is selected (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details), the ADE9112 and ADE9113 generate an active low signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE9112 and ADE9113.
18, 25	18, 25	DGND	Ground Reference.
19	19	MOSI	Data Input for the SPI Port.
20	20	MISO	Data Output for the SPI Port. Attach a 10 kΩ pull-up resistor to the VDD supply voltage for increased EMC robustness.
21	21	SCLK	Serial Clock Input for the SPI Port. All serial data transfers are synchronized to this clock (see Table 3 for SPI interface timing parameters and SPI Compatible Communication section for additional SPI port details).
22	22	$\overline{\text{CS}}$	Chip Select for SPI Port (Active Low).
23	23	VLDOOUT	1.8 V Output of Digital LDO Regulator. Decouple the VLDOOUT pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to DGND, Pin 25. Do not connect the external load circuitry to the VLDOOUT pin.
24	24	VDD	Primary Supply Voltage. The VDD pin provides the supply voltage for the and ADE9113. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple the VDD pin to DGND, Pin 25, with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
26	26	XTALOUT	Crystal Output. A crystal must be chosen based on the transconductance (g_m) in Table 2.The crystal is connected across the XTALIN and XTALOUT pins to provide a clock source for the ADE9112 and ADE9113. The XTALOUT pin must float when unused.
27	27	XTALIN	Main Clock Input. An external clock can be provided at this logic input. The CLKOUT signal of another appropriately configured ADE9103/ADE9112/ADE9113 (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for details) can be provided at the XTALIN pin. Alternatively, a crystal can be connected across the XTALIN and XTALOUT pins to provide a clock source for the ADE9112 and ADE9113. See the Crystal Oscillator/External Clock section for more details.
28	28	$\overline{\text{RESET}}$	Active Low Reset Input. To initiate a hardware reset, the $\overline{\text{RESET}}$ pin must be brought low for a minimum of 1.5 µs.

TYPICAL PERFORMANCE CHARACTERISTICS

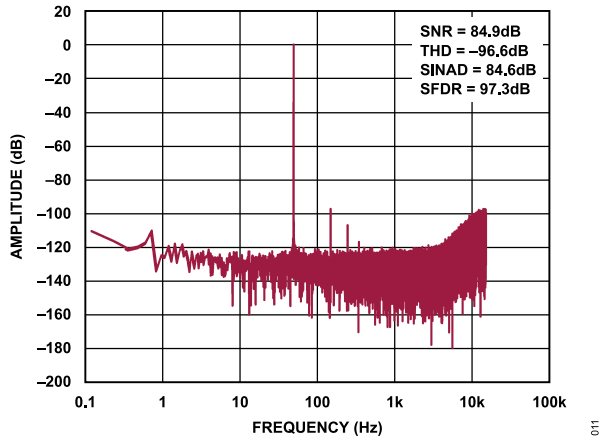

Figure 11. Current Channel Fast Fourier Transform (FFT), 32 kSPS Sinc3 Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 000b)

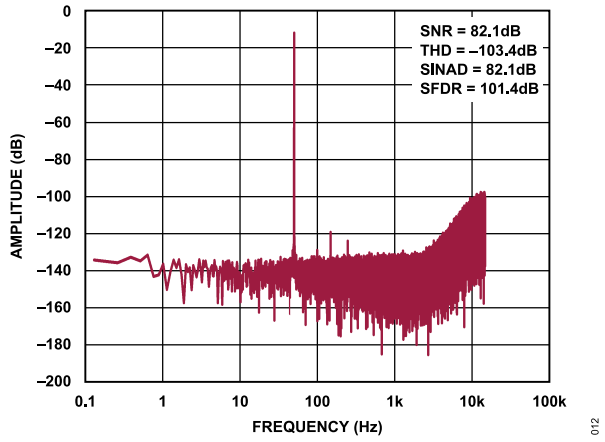

Figure 12. Voltage Channel V1 FFT, 32 kSPS Sinc3 Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 000b)

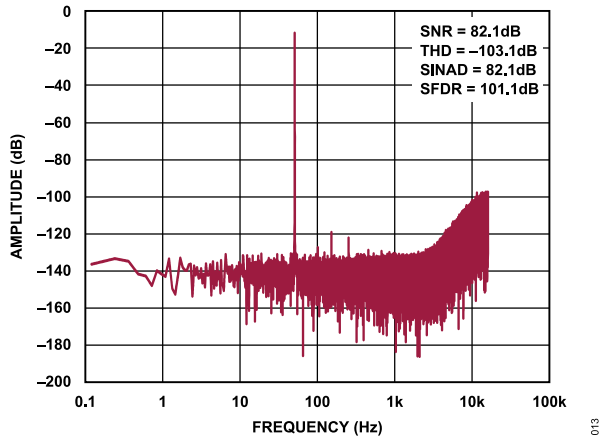

Figure 13. Voltage Channel V2 FFT, 32 kSPS Sinc3 Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 000b)

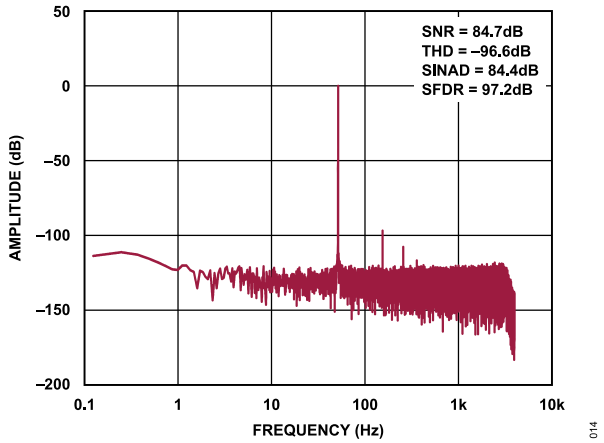

Figure 14. Current Channel FFT, 8 kSPS Sinc3 + Compensation + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 100b)

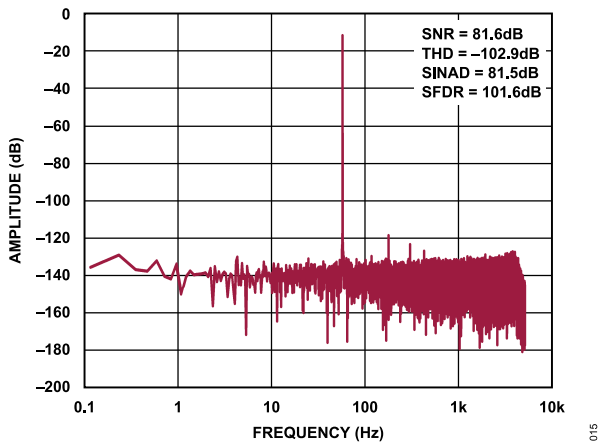

Figure 15. Voltage Channel V1 FFT, 8 kSPS Sinc3 + Compensation + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 100b)

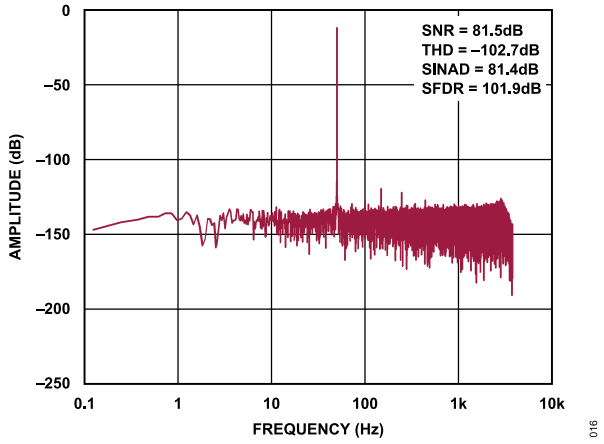

Figure 16. Voltage Channel V2 FFT, 8 kSPS Sinc3 + Compensation + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 100b)

TYPICAL PERFORMANCE CHARACTERISTICS

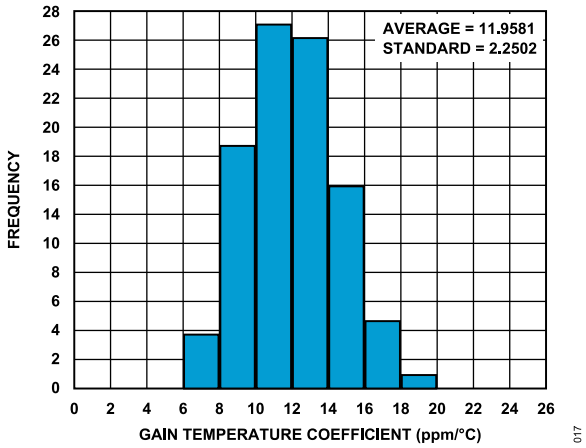

Figure 17. ADE9112 and ADE9113 Current Channel Gain Temperature Coefficient Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

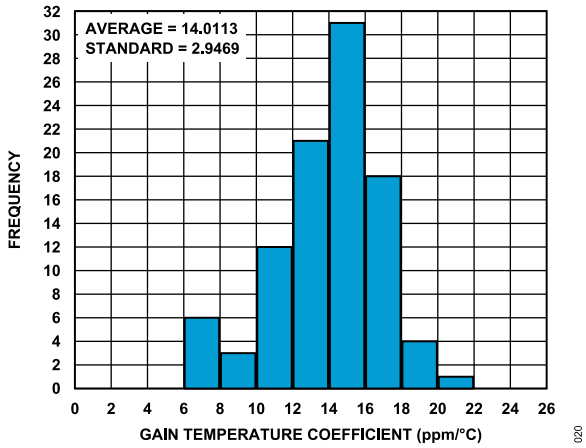

Figure 20. ADE9103 Voltage Channel V1 and V2 Gain Temperature Coefficient Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

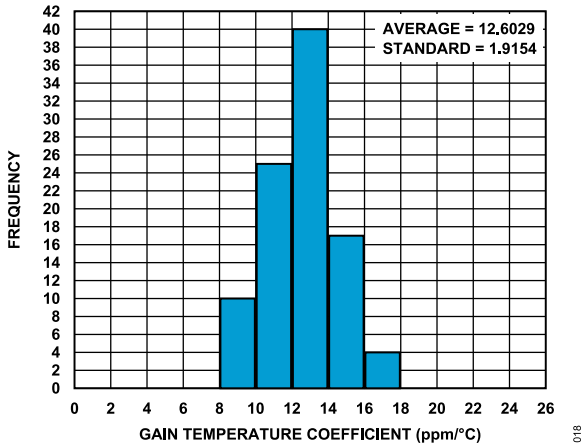

Figure 18. ADE9112 and ADE9113 Voltage Channel V1 and V2 Gain Temperature Coefficient Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

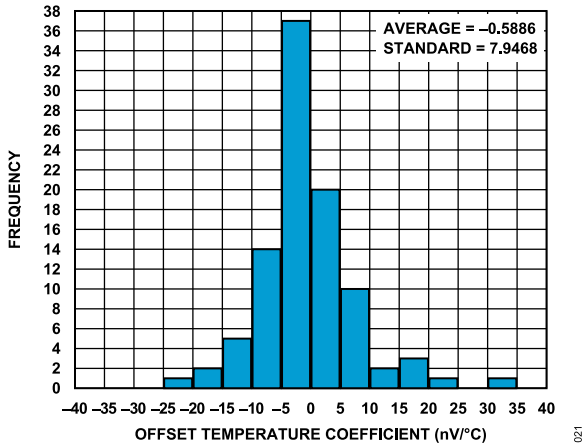

Figure 21. ADE9112 and ADE9113 Current Channel Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

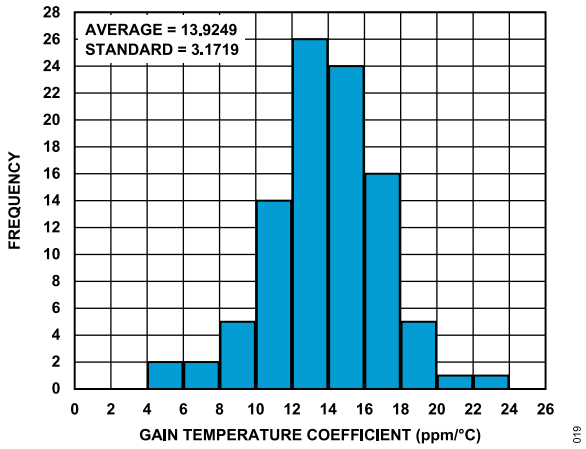

Figure 19. ADE9103 Current Channel Gain Temperature Coefficient Histogram, 8 kSPS Sinc3 + LPF Output(Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

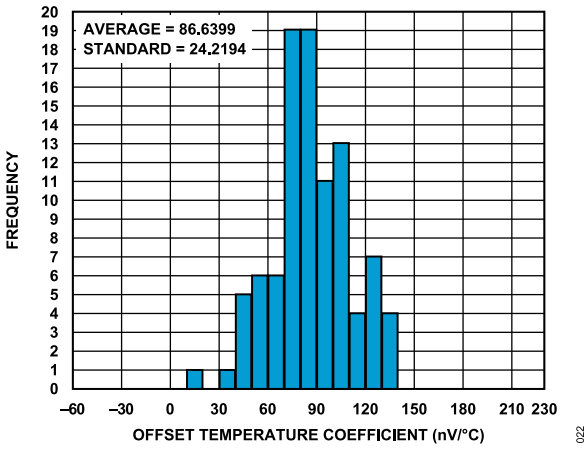

Figure 22. ADE9112 and ADE9113 Voltage Channel V1 Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

TYPICAL PERFORMANCE CHARACTERISTICS

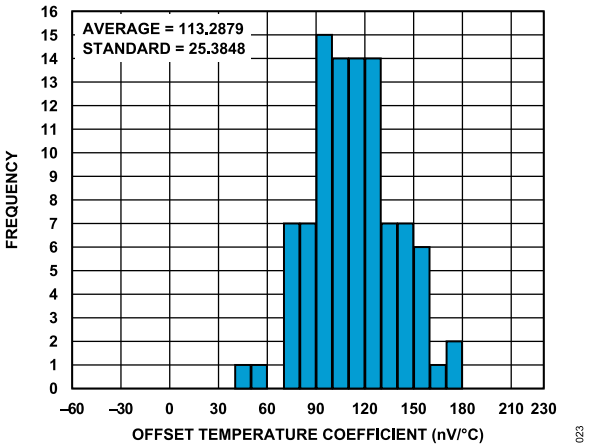

Figure 23. ADE9112 and ADE9113 Voltage Channel V2 Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

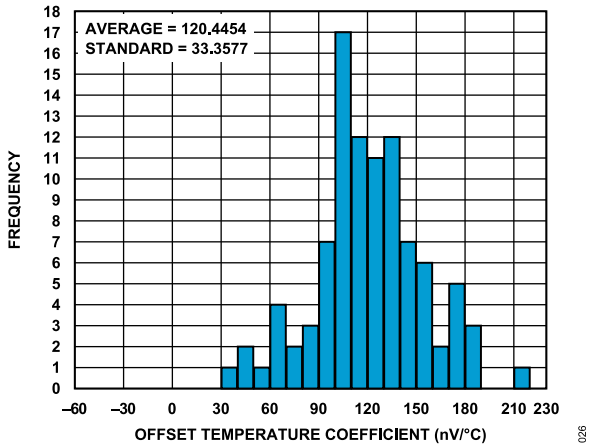

Figure 26. ADE9103 Voltage Channel V2 Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

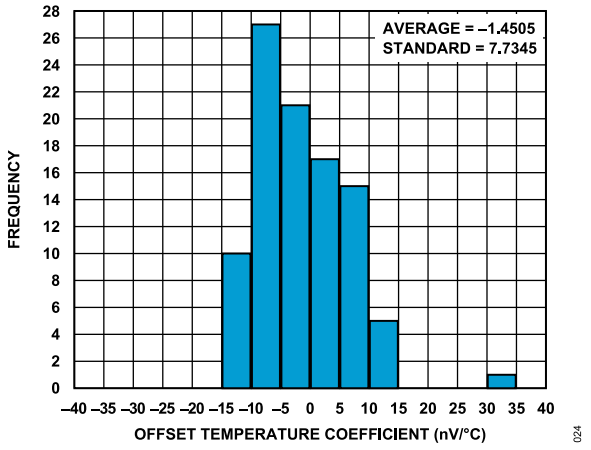

Figure 24. ADE9103 Current Channel Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

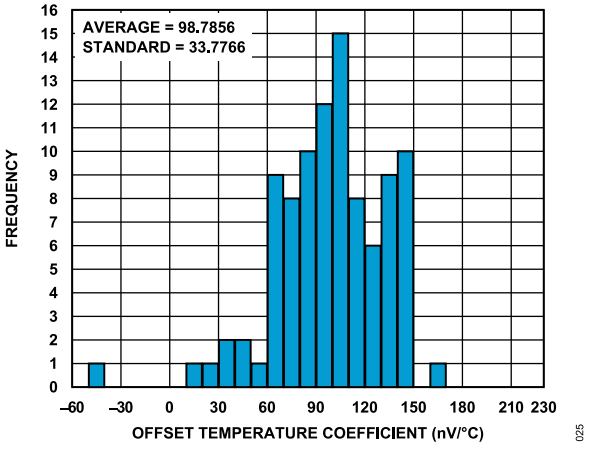

Figure 25. ADE9103 Voltage Channel V1 Offset Drift Histogram, 8 kSPS Sinc3 + LPF Output (Register CONFIG_FILT, DATAPATH_CONFIG Bits = 011b)

TEST CIRCUIT

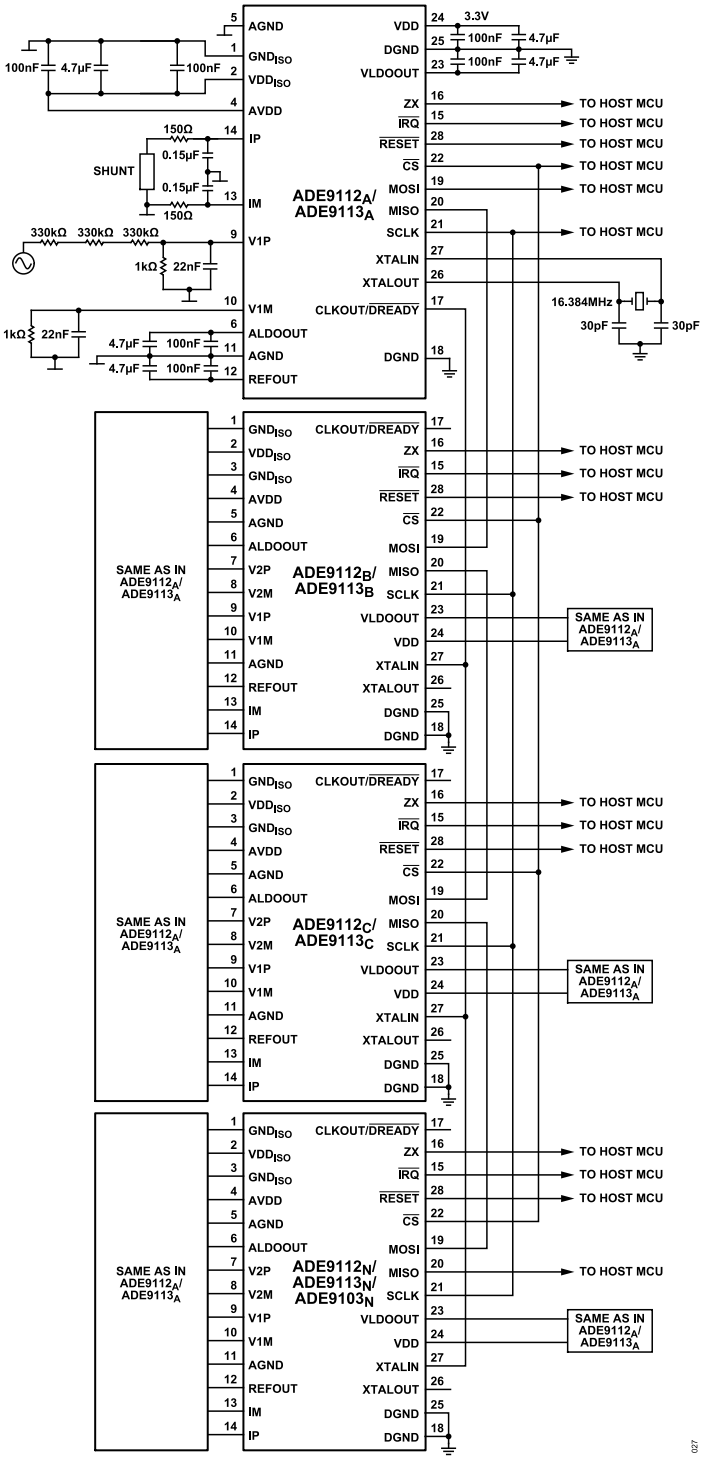

Figure 27. Test Circuit

TERMINOLOGY

Signal Voltage Range Between the IP and IM, V1P and V1M, and V2P and V2M Pins

The ADE9103 and ADE9113 contain three fully-differential ADCs, while the ADE9112 has two fully-differential ADCs, allowing flexibility in terms of the measurement and how the ADCs are used. The application typically uses a shunt sensor for the current and a potential divider for the voltage, which means that the signal applied at the input can be seen as pseudo differential. The input range on the current channel represents the peak-to-peak pseudo differential voltage that must be applied to the ADC to generate a full-scale response when the IM pin is connected to AGND, Pin 11. The input range on the voltage channel is represented in two ways: differential, where a signal is applied to both VxP and VxM to generate a full-scale response, and pseudo differential, where the signal is only applied to the VxP pin to generated a ½ of full-scale response when the VxM pin is connected to AGND. When psuedo differential, the IM and VxM pins are connected to AGND using antialiasing filters. Figure 28 illustrates the input voltage range between IP and IM, and Figure 29 illustrates the input voltage range between V1P and V1M and between V2P and V2M.

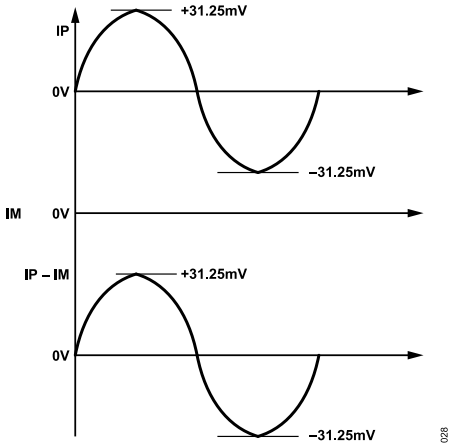

Figure 28. Pseudo Differential Input Voltage Range Between the IP and IM Pins

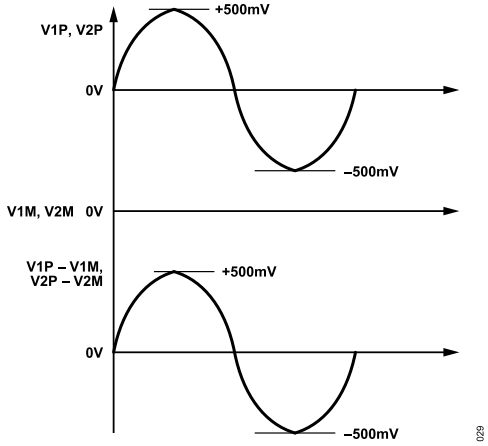

Figure 29. Pseudo Differential Input Voltage Range Between the V1P and V1M Pins and Between the V2P and V2M Pins

Maximum VxM and IM Voltage Range

This range represents the maximum allowed voltage at the V1P, V1M, V2P, IP, and IM pins relative to AGND, Pin 11 on the ADE9112 and ADE9113, or DGND, Pin 11 on the ADE9103.

Crosstalk

Crosstalk represents the leakage of signals, usually via the capacitance between circuits. Crosstalk is measured in the current channel by setting the IP and IM pins to the local ground reference, Pin 11, supplying a full-scale differential voltage between the V1P and V1M voltage channel pins and between the V2P and V2M voltage channel pins, and measuring the output of the current channel. It is measured in the V1 voltage channel by setting the V1P and V1M pins to the local ground reference, Pin 11, supplying a full-scale differential voltage between the IP and IM pins and between the V2P and V2M pins, and measuring the output of the V1 voltage channel. Crosstalk is measured in the V2 voltage channel by setting the V2P and V2M pins to the local ground reference, Pin 11, supplying a full-scale differential voltage between the IP and IM pins and between the V1P and V1M pins, and measuring the output of the V2 voltage channel. Crosstalk is equal to the ratio between the grounded ADC output value and the ADC full-scale output value. The ADC outputs are acquired for 2 sec. Crosstalk is expressed in decibels.

Input Impedance to Ground (DC)

The input impedance to ground represents the impedance measured at each ADC input pin (IP, IM, V1P, V2P, V1M, and V2M) with respect to AGND, Pin 11 on the ADE9112 and ADE9103, and DGND, Pin 11 on the ADE9103.

ADC Offset

The ADC offset error is the average measured ADC output code with both inputs connected to AGND of the ADE9112 and ADE9113 and DGND of the ADE9103.

TERMINOLOGY

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +125°C. The offset drift over temperature is computed as follows:

$$\text{Drift}_{-40 \text{ to } +125} = \left| \frac{\text{Offset}(-40) - \text{Offset}(+125)}{(-40 - 125)} \right|$$

Offset drift is expressed in nV/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when the internal voltage reference is used (see the Analog-to-Digital Conversion section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one of the current or one of the voltage channels.

Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain and of the internal voltage reference. It represents the overall temperature coefficient of one current or one of the voltage channels. With the internal voltage reference in use, the ADC gain is measured at −40°C, +25°C, and +125°C. The temperature coefficient is computed as follows:

$$\text{Drift}_{-40 \text{ to } +125} = \left| \frac{\text{Gain}(-40) - \text{Gain}(+125)}{\text{Gain}(+25) \times (-40 - 125)} \right|$$

Gain drift is measured in ppm/°C.

Power Supply Rejection (PSR)

PSR quantifies the measurement error as a percentage of reading when the power supplies are varied. For the AC PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage at the input pins is 0 V. A second reading is obtained with the same input signal levels when an AC signal (120 mV RMS at 50 Hz or 100 Hz) is introduced onto the supplies. Any error introduced by this AC signal is expressed as a percentage of the reading (PSRR). PSR = 20 $\log_{10}$ (PSRR).

For the DC PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage between the IP and IM pins is 3.125 mV peak, and the voltages between the V1P and V1M pins and between the V2P and V2M pins are 100 mV peak. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then, PSR = 20 $\log_{10}$ (PSRR).

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the differential gain of the channel divided by the common-mode gain.

IP − IM = 31.25 mV peak differential is applied, and an FFT is used to measure the fundamental in dB.

IP = IM = 31.25 mV peak to the local ground reference, Pin 11, common-mode is applied, and an FFT is used to measure the fundamental in dB.

VxP - VxM = 100 mV peak differential is applied, and an FFT is used to measure the fundamental in dB.

VxP = VxM = 100 mV peak to the local ground reference, Pin 11, common-mode is applied, and an FFT is used to measure the fundamental in dB.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components within the bandwidth, excluding harmonics and DC. The waveform samples are coherently sampled over approximately 8 sec to avoid using a window function. The value for SNR is expressed in decibels relative to full-scale (dBFS).

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components within the bandwidth, including harmonics but excluding DC. The waveform samples are coherently sampled over approximately 8 sec to avoid using a window function. The value for SINAD is expressed in decibels relative to full-scale (dBFS).

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of all harmonics (excluding the noise components) to the RMS value of the fundamental. The waveform samples are coherently sampled over approximately 8 sec to avoid using a window function. The value for SNR is expressed in decibels relative to full-scale (dBFS).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS value of the actual input signal to the RMS value of the peak spurious component over the measurement bandwidth of the waveform samples. The waveform samples are coherently sampled over approximately 8 sec to avoid using a window function. The value of SFDR is expressed in decibels relative to full scale (dBFS).

THEORY OF OPERATION

ANALOG INPUTS

The ADE9113 has three analog inputs: one current channel and two voltage channels. The ADE9112 does not include the second voltage channel. The current channel has two fully differential voltage input pins, IP and IM, that accept a maximum differential signal of ±31.25 mV.

The maximum IP voltage (V_{IP}) signal level is also ±31.25 mV. The maximum IM voltage (V_{IM}) signal level allowed at the IM input is ±25 mV. Figure 30 shows a schematic of the input for the current channel and the relation to the maximum IM pin voltage.

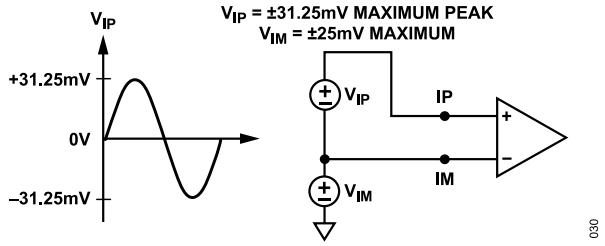

Figure 30. Maximum Input Level, Current Channel

Note that the current channel senses the voltage across a shunt. In this case, one pole of the shunt becomes the ground of the meter (see Figure 35) and, therefore, the current channel is used in a pseudo differential configuration, similar to the voltage channel configuration (see Figure 31).

The V1 and V2 voltage channels are fully differential, but most typically used in a pseudo differential setup. These differential voltage inputs have a maximum input voltage of ±1000 mV. If setup pseudo differentially, the voltage inputs have a maximum input voltage of ±500 mV with respect to V1M or V2M. The maximum signal allowed on the VxP or VxM pins is ±600 mV. Figure 31 shows a schematic of the voltage channel inputs and their relation to the maximum VxM voltage.

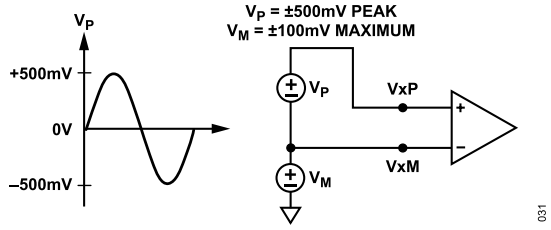

Figure 31. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE9103/ADE9112/ADE9113 have three, second-order, multi-bit Σ-Δ ADCs. For simplicity, the block diagram in Figure 32 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter (LPF), separated by the digital isolation block.

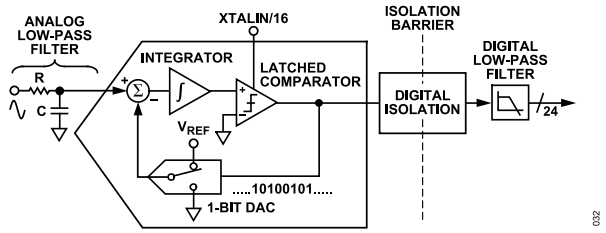

Figure 32. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE9103/ADE9112/ADE9113, the sampling clock is equal to XTALIN/16 (1.024 MHz when XTALIN = 16.384 MHz). The 1-bit DAC in the feedback loop is driven by the serial stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is completed in the second part of the ADC, the digital LPF, after the data passes through the digital isolators. By averaging a large number of bits from the modulator, the LPF can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first technique is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when XTALIN = 16.384 MHz, the sampling rate in the ADE9103/ADE9112/ADE9113 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the bandwidth of interest is lowered, as shown in Figure 33.

However, oversampling alone is not sufficient to improve the SNR in the band of interest. For example, an oversampling factor of 4 is required to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. Noise shaping is the second technique that achieves high resolution. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the

THEORY OF OPERATION

higher frequencies where it can be removed by the digital LPF. This noise shaping is shown in Figure 33.

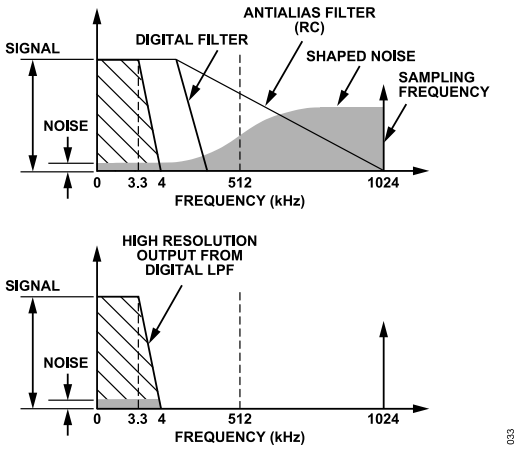

Figure 33. Noise Reduction due to Oversampling and Noise Shaping in the Analog Modulator

The bandwidth of interest is a function of the input clock frequency and the ADC output frequency (selectable by the CONFIG_FILT register, see the ADC Output Values section for details).

Antialiasing Filter

Figure 32 shows an analog LPF (RC) on the input to the ADC. This filter is placed outside of the ADE9103/ADE9112/ADE9113, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems, as shown in Figure 34. Aliasing refers to the frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC and appear in the sampled signal at a frequency less than half the sampling rate. Frequency components more than half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down to less than 512 kHz, which happens with all ADCs, regardless of the architecture. In Figure 34, only frequencies near the sampling frequency of 1.024 MHz move into the bandwidth of interest for metering, that is, 40 Hz to 3.3 kHz, or 40 Hz to 2 kHz. To attenuate the high frequency noise (near 1.024 MHz) and prevent the distortion of the bandwidth of interest, a LPF must be introduced. It is recommended that one RC filter with a corner frequency of 7 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing.

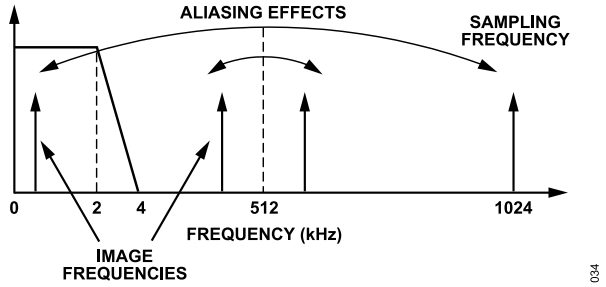

Figure 34. Aliasing Effects

ADC Transfer Function

All ADCs in the ADE9103/ADE9112/ADE9113 produce signed 24-bit output codes. With a full-scale input signal of ±31.25 mV on the current channel and ±1000 mV on the voltage channels, and with an internal reference of 1.25 V, the ADC output code is nominally 6,710,886 and based on the gain error, varies for each ADE9103/ADE9112/ADE9113 around this value. Do not exceed the nominal range of ±31.25 mV for the current channel and ±1000 mV differentially (±500 mV pseudo differentially) for the voltage channels; ADC performance is guaranteed only for input signals within these limits.

$$Approximate \quad Output \quad Code = \frac{VxP - VxM}{V_{REF}} \times 2^{23} \tag{1}$$

$$Approximate \quad Output \quad Code = 32 \times \frac{IP - IM}{V_{REF}} \times 2^{23} \tag{2}$$

ADC Output Values

The signed 24-bit ADC output values are each stored in three subsequent registers. The current channel ADC outputs are stored in the I_WAV bits, Bits[23:0], the V1 voltage channel ADC outputs in the V1_WAV bits, Bits[23:0], and the V2 voltage channel outputs in the V2_WAVbits, Bits[23:0], see Table 19. The output frequency is 32 kHz (XTALIN/512), 8 kHz (XTALIN/2048), 4 kHz (XTALIN/4096), 2 kHz (XTALIN/8192), or 1 kHz (XTALIN/16384), and XTALIN is 16.384 MHz.

The microcontroller reads the ADC output registers one at a time in a short transaction or all at once in a long transaction. See the SPI Long Format Operation section and the SPI Short Format Operation section for more information.

REFERENCE VOLTAGE

The nominal reference voltage at the REFOUT pin is 1.25 V. This reference voltage is used for the ADCs in the ADE9103/ADE9112/ADE9113. Because the on-chip dc-to-dc converter cannot supply external loads, the REFOUT pin of the ADE9112 and ADE9113 cannot be overdriven by a standalone external voltage reference.

The voltage of the ADE9103/ADE9112/ADE9113 reference drifts slightly with temperature. Table 2 lists the gain drift over temperature specification of each ADC channel. This value includes the

THEORY OF OPERATION

temperature variation of the ADC gain, together with the temperature variation of the internal voltage reference.

THEORY OF OPERATION

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration lock feature protects the ADE9103/ADE9112/ADE9113 configuration registers from unwanted changes. To enable this feature, write the Lock Key 0xD4 to the WR_LOCK register (Address 0x01F). To disable this feature, write the Unlock Key 0x5E.

To determine whether the feature is enabled or disabled read back the WR_LOCK register. This register reads back as the lock or unlock key corresponding to the state it is in.

When this feature is enabled, it prevents writing from Address 0x001 to Address 0x018.

CRC OF CONFIGURATION REGISTERS

A 16-bit CRC is calculated over the configuration registers approximately every 8 ms. The result is stored in CRC_RESULT bits, which is split into a high and low byte, CRC_RESULT_HI and CRC_RESULT_LO. The default value in the CRC_RESULT bits is the CRC result of the default configuration registers. If there is a change in the CRC result, the CRC_CHG bit inside of STATUS0 is set. The configuration registers, CONFIG0, CONFIG_FILT, CONFIG_ISO_ACC, EMI_CONFIG, EMI_HI_MASK, EMI_LO_MASK, MASK0, MASK1, MASK2, CONFIG_ZX, SCRATCH, as well as other critical reserved registers are covered by this CRC. The CRC calculation cannot be disabled.

The CRC calculation of the configuration registers can also be performed on command by writing to the CRC_FORCE bit in the CONFIG_CRC register. Writing the CRC_FORCE bit resets the CRC interval counter and deasset CRC_DONE if previously set until the CRC calculation is complete. The CRC_FORCE bit is cleared and the CRC_DONE bit is set once the CRC calculation is complete. If CRC_FORCE is written high and then rewritten high or low while recalculating, the second write is ignored. See Table 20 for more details.

STATUS REGISTERS

The bits in the STATUS0, STATUS1, and STATUS2 registers of the ADE9103/ADE9112/ADE9113 characterize the state of the device.

At power-up, or after a hardware or software reset, the ADE9103/ADE9112/ADE9113 signal the end of the reset period by setting Bit 5 (RESET_DONE) to 1 in the STATUS0 register, indicating that the IC is ready for SPI transactions. Then, Bit 4 (COM_UP) of STATUS0 gets set to 1 to indicate that the entire IC is up and ready to transmit the ADC waveform data.

The COMFLT_ERR bit (Bit 0) in the STATUS0 register indicates when there was a communications failure across the isolation barrier. This status bit is used together with the COM_FLT_TYPE and COM_FLT_COUNT registers. COM_FLT_TYPE gives more detail as to the type of error that was detected across the isolation barrier, and then, COM_FLT_COUNT keeps track of the number of error correction codes (ECC) or physical layer (PHY) errors from the ISO side to the NONISO side. ECC across the isolation barrier allows 1-bit detect and 1-bit correct and increases the communication robustness across the barrier. Even though the ADE9103 does not have isolation, the ECC function of the internal communication is still present.

The STATUS0 and STATUS1 registers can be read by executing an SPI register read. STATUS0 and STATUS1 can also be read as part of the long SPI read operation. See the SPI Long Format Operation and the SPI Short Format Operation sections for more information.

The STATUS2 register provides insight into internal errors that have been detected and corrected. No additional actions are required outside of acknowledging the change through a write 1 command. If a bit in STATUS2 is continuously being set, this could indicate that the ADE9103/ADE9112/ADE9113 is in an unrecoverable state.

For more information on individual bits in the STATUSx registers, go to the bit field descriptions in the Table 20 section.

ZERO CROSSING

The ADE9103/ADE9112/ADE9113 devices have independent zero crossing detection circuits on each ADC channel. The ZX pin indicates a zero crossing event and can be used to extract a low latency power line frequency measurement. Other common uses for zero crossing detection are indicating opportunities to open and close relay contacts for minimal switching voltage or deriving time periods when power line voltage is sufficiently low for power-line communications in energy metering and programmable logic controller (PLC) systems. See zero crossing output latency and jitter specification in Table 2.

The ZX_CHANNEL_CONFIG bits in the CONFIG_ZX register set which ADC channel zero crossing detection circuit is routed to the ZX output pin. The response and behavior of the ZX pin output are selectable and allow the flexibility to choose which zero crossing events are reported by setting the ZX_EDGE_SEL bits. Options and settings for the CONFIG_ZX register are described in Table 20. The ZX pin output is disabled by default.

The input of each zero crossing detection circuit has a first order LPF to filter line harmonics. The typical cutoff frequency is 80 Hz. The V1 and V2 voltage channels both have integrated hysteresis to minimize the effects of line noise and bounce. The current channel does not have hysteresis.

INTERRUPTS

The ADE9103/ADE9112/ADE9113 have two methods for indicating an event has occurred: the STATUS0, STATUS1, and STATUS2 registers and the $\overline{\text{IRQ}}$ pin. Details for the STATUS0, STATUS1, and STATUS2 registers can be found in Status Registers and Table 20. The interrupt pin ($\overline{\text{IRQ}}$), connected to the STATUSx registers through the MASKx registers, helps detect critical faults to create a reliable and robust system. The $\overline{\text{IRQ}}$ pin is open drain, allowing multiple interrupts to be connected together with a single 10 kΩ

THEORY OF OPERATION

pull-up resistor. In this configuration, a single pin on the host can sense if any one of the connected ADCs has generated an interrupt.

The MASK0 registers configures what events within the STATUS0 register trigger the $\overline{\text{IRQ}}$ pin. The MASK1 register configures what events within the STATUS1 register trigger the STATUS1X bit in the STATUS0 register. Similarly, the MASK2 register configures which events in STATUS2 trigger the STATUS2X bit in the STATUS0 register, which means that with the combination of MASK0, MASK1 and MASK2, any bit from the STATUS0, STATUS1, and STATUS2 registers can trigger the $\overline{\text{IRQ}}$ pin.

The RESET_DONE interrupt is nonmaskable and always triggers the $\overline{\text{IRQ}}$ pin. The EFUSE_MEM_ERR bit within the STATUS0 register is another example of a nonmaskable bit. The bits within STATUS2 can be masked with the MASK2 register because all of those faults cause action on the ISO side such as reset.

APPLICATIONS INFORMATION

POLYPHASE ENERGY METERS

The ADE9103/ADE9112/ADE9113 are designed for use in 3-phase energy metering systems in which two, three, or four ADE9103/ADE9112/ADE9113 devices are managed by a main device containing a SPI, usually a microcontroller. The integrated signal and power isolation of the ADE9112 and ADE9113 is required for phase current and voltage sensing often referred to as high-side sensing. Isolation provides both a safety barrier against high voltages for personnel and enables SPI communication across the high voltage offset between the ADC connected to each phase and a shared microcontroller. The ADE9103 can be used for neutral measurements where safety isolation is not required.

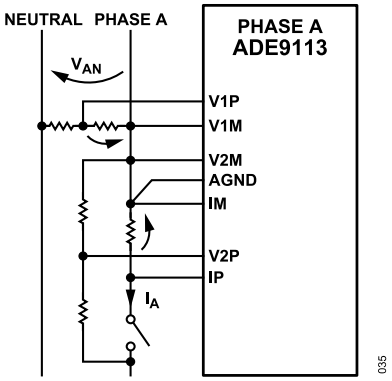

Figure 35. Phase A Current and Voltage Sensing

Figure 35 shows Phase A of a 3-phase energy meter. The Phase A current, I_A, is sensed with a shunt. A terminal of the shunt is connected to the IM pin of the ADE9112 and ADE9113 and becomes the ground reference of the isolated side of the ADE9112 and ADE9113. Phase A to the neutral voltage, V_{AN}, is sensed with a resistor divider. The V1M, IM, and AGND pins are connected as a single node. Note that the voltages measured by the ADCs of the ADE9112 and ADE9113 are opposite to V_{AN} and I_A, a classic approach in single-phase metering. The other ADE9112 and ADE9113 devices that monitor Phase B and Phase C are connected in a similar way.

The V2 voltage channel (V2P and V2M pins) is intended for a secondary voltage measurement, and it is available only on the ADE9103 and ADE9113. In Figure 35, the V2 voltage channel is used to measure the voltage across a relay to verify the state of the relay. If the V2 voltage channel is not used on the ADE9103 and ADE9113 devices, connect the V2P pin to the V2M pin. For the ADE9112, Pin 7 and Pin 8 are no connect, and these pins must be left floating or tied together.

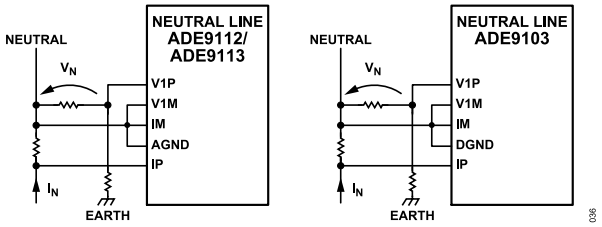

Figure 36. Neutral Line and Neutral to Earth Voltage Monitoring

Figure 36 shows how the ADE9103/ADE9112/ADE9113 inputs are connected when the neutral line of a 3-phase system is monitored. The neutral current is sensed using a shunt and the voltage across the shunt is measured at the fully differential inputs, IP and IM. The earth to neutral voltage is sensed with a voltage divider at the single-ended inputs, V1P and V1M.

Figure 37 shows a block diagram of a 3-phase energy meter that uses four ADE9103/ADE9112/ADE9113 devices and a microcontroller. One 16.384 MHz crystal provides the clock to the ADE9112 and ADE9113 that senses the Phase A current and voltage. The ADE9103/ADE9112/ADE9113 devices that sense the Phase B, Phase C, and neutral currents and voltages are clocked by a signal generated at the CLKOUT/ $\overline{\text{DREADY}}$ pin of the ADE9112 and ADE9113 that is placed to sense the Phase A current and voltage. As an alternative configuration, the microcontroller can generate a 16.384 MHz clock to all ADE9103/ADE9112/ADE9113 devices at the XTALIN pin. Note that the XTALIN pin can receive a clock with a frequency within the 15.84 MHz to 16.547 MHz range, as specified in Table 2.

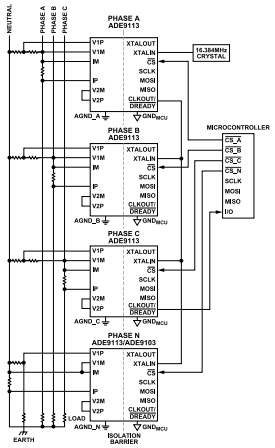

Figure 37. 3-Phase Energy Meter Using Four Devices

The microcontroller uses the SPI port to communicate with the ADE9103/ADE9112/ADE9113 devices. Four of the input and output pins, $\overline{\text{CS\_A}}$, $\overline{\text{CS\_B}}$, $\overline{\text{CS\_C}}$, and $\overline{\text{CS\_N}}$, generate the SPI $\overline{\text{CS}}$ signals. The SCLK, MOSI, and MISO pins of the microcontroller are directly connected to the corresponding SCLK, MOSI, and MISO pins of each ADE9103/ADE9112/ADE9113 device corresponding to the SPI configuration (see Figure 38 and Figure 39). In the case of the SPI daisy-chain configuration, the $\overline{\text{CS}}$ signals from all

APPLICATIONS INFORMATION

ADE9103/ADE9112/ADE9113 are connected, which helps to free up microcontroller pins for other purposes.

In Figure 37, the CLKOUT/$\overline{\text{DREADY}}$ pin of the ADE9103/ADE9112/ADE9113 that senses the Phase C current and voltage is connected to the input and output pin of the microcontroller. CLKOUT/$\overline{\text{DREADY}}$ provides an active low pulse for 256 CLKIN cycles (15.625 µs at CLKIN = 16.384 MHz) when the ADC conversion data is available. It signals when the ADC outputs of all ADE9103/ADE9112/ADE9113 devices become available and when the microcontroller starts to read them. See the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for more information about synchronizing multiple ADE9103/ADE9112/ADE9113 devices.

At power-up, or after a hardware or software reset, follow the procedure described in the Power-Up Procedure for Systems with Multiple Devices That Use a Single Crystal section or the Power-Up Procedure for Systems with Multiple Devices That Use a Clock Signal Generated from a Microcontroller section to ensure that the ADE9103/ADE9112/ADE9113 devices function appropriately.

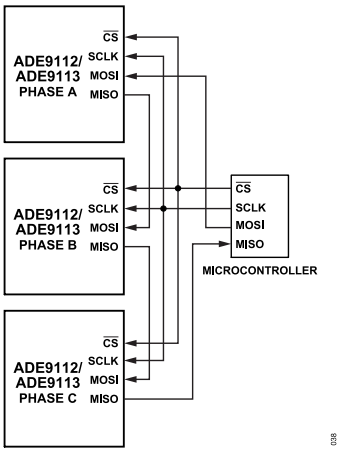

Figure 38. SPI Connection Between Three ADE9103/ADE9112/ADE9113 Devices in a Daisy Chain and a Microcontroller

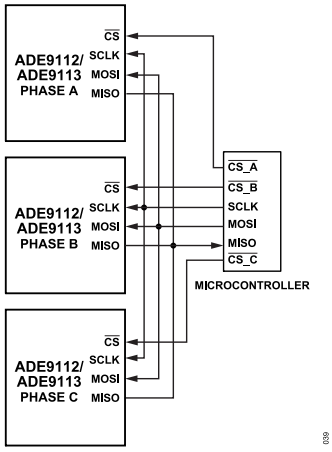

Figure 39. SPI Connections Between Three ADE9103/ADE9112/ADE9113 Devices and a Microcontroller

DC METERING

The ADE9103/ADE9112/ADE9113 can also be used in DC metering applications.

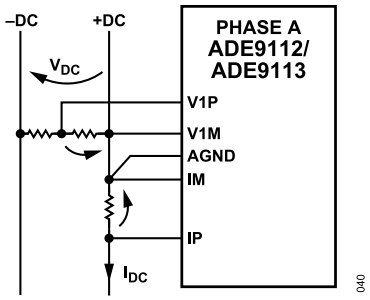

Figure 40. DC Current and Voltage Sensing

Figure 40 shows the ADE9112 and ADE9113 as a DC voltage and current sensor. The DC current, I_{DC}, is sensed with a shunt. A terminal of the shunt is connected to the IM pin of the ADE9112 and ADE9113 and becomes the ground, AGND (Pin 11), of the isolated side of the ADE9112 and ADE9113. The DC+ to DC− voltage, V_{DC}, is sensed with a resistor divider, and the V1M pin is also connected to the IM and AGND pins. Note that the voltages measured by the ADCs of the ADE9112 and ADE9113 are opposite to V_{DC} and I_{DC}, a classic approach in single-phase metering.

The V2P and V2M voltage channel is intended for a secondary voltage measurement, and it is available only on the ADE9113. If V2P is not used, as is the case of the ADE9112, connect V2P to V2M.

DC applications requiring working voltage capabilities beyond the ADE9112 and ADE9113 can use the ADE9103 in series with discrete signal and power isolation.

DC Offset Mode

The ADE9103/ADE9112/ADE9113 has a mode where the inputs of the current channel (IP and IM) can be internally shorted together, while disconnecting the external pin, to perform an offset measurement without the influence of circuits outside of the IC. This shorting can happen at any time while powered.

To use DC offset mode, take the following steps:

1. Set the ISO_WR_ACC_EN bit (Bit 0) within the CONFIG_ISO_ACC register (Address 0x005) to 1.
2. Wait at least 200 µs.
3. Set the DC_OFFSET_MODE register (Address 0x0CC) to 1.
4. Wait for appropriate settling time for the system and capture waveform data to perform the offset measurement.
5. Set the DC_OFFSET_MODE register (Address 0x0CC) to 0.
6. Clear the ISO_WR_ACC_EN bit (Bit 0) within the CONFIG_ISO_ACC register (Address 0x005) to 0.

APPLICATIONS INFORMATION

When using this feature, there could be a discontinuity in the waveform when going through the previous steps to enable and to disable the input shorting. The appropriate amount of settling time based on the speed and accuracy required for the measurement must be allowed.

MAGNETIC FIELD IMMUNITY OF ISOLATION

The ADE9112 and ADE9113 are immune to DC magnetic fields because these devices use air core transformers. The limitation on the ADE9112 and ADE9113 AC magnetic field immunity is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition is examined because it is the nominal supply of the ADE9112 and ADE9113.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by the following:

$$V = \left(-\frac{dB}{dt}\right) \sum_{n=1}^{N} \pi r_n^2$$

where:
B is the AC magnetic field: $B(t) = B \times \sin(\omega t)$.
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil.

Given the geometry of the receiving coil in the ADE9112/ADE9113 and an imposed requirement that the induced voltage, V_{THR}, be at most 50% of the 0.5 V margin at the decoder, a maximum allowable external magnetic field, B, is calculated (see the following equation and Figure 41).

$$B = \frac{V_{THR}}{2\pi f \times \sum_{n=1}^{N} \pi r_n^2}$$

where:
f is the frequency of the magnetic field.
B is the amplitude of the AC magnetic field.

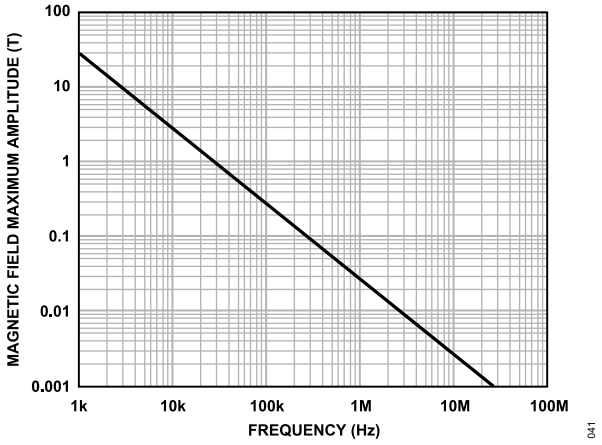

Figure 41. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 10 kHz, the maximum allowable magnetic field of 2.8 T induces a voltage of 0.25 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is of the worst-case polarity, it reduces the received pulse from more than 1.0 V to 0.75 V, still well more than the 0.5 V sensing threshold of the decoder.

The preceding magnetic field values correspond to specific current magnitudes at given distances from the ADE9112 and ADE9113 transformers.

$$I = \frac{B}{\mu_0} \times 2\pi d = \frac{V \times d}{\mu_0 \times f \times \sum_{n=1}^{N} \pi r_n^2}$$

where μ_0 is $4\pi \times 10^{-7}$ H/m, the magnetic permeability of the air.

Figure 42 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 50, the ADE9112/ADE9113 are extremely immune and can be affected only by extremely large currents operating at high frequency close to the component. For the 10 kHz example previously noted, a current with an amplitude of 69 kA placed 5 mm from the ADE9112/ADE9113 is required to affect component operation.

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility (see the Layout Guidelines section).

APPLICATIONS INFORMATION

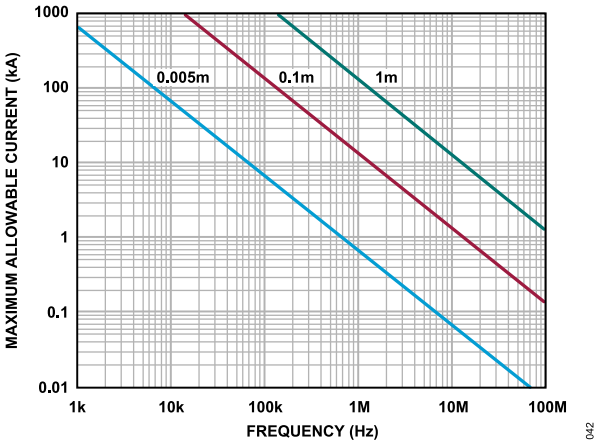

Figure 42. Maximum Allowable Current for Various Current to ADE9112 and ADE9113 Spacings

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

The ADE9103/ADE9112/ADE9113 requires either an external digital clock signal or a crystal for operation. A digital clock signal is routed to the XTALIN pin to clock the ADE9103/ADE9112/ADE9113. The XTALOUT pin is left floating when XTALIN is provided an external digital clock source. The requirements for external digital clock source frequency, duty cycle, and voltage levels are provided in Table 2.

When a crystal is used as the clock source for the ADE9103/ADE9112/ADE9113, attach the crystal and the ceramic capacitors, with capacitance of C_1 and C_2, as shown in Figure 43. It is not recommended to attach an external feedback resistor in parallel to the crystal.

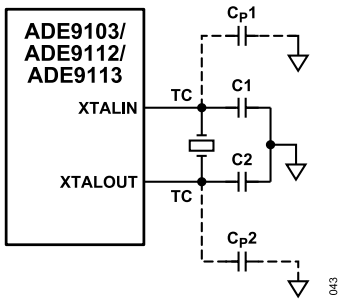

Figure 43. Crystal Circuitry

APPLICATIONS INFORMATION

Crystal Selection

A 16.384 MHz crystal with a critical transconductance, $gm_{CRITICAL}$, which is 5 times smaller than the minimum transconductance specification, g_m, in Table 2 can be connected across the XTALIN and XTALOUT pins to provide a clock source for the ADE9103/ADE9112/ADE9113. The term $gm_{CRITICAL}$ is defined as the minimum gain required to start the crystal oscillator circuit, expressed in mA/V, and found with Equation 3.

$$gm_{CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK})^2 \times (C_0 + C_L)^2 \quad (3)$$

where:
ESR_{MAX} is the maximum ESR, expressed in ohms.
f_{CLK} is 16.384 MHz expressed in Hz as 16.384 x 10^6.
C_0 is the maximum shunt capacitance, expressed in farads.
C_L is the load capacitance, expressed in farads.

The figures ESR_{MAX}, C_0, and C_L are provided by the manufacturer of the crystal in the associated component data sheet. Crystals with low ESR and smaller load capacitance have a lower $gm_{CRITICAL}$ and are easier to drive.

Load Capacitor Calculation

Crystal manufacturers specify the combined load capacitance across the crystal, C_L. The capacitances across the crystal are shown in Figure 43 can be described as follows:

- C_{P1} and C_{P2}: parasitic capacitances on the clock pins formed due to printed circuit board (PCB) traces.
- C_{IN1} and C_{IN2}: internal capacitances of the XTALIN and XTALOUT pins respectively and provided in Table 2.
- C_1 and C_2: selected load capacitors to get the correct combined C_L for the crystal.

The combined load capacitance, C_L, at the XTALIN and XTALOUT pins is

$$C_L = \frac{(C_1 + C_{P1} + C_{IN1}) \times (C_2 + C_{P2} + C_{IN2})}{C_1 + C_{P1} + C_{IN1} + C_2 + C_{P2} + C_{IN2}} \quad (4)$$

Keep the total capacitance on both the XTALIN pin and XTALOUT pin equal. Layout the crystal circuitry such that $C_{P1} = C_{P2}$. Select load capacitors such that $C_1 = C_2$.

$$C_1 + C_{P1} + C_{IN1} = C_2 + C_{P2} + C_{IN2} \quad (5)$$

Using Equation 4 and Equation 5, the values of C_1 and C_2 can be calculated.

POWER-UP AND INITIALIZATION PROCEDURES

At power-up or after a hardware or software reset, the following steps must be executed for a microcontroller managing a system formed by one or multiple ADE9103 or ADE9112 or ADE9113 devices.

Power-Up Procedure for Systems with a Single Device

For one standalone ADE9103/ADE9112/ADE9113 device managed by a microcontroller and clocked by a crystal, the power-up procedure is as follows (see Figure 44):

1. Connect a crystal between the XTALIN and XTALOUT pins with appropriate load capacitance.
2. Supply VDD to the ADE9103/ADE9112/ADE9113 device. To ensure that the ADE9103/ADE9112/ADE9113 device starts functioning correctly, the supply must reach 3.3 V − 10% in less than 16 ms from approximately a 2.5 V level. The ADE9103/ADE9112/ADE9113 device then starts to function.
3. The DC-to-DC converter powers up and supplies the isolated side of the ADE9112 and ADE9113. The Σ-Δ modulators then become functional. This process takes approximately 62 ms to execute when the recommended capacitors on the VDD_{ISO}, ALDOOUT, and REFOUT pins described in Table 12 are used. After this time, the isolated side of the ADE9112 and ADE9113 is fully functional. While the ADE9103 has no isolation and is entirely powered by VDD, the power-up timing remains the same.
4. To determine when the ADE9103/ADE9112/ADE9113 device is ready to accept commands, read the STATUS0 register until Bit 5 (RESET_DONE) is set to 1, which happens approximately 32 ms after the ADE9103/ADE9112/ADE9113 start to function and indicates that the nonisolated side of the ADE9103/ADE9112/ADE9113 is fully functional and using the default settings.
5. Initialize the registers required.
6. Set the WR_LOCK register to 0xD4 to protect the user accessible and internal configuration registers. See the Protecting the Integrity of Configuration Registers section.
7. When the ADC conversion data is available, the ADE9103/ADE9112/ADE9113 set the STATUS0 register, Bit 4 (COMM_UP), and begin generating a signal that is active low at the CLKOUT/$\overline{\text{DREADY}}$ pin for 256 XTALIN cycles (15.625 µs for XTALIN = 16.384 MHz). $\overline{\text{DREADY}}$ functionality is enabled by default at the CLKOUT/$\overline{\text{DREADY}}$ pin.

The microcontroller reads the I_WAV, V1_WAV V2_WAV, STATUS0, and STATUS1 registers as well as the CRC of the response packet during every long SPI transaction. For information on SPI burst mode, see the SPI Long Format Operation section for more information.

APPLICATIONS INFORMATION

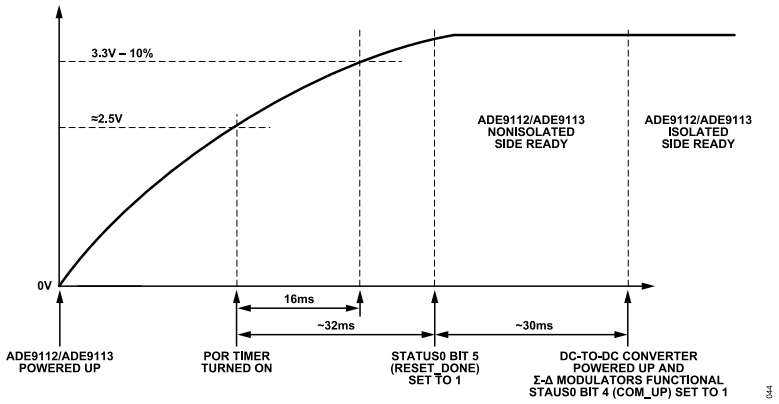

Figure 44. Power-Up Procedure for Systems with One or Multiple ADE9112 and ADE9113 Devices, Each Clocked from the Crystal

APPLICATIONS INFORMATION

Power-Up Procedure for Systems with Multiple Devices That Use a Single Crystal

For the polyphase energy meters detailed in the Polyphase Energy Meters section, in which, one single crystal is used, the power-up procedure is as follows (see Figure 45):

1. Supply VDD to the ADE9103/ADE9112/ADE9113 devices. To ensure that the Phase A ADE9112/ADE9113 (shown as $ADE9112_A$/$ADE9113_A$ in Figure 45) device starts functioning correctly, the supply must reach 3.3 V − 10% in less than 16 ms from approximately a 2.5 V level. The $ADE9112_A$/$ADE9113_A$ device is clocked by the 16.384 MHz crystal and then starts functioning. The other ADE9103/ADE9112/ADE9113 devices are not clocked yet.
2. The DC-to-DC converter powers up and supplies the isolated side of the $ADE9112_A$/$ADE9113_A$. The Σ-Δ modulators then become functional. This process takes approximately 62 ms to execute when the recommended capacitors on the VDD_{ISO}, ALDOOUT, and REFOUT pins described in Table 12 are used. After this time, the isolated side of the $ADE9112_A$/$ADE9113_A$ is fully functional.
3. To determine when the $ADE9112_A$/$ADE9113_A$ device is ready to accept commands, the STATUS0 register is read until Bit 5 (RESET_DONE) is set to 1, which happens approximately 32 ms after the $ADE9112_A$/$ADE9113_A$ start to function and indicates that the controller side of the $ADE9112_A$/$ADE9113_A$ is fully functional using the default settings.
4. Initialize the CONFIG0 register of the $ADE9112_A$/$ADE9113_A$ with Bit 0 (CLKOUT_EN) set to 1. The CLKOUT signal is provided at the CLKOUT/$\overline{DREADY}$ pin, and the ADE9103/ADE9112/ADE9113 devices on the other phases are now clocked.
5. The DC-to-DC converters of the otherADE9112 and ADE9113 devices power up and supply their isolated sides. The Σ-Δ modulators then become functional. This process takes approximately 62 ms to execute when the recommended capacitors on the VDD_{ISO}, ALDOOUT, and REFOUT pins described in Table 12 are used. The isolated sides of the ADE9112 and ADE9113 devices are now fully functional. While the ADE9103 has no isolation and is entirely powered by VDD, the power-up timing remains the same.
6. Read the STATUS0 registers of the remaining ADE9103/ADE9112/ADE9113 devices until Bit 5 (RESET_DONE) is set to 1, indicating that their nonisolated sides are fully functional with default settings, which happens approximately 32 ms after the clock signal is provided.
7. Initialize any registers of all remaining ADE9103/ADE9112/ADE9113 devices. Select one ADE9112/ADE9113 device (Phase C, for example, $ADE9112_C$/$ADE9113_C$ in Figure 45) and connect the CLKOUT/$\overline{DREADY}$ pin to an external interrupt input and output pin of the microcontroller. $ADE9112_C$/$ADE9113_C$ must have Bit 0 (CLKOUT_EN) in the CONFIG0 register left at the default value of 0 to use the $\overline{DREADY}$ functionality of the CLKOUT/$\overline{DREADY}$ pin.
8. Execute a SYNC_SNAP = 0x02 write broadcast to synchronize all the ADE9103/ADE9112/ADE9113 devices of the meter (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section).
9. Execute a WR_LOCK = 0xD4 write broadcast to protect the configuration registers of all ADE9103/ADE9112/ADE9113 devices. See the Protecting the Integrity of Configuration Registers section.

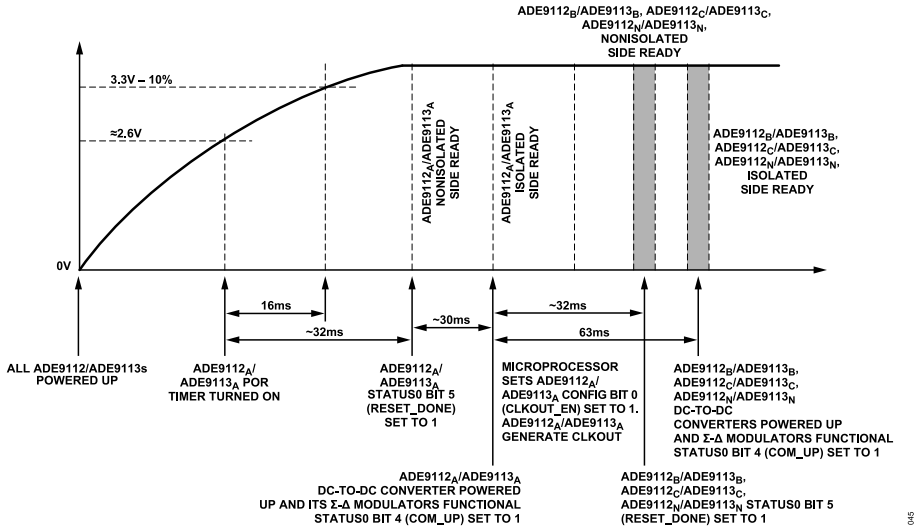

Figure 45. Power-Up Procedure for Systems with Multiple Devices; Only Phase A $ADE9112_A$/$ADE9113_A$ Is Clocked from a Crystal

APPLICATIONS INFORMATION

Power-Up Procedure for Systems with Multiple Devices That Use a Clock Signal Generated from a Microcontroller

For polyphase energy meters in which the microcontroller generates the clock signal used by all ADE9103/ADE9112/ADE9113 devices, the power-up procedure is as follows:

1. Supply VDD to the ADE9103/ADE9112/ADE9113 devices. To ensure that the ADE9103/ADE9112/ADE9113 devices start functioning correctly, the supply must reach 3.3 V − 10% in less than 16 ms from approximately a 2.5 V level.
2. Generate the clock signal from the microcontroller to all ADE9103/ADE9112/ADE9113 devices.
3. The DC-to-DC converters power up and supply the isolated side of the ADE9112/ADE9113 devices. The Σ-Δ modulators then become functional. This process takes approximately 62 ms to execute when the recommended capacitors on the VDD_{ISO}, LDO, and REFOUT pins described in Table 12 are used. After this time, the isolated sides of the ADE9112/ADE9113 devices are fully functional. While the ADE9103 has no isolation and is entirely powered by VDD, the power-up timing remains the same.
4. Read the STATUS0 registers of the ADE9103/ADE9112/ADE9113 devices until Bit 5 (RESET_DONE) is set to 1, indicating that the nonisolated side of the ADE9103/ADE9112/ADE9113 devices is fully functional with default settings, which happens approximately 32 ms after the clock signal is provided.
5. Initialize the CONFIG0 register of the ADE9103/ADE9112/ADE9113 devices with Bit 0 (CLKOUT_EN) cleared to 0 to avoid generating an unnecessary clock at the CLKOUT/$\overline{\text{DREADY}}$ pin. Select one ADE9112/ADE9113 device (Phase C, for example, $ADE9112_C$/$ADE9113_C$) and connect the CLKOUT/$\overline{\text{DREADY}}$ pin to an external interrupt input and output pin of the microcontroller.
6. Execute a SYNC_SNAP = 0x02 broadcast to synchronize all the ADE9103/ADE9112/ADE9113 devices of the meter (see the Synchronizing Multiple ADE9103/ADE9112/ADE9113 Devices section for more information).
7. Execute a WR_LOCK = 0xD4 write broadcast to protect the configuration registers of all ADE9103/ADE9112/ADE9113 devices. See the Protecting the Integrity of Configuration Registers section.

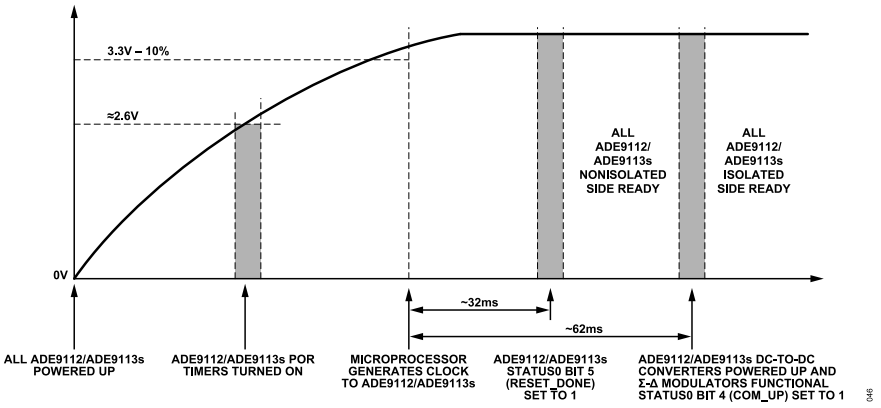

Figure 46. Power-Up Procedure for Systems with Multiple ADE9112/ADE9113 Devices Clocked from a Microcontroller

APPLICATIONS INFORMATION

SPI COMPATIBLE COMMUNICATION

The SPI port of the ADE9103/ADE9112/ADE9113 is a subordinate device of the main communication device on the SPI bus. The interface consists of SCLK, MOSI, MISO, and $\overline{CS}$ signals. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. The maximum and minimum serial clock frequencies supported by this interface are specified by the SCLK Frequency, f_{SCLK}, parameter in Table 3.

The $\overline{CS}$ logic input is the chip select input. Drive the $\overline{CS}$ input low for the entire data transaction. Each SPI transaction consists of a response to the previous command of up to 16 bytes on the MISO logic and a command packet as the last 4 bytes of the transaction on the MOSI logic. The response has both a long format, described in SPI Long Format Operation, and a short format, described in SPI Short Format Operation, as specified by the command packet. The most significant bits of the word are shifted in and out first during both long and short format operations.

Data transmission to and from the SPI port of the ADE9103/ADE9112/ADE9113 is protected by bidirectional CRC. An 8-bit CRC is required to be transmitted by the main communication device as Bits[7:0] of the command packet. An incorrect CRC results in an error. The error response can be disabled in the CONFIG0 register. More details on the CRC calculation can be found in CRC of Command Packet. Details of the 16-bit CRC sent by the ADE9103/ADE9112/ADE9113 in the response can be found in the CRC of Response Packet section.

ADE9103/ADE9112/ADE9113 devices may be connected independently as those shown in Figure 39 or in daisy chain, as shown in Figure 38. There is no configuration required to indicate whether each ADE9103/ADE9112/ADE9113 device is being addressed individually or as a member of a daisy chain. Individually addressed devices may be issued both 32 bit short, 48 bit short and 128 bit long format commands. Devices connected in daisy chain must be issued commands only in the 128 bit long format. The full SPI transaction length for daisy chain connected devices must be exactly 128 bits multiplied by the number of daisy chain connected devices.

The SPI port of each ADE9103/ADE9112/ADE9113 device interprets the last 32 bits received by the MOSI shift register only at the instant the $\overline{CS}$ pin transitions high. Read and write command responses are given in the next SPI response. The CMD ECHO byte of SPI read and write responses echos the characteristics of the command. The RWB indicates if the command was read or write. The long bit indicates if the command was long or short format. The RSRVD bits are reserved and wll be masked. SPI_CRC_ERR is a flag bit that indicates a CRC error was encountered in the previous SPI command decode when set to 1. The IRQ flag bit indicates a pending interrupt request when set to 1.

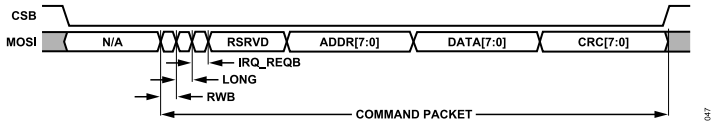

Figure 47. SPI Command Packet Structure

LONG READ	CMD ECHO	I_WAV[23:0]	STATUS0	V1_WAV[23:0]	STATUS1	V2_WAV[23:0]	DATA (ADDR + 1)	DATA (ADDR)	CRC_CCIT
LONG WRITE	CMD ECHO	I_WAV[23:0]	STATUS0	V1_WAV[23:0]	STATUS1	V2_WAV[23:0]	WR_ADDR	RD_DATA	CRC_CCIT

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Figure 48. SPI Long Read and Write Response

APPLICATIONS INFORMATION

SPI Long Format Operation

Every long format operation consists of a 128-bit response on the MISO data line. Every transaction regardless of read or write includes the command response, STATUS0, STATUS1, I_WAV, V1_WAV, V2_WAV, and CRC_CCITT. The remaining bits are dependent on whether the previous command was a read or a write. See Table 13 for details. Long format SPI transactions are required when using the daisy-chain SPI configuration.

The read operation using the ADE9103/ADE9112/ADE9113 SPI is initiated when the main sets the $\overline{CS}$ pin low and begins outputting the SCLK signal. The main transmits the command packet on the last 32 clock cycles of the transaction. The bit composition of the command packet is shown in Table 13. Bit 31 (R/$\overline{W}$) determines the type of operation. For a read, R/$\overline{W}$ must be set to 1. For a write, R/$\overline{W}$ must be cleared to 0. Bit 30 (LONG) determines the size of the response on the next operation. For a long format response, LONG must be set to 1. For a short format response, LONG must be cleared to 0. Bits[29:24] are unused and must be set to 0x00. Bits[23:16] (ADDR) represent the address of the register to be read or written. The ADE9103/ADE9112/ADE9113 SPI samples data on the low to high transitions of SCLK. During this operation, the MISO line contains the response to the previous command packet. After the main device completes 128 SCLK cycles, it sets the $\overline{CS}$ and SCLK lines high, and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. During the following transaction, the ADE9103/ADE9112/ADE9113 line outputs its 128-bit read response on MISO. This operation contains the data read in ADDR as well as ADDR + 1. Figure 49 shows a long format read operation followed by the response.

The write operation using the ADE9103/ADE9112/ADE9113 SPI is initiated when the main sets the $\overline{CS}$ pin low and begins outputting the SCLK signal. The main transmits the command packet on the last 32 clock cycles of the transaction. R/$\overline{W}$ must be cleared to 0. LONG must be set to 1. ADDR represents the address of the register to be read or written. DATA represents the data to be written into the address in ADDR. The ADE9103/ADE9112/ADE9113 SPI samples data on the low to high transitions of SCLK. During this operation, the MISO line contains the response to the previous command packet. After the main device completes 128 SCLK cycles, it sets the $\overline{CS}$ and SCLK lines high, and the communication ends. The data lines, MOSI and MISO, go into a high impedance state, and the write completes with a single operation. During the following transaction, the ADE9103/ADE9112/ADE9113 line outputs its 128-bit write response on MISO. This response includes a read back of the address written to on the previous operation. See Figure 50 for details of the SPI write operation.

Table 13. Command Byte for SPI Read/Write Operations

Bit Field Location	Bit Field Name	Description
31	R/$\overline{W}$	Set this bit to 1 if an SPI read operation is executed. Clear this bit to 0 if an SPI write operation is executed.
30	LONG	Set this bit to 1 for a long frame structure. Set this bit to 0 for a short frame structure.
[29:24]	RSRVD	Program to 0x00.
[23:16]	ADDR	Address of the register to be read or written.
[15:8]	DATA	Data payload if a write operation is executed.
[7:0]	CRC	CRC calculation over Bits[31:8].

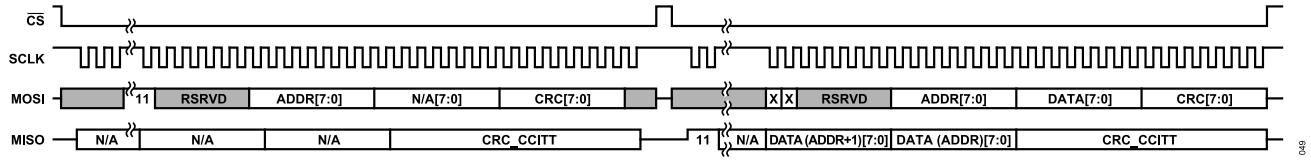

Figure 49. Long Format Read SPI Transaction

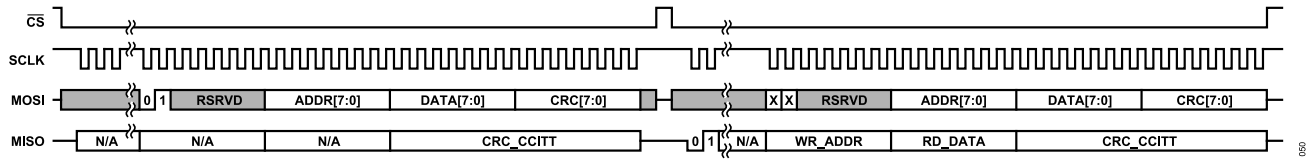

Figure 50. Long Format Write SPI Transaction

APPLICATIONS INFORMATION

Table 14. SPI Long Format Read Response

Bits	Details
[127]	CMD ECHO, RWB = 1
[126]	CMD ECHO, LONG = 1
[125:122]	CMD ECHO, RSRVD
[121]	CMD ECHO, SPI_CRC_ERR
[120]	CMD ECHO, IRQ
[119:96]	I_WAV
[95:88]	STATUS0
[87:64]	V1_WAV
[63:56]	STATUS1
[55:32]	V2_WAV
[31:24]	DATA (ADDR + 1)
[23:16]	DATA (ADDR)
[15:0]	CRC_CCITT

Table 15. SPI Long Format Write Response

Bits	Details
[127]	CMD ECHO, RWB = 0
[126]	CMD ECHO, LONG = 1
[125:122]	CMD ECHO, RSRVD
[120]	CMD ECHO, SPI_CRC_ERR
[127:120]	CMD ECHO, IRQ
[119:96]	I_WAV
[95:88]	STATUS0
[87:64]	V1_WAV
[63:56]	STATUS1
[55:32]	V2_WAV
[31:24]	WR_ADDR
[23:16]	RD_DATA
[15:0]	CRC_CCITT

APPLICATIONS INFORMATION

SPI Short Format Operation

A short format operation can consist of either 32 bits or 48 bits. The command packet is always the final 32 bits or 48 bits of the transaction on the MOSI data line. The command response is always the first 8 bits of the MISO data line. The CRC_CCITT is the final 16 bits only when the main transmits 48 cycles on SCLK. A short SPI transaction is only compatible with a dedicated SPI configuration because the daisy chain requires 128-bit responses.

The short format read operation using the ADE9103/ADE9112/ADE9113 SPI is initiated when the main sets the $\overline{CS}$ pin low and begins outputting the SCLK signal. Bit 31 (R/$\overline{W}$) must be set to 1. Bit 30 (LONG) must be cleared to 0. Bits[23:16] (ADDR) represent the address of the register to be read or written. The ADE9103/ADE9112/ADE9113 SPI samples data on the low to high transitions of SCLK. During this operation, the MISO line contains the response to the previous command packet. After the main device complete 32 SCLK cycles or 48 SCLK cycles, it sets the $\overline{CS}$ and SCLK lines high, and the communication ends. The MISO data lines are set to a high impedance state when $\overline{CS}$ is not asserted. During the following transaction, the ADE9103/ADE9112/ADE9113 line outputs its 32-bit or 48-bit read response on MISO. This operation contains the data in ADDR as well as ADDR + 1 as requested in the prior operation as well as STATUS0. See Figure 51 for details of the SPI short read operation.

In the case of reading any x_WAV_x register, STATUS0 is excluded, and all 24 bits of the x_WAV_x is used instead.

The short format write operation using the ADE9103/ADE9112/ADE9113 SPI is initiated when the main sets the $\overline{CS}$ pin low and begins outputting the SCLK signal. Bit 31 (R/$\overline{W}$) must be cleared to 0. Bit 30 (LONG) must be cleared to 0. Bits[23:16] (ADDR) represent the address of the register to be read or written. Bits[15:8] (DATA) represents the data to be written into the address in ADDR. The ADE9103/ADE9112/ADE9113 SPI samples data on the low to high transitions of SCLK. During this operation, the MISO line contains the response to the previous command packet. After the main device completes 32 SCLK cycles or 48 SCLK cycles, it sets the $\overline{CS}$ and SCLK lines high, and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. The write is completed with a single operation. During the following transaction, the ADE9103/ADE9112/ADE9113 line outputs its 32-bit or 48-bit write response on MISO. This response includes a readback of the address written to on the previous operation and STATUS0. See Figure 52 for details of the SPI short write operation.

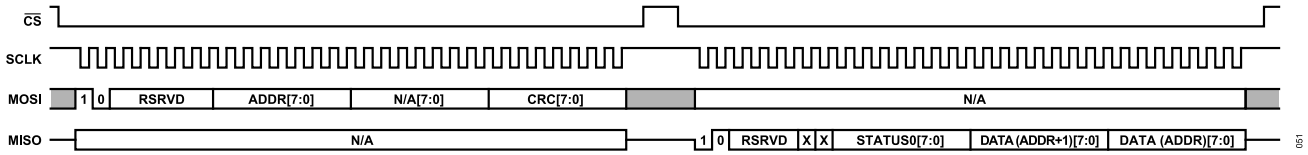

Figure 51. Short Format Read Transaction

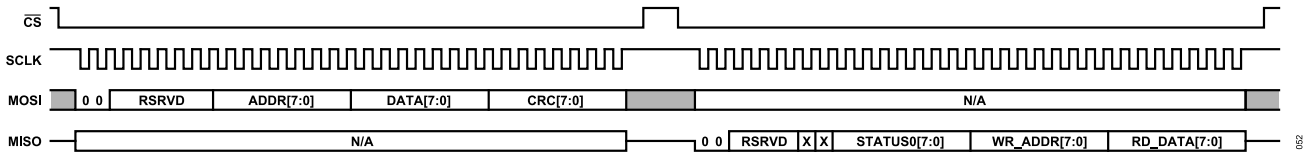

Figure 52. Short Format Write Transaction

APPLICATIONS INFORMATION

SPI Format Transitions

Using a dedicated SPI configuration, there are two SPI transaction lengths: a long or short. Within every command packet, the length of the following SPI transaction is defined as shown in Figure 47. The main communicating with the ADE9103/ADE9112/ADE9113 must keep track of what size the following SPI transaction is to output the appropriate number of SCLK pulses. A scenario during which there are transitions between long and short is as follows:

1. The first successful command received by the microcontroller unit (MCU) is long.
2. The MCU disables long.
3. The MCU performs all of its register initialization as short SPI transactions.
4. At the last initialization command, long is enabled, and the MCU waits for $\overline{\text{DREADY}}$ before reading the ADC samples.

Multiple Devices

Communicating with multiple ADE9103/ADE9112/ADE9113 can be accomplished through two methods: daisy chain and dedicated SPI. The method is determined by the hardware configuration of the ADE9103/ADE9112/ADE9113 and requires no additional configuration.

When using daisy chain, each SPI transaction must be exactly 128 bits multiplied by the number of connected ADE9103/ADE9112/ADE9113 devices. The entire transaction is shifted through the connected ADE9103/ADE9112/ADE9113 devices, and each device only interprets the command packet, which is the last 32 bits of the input on the MOSI data line at the instant that $\overline{\text{CS}}$ transition high. Each ADE9103/ADE9112/ADE9113 produces a 128-bit response, which is transmitted on MISO.

Daisy chain can consist between two and four ADE9112 and ADE9113 devices. Devices are numbered for timing diagram purposes, incrementing from zero from the main MOSI input. A generic transaction with four ADE9103/ADE9112/ADE9113 devices can be found in Figure 53.

While using the dedicated SPI method, each ADE9103/ADE9112/ADE9113 has its own dedicated $\overline{\text{CS}}$ logic. All ADE9103/ADE9112/ADE9113 devices share the MOSI and MISO data lines. Transactions can be either short or long. Communication for each individual ADE9103/ADE9112/ADE9113 functions the same way as when only a single device is in use. A generic transaction with four ADE9103/ADE9112/ADE9113 devices using dedicated SPI can be found in Figure 54.

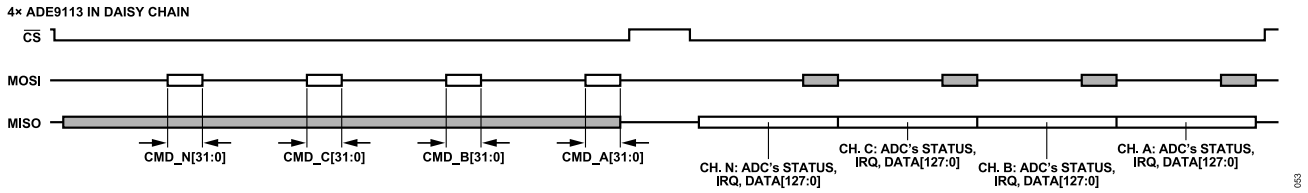

Figure 53. Multiple Devices - Daisy Chain

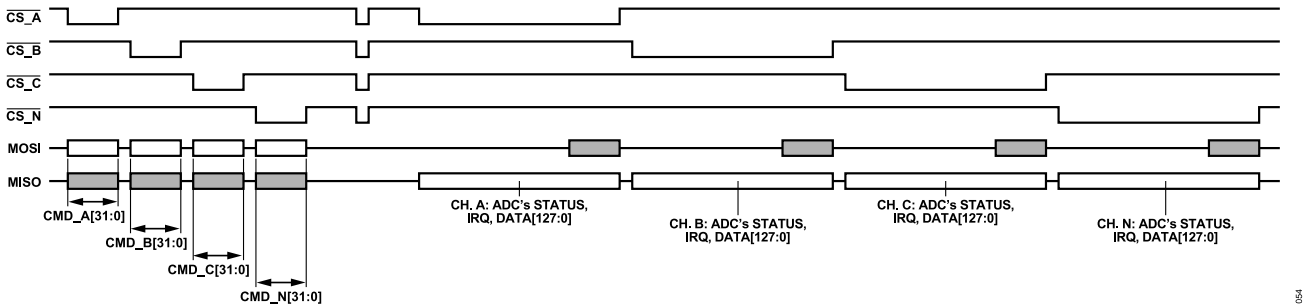

Figure 54. Multiple Devices - Dedicated SPI

APPLICATIONS INFORMATION

SPI Debug Features

The ADE9103/ADE9112/ADE9113 has two modes to aid in debugging the SPI communication: static and count mode. The two modes can be enabled by writing to Bits[3:2], STREAM_DBG, in the CONFIG0 register. In static mode, the ADC registers become static and hold their value until they are written to. The register values can be read as usual through either short or long SPI transactions. To write and hold a value to the ADC registers, take the following steps:

1. Set STREAM_DBG equal to count mode (10b).
2. Wait for $\overline{\text{DREADY}}$.
3. Write the desired values to the ADC register before the next $\overline{\text{DREADY}}$.
4. Set STREAM_DBG equal to static mode (01b).

By outputting a known ADC value with every transaction, a user can verify that the data is being transmitted properly.

The count mode increments the values inside the ADC registers at the ADC conversion rate that is configured in Bits[2:0], DATAPATH_CONFIG, in the CONFIG_FILT register. This mode allows a user to verify their waveform streaming interface. By verifying that the read count is unbroken, the user can be assured that no data has been missed or duplicated. When entering count mode, the incrementing starts from the last value in the ADC registers. To enter count mode at a specific value, take the following steps:

1. Set STREAM_DBG equal to count mode (10b).
2. Wait for $\overline{\text{DREADY}}$.
3. Write the desired values to the ADC register before the next $\overline{\text{DREADY}}$.
4. On each following $\overline{\text{DREADY}}$ trigger, the ADC register values increment.

To exit either debug mode, set STREAM_DBG to normal mode.

Table 16. STREAM_DBG Bit Configuration

STREAM_DBG	Data Mode
00	Normal mode
01	Static mode
10	Count mode

CRC of Command Packet

The 8-bit CRC required in the command packet is calculated over Bits[31:8], has a polynomial of 0x7 as follows, an initial value of 0x0, and a final XOR of 0x55:

$x^8 + x^2 + x + 1$

For example, a write command to disable the CRC_EN_SPI_WRITE bit in the CONFIG0 register sends the following data on the MOSI line: 0x40 02 00 F9, where 0xF9 is the CRC.

The ADE9103/ADE9112/ADE9113 calculates the CRC after every calculation to verify successful communication. If the calculated CRC does not match the received CRC, the SPI_CRC_ERR bit (Bit 1) in STATUS0 is set, and the command is not processed. This behavior can be disabled by the CRC_EN_SPI_WRITE bit (Bit 1) in the CONFIG0 register.

CRC of Response Packet

Each response from the ADE9103/ADE9112/ADE9113 is protected by a CCITT-16 CRC with a polynomial of $x^{16} + x^{12} + x^5 + 1$, with an initial value of 0xffff, also known as CCITT-False, which ensures a nonzero output with zero input.

SYNCHRONIZING MULTIPLE ADE9103/ADE9112/ADE9113 DEVICES

There are two methods for clocking multiple ADE9103/ADE9112/ADE9113 which are described in the Power-Up and Initialization Procedures section. By initializing multiple ADE9103/ADE9112/ADE9113 as described, all devices are using the same clock frequency. To configure all ADE9103/ADE9112/ADE9113 devices in an energy meter and provide coherent ADC output samples obtained in the same output cycle, all ADE9103/ADE9112/ADE9113 devices must have the same ADC output frequency in addition to a shared clock frequency. The DATAPATH_CONFIG bits (Bits[2:0]) in the CONFIG_FILT register selects the ADC output frequency; therefore, they must be initialized to the same value (see the ADC Output Values section for more details).

To ensure the ADC outputs of all ADE9103/ADE9112/ADE9113 devices generate samples synchronously, the MCU can perform an ALIGN, which can be used in either dedicated SPI or daisy chain. Setting the PREP_BROADCAST = 1 sets the ADE9103/ADE9112/ADE9113 MISO pin to a high impedance state for the duration of the next SPI frame. For devices configured with dedicated SPI, set PREP_BROADCAST = 1 in the SYNC_SNAP register to prevent contention between multiple device outputs sharing the same signal. For devices configured in daisy-chain SPI, PREP_BROADCAST = 0 in the SYNC_SNAP register.

The ADE9103/ADE9112/ADE9113 contains an internal 14-bit counter that functions at the XTALIN frequency. The counter is synchronized with the ADC output period and the CLKOUT/$\overline{\text{DREADY}}$ pin. When a new output period starts, the counter starts decreasing from a value determined by the DATAPATH_CONFIG bits in the CONFIG_FILT register. Table 17 details these values. Monitoring this counter enables the user to observe if any ADE9103/ADE9112/ADE9113 device is out of sync.

APPLICATIONS INFORMATION

Table 17. Counter Initial Values as a Function of DATAPATH_CONFIG Bits

Bits[2:0], DATAPATH_CONFIG, in CONFIG_FILT Register	ADC Output Frequency (kHz) (XTALIN = 16.384 MHz)	Counter C_0 Initial Value
000	32	511
001		
010		
011	8	2047
100		
101	4	4095
110	2	8191
111	1	16383

The value of the counter is latched on the first falling $\overline{CS}$ edge after either ALIGN or SNAPSHOT are set in the SYNC_SNAP register. A broadcast write to all ADE9103/ADE9112/ADE9113 devices ensures that all the counters of every ADE9103/ADE9112/ADE9113 are latched at the same moment. The ALIGN or SNAPSHOT bit clears itself to 0 after one XTALIN cycle. The values of the counters offer a measure of the ADC output synchronization across all ADE9103/ADE9112/ADE9113 devices. Ideally, the values must be perfectly equal, indicating that all ADE9103/ADE9112/ADE9113 devices are fully synchronized. In reality, due to the uncertainty between the SPI clock generated by the MCU and the ADE9103/ADE9112/ADE9113 XTALIN, a ±1 count difference between counters is acceptable. The 14-bit counter is accessed via two 8-bit registers SNAPSHOT_COUNT_HI and SNAPSHOT_COUNT_LO as seen in Figure 55.

If the internal counter of one of the ADE9103/ADE9112/ADE9113 devices does not have a value correlated with the values of the counters of any the other ADE9103/ADE9112/ADE9113, then the ADC outputs of one device are no longer synchronized with the ADC outputs from the others. The ADE9103/ADE9112/ADE9113 provides a method to resynchronize all the ADE9103/ADE9112/ADE9113 devices through ALIGN. To perform ALIGN with a daisy-chain SPI configuration, take the following steps:

1. Write to SYNC_SNAP of all ADE9103/ADE9112/ADE9113 devices to prepare for an ALIGN. Set PREP_BROADCAST = 0, ALIGN = 1, and SNAPSHOT = 0.
2. Toggle the $\overline{CS}$ signal of all ADE9103/ADE9112/ADE9113 devices simultaneously, which can be either a null SPI command with no SCLK toggles or part of a valid command.
3. Wait 3 cycles of $\overline{DREADY}$ for the update to take effect.

To perform an ALIGN using dedicated SPI, set PREP_BROADCAST = 1 during Step 1. When an ALIGN is performed, all phases present ADC output distortions. It is recommended that this command be executed at power-up or after a hardware or software reset to minimize impact on accuracy.

To only verify the counters of all devices using a daisy-chain SPI configuration, take the following steps:

1. Write to SYNC_SNAP of all ADE9103/ADE9112/ADE9113 devices to prepare for an ALIGN. Set PREP_BROADCAST = 0, ALIGN = 0, and SNAPSHOT = 1
2. Toggle the $\overline{CS}$ signal of all ADE9103/ADE9112/ADE9113 devices simultaneously, which can be either a null SPI command with no SCLK toggles or part of a valid command.
3. Read back the ADC synchronization counter via the SNAPSHOT_COUNT_HI and SNAPSHOT_COUNT_LO registers.
4. Compare values from each ADE9103/ADE9112/ADE9113 counter and ensure these values are within ±1 count difference between them.

If an ALIGN broadcast is performed while actively sampling instead of during the start-up procedure, it results in a discontinuity in the waveform samples impacting up to three samples. This discontinuity can result in up to a 0.1% error at half of the full-scale inputs during a RMS calculation. Synchronization typically only has to be performed at power up unless the SNAPSHOT_COUNT_HI and SNAPSHOT_COUNT_LO registers show more than a ±1 count difference. It is not recommended to continuously synchronize in a short period of time.

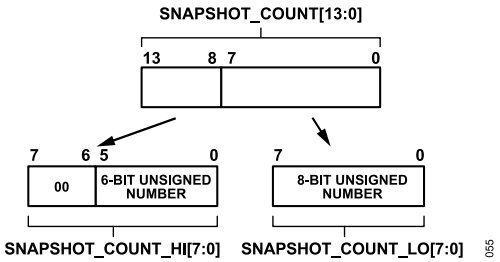

Figure 55. Counter Value Communicated Using Two 8-Bit Registers

POWER MANAGEMENT

DC-TO-DC CONVERTER

The DC-to-DC converter section of the ADE9112 and ADE9113 works on principles that are common to most modern power supply designs. The internal DC-to-DC converter of the ADE9112 and ADE9113 is supplied by the VDD pin and is continuously active as long as the $\overline{\text{RESET}}$ pin is not asserted. In normal operation, maintain VDD between 2.97 V and 3.63 V.

VDD power is supplied to an oscillating circuit that drives the primary side of a chip-scale air core transformer. Using another chip-scale air core transformer, a feedback circuit measures VDD_{ISO} and passes the information back into the VDD domain, where a pulse-width modulation (PWM) control block controls the AC source to maintain the floating VDD_{ISO} supply at 2.0 V as shown in Figure 56. This isolated voltage supply is then fed to the integrated 1.8 V LDO regulator at the AVDD pin.

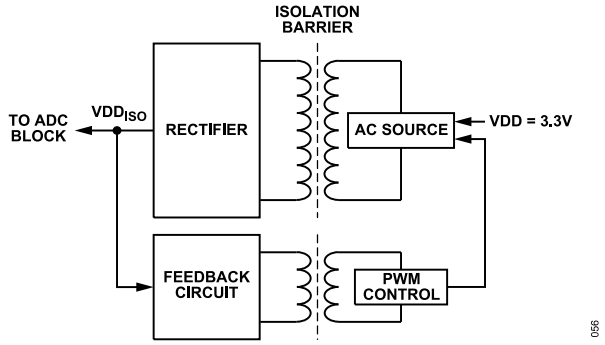

Figure 56. Isolated DC-to-DC Converter Block Diagram

During normal operations, the frequency of emissions is hopping between 300 MHz and 420 MHz as described in the EMI_CONFIG register (see Table 20). The EMI_CONFIG register offers four different modes for controlling the frequency spread of the AC source. The EMI_HI_LIMIT, EMI_MID_LIMIT, and EMI_LO_LIMIT are read only registers that contain the values that correspond to the frequency limits of 420 MHz, 360 MHz, and 300 MHz. The EMI_LO_MASK and EMI_HI_MASK allows frequencies to be removed from the sawtooth and ramp frequency sweeps. The range of removed frequencies is inclusive of EMI_LO_MASK and EMI_HI_MASK. The EMI_LO_LIMIT and EMI_HI_LIMIT registers can be used as a reference to calculate the desired values to mask. The equations to calculate the EMI_LO_LIMIT and EMI_HI_LIMIT for a desired frequency range using the EMI_LO_LIMIT and EMI_HI_LIMIT registers is as follow:

$$\text{EMI\_LO\_MASK} = \text{ROUNDUP}\left[\frac{\text{EMI\_LO\_LIMIT - EMI\_HI\_LIMIT}}{\text{300 MHz - 420 MHz}} \times (f_{LO\_MASK}\text{-300 MHz}) + \text{EMI\_LO\_LIMIT}\right] \quad (6)$$

$$\text{EMI\_HI\_MASK} = \text{ROUNDDOWN}\left[\frac{\text{EMI\_LO\_LIMIT - EMI\_HI\_LIMIT}}{\text{300 MHz - 420 MHz}} \times \left(f_{HI\_MASK}\text{-300 MHz}\right) + \text{EMI\_LO\_LIMIT}\right] \quad (7)$$

POWER MANAGEMENT

When EMI_LO_MASK = EMI_HI_MASK, the frequency masking is disabled. As shown in Figure 57, a smaller value in the EMI_LO_MASK or EMI_HI_MASK corresponds to a higher frequency and a larger value corresponds to a lower frequency. When a new value is written into EMI_LO_MASK or EMI_HI_MASK, the ongoing ramp is not interrupted. The new value is loaded when the sawtooth reverts to the minimum or maximum or when the ramp changes directions. To prevent any errors, avoid the following scenarios:

1. The value written to EMI_LO_MASK being less than EMI_HI_MASK.
2. EMI_LO_MASK is equal to EMI_LO_LIMIT, and EMI_HI_MASK is equal to EMI_HI_LIMIT.

During these scenarios, the emissions are no longer a spread spectrum but a single tone at 360 MHz, which leads to stronger emissions that are more difficult to manage in the PCB layout.

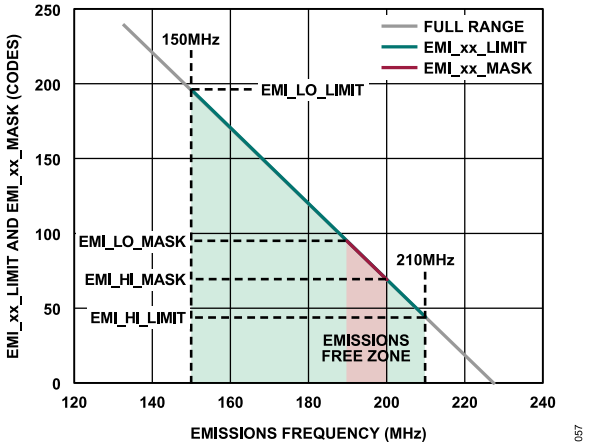

Figure 57. Available Frequency Range with Masking Enabled

Table 18. Address 0x009, EMI_CONFIG, Bits[2:0], Electromagnetic Interference (EMI) Frequency Hopping Selection

Bits[2:0]	Mode	Description
000	Sawtooth frequency rising	The frequency starts at the low limit, ramps up to the high limit, and then returns to the low limit.
001	Sawtooth frequency falling	Frequency starts at the high limit, ramps down to the low limit, and then returns to the high limit.
010	Ramp	Frequency ramps up and down between the low and high limit.
011	Random hopping frequency (default)	Frequency randomly hops around the 360 MHz center frequency, which is the recommended mode.

SOFTWARE RESET

The SWRST register (Address 0x001) manages the software reset functionality. The default value of this register is 0x00. If this register is set to 0xD6, the ADE9103/ADE9112/ADE9113 enter the software reset state. In this state, all the internal registers are reset to their default values. The DC-to-DC converter continues to function. When the software reset ends, the SWRST register clears automatically to 0, and Bit 5 (RESET_DONE) in the STATUS0 register is set to 1. If the configuration registers are protected using a WR_LOCK = 0xD4 register write, first unlock the registers by writing WR_LOCK = 0x5E and then write 0xD6 to the SWRST register to start a software reset. At this point, one of the procedures described in the Power-Up and Initialization Procedures section must be followed to initialize the ADE9103/ADE9112/ADE9113.

HARDWARE RESET

The ADE9103/ADE9112/ADE9113 have a dedicated reset pin ($\overline{\text{RESET}}$). Hardware reset occurs when the $\overline{\text{RESET}}$ pin is brought low (default state is a weak pullup) for at least 1.5 µs.

During a hardware reset, all the registers are set to their default values, and the DC-to-DC converter and LDO regulators are shut down. This procedure can be done simultaneously for all ADE9103/ADE9112/ADE9113 devices in a polyphase energy meter. At the end of the reset period, the ADE9103/ADE9112/ADE9113 sets Bit 5 (RESET_DONE) to 1 in the STATUS0 register. At this point, one of the procedures described in the Power-Up and Initialization Procedures section must be followed to initialize the ADE9103/ADE9112/ADE9113 devices correctly.

POWER-DOWN MODE

There are situations in which the ADCs of the ADE9112 and ADE9113 are not required to function, and it is desirable to lower the current consumption of the device. Holding the $\overline{\text{RESET}}$ pin low forces low power mode. In low power mode, the VLDOOUT, crystal oscillator, and isolated power delivery are disabled.

$\overline{\text{RESET}}$ low on the ADE9103 sets only the digital block, SPI port, and the clocking to low power mode. However, the analog circuit blocks remain powered.

In systems with more than one ADE9103/ADE9112/ADE9113, the $\overline{\text{RESET}}$ pins are tied together to lower the total current of all the ADE9103/ADE9112/ADE9113.

LAYOUT GUIDELINES

For detailed information on the layout guidelines to follow when using the ADE9103/ADE9112/ADE9113, go to the ADE9113 product page.

ADE9113 EVALUATION BOARD

An evaluation board built upon the ADE9113 allows users to quickly evaluate this IC. It is used in conjunction with the system demonstration platform (EVAL-SDP-CB1Z) or an external MCU board. Users must order both the EVAL-ADE9113KTZ evaluation board and the system demonstration platform from the ADE9113 product page to evaluate the ADE9103, ADE9112 and/or ADE9113. The features of the ADE9113 are similar to the ADE9103 and ADE9112; therefore, the EVAL-ADE9113KTZ can be used to evaluate all three ICs.

HARDWARE IDENTIFIERS

VERSION_PRODUCT Address 0x07E identifies the version of the ADE9103/ADE9112/ADE9113, SILICON_REVISION Address 0x07D identifies the version of the ADE9103/ADE9112/ADE9113, and UNIQUE_PART_ID_x Address 0x075 to Address 0x07A identify the ID of the ADE9103/ADE9112/ADE9113.

The UNIQUE_PART_ID_5 to UNIQUE_PART_ID_0 registers are a 48-bit unique ID number for each device, which enables traceability of all devices even after these devices are deployed.

REGISTER SUMMARY

In Table 19, R means a register can be read, W means a register can be written, and W1C means write 1 to clear.

Table 19. Register Summary

Address	Name	Description	Default Value	Access
0x001	SWRST	Software Reset.	0x00	W
0x002	CONFIG0	ADC Configuration.	0x02	R/W
0x003	CONFIG_FILT	Digital Filter Configuration.	0x00	R/W
0x005	CONFIG_ISO_ACC	Enable Access to Isolated (ISO) Register Space. The ISO side is Pin 1 to Pin 14.	0x00	R/W
0x006	CRC_RESULT_HI	Background Register Map CRC Most Significant Byte.	0xDD	R
0x007	CRC_RESULT_LO	Background Register Map CRC Least Significant Byte.	0x8D	R
0x008	EFUSE_REFRESH	eFuse Refresh.	0x00	R/W
0x009	EMI_CONFIG	Configure Isolation Frequency Hopping Method.	0x03	R/W
0x00A	EMI_HI_MASK	Emissions Mask, High Frequency Bounds.	0x00	R/W
0x00B	EMI_LO_MASK	Emissions Mask, Low Frequency Bounds.	0x00	R/W
0x00C	EMI_HI_LIMIT	Factory Stored High Frequency Limit. Corresponds to emissions at 420 MHz.	0x00	R
0x00D	EMI_MID_LIMIT	Factory Stored Center Frequency Value. Corresponds to emissions at 360 MHz.	0x00	R
0x00E	EMI_LO_LIMIT	Factory Stored Low Frequency Limit. Corresponds to emissions at 300 MHz.	0x00	R
0x00F	MASK0	Interrupt Mask 0 Register. Mask register for STATUS0.	0x00	R/W
0x010	MASK1	Interrupt Mask 1 Register. Mask register for STATUS1.	0x00	R/W
0x011	MASK2	Interrupt Mask 2 Register. Mask register for STATUS2.	0x10	R/W
0x012	CONFIG_ZX	Zero-Crossing Configuration.	0x00	R/W
0x013	SCRATCH	Software Debug Register for Testing SPI R/W.	0x00	R/W
0x014	SYNC_SNAP	ADC Synchronization Register.	0x00	R/W
0x017	SNAPSHOT_COUNT_HI	System Timing Controller Counter Most Significant Byte.	0x00	R
0x018	SNAPSHOT_COUNT_LO	System Timing Controller Counter Least Significant Byte.	0x00	R
0x01F	WR_LOCK	Configuration Lock Register.	0x5E	R/W
0x020	STATUS0	Latched Status of High Priority Interrupts.	0x00	R/W
0x021	STATUS1	Latched Status of Low Priority Interrupts.	0x00	R/W
0x022	STATUS2	Latched Status of Isolated ADC Interrupts.	0x00	R/W
0x023	COM_FLT_TYPE	ISO to NONISO Communications Fault Type.	0x00	R
0x024	COM_FLT_COUNT	ISO to NONISO Communications Fault Count.	0x00	R
0x025	CONFIG_CRC	Configuration of Background Register Map CRC.	0x00	R/W
0x026	I_WAV_HI	Current Channel Waveform Data Most Significant Byte.	0x00	R/W
0x027	I_WAV_MD	Current Channel Waveform Data Middle Byte.	0x00	R/W
0x028	I_WAV_LO	Current Channel Waveform Data Least Significant Byte.	0x00	R/W
0x029	V1_WAV_HI	V1 Channel Waveform Data Most Significant Byte.	0x00	R/W
0x02A	V1_WAV_MD	V1 Channel Waveform Data Middle Byte.	0x00	R/W
0x02B	V1_WAV_LO	V1 Channel Waveform Data Least Significant Byte.	0x00	R/W
0x02C	V2_WAV_HI	V2 Channel Waveform Data Most Significant Byte.	0x00	R/W
0x02D	V2_WAV_MD	V2 Channel Waveform Data Middle Byte.	0x00	R/W
0x02E	V2_WAV_LO	V2 Channel Waveform Data Least Significant Byte.	0x00	R/W
0x075	UNIQUE_PART_ID_5	Unique Part ID Most Significant Byte (Byte 5).	0x00	R
0x076	UNIQUE_PART_ID_4	Unique Part ID Byte 4.	0xXX[1]	R
0x077	UNIQUE_PART_ID_3	Unique Part ID Byte 3.	0xXX[1]	R
0x078	UNIQUE_PART_ID_2	Unique Part ID Byte 2.	0xXX[1]	R
0x079	UNIQUE_PART_ID_1	Unique Part ID Byte 1.	0xXX[1]	R
0x07A	UNIQUE_PART_ID_0	Unique Part ID Least Significant Byte (Byte 0).	0xXX[1]	R
0x07D	SILICON_REVISION	Revision Value of ISO and NONISO Silicon.	0x32[2]	R
0x07E	VERSION_PRODUCT	Product Version Identifier.	0x00	R

REGISTER SUMMARY

Table 19. Register Summary (Continued)

Address	Name	Description	Default Value	Access
0x0CC	DC_OFFSET_MODE	Enable the Current Channel Input Short.	0x00	R/W

[1] The default value is unique to every individual IC.

[2] Subject to change with each silicon revision.

REGISTER DETAILS

Table 20. Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x001	SWRST	[7:0]	SWRST		Software Reset.	0x0	W
				0xD6	Software Reset Command. The software resets all registers to their default values. Power cycling the device may be required to correct hardware functionality.		
0x002	CONFIG0	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	STREAM_DBG		Stream Debug. Stream debug mode allows configuration of the x_WAV_x ADC output registers to simplify the debugging of the communication interface.	0x0	R/W
				00	Normal Mode. The x_WAV_x registers contain the ADC results.		
				01	Static Mode. The x_WAV_x registers are static and hold their value. The x_WAV_x registers can be written to change to a new value. The x_WAV_x registers become static and hold their value until a register write is performed to the x_WAV_x register with a new value. Programming must first be enabled with the count mode. setting before this static mode functions.		
				10	Count Mode. Data Increments at ADC Conversion Rate. Enables write access to x_WAV_x registers and increments the x_WAV_x register with every $\overline{\text{DREADY}}$ pulse.		
				11	Reserved. Same operation as normal mode.		
		1	CRC_EN_SPI_WRITE		Enables CRC Check on SPI Writes.	0x1	R/W
		0	CLKOUT_EN		CLKOUT Enable. Set this bit to 1 to enable CLKOUT when the device is providing the clock to the remaining ADE9103/ADE9112/ADE9113 devices. Clear this bit to 0 if receiving an external clock, in which case, the pin is $\overline{\text{DREADY}}$.	0x0	R/W
0x003	CONFIG_FILT	7	RESERVED		Reserved.	0x0	R
		6	V2_ADC_INVERT		Invert V2 Channel Inputs. The invert bit can be used to correct for a sensor output connected up backwards.	0x0	R/W
		5	V1_ADC_INVERT		Invert V1 Channel Inputs. See the V2_ADC_INVERT description.	0x0	R/W
		4	I_ADC_INVERT		Invert Current Channel Inputs. See the V2_ADC_INVERT description.	0x0	R/W
		3	LPF_BW		Filter Bandwidth Configuration. Selects the bandwidth of the digital LPF of the ADC. See the Analog-to-Digital Conversion section for details on how the ADC output frequency influences the bandwidth selection.	0x0	R/W
				1	Bandwidth of 2.7 kHz at 8 kSPS output data rate.		
				0	Bandwidth of 3.3 kHz at 8 kSPS output data rate.		
		[2:0]	DATAPATH_CONFIG		Digital Signal Processing Configuration.	0x0	R/W
				000	Sinc3, 32 kHz Sampling.		
				001	Sinc3, LPF Enabled, 32 kHz Sampling.		
				010	Sinc3, Compensation Enabled, LPF Enabled, 32 kHz Sampling.		
				011	Sinc3, LPF Enabled, 8 kHz Sampling.		
				100	Sinc3, Compensation Enabled, LPF Enabled, 8 kHz Sampling.		
				101	Sinc3, LPF Enabled, 4 kHz Sampling.		
				110	Sinc3, LPF Enabled, 2 kHz Sampling.		
				111	Sinc3, LPF Enabled, 1 kHz Sampling.		
0x005	CONFIG_ISO_ACC	[7:1]	RESERVED		Reserved.	0x0	R
		0	ISO_WR_ACC_EN		Enable Write Access to DC_OFFSET_MODE Register.	0x0	R/W
0x006	CRC_RESULT_HI	[7:0]	CRC_RESULT[15:8]		Register Map CRC.	0xDD	R
0x007	CRC_RESULT_LO	[7:0]	CRC_RESULT[7:0]		Register Map CRC.	0x8D	R
0x008	EFUSE_REFRESH	[7:1]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 20. Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	EFUSE_REFRESH		Forces a Refresh of the eFuse Memory. This bit can be used as a recovery method from a eFuse memory error without having to undertake the penalty of a hardware reset. This bit auto clears on completion of eFuse refresh.	0x0	R/W
0x009	EMI_CONFIG	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	EMI_CONFIG		EMI Frequency Hopping Selection. No functionality on the ADE9103.	0x3	R/W
				000	Sawtooth Frequency Rising. Frequency starts at frequency defined by EMI_LO_LIMIT and ramps to higher frequency as defined by EMI_HI_LIMIT and then returns to EMI_LO_LIMIT.		
				001	Sawtooth Frequency Falling. Frequency starts at frequency defined by EMI_HI_LIMIT and ramps to a lower frequency as defined by EMI_LO_LIMIT and then returns to EMI_LO_LIMIT.		
				010	Ramp. Linear ramp up and down in frequency between the limits, EMI_LO_LIMIT and EMI_HI_LIMIT.		
				011	Random Hopping Frequency. The isolated power oscillator frequency varies ±63 trim codes around the calibrated center frequency of EMI_MID_LIMIT.		
0x00A	EMI_HI_MASK	[7:0]	EMI_HI_MASK		Emissions Mask, High Frequency Bounds. No functionality on the ADE9103.	0x0	R/W
0x00B	EMI_LO_MASK	[7:0]	EMI_LO_MASK		Emissions Mask, Low Frequency Bounds. No functionality on the ADE9103.	0x0	R/W
0x00C	EMI_HI_LIMIT	[7:0]	EMI_HI_LIMIT		Factory Stored High Frequency Limit. This stored value corresponds to emissions of ≈420 MHz and can be used to set the EMI_xx_MASK. No functionality on the ADE9103.	0x0	R
0x00D	EMI_MID_LIMIT	[7:0]	EMI_MID_LIMIT		Factory Stored Center Frequency Value. This stored value corresponds to emissions of ≈360 MHz and can be used to set the EMI_xx_MASK. No functionality on the ADE9103.	0x0	R
0x00E	EMI_LO_LIMIT	[7:0]	EMI_LO_LIMIT		Factory Stored Low Frequency Limit. This stored value corresponds to emissions of ≈300 MHz and can be used to set the EMI_xx_MASK. No functionality on the ADE9103.	0x0	R
0x00F	MASK0	7	STATUS1X		STATUS1 Interrupt Mask. See the STATUS0 register details description for corresponding status bit. Mask high to allow interrupt source to drive the $\overline{\text{IRQ}}$ pin.	0x0	R/W
		6	STATUS2X		STATUS2 Interrupt Mask. See the STATUS0 register details description for corresponding status bit. See the STATUS1X description for mask bit functionality.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		4	COM_UP		COM_UP Interrupt Mask. See the STATUS0 register details description for corresponding status bit. See the STATUS1X description for mask bit functionality.	0x0	R/W
		3	CRC_CHG		CRC_CHG Interrupt Mask. See the STATUS0 register details description for corresponding status bit. See the STATUS1X description for mask bit functionality.	0x0	R/W
		2	RESERVED		Reserved.	0x0	R
		1	SPI_CRC_ERR		SPI_CRC_ERR Interrupt Mask. See the STATUS0 register details description for corresponding status bit. See the STATUS1X description for mask bit functionality.	0x0	R/W
		0	COMFLT_ERR		COM_FLT_ERR Interrupt Mask. See the STATUS0 register details description for corresponding status bit. See the STATUS1X description for mask bit functionality.	0x0	R/W
0x010	MASK1	[7:4]	RESERVED		Reserved.	0x0	R
		3	V2_WAV_OVRNG		V2 Channel Overrange Interrupt Mask.	0x0	R/W

REGISTER DETAILS

Table 20. Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	V1_WAV_OVRNG		V1 Channel Overrange Interrupt Mask.	0x0	R/W
		1	I_WAV_OVRNG		Current Channel Overrange Interrupt Mask.	0x0	R/W
		0	ADC_SYNC_DONE		ADC Sync Done Update Interrupt Mask.	0x0	R/W
0x011	MASK2	7	RESERVED		Reserved.	0x0	R
		6	ISO_CLK_STBL_ERR		Clock Stability Error Interrupt Mask.	0x0	R/W
		5	ISO_PHY_CRC_ERR		Data Link CRC Error Interrupt Mask.	0x0	R/W
		4	ISO_EFUSE_MEM_ERR		EFuse Memory Error Interrupt Mask.	0x1	R/W
		3	ISO_DIG_MOD_V2_OVF		Digital Modulator V2 Channel Overflow Interrupt Mask.	0x0	R/W
		2	ISO_DIG_MOD_V1_OVF		Digital Modulator V1 Channel Overflow Interrupt Mask.	0x0	R/W
		1	ISO_DIG_MOD_I_OVF		Digital Modulator Current Channel Overflow Interrupt Mask.	0x0	R/W
		0	ISO_TEST_MMR_ERR		Test Memory Mapped Register (MMR) Field Detected Interrupt Mask.	0x0	R/W
0x012	CONFIG_ZX	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	ZX_EDGE_SEL		Zero-Crossing Edge Select. Select the edge behavior of the zero-crossing (ZX) circuit.	0x0	R/W
				00	ZX Pin Reflects the Sign of the Input Signal. The ZX pin goes high on negative to positive ZX and low on positive to negative ZX.		
				01	Detect Zero Crossings with Positive Slope. When zero crossing from negative to positive, a high pulse duration of 512 µs is generated.		
				10	Detect Zero Crossings with Negative Slope. When zero crossing from positive to negative, a high pulse duration of 512 µs is generated.		
				11	Detect Zero Crossings with Positive or Negative Slopes. Combines 01 and 10.		
		[1:0]	ZX_CHANNEL_CONFIG		Zero-Crossing Channel Select.	0x0	R/W
				00	Disable Zero-Crossing Output.		
				01	Output Zero-Crossing Function from the Current Channel on the ZX Pin.		
				10	Output Zero-Crossing Function from the V1 Channel on the ZX Pin.		
				11	Output Zero-Crossing Function from the V2 Channel on the ZX Pin.		
0x013	SCRATCH	[7:0]	SCRATCH		Software Debug Register for Testing SPI R/W. Allows development of SPI and user software by providing a register that is R/W but has no other function on the chip.	0x0	R/W
0x014	SYNC_SNAP	[7:3]	RESERVED		Reserved.	0x0	R
		2	PREP_BROADCAST		ADC Prepare Broadcast. Set this bit only when operating with a dedicated SPI interface and preparing to ALIGN or SNAPSHOT. The MISO pin is tristated for the next SPI frame. This tristating of the pad allows a ADC synchronization to be performed on several chips simultaneously connected to single SPI main. This bit auto clears once complete.	0x0	R/W
		1	ALIGN		ADC Align. When the ALIGN bit is set to 1 via a broadcast SPI write operation, all devices in the system generate ADC outputs in the same exact moment. The bit clears itself back to 0 after one XTALIN cycle.	0x0	R/W
		0	SNAPSHOT		ADC Snapshot. When the SNAPSHOT bit is set to 1 via a broadcast SPI write operation, the internal counters are latched. The bit clears itself back to 0 after one XTALIN cycle.	0x0	R/W
0x017	SNAPSHOT_COUNT_HI	[7:6]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 20. Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[5:0]	SNAPSHOT_COUNT[13:8]		System Timing Controller Count. Snapshot value of the system timing controller counter used in the synchronization operation.	0x0	R
0x018	SNAPSHOT_COUNT_LO	[7:0]	SNAPSHOT_COUNT[7:0]		System Timing Controller Count. Snapshot value of the system timing controller counter used in the synchronization operation.	0x0	R
0x01F	WR_LOCK	[7:0]	WR_LOCK		Configuration Register Write Lock. When enabled, the lock feature does not allow changes to writable registers of Address 0x001 to Address 0x018.	0x5E	R/W
				0xD4	Lock Key. If register map is locked, the lock key value can be read.		
				0x5E	Unlock Key. if the register map is unlocked, any value can be written or read from this location.		
0x020	STATUS0	7	STATUS1X		STATUS1 Indicator. Logical OR of the STATUS1 bit fields that have the corresponding MASK1 bit set. When this condition is satisfied, STATUS1X asserts. To clear this bit field, the source driving interrupt in STATUS1 must be cleared via a write 1 to clear (W1C).	0x0	R
		6	STATUS2X		STATUS2 Indicator. See the STATUS1X description but for the STATUS2 register.	0x0	R
		5	RESET_DONE		Reset Done Interrupt. Nonmaskable interrupt. This interrupt signals that the IC is ready for configuration.	0x0	R/W1C
		4	COM_UP		Communication Across Isolation Established. The ADE9103/ADE9112/ADE9113 is now fully operational and ready to send ADC waveform data.	0x0	R/W1C
		3	CRC_CHG		Register Map Background CRC Change Interrupt. The value of a register included in the CRC has changed. This change may be the result of user software reconfiguration; however, if this is not the case, issue a software reset and reconfigure the ADE9103/ADE9112/ADE9113.	0x0	R/W1C
		2	EFUSE_MEM_ERR		eFuse Memory Error. Nonmaskable interrupt. There was an uncorrectable error in the eFuse memory. This bit field is not W1C, and user action is to request an eFuse memory refresh using EFUSE_REFRESH.	0x0	R
		1	SPI_CRC_ERR		SPI Write CRC Error Interrupt. A CRC error was detected on the previous SPI command received by the ADE9103/ADE9112/ADE9113, and this error bit is set on the SPI read response.	0x0	R/W1C
		0	COMFLT_ERR		Isolation Communications Fault Interrupt. There was a fault in the communication across the isolation. See the COM_FLT_TYPE and COM_FLT_COUNT registers for more details on the error.	0x0	R/W1C
0x021	STATUS1	[7:4]	RESERVED		Reserved.	0x0	R
		3	V2_WAV_OVRNG		ADC V2 Channel Waveform Overrange. The V2 channel ADC has exceeded the maximum range, and the output V2_WAV was clamped to 7549748d.	0x0	R/W1C
		2	V1_WAV_OVRNG		ADC V1 Channel Waveform Overrange. The V1 channel ADC has exceeded the maximum range, and the output V1_WAV was clamped to 7549748d.	0x0	R/W1C
		1	I_WAV_OVRNG		ADC Current Channel Waveform Overrange. The current channel ADC has exceeded the maximum range, and the output I_WAV was clamped to 7549748d.	0x0	R/W1C
		0	ADC_SYNC_DONE		SPI Write to ADC Synchronization Registers. When the SYNC_SNAP register is written to, this interrupt triggers.	0x0	R/W1C
0x022	STATUS2	7	RESERVED		Reserved.	0x0	R
		6	ISO_CLK_STBL_ERR		ISO ADC Clock Stability Error Detected.	0x0	R/W1C

REGISTER DETAILS

Table 20. Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	ISO_PHY_CRC_ERR		ISO PHY Error or Data Link CRC or Error Correcting Code (ECC) Error Detected. An error was detected on NONISO to ISO communications. No action necessary unless error repeatedly set.	0x0	R/W1C
		4	ISO_EFUSE_MEM_ERR		ISO eFuse Memory Error. An uncorrectable eFuse error occurred on the ISO die, and the die was automatically reinitialized. No action necessary unless error repeatedly set.	0x0	R/W1C
		3	ISO_DIG_MOD_V2_OVF		ISO Digital Modulator V2 Channel Overflow Detected. The modulators on the ISO die are automatically reset.	0x0	R/W1C
		2	ISO_DIG_MOD_V1_OVF		ISO Digital Modulator V1 Channel Overflow Detected. The modulators on the ISO die are automatically reset.	0x0	R/W1C
		1	ISO_DIG_MOD_I_OVF		ISO Digital Modulator Current Channel Overflow Detected on the ISO Die. The modulators on the ISO die are automatically reset.	0x0	R/W1C
		0	ISO_TEST_MMR_ERR		ISO Die Register Change Detected and Corrected. The watchdog on the ISO die detected that a register value changed, and the watchdog automatically corrected the change.	0x0	R/W1C
0x023	COM_FLT_TYPE	[7:3]	RESERVED		Reserved.	0x0	R
		2	ISO_STATUS_RD_ECC_ERR		ISO to NONISO Status Read Error Detected. An error was detected on the transfer of status from the ISO die to NONISO die. Single bit ECC errors are corrected. This field clears when the STATUS0 register, COMFLT_ERR bit (Bit) is written to 1.	0x0	R
		1	ISO_PHY_ERR		PHY Error Detected on ISO to NONISO Communications. An incorrect number of pulses was detected on the ISO interface. This field clears when the STATUS0 register, Bit 0 (COMFLT_ERR) is written to 1.	0x0	R
		0	ISO_ECC_ERR		ECC Error Detected on ISO to NONISO Communications. Note that only single bit ECC errors are detected, and single bit errors are also corrected. This field clears when the STATUS0 register, Bit 0 (COMFLT_ERR) is written to 1.	0x0	R
0x024	COM_FLT_COUNT	[7:0]	COM_FLT_COUNT		ECC or PHY Error Count on ISO to NONISO Communications. This counter clears when the STATUS0 register, Bit 0 (COMFLT_ERR) is written to 1. The counter does not roll over when it reaches 255.	0x0	R
0x025	CONFIG_CRC	[7:2]	RESERVED		Reserved.	0x0	R
		1	CRC_DONE		CRC Done Flag. Indicates that CRC recalculation initiated by a CRC_FORCE has completed. Or, if a scheduled CRC recalculation has yielded n updated CRC flag, this flag asserts.	0x0	R/W1C
		0	CRC_FORCE		Force Background Register Map CRC Recalculation. Automatically clears when CRC recalculation completes.	0x0	R/W
0x026	I_WAV_HI	[7:0]	I_WAV[23:16]		ADC Current Channel Waveform Data.	0x0	R/W
0x027	I_WAV_MD	[7:0]	I_WAV[15:8]		ADC Current Channel Waveform Data.	0x0	R/W
0x028	I_WAV_LO	[7:0]	I_WAV[7:0]		ADC Current Channel Waveform Data.	0x0	R/W
0x029	V1_WAV_HI	[7:0]	V1_WAV[23:16]		ADC V1 Channel Waveform Data.	0x0	R/W
0x02A	V1_WAV_MD	[7:0]	V1_WAV[15:8]		ADC V1 Channel Waveform Data.	0x0	R/W
0x02B	V1_WAV_LO	[7:0]	V1_WAV[7:0]		ADC V1 Channel Waveform Data.	0x0	R/W
0x02C	V2_WAV_HI	[7:0]	V2_WAV[23:16]		ADC V2 Channel Waveform Data. The value of this register is always 0x0 on the ADE9112.	0x0	R/W
0x02D	V2_WAV_MD	[7:0]	V2_WAV[15:8]		ADC V2 Channel Waveform Data. The value of this register is always 0x0 on the ADE9112.	0x0	R/W
0x02E	V2_WAV_LO	[7:0]	V2_WAV[7:0]		ADC V2 Channel Waveform Data. The value of this register is always 0x0 on the ADE9112.	0x0	R/W
0x075	UNIQUE_PART_ID_5	[7:0]	UNIQUE_PART_ID[47:40]		Unique Part ID.	0xX[1]	R
0x076	UNIQUE_PART_ID_4	[7:0]	UNIQUE_PART_ID[39:32]		Unique Part ID.	0xX[1]	R

REGISTER DETAILS

Table 20. Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x077	UNIQUE_PART_ID_3	[7:0]	UNIQUE_PART_ID[31:24]		Unique Part ID.	0xX[1]	R
0x078	UNIQUE_PART_ID_2	[7:0]	UNIQUE_PART_ID[23:16]		Unique Part ID.	0xX[1]	R
0x079	UNIQUE_PART_ID_1	[7:0]	UNIQUE_PART_ID[15:8]		Unique Part ID.	0xX[1]	R
0x07A	UNIQUE_PART_ID_0	[7:0]	UNIQUE_PART_ID[7:0]		Unique Part ID.	0xX[1]	R
0x07D	SILICON_REVISION	[7:4]	NONISO_CHIP_REV		Silicon Revision for NONISO Chip.	0x3[2]	R
		[3:0]	ISO_CHIP_REV		Silicon Revision for ISO Chip.	0x2[2]	R
0x07E	VERSION_PRODUCT	[7:0]	VERSION_PRODUCT		Version Product.	0xX[3]	R
				0	ADE9113.		
				1	ADE9112.		
				3	ADE9103.		
0x0CC	DC_OFFSET_MODE	[7:0]	DC_OFFSET_MODE		DC Offset Mode. This mode enables the current channel input short. To short the inputs, write a 1 to the register. To disable the short, write a 0. This register must first be unlocked with the CONFIG_ISO_ACC register.		

[1] The default value is unique to every individual IC.

[2] Subject to change with each silicon revision.

[3] Default value follows product version.

OUTLINE DIMENSIONS

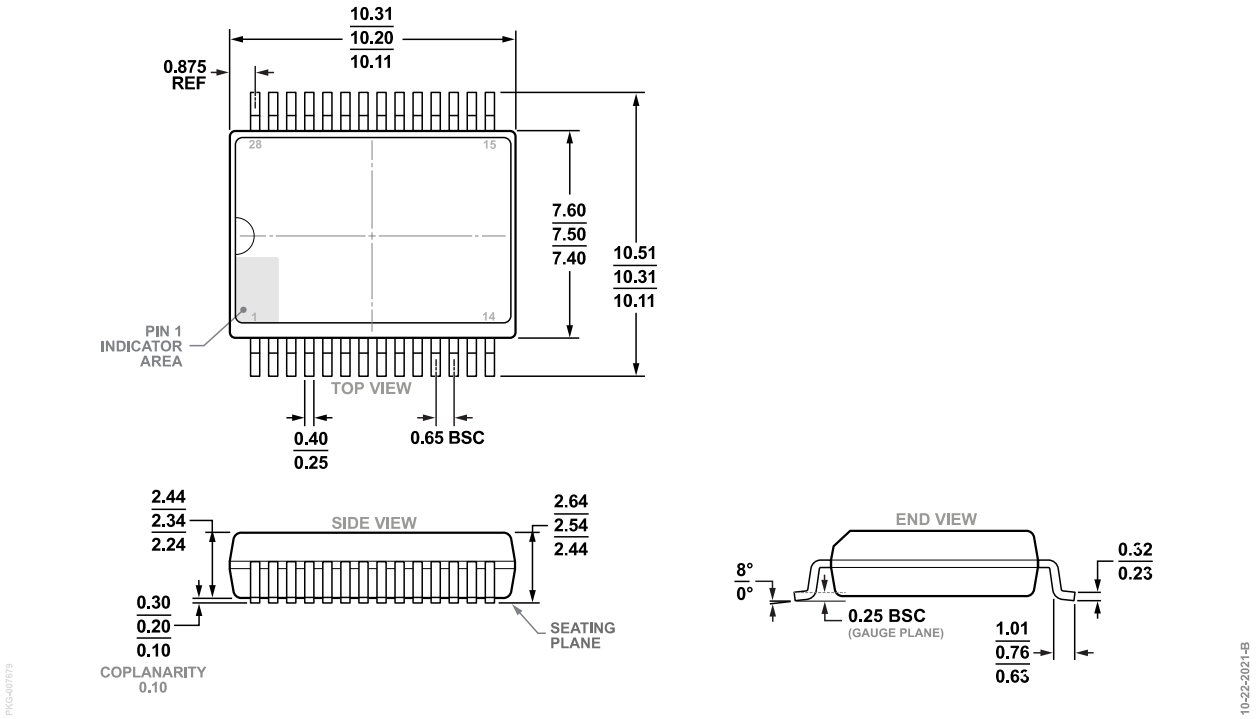

Figure 58. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions shown in millimeters

Updated: October 25, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADE9103ARNZ	−40°C to +125°C	28-Lead SOIC_W_FP	Tube, 46	RN-28-1
ADE9103ARNZ-REEL	−40°C to +125°C	28-Lead SOIC_W_FP	Reel, 1000	RN-28-1
ADE9112ARNZ	−40°C to +125°C	28-Lead SOIC_W_FP	Tube, 46	RN-28-1
ADE9112ARNZ-REEL	−40°C to +125°C	28-Lead SOIC_W_FP	Reel, 1000	RN-28-1
ADE9113ARNZ	−40°C to +125°C	28-Lead SOIC_W_FP	Tube, 46	RN-28-1
ADE9113ARNZ-REEL	−40°C to +125°C	28-Lead SOIC_W_FP	Reel, 1000	RN-28-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 21. Evaluation Boards

Model[1]	Description
EVAL-ADE9113KTZ	Evaluation Kit (Includes All Subboards)
EVAL-SDP-CB1Z	Evaluation Syhstem Controller Board

[1] The EVAL-SDP-CB1Z is the controller board that manages the EVAL-ADE9113KTZ evaluation board. Both boards must be ordered together.

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AD-ACEVSECRDSET-SL ADE9113ARNZ-REEL ADE9113ARNZ EVAL-ADE9113KTZ