

## Single-Channel, Software Configurable Input and Output

### FEATURES

- ▶ Single-channel software configurable input and output
- ▶ Multiple configurable modes to a single pin
  - ▶ Voltage input
  - ▶ Current input
  - ▶ Voltage output
  - ▶ Current output
  - ▶ Digital input
  - ▶ Digital output
  - ▶ 2-wire, 3-wire, or 4-wire RTD measurements
  - ▶ Thermocouple measurement
- ▶ Overvoltage tolerant on screw terminal facing pins, powered or unpowered
- ▶ Auxiliary high voltage sense pins
- ▶ 10 ppm/ $^{\circ}\text{C}$  reference temperature coefficient
- ▶ 16-bit,  $\Sigma\Delta$  ADC with optional 50 Hz and 60 Hz rejection
- ▶ 14-bit monotonic DAC
- ▶ Unipolar and bipolar capability
- ▶ On-chip diagnostics including open-circuit and short-circuit detection
- ▶ Internal temperature sensor,  $\pm 5^{\circ}\text{C}$  accuracy
- ▶ SPI-compatible
- ▶ Wide power supply range
- ▶ Programmable power control
- ▶ Temperature range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- ▶ **48-lead LFCSP**

### APPLICATIONS

- ▶ Isolated industrial control systems
- ▶ Process control
- ▶ Factory automation
- ▶ Building control systems

### FUNCTIONAL BLOCK DIAGRAM

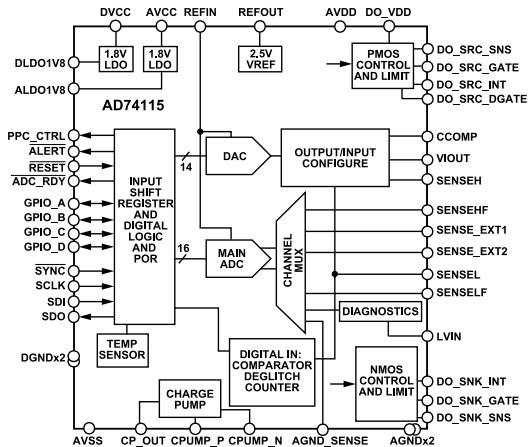


Figure 1. Functional Block Diagram

### GENERAL DESCRIPTION

The AD74115 is a single-channel, software-configurable, input and output device for industrial control applications. The AD74115 provides a wide range of use cases, integrated on a single chip. These use cases include analog output, analog input, digital output, digital input, resistance temperature detector (RTD), and thermocouple measurement capability. A serial peripheral interface (SPI) is used to handle all communications to the device. The digital input and digital outputs can be accessed via the SPI or the general-purpose input and output (GPIO) pins to support higher speed data rates.

The device features a 16-bit,  $\Sigma\Delta$  analog-to-digital converter (ADC) and a 14-bit digital-to-analog converter (DAC). The AD74115 contains a high accuracy 2.5 V on-chip reference that can be used as the DAC and ADC reference.

Power and isolation can be provided using the [ADP1034](#) companion product. When using the ADP1034 and AD74115 together, programmable power control (PPC) is available on the positive analog supply, AVDD, which allows for an optimized power solution in the end application. An on-chip charge pump can be enabled if unipolar capability is required.

### COMPANION PRODUCTS

- ▶ **Power and Data Isolation with PPC: [ADP1034](#)**
- ▶ **Voltage Reference: [ADR4525](#)**

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**REVISION HISTORY****1/2023—Revision 0: Initial Version**

## SPECIFICATIONS

## VOLTAGE OUTPUT

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted. The sense resistor ( $R_{SENSE}$ ) = 100  $\Omega$  (ideal), the load resistor ( $R_{LOAD}$ ) = 100 k $\Omega$ , and the load capacitor ( $C_{LOAD}$ ) = 4.7 nF per the recommended configuration. Note that the headroom specification for AVDD and AVSS must be considered when setting supply voltages.

Table 1. Voltage Output

| Parameter   | Min      | Typ       | Max | Unit          | Test Conditions/Comments  |
|---|----------|-----------|-----|---------------|---|
| VOLTAGE OUTPUT                                      |          |           |     |               |   |
| Resolution  | 14       |           |     | Bits          |   |
| Output Range  | 0<br>-12 | 12<br>+12 |     | V             |   |
| ACCURACY  |          |           |     |               |   |
| Total Unadjusted Error (TUE)                        | -0.2     | +0.2      |     | %FSR          |   |
| TUE at $25^\circ\text{C}$                           | -0.1     | +0.1      |     | %FSR          |   |
| Integral Nonlinearity (INL)                         | -3.0     | +3.0      |     | LSB           |   |
| Differential Nonlinearity (DNL)                     | -1.0     | +1.0      |     | LSB           | Guaranteed monotonic  |
| Offset Error  | -5.5     | +5.5      |     | mV            | Error with Code 0x0000 loaded to the DAC, 0 V to 12 V range only  |
| Offset Error at $25^\circ\text{C}$                  | -3.0     | +3.0      |     | mV            | 0 V to 12 V range only  |
| Bipolar Zero Error                                  | -13      | +13       |     | mV            | Error with midscale code loaded to the DAC in a $\pm 12$ V range  |
| Bipolar Zero Error at $25^\circ\text{C}$            | -13      | +13       |     | mV            | $\pm 12$ V range only   |
| Gain Error  | -0.2     | +0.2      |     | %FSR          |   |
| Gain Error $25^\circ\text{C}$                       | -0.12    | +0.12     |     | %FSR          |   |
| OUTPUT CHARACTERISTICS                              |          |           |     |               |   |
| Load <sup>1</sup>                                   | 1        | 100       |     | k $\Omega$    |   |
| Headroom <sup>1</sup>                               |          | 2.2       |     | V             | Voltage difference required between AVDD and the input and output positive (I/O) screw terminal to provide 12 V across a 1 k $\Omega$ load                        |
| Footroom <sup>1</sup>                               |          | 2.2       |     | V             | Voltage difference required between AVSS and the I/O screw terminal to provide -12 V across a 1 k $\Omega$ load   |
| Short-Circuit Current                               | 32       |           |     | mA            | Sourcing and sinking, I_LIMIT bit = 0 (default)   |
|   | 16       |           |     | mA            | Sourcing and sinking, I_LIMIT bit = 1   |
| Short-Circuit Activation Time <sup>1</sup>          | 2        |           |     | ms            | Time in short circuit before alert is generated   |
| Maximum Capacitive Load <sup>1</sup>                |          | 14        |     | nF            | Maximum system capacitance on the I/O screw terminal, including the recommended 4.7 nF $C_{LOAD}$ when the compensation capacitor ( $C_{COMP}$ ) is not connected |
|   |          | 2         |     | $\mu\text{F}$ | Maximum system capacitance on the I/O screw terminal, including the recommended 4.7 nF $C_{LOAD}$ when a $C_{COMP}$ = 220 pF is connected                         |
| DC Output Impedance <sup>1</sup>                    | 0.1      |           |     | $\Omega$      |   |
| DC Power Supply Rejection Ratio (PSRR) <sup>1</sup> | 90       |           |     | dB            | PSRR measured with a change in AVDD   |
| DYNAMIC PERFORMANCE <sup>1</sup>                    |          |           |     |               |   |
| Output Voltage ( $V_{OUT}$ ) Settling Time          | 85       |           |     | $\mu\text{s}$ | 11 V step (0.5 V to 11.5 V or 11.5 V to 0.5 V) to $\pm 0.05\%$ FSR, $C_{LOAD}$ = 4.7 nF, and no $C_{COMP}$ is connected   |
|   | 110      |           |     | $\mu\text{s}$ | 22 V step (-11 V to +11 V or +11 V to -11 V) to $\pm 0.05\%$ FSR, $C_{LOAD}$ = 4.7 nF, and no $C_{COMP}$ is connected   |
| Output Voltage Settling Time with CCOMP Connected   | 400      |           |     | $\mu\text{s}$ | 11 V step (0.5 V to 11.5 V or 11.5 V to 0.5 V) to $\pm 0.05\%$ FSR, $C_{LOAD}$ = 4.7 nF, and 220 pF $C_{COMP}$ is connected                                       |
|   | 400      |           |     | $\mu\text{s}$ | 22 V step (-11 V to +11 V or +11 V to -11 V) to $\pm 0.05\%$ FSR, $C_{LOAD}$ = 4.7 nF, and 220 pF $C_{COMP}$ is connected   |

## SPECIFICATIONS

Table 1. Voltage Output (Continued)

| Parameter                     | Min | Typ  | Max | Unit    | Test Conditions/Comments                                  |
|-------------------------------|-----|------|-----|---------|---|
| Noise (External Reference)    |     |      |     |         | Measured at the I/O/P screw terminal, 2.5 V output        |
| Output Noise                  |     | 0.17 |     | LSB p-p | 0.1 Hz to 10 Hz bandwidth, 100 kΩ load                    |
| Output Noise Spectral Density |     |      |     |         |   |
| 0 V to 12 V Range             |     | 405  |     | nV/√Hz  | Measured at 1 kHz, midscale output                        |
| -12 V to +12 V Range          |     | 815  |     | nV/√Hz  | Measured at 1 kHz, midscale output                        |
| AC PSRR                       |     | 65   |     | dB      | 200 mV at 1 kHz sine wave superimposed on the AVDD supply |

<sup>1</sup> Guaranteed by design and characterization.

CURRENT OUTPUT ( $I_{OUT}$ )

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{SENSE} = 100 \Omega$  (ideal),  $R_{LOAD} = 250 \Omega$ , and  $C_{LOAD} = 4.7 \text{ nF}$  per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

Table 2. Current Output ( $I_{OUT}$ )

| Parameter                                     | Min  | Typ  | Max  | Unit  | Test Conditions/Comments  |
|---|------|------|------|-------|---|
| $I_{OUT}$                                     |      |      |      |       |   |
| Resolution                                    | 14   |      |      | Bits  |   |
| Output Range                                  | 0    |      | 25   | mA    |   |
| ACCURACY                                      |      |      |      |       |   |
| TUE <sup>1</sup>                              | -0.2 |      | +0.2 | % FSR |   |
| TUE at $25^\circ\text{C}$ <sup>1</sup>        | -0.1 |      | +0.1 | % FSR |   |
| INL   | -4   |      | +4   | LSB   | From zero-scale to full-scale   |
| DNL   | -1   |      | +1   | LSB   | Guaranteed monotonic  |
| Offset Error                                  | -15  |      | +15  | μA    |   |
| Offset Error at $25^\circ\text{C}$            | -8   |      | +8   | μA    |   |
| Gain Error <sup>1</sup>                       | -0.2 |      | +0.2 | % FSR |   |
| Gain Error at $25^\circ\text{C}$ <sup>1</sup> | -0.1 |      | +0.1 | % FSR |   |
| OUTPUT CHARACTERISTICS <sup>2</sup>           |      |      |      |       |   |
| Headroom                                      |      | 3.3  |      | V     | Voltage difference required between AVDD and the I/O/P screw terminal to source 20 mA                     |
| Open Circuit Voltage                          |      | AVDD |      | V     |   |
| Sinking Current Limit                         | 3.7  |      |      | mA    | I_LIMIT bit = 0 (default)   |
|   | 1.2  |      |      | mA    | I_LIMIT bit = 1   |
| Alert Activation Time                         | 2    |      |      | ms    | Time in open or short circuit before alert is generated   |
| Output Impedance                              | 4    |      |      | MΩ    |   |
| DC PSRR                                       | 50   |      |      | nA/V  | PSRR measured with a change in AVDD   |
| DYNAMIC PERFORMANCE <sup>2</sup>              |      |      |      |       |   |
| Output Current Settling Time                  | 90   |      |      | μs    | 3.2 mA to 23 mA step up or down, time to settle within a window of $\pm 100 \mu\text{A}$ of final current |

## SPECIFICATIONS

Table 2. Current Output ( $I_{out}$ ) (Continued)

| Parameter                     | Min | Typ  | Max | Unit                   | Test Conditions/Comments  |
|-------------------------------|-----|------|-----|------------------------|---|
| Noise                         |     |      |     |                        | Measured at the I/O/P screw terminal with 250 $\Omega$ load, 12.5 mA output |
| Output Noise                  |     | 0.34 |     | LSB p-p                | 0.1 Hz to 10 Hz bandwidth   |
| Output Noise Spectral Density |     | 2    |     | nA/ $\sqrt{\text{Hz}}$ | Measured at 1 kHz, 12.5 mA output   |
| AC PSRR                       |     | 75   |     | dB                     | Voltage on the supply at 1 kHz to the voltage across the 250 $\Omega$       |

<sup>1</sup>  $R_{SENSE}$  accuracy directly impacts the TUE and gain error.

<sup>2</sup> Guaranteed by design and characterization.

## VOLTAGE INPUT

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A$  = -40°C to +105°C, unless otherwise noted.  $R_{SENSE}$  = 100  $\Omega$  (ideal), and  $C_{LOAD}$  = 4.7 nF per the recommended configuration. Note that the required input range for AVDD and AVSS must be considered when setting the supply voltages.

Table 3. Voltage Input

| Parameter                          | Min      | Typ        | Max | Unit            | Test Conditions/Comments   |
|------------------------------------|----------|------------|-----|-----------------|--|
| VOLTAGE INPUT                      |          |            |     |                 |  |
| Input Resolution                   | 16       |            |     | Bits            |  |
| Input Range (SENSELF)              | 0        | 12         |     | V               |  |
|                                    | -12      | +12        |     | V               |  |
| ACCURACY <sup>1</sup>              |          |            |     |                 |  |
| TUE                                | -0.1     | +0.1       |     | % FSR           |  |
| TUE at 25°C                        | -0.02    | +0.02      |     | % FSR           |  |
| INL                                | -4       | +4         |     | LSB             |  |
| Offset Error                       | -4       | +4         |     | LSB             |  |
| Offset Error at 25°C               | -2       | +2         |     | LSB             |  |
| Gain Error                         | -750     | +750       |     | ppm FSR         |  |
| Gain Error at 25°C                 | -330     | +330       |     | ppm FSR         |  |
| OTHER INPUT SPECIFICATIONS         |          |            |     |                 |  |
| Footroom <sup>1</sup>              | AVSS + 2 |            |     | V               |  |
| Headroom <sup>1</sup>              |          | AVDD - 0.2 |     | V               |  |
| DC PSRR <sup>1</sup>               |          | 10         |     | $\mu\text{V/V}$ | PSRR measured with a change in AVDD, AVSS, AVCC, and DVCC  |
| Normal Mode Rejection <sup>1</sup> |          | 80         |     | dB              | 50 Hz $\pm$ 1 Hz and 60 Hz $\pm$ 1 Hz  |
| Input Bias Current                 | -30      | +30        |     | nA              | As seen from the I/O/P screw terminal, ADC is either idle or converting; does not include transient voltage suppressor (TVS) leakage |
| Input Bias Current at 25°C         |          | $\pm 6$    |     | nA              |  |

<sup>1</sup> Guaranteed by design and characterization.

**SPECIFICATIONS****CURRENT INPUT EXTERNALLY POWERED**

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{\text{SENSE}} = 100 \Omega$  (ideal), and  $C_{\text{LOAD}} = 4.7 \text{ nF}$  per the recommended configuration.

**Table 4. Current Input Externally Powered**

| Parameter                                     | Min   | Typ               | Max   | Unit     | Test Conditions/Comments   |
|---|-------|-------------------|-------|----------|--|
| CURRENT INPUT                                 |       |                   |       |          |  |
| Input Resolution                              | 16    |                   |       | Bits     |  |
| Input Range                                   | 0     |                   | 25    | mA       | Sensed across the external 100 $\Omega$ resistor   |
| Screw Terminal Voltage                        | 0     |                   |       | V        |  |
| Short-Circuit Current Limit                   | 25    |                   | 35    | mA       | Nonprogrammable  |
| ACCURACY                                      |       |                   |       |          |  |
| TUE <sup>1</sup>                              | -0.1  |                   | +0.1  | % FSR    |  |
| TUE at $25^\circ\text{C}$ <sup>1</sup>        | -0.05 |                   | +0.05 | % FSR    |  |
| INL   | -4    | $\pm 2$           | +4    | LSB      | Linearity specified from 0.1 mA to 25 mA   |
| Offset Error                                  | -4    |                   | +4    | LSB      |  |
| Offset Error at $25^\circ\text{C}$            | -1.5  |                   | +1.5  | LSB      |  |
| Gain Error <sup>1</sup>                       | -250  |                   | +250  | ppm FSR  |  |
| Gain Error at $25^\circ\text{C}$ <sup>1</sup> | -150  |                   | +150  | ppm FSR  |  |
| OTHER INPUT SPECIFICATIONS                    |       |                   |       |          |  |
| DC PSRR <sup>2</sup>                          |       | In order of noise |       |          |  |
| Input Impedance                               | 165   |                   |       | $\Omega$ | Current input, externally powered selected, including 100 $\Omega$ $R_{\text{SENSE}}$                            |
| Compliance <sup>2</sup>                       | 4.2   |                   |       | V        | Current input, externally powered selected, and minimum voltage required at the I/O screw terminal to sink 25 mA |

<sup>1</sup>  $R_{\text{SENSE}}$  accuracy directly impacts the TUE and gain error.

<sup>2</sup> Guaranteed by design and characterization.

**CURRENT INPUT LOOP POWERED**

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{\text{SENSE}} = 100 \Omega$  (ideal), and  $C_{\text{LOAD}} = 4.7 \text{ nF}$  per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

**Table 5. Current Input Loop Powered**

| Parameter              | Min | Typ | Max  | Unit | Test Conditions/Comments                      |
|------------------------|-----|-----|------|------|---|
| CURRENT INPUTS         |     |     |      |      |   |
| Input Resolution       | 16  |     |      | Bits |   |
| Input Range            | 0   |     | 25   | mA   | Sensed across external 100 $\Omega$ resistor  |
| Screw Terminal Voltage |     |     | AVDD | V    |   |
| Current Limit          | 0   |     | 25   | mA   | Programmable current limit, 14-bit resolution |

## SPECIFICATIONS

Table 5. Current Input Loop Powered (Continued)

| Parameter                       | Min   | Typ               | Max   | Unit    | Test Conditions/Comments  |
|---------------------------------|-------|-------------------|-------|---------|---|
| ACCURACY                        |       |                   |       |         |   |
| TUE <sup>1</sup>                | -0.1  |                   | +0.1  | % FSR   |   |
| TUE at 25°C <sup>1</sup>        | -0.05 |                   | +0.05 | % FSR   |   |
| INL                             | -4    |                   | +4    | LSB     | Linearity specified from 0.1 mA to 25 mA range  |
| Offset Error                    | -4    |                   | +4    | LSB     |   |
| Offset Error at 25°C            | -1.5  |                   | +1.5  | LSB     |   |
| Gain Error <sup>1</sup>         | -250  |                   | +250  | ppm FSR |   |
| Gain Error at 25°C <sup>1</sup> | -150  |                   | +150  | ppm FSR |   |
| OTHER INPUT SPECIFICATIONS      |       |                   |       |         |   |
| DC PSRR <sup>2</sup>            |       | In order of noise |       |         |   |
| Input Impedance                 | 165   |                   |       | Ω       | With current input, loop powered selected, includes 100 Ω $R_{SENSE}$   |
| Headroom <sup>2</sup>           | 3.8   |                   |       | V       | Minimum required difference between AVDD and the I/O/P screw terminal voltage to source 25 mA, and current input, loop powered selected |

<sup>1</sup>  $R_{SENSE}$  accuracy directly impacts the TUE and gain error.

<sup>2</sup> Guaranteed by design and characterization.

## RESISTANCE 2-WIRE MEASUREMENT

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A$  = -40°C to +105°C, unless otherwise noted.  $R_{SENSE}$  = 100 Ω (ideal), and  $C_{LOAD}$  = 4.7 nF per the recommended configuration.

Table 6. Resistance 2-Wire Measurement

| Parameter                          | Min | Typ             | Max | Unit    | Test Conditions/Comments   |
|------------------------------------|-----|-----------------|-----|---------|--|
| RESISTANCE MEASUREMENT             |     |                 |     |         |  |
| Input Range                        | 0   |                 | 1   | MΩ      | 2-wire RTD measurements supported  |
| Bias Voltage                       |     | 2.5             |     | V       |  |
| Pull-Up Resistor ( $R_{PULL-UP}$ ) |     | 2.1             |     | kΩ      | $R_{PULL-UP}$ is composed of the external 2 kΩ resistor and the external 100 Ω $R_{SENSE}$ |
| ACCURACY <sup>1</sup>              |     |                 |     |         | Refer to Figure 13   |
| Measurement Range                  |     |                 |     |         |  |
| 1 Ω to 50 Ω                        |     | 0.28            |     | Ω       |  |
| 50 Ω to 3 kΩ                       |     | ±0.07,<br>±0.28 |     | %,<br>Ω | ±% of the measured value plus ± fixed error  |
| 3 kΩ to 10 kΩ                      |     | ±0.1            |     | %       | ±% of the measured value   |
| 10 kΩ to 200 kΩ                    |     | ±1.3            |     | %       | ±% of the measured value   |
| 200 kΩ to 1 MΩ                     |     | ±6.0            |     | %       | ±% of the measured value   |

<sup>1</sup> Guaranteed by design and characterization.

**SPECIFICATIONS****3-WIRE RTD MEASUREMENT**

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{\text{SENSE}} = 100 \Omega$  (ideal) and  $C_{\text{LOAD}} = 4.7 \text{ nF}$  per the recommended configuration.

**Table 7. 3-Wire RTD Measurement**

| Parameter                       | Min   | Typ           | Max  | Unit                        | Test Conditions/Comments  |
|---------------------------------|-------|---------------|------|-----------------------------|---|
| RESISTANCE MEASUREMENT          |       |               |      |                             |   |
| Input Range                     | 0.001 |               | 4    | $\text{k}\Omega$            |   |
| Programmable Excitation Current |       | 250           |      | $\mu\text{A}$               | The voltage generated across the (reference resistor ( $R_{\text{REF}}$ ) + the RTD resistor ( $R_{\text{RTD}}$ )) must be less than the AVCC voltage ( $V_{\text{AVCC}}$ ) |
|                                 |       | 500           |      | $\mu\text{A}$               |   |
|                                 |       | 750           |      | $\mu\text{A}$               |   |
|                                 |       | 1             |      | $\text{mA}$                 |   |
| Current Matching                |       |               |      |                             |   |
| Excitation Current Matching     | -0.5  |               | +0.5 | %                           | For 500 $\mu\text{A}$ , 750 $\mu\text{A}$ , and 1 mA  |
| Current Matching Drift          |       | 5             |      | $\text{ppm}/^\circ\text{C}$ |   |
| Open-Circuit Detect Voltage     |       |               |      |                             | Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit   |
| SENSEH                          |       | 4.0           |      | V                           |   |
| SENSE_EXT1                      |       | 2.7           |      | V                           |   |
| ACCURACY <sup>1</sup>           |       |               |      |                             |   |
| Measurement Range               |       |               |      |                             |   |
| 1 $\Omega$ to 40 $\Omega$       |       | $\pm 0.036$ , |      | %                           | $\pm$ % of the measured value plus $\pm$ the fixed error, suitable for Pt10, Cu10, or similar, 1 mA excitation current and 104.16 mV ADC range                              |
|                                 |       | $\pm 0.023$   |      | $\Omega$                    |   |
| 10 $\Omega$ to 400 $\Omega$     |       | $\pm 0.037$ , |      | %                           | $\pm$ % of the measured value, suitable for Pt100 or similar, 1 mA excitation current, and 0.625 V ADC range  |
|                                 |       | $\pm 0.037$   |      | $\Omega$                    |   |
| 100 $\Omega$ to 4 k $\Omega$    |       | $\pm 0.084$ , |      | %                           | $\pm$ % of the measured value, suitable for Pt1000, and 500 $\mu\text{A}$ excitation current, and 0 V to 12 V ADC range   |
|                                 |       | $\pm 0.358$   |      | $\Omega$                    |   |

<sup>1</sup> Guaranteed by design and characterization.

**4-WIRE RTD MEASUREMENT**

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{\text{SENSE}} = 100 \Omega$  (ideal) and  $C_{\text{LOAD}} = 4.7 \text{ nF}$  per the recommended configuration.

**Table 8. 4-Wire RTD Measurement**

| Parameter                          | Min   | Typ | Max | Unit             | Test Conditions/Comments  |
|------------------------------------|-------|-----|-----|------------------|---|
| RESISTANCE MEASUREMENT             |       |     |     |                  |   |
| Input Range                        | 0.001 |     | 4   | $\text{k}\Omega$ |   |
| Programmable Excitation Current    |       | 250 |     | $\mu\text{A}$    | The voltage generated across ( $R_{\text{REF}} + R_{\text{RTD}}$ ) must be less than $V_{\text{AVCC}}$          |
|                                    |       | 500 |     | $\mu\text{A}$    |   |
|                                    |       | 750 |     | $\mu\text{A}$    |   |
|                                    |       | 1   |     | $\text{mA}$      |   |
| SENSEH Open-Circuit Detect Voltage |       | 4.0 |     | V                | Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit |

## SPECIFICATIONS

Table 8. 4-Wire RTD Measurement (Continued)

| Parameter             | Min | Typ               | Max | Unit    | Test Conditions/Comments   |
|-----------------------|-----|-------------------|-----|---------|--|
| ACCURACY <sup>1</sup> |     |                   |     |         |  |
| Measurement Range     |     |                   |     |         |  |
| 1 Ω to 40 Ω           |     | ±0.036,<br>±0.006 |     | %,<br>Ω | ±% of the measured value plus ± the fixed error, suitable for Pt10, Cu10, or similar, and 1 mA excitation current, and 104.16 mV ADC range |
| 10 Ω to 400 Ω         |     | ±0.037,<br>±0.018 |     | %,<br>Ω | ±% of the measured value, suitable for Pt100 or similar, and 1 mA excitation current, and 0.625 V ADC range                                |
| 100 Ω to 4 kΩ         |     | ±0.084,<br>±0.344 |     | %,<br>Ω | ±% of the measured value, suitable for Pt1000, 500 μA excitation current, and 0 V to 12 V ADC range  |

<sup>1</sup> Guaranteed by design and characterization.

## DIGITAL INPUT LOGIC

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A$  = -40°C to +105°C, unless otherwise noted.  $R_{SENSE}$  = 100 Ω (ideal) and  $C_{LOAD}$  = 4.7 nF per the recommended configuration.

Table 9. Digital Input Logic

| Parameter                        | Min        | Typ     | Max        | Unit  | Test Conditions/Comments   |
|----------------------------------|------------|---------|------------|-------|--|
| DIGITAL INPUTS                   |            |         |            |       |  |
| Unbuffered Input Data Rate       |            |         | 200        | kHz   | The VOUT pin is driven by a low impedance source, 0 V to 12 V signal, duty cycle: 60:40                      |
| Buffered Input Data Rate         |            | 20      |            | kHz   | The SENSEL pin is driven by a low impedance source, 0 V to 12 V signal, duty cycle: 60:40                    |
| Input Voltage Range <sup>1</sup> | -45        |         | +45        | V     |  |
| Input Resistance                 |            | 1.3     |            | MΩ    | High speed mode  |
| Open-Circuit Detect Current      | 0.05       |         | 0.35       | mA    | Window for open-circuit detection for compliance with IEC 61131-2 Type 3D                                    |
| Short-Circuit Detect Current     | 6          |         |            | mA    | For IEC 61131-2 Type 3D  |
| CURRENT SINK                     |            |         |            |       |  |
| Range 0                          |            |         |            |       |  |
| Series Resistor Value            |            | 2.7     |            | kΩ    |  |
| Current Sink Range               | 0          |         | 3.7        | mA    | Typical programmable current sink to AGND  |
| Current Sink Resolution          |            | 120     |            | μA    |  |
| Current Sink Accuracy            |            | ±2      |            | % FSR |  |
| Current Sink at Decimal Code 20  | 2.1        | 2.4     |            | mA    | Recommended for IEC 61131-2 Type I and Type III for the I/O screw terminal > 6 V, DIN_SINK = Decimal Code 20 |
| Current Sink at Decimal 15       |            | 1.8     |            | mA    | Recommended for IEC 61131-2 Type 3D, DIN_SINK bits = Decimal Code 15   |
| Range 1                          |            |         |            |       |  |
| Series Resistor Value            |            | 1       |            | kΩ    |  |
| Current Sink Range               | 0          |         | 7.4        | mA    | Typical programmable current sink to AGND  |
| Current Sink Resolution          |            | 240     |            | μA    |  |
| Current Sink Accuracy            |            | ±2      |            | % FSR |  |
| Current Sink at Decimal Code 29  | 6.1        | 7.0     |            | mA    | Recommended for IEC 61131-2 Type II for the I/O screw terminal > 7 V, DIN_SINK bits = Decimal Code 29        |
| VOLTAGE THRESHOLDS MODES         |            |         |            |       |  |
| Threshold Range                  | AVSS + 2.0 |         | AVDD - 1.5 | V     | Programmable trip level  |
| AVDD Threshold Mode              |            |         |            |       |  |
| Threshold Resolution             |            | AVDD/50 |            | V     |  |

## SPECIFICATIONS

Table 9. Digital Input Logic (Continued)

| Parameter                            | Min | Typ     | Max | Unit  | Test Conditions/Comments   |
|--------------------------------------|-----|---------|-----|-------|--|
| Hysteresis                           |     | AVDD/50 |     | V     |  |
| Fixed Threshold Mode                 |     |         |     | V     |  |
| Threshold Resolution                 |     | 0.5     |     | V     |  |
| Hysteresis                           |     | 0.5     |     | V     |  |
| Threshold Voltage at Decimal Code 55 | 8.0 | 8.5     | 8.8 | V     | Rising trip point, recommended for IEC 61131-2 Type I, Type II, and Type III, COMP_THRESH bits = Decimal Code 55 |
| Threshold Accuracy                   |     | 2       |     | % FSR |  |

<sup>1</sup> Guaranteed by design and characterization.

## DIGITAL INPUT LOOP POWERED

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{SENSE} = 100 \Omega$  (ideal) and  $C_{LOAD} = 4.7 \text{ nF}$  per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

Table 10. Digital Input Loop Powered

| Parameter                         | Min        | Typ     | Max        | Unit  | Test Conditions/Comments  |
|-----------------------------------|------------|---------|------------|-------|---|
| DIGITAL INPUTS                    |            |         |            |       |   |
| Input Data Rate <sup>1</sup>      |            |         | 5          | kHz   | Unfiltered input, typically dominated by wetting current, load capacitance, and threshold voltage |
| Dry Contact Wetting Current Range | 0          |         | 25         | mA    | Loop powered, programmable current  |
| Headroom <sup>1</sup>             |            | 3.3     |            | V     | Required voltage difference between AVDD and the I/O screw terminal to source 20 mA               |
| THRESHOLD MODES                   |            |         |            |       |   |
| Threshold Range                   | AVSS + 2.0 |         | AVDD - 1.5 | V     | Programmable trip level   |
| AVDD Threshold Mode               |            |         |            |       |   |
| Threshold Resolution              |            | AVDD/50 |            | V     |   |
| Hysteresis                        |            | AVDD/50 |            | V     |   |
| Fixed Threshold Mode              |            |         |            |       |   |
| Threshold Resolution              |            | 0.5     |            | V     |   |
| Hysteresis                        |            | 0.5     |            | V     |   |
| Threshold Accuracy                |            | 2       |            | % FSR |   |

<sup>1</sup> Guaranteed by design and characterization.

## SPECIFICATIONS

## DIGITAL OUTPUTS (SOURCING AND SINKING)

DO\_VDD = +10 V to +35 V, AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $C_{\text{LOAD}} = 4.7 \text{ nF}$  per the recommended configuration.

Table 11. Digital Outputs (Sourcing and Sinking)

| Parameter                               | Min   | Typ | Max  | Unit | Test Conditions/Comments  |
|---|-------|-----|------|------|---|
| DO_VDD SUPPLY RANGE                     | 10    | 24  | 35   | V    |   |
| EXTERNAL DIGITAL OUTPUT                 |       |     |      |      | Sourcing and sinking  |
| Short Circuit                           |       |     |      |      |   |
| Short-Circuit Voltage, $V_{\text{SC1}}$ | 160   |     | 240  | mV   | With a $0.15 \Omega$ set resistor ( $R_{\text{SET}}$ ), the current clamps at 1.3 A   |
| Short-Circuit Voltage, $V_{\text{SC2}}$ | 80    |     | 120  | mV   | With a $0.15 \Omega$ $R_{\text{SET}}$ , the current clamps at 667 mA  |
| Short-Circuit Clamp Time <sup>1</sup>   |       | 1.2 |      | μs   | FET input capacitance ( $C_{\text{ISS}}$ ) < 500 pF, and the time for the short-circuit clamp to engage during a $0 \Omega$ short-circuit |
| Time Out 1, $T_1^1$                     | 0.1   |     | 100  | ms   | Typical programmable times  |
| Time Out 2, $T_2^1$                     | 0.1   |     |      | ms   | Typical programmable times  |
| On and Off Times <sup>1</sup>           |       |     |      |      |   |
| On Time, $t_{\text{ON}}$                |       | 20  |      | μs   | FET $C_{\text{ISS}} < 500 \text{ pF}$ , and the time from $\overline{\text{SYNC}}$ rising edge to settle to 90%                           |
| Off Time, $t_{\text{OFF}}$              |       | 3   |      | μs   | FET $C_{\text{ISS}} < 500 \text{ pF}$ , and the time from the $\overline{\text{SYNC}}$ rising edge to FET disable                         |
| Gate Drive Voltage                      |       |     |      |      |   |
| Current Sourcing                        | -12   | -10 | -8   | V    | The DO_SRC_GATE voltage with respect to DO_VDD  |
| Current Sinking                         |       |     | AVCC | V    | The DO_SNK_GATE voltage   |
| DO_SRC_DGATE Current Sink               |       | 1   |      | mA   | To AVSS, when DO_EXT_MODE is configured for the external source with a smart diode  |
| INTERNAL DIGITAL OUTPUT                 |       |     |      |      |   |
| On Resistance, $R_{\text{ON}}$          |       |     |      |      |   |
| Sourcing Mode                           |       | 7   |      | Ω    |   |
| Sinking Mode                            |       | 3.5 |      | Ω    |   |
| Short-Circuit                           |       |     |      |      |   |
| Short-Circuit Current 1                 | 220   |     | 350  | mA   |   |
| Short-Circuit Current 2                 | 105   |     | 180  | mA   |   |
| Short-Circuit Clamp Time <sup>1</sup>   |       | 2   |      | μs   | Time for the short-circuit clamp to engage during a $0 \Omega$ short circuit  |
| Time Out 1, $T_1^1$                     | 0.018 |     | 100  | ms   | Typical programmable times  |
| Time Out 2, $T_2^1$                     | 0.018 |     |      | ms   | Typical programmable times  |
| Thermal Shutdown <sup>1</sup>           |       |     |      |      | Thermal shutdown for internal digital output  |
| Disabled Temperature                    |       | 140 |      | °C   |   |
| Reenabled Temperature                   |       | 130 |      | °C   |   |
| On and Off Times <sup>1</sup>           |       |     |      |      |   |
| On Time, $t_{\text{ON}}$                |       | 10  |      | μs   | Time from the $\overline{\text{SYNC}}$ rising edge to settle to 90%   |
| Off Time, $t_{\text{OFF}}$              |       | 2   |      | μs   | Time from the $\overline{\text{SYNC}}$ rising edge to FET disable   |
| PUSH AND PULL MODE <sup>1</sup>         |       |     |      |      | Push and pull timing for the external FET is dependent on the $C_{\text{ISS}}$ of the external FET  |
| Output Data Rate                        |       |     |      |      |   |
| Internal FETs                           |       | 50  |      | kHz  |   |
| External FETs                           |       | 10  |      | kHz  |   |

## SPECIFICATIONS

Table 11. Digital Outputs (Sourcing and Sinking) (Continued)

| Parameter  | Min | Typ | Max | Unit | Test Conditions/Comments  |
|--|-----|-----|-----|------|---|
| Propagation Delay <sup>1</sup>   |     |     |     |      | From the $\overline{\text{SYNC}}$ rising or the GPIO edge (whichever is in use) to a 0.5 V transition on the I/O screw terminal |
| Propagation High Time, $t_{PH}$ , and Propagation Low Time, $t_{PL}$ , Internal FETs | 4   |     |     | μs   |   |
| $t_{PH}$ and $t_{PL}$ , External FETs  | 7   |     |     | μs   | FET $C_{ISS} < 1 \text{ nF}$  |
| Transition Time <sup>1</sup>   |     |     |     |      | 10% to 90% of the transition on the I/O screw terminal  |
| Rise, $t_R$ , and Fall, $t_F$ , Internal FETs  | 2   |     |     | μs   |   |
| $t_R$ and $t_F$ , External FETs  | 5   |     |     | μs   |   |

<sup>1</sup> Guaranteed by design and characterization.

## SPECIFICATIONS

## ADC SPECIFICATIONS

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{SENSE} = 100 \Omega$  (ideal) and  $C_{LOAD} = 4.7 \text{ nF}$  per the recommended configuration. Note that the required input range for AVDD and AVSS must be considered when setting the supply voltages.

Table 12. ADC Specifications

| Parameter                                      | Min      | Typ   | Max        | Unit    | Test Conditions/Comments  |
|--|----------|-------|------------|---------|---|
| ADC SPECIFICATIONS                             |          |       |            |         |   |
| Resolution                                     | 16       |       |            | Bits    |   |
| No Missing Codes <sup>1</sup>                  | 16       |       |            | Bits    |   |
| Conversion Rates <sup>1</sup>                  |          |       |            |         | Sample rates vary depending on the number of ADC measurements selected and the use of single or continuous conversion modes   |
|  |          | 10    |            | SPS     | 50 Hz and 60 Hz rejection enabled   |
|  |          | 20    |            | SPS     | 50 Hz and 60 Hz rejection enabled   |
|  |          | 1.2   |            | kSPS    | 50 Hz and 60 Hz rejection disabled  |
|  |          | 4.8   |            | kSPS    | 50 Hz and 60 Hz rejection disabled  |
|  |          | 9.6   |            | kSPS    | 50 Hz and 60 Hz rejection disabled  |
| Absolute Input Voltage <sup>1</sup>            | AVSS + 2 |       | AVDD - 0.2 | V       |   |
| Noise <sup>1</sup>                             |          |       |            |         | Refer to Table 27   |
| Common-Mode Rejection Ratio <sup>1</sup>       |          | 95    |            | dB      |   |
| ADC INPUT RANGES                               |          |       |            |         |   |
| 0 V to +12 V, $\pm 12\text{V}$                 |          |       |            |         | Typically used to measure the voltage across the I/OP to I/ON screw terminals (I/ON is the input and output negative, and I/OP is the input and output positive), and also used for SENSE_EXT1 and SENSE_EXT2 |
| Range  | 0        | 12    |            | V       |   |
|  | -12      | +12   |            | V       |   |
| TUE <sup>1</sup>                               | -0.1     | +0.1  |            | % FSR   |   |
| INL <sup>1</sup>                               | -4       | +4    |            | LSB     |   |
| Offset Error                                   | -4       | +4    |            | LSB     |   |
| Gain Error                                     | -750     | +750  |            | ppm FSR |   |
| 0 V to 2.5 V, -2.5 V to 0 V, $\pm 2.5\text{V}$ |          |       |            |         | Typically used to measure the current through the $R_{SENSE}$ resistor  |
| Range  | 0        | 2.5   |            | V       | For current flowing out of the AD74115 through the $100 \Omega R_{SENSE}$   |
|  | -2.5     | 0     |            | V       | For current flowing into the AD74115 across the $100 \Omega R_{SENSE}$  |
|  | -2.5     | +2.5  |            | V       | Typically used to measure bidirectional current across the $100 \Omega R_{SENSE}$ in voltage output mode  |
| TUE  | -0.1     | +0.1  |            | % FSR   |   |
| INL  | -4       | +4    |            | LSB     |   |
| Offset Error                                   | -4       | +4    |            | LSB     |   |
| Gain Error                                     | -250     | +250  |            | ppm FSR |   |
| 0 V to 0.625 V                                 |          |       |            |         | Typically used to measure 3-wire and 4-wire RTDs  |
| Range  | 0        | 0.625 |            | V       |   |
| TUE <sup>1</sup>                               | -0.1     | +0.1  |            | % FSR   |   |
| INL <sup>1</sup>                               | -4       | +4    |            | LSB     |   |
| Offset Error                                   | -10      | +10   |            | LSB     |   |
| Gain Error                                     | -250     | +250  |            | ppm FSR |   |
| $\pm 104.16\text{ mV}$                         |          |       |            |         | Typically used to measure thermocouple voltages in voltage input mode   |
| Range  | -104.16  |       | +104.16    | mV      |   |
| TUE <sup>1</sup>                               | -0.1     | +0.1  |            | % FSR   |   |
| INL <sup>1</sup>                               | -4       | +4    |            | LSB     |   |

## SPECIFICATIONS

Table 12. ADC Specifications (Continued)

| Parameter                       | Min   | Typ   | Max     | Unit    | Test Conditions/Comments   |
|---------------------------------|-------|-------|---------|---------|--|
| Offset Error                    | -25   | +3    | +25     | LSB     | Offset at high temperatures is dominated by leakage through external $R_{SENSE}$ |
| Gain Error                      | -500  |       | +500    | ppm FSR |  |
| DIAGNOSTICS SPECIFICATIONS      |       |       |         |         |  |
| External Diagnostics            |       |       |         |         |  |
| LVIN Pin 2.5 V Range            |       |       |         |         |  |
| Range                           | 0     | 2.5   | V       |         |  |
| TUE <sup>1</sup>                | -0.05 | +0.05 | % FSR   |         |  |
| INL <sup>1</sup>                | -4    | +4    | LSB     |         |  |
| Offset Error                    | -4    | +4    | LSB     |         |  |
| Gain Error                      | -200  | +200  | ppm FSR |         |  |
| Noise <sup>1</sup>              |       |       |         |         | Refer to Table 27  |
| Sense Pins Diagnostics          |       |       |         |         | SENSEL, SENSE_EXT1, and SENSE_EXT2   |
| Accuracy                        | ±0.25 |       | % FSR   |         |  |
| DO Current Sense Accuracy       |       |       |         |         |  |
| External DO                     | ±2    |       | mV      |         |  |
| Internal DO                     | ±5    |       | mA      |         | At 25°C, sourcing and sinking modes  |
| Internal Diagnostics            |       |       |         |         |  |
| Accuracy                        | ±2    |       | %       |         | Percentage of measured value   |
| TEMPERATURE SENSOR <sup>1</sup> |       |       |         |         |  |
| Accuracy                        | ±5    |       | °C      |         |  |
| Resolution                      | 0.2   |       | °C      |         |  |

<sup>1</sup> Guaranteed by design and characterization; not production tested.

## GENERAL SPECIFICATIONS

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.  $R_{SENSE} = 100 \Omega$  (ideal) and  $C_{LOAD} = 4.7 \text{ nF}$  per the recommended configuration.

Table 13. General Specifications

| Parameter                                      | Min   | Typ   | Max   | Unit    | Test Conditions/Comments  |
|--|-------|-------|-------|---------|---|
| REFERENCE SPECIFICATIONS                       |       |       |       |         |   |
| Reference Input                                |       |       |       |         |   |
| Reference Input Voltage                        |       | 2.5   |       | V       | Accuracy of the external reference has an impact on the accuracy of the AD74115         |
| DC Input Current                               | -1    |       | +1    | µA      |   |
| Reference Output                               |       |       |       |         |   |
| Output Voltage                                 | 2.495 | 2.5   | 2.505 | V       | $T_A = 25^\circ\text{C}$  |
| Reference Temperature Coefficient <sup>1</sup> |       |       | 10    | ppm/°C  |   |
| Output Voltage Drift vs. Time <sup>1</sup>     | 500   |       |       | ppm FSR | Drift after 1000 hours, $T_A = 85^\circ\text{C}$  |
| Output Noise <sup>1</sup>                      | 18    |       |       | µV p-p  | 0.1 Hz to 10 Hz bandwidth.  |
| Output Noise Spectral Density <sup>1</sup>     | 95    |       |       | nV/√Hz  | Frequency = 10 kHz  |
| Capacitive Load <sup>1</sup>                   | 22    | 50    |       | nF      | On REFOUT pin   |
| CHARGE PUMP <sup>2</sup>                       |       |       |       |         |   |
| Voltage  |       | -DVCC |       | V       | When enabled, the charge pump generates a voltage that is equal to the negative of DVCC |
| Accuracy                                       |       | ±10   |       | %       |   |
| Output Impedance <sup>1</sup>                  |       | 12.5  |       | Ω       |   |

## SPECIFICATIONS

Table 13. General Specifications (Continued)

| Parameter                                      | Min               | Typ              | Max               | Unit       | Test Conditions/Comments  |
|--|-------------------|------------------|-------------------|------------|---|
| Power-Up Time <sup>1</sup>                     |                   | 2.2              |                   | ms         |   |
| FET LEAKAGE COMPENSATION <sup>1</sup>          |                   |                  |                   |            |   |
| Input Voltage Range                            |                   |                  |                   |            | Voltage range on the I/O terminal when leakage compensation is enabled                              |
| Sourcing External FET                          | AVSS + 2          |                  | AVDD - 1          |            | Typical input voltage range for leakage compensation  |
| Sinking External FET                           | 0                 |                  | AVDD - 1          |            | Typical input voltage range for leakage compensation  |
| Voltage Across External Blocking Diode         |                   | 15               |                   | mV         | FET leakage compensation enabled, for currents up to 40 $\mu$ A leakage current in screw terminal   |
| SENSE PINS                                     |                   |                  |                   |            | SENSEH, SENSEL, SENSEHF, SENSELF, SENSE_EXT1, and SENSE_EXT2  |
| Input Bias Current                             | -25               |                  | +25               | nA         |   |
| Input Bias Current at 25°C                     |                   | 2                |                   | nA         |   |
| Input Bias Matching                            |                   |                  | 10                | nA         | Worst case difference between any of the SENSEHF, SENSELF, SENSE_EXT1, and SENSE_EXT2 pins          |
| High Voltage Buffer Supply Current             |                   |                  |                   |            |   |
| AVDD Current                                   |                   | 190              |                   | $\mu$ A    |   |
| AVSS Current                                   |                   | 190              |                   | $\mu$ A    |   |
| High Voltage Buffer Power-Up Time <sup>1</sup> |                   | 100              |                   | $\mu$ s    |   |
| BURNOUT CURRENTS                               |                   |                  |                   |            | Programmable source or sink currents  |
| V <sub>OUT</sub> Current                       |                   | 1, 10            |                   | $\mu$ A    |   |
| SENSE_EXT1 and SENSE_EXT2 Current              |                   | 0.05, 0.5, 1, 10 |                   | $\mu$ A    |   |
| TEMPERATURE ALERT AND RESET <sup>1</sup>       |                   |                  |                   |            |   |
| Temperature Alert                              |                   | 115              |                   | °C         | Junction temperature, high temperature event flags the alert status and the ALERT pin (if unmasked) |
| Temperature Alert Accuracy                     |                   | 5                |                   | °C         |   |
| Temperature Reset                              |                   | 145              |                   | °C         | Junction temperature, resets the device if over temperature event when the EN_THERM_RST bit = 1     |
| Temperature Reset Accuracy                     |                   | 5                |                   | °C         |   |
| LOGIC INPUTS                                   |                   |                  |                   |            | SCLK, SDI, RESET, SYNC, GPIO_x (as inputs), and PPC_CTRL (as an input)                              |
| Input Voltage                                  |                   |                  |                   |            |   |
| High (V <sub>IH</sub> )                        | 0.7 $\times$ DVCC |                  |                   | V          |   |
| Low (V <sub>IL</sub> )                         |                   |                  | 0.2 $\times$ DVCC | V          |   |
| Input Current                                  | -1                |                  | +1                | $\mu$ A    | Per pin   |
| Input Capacitance <sup>1</sup>                 |                   | 3                |                   | pF         | Per pin   |
| LOGIC OUTPUTS                                  |                   |                  |                   |            |   |
| SDO and PPC_CTRL Pins                          |                   |                  |                   |            |   |
| Output Low Voltage (V <sub>OL</sub> )          |                   |                  | 0.4               | V          | Sink current (I <sub>SINK</sub> ) = 200 $\mu$ A   |
| Output High Voltage (V <sub>OH</sub> )         | DVCC - 0.4        |                  |                   | V          | Source current (I <sub>SOURCE</sub> ) = 200 $\mu$ A   |
| High Impedance Leakage Current                 | -1                |                  | +1                | $\mu$ A    | SDO pin only  |
| High Impedance Output Capacitance <sup>1</sup> |                   | 3                |                   | pF         | SDO pin only  |
| GPIO_x Pin                                     |                   |                  |                   |            | As outputs  |
| V <sub>OL</sub>                                |                   |                  | 0.4               | V          | Capable of sinking 3 mA   |
| V <sub>OH</sub>                                | DVCC - 0.4        |                  |                   | V          |   |
| Pull-Down Resistance                           |                   | 100              |                   | k $\Omega$ |   |
| High Impedance Leakage Current                 | -1                |                  | +1                | $\mu$ A    |   |
| OPEN-DRAIN LOGIC OUTPUTS                       |                   |                  |                   |            | ADC_RDY and ALERT   |
| V <sub>OL</sub>                                |                   |                  | 0.4               | V          | Capable of sinking 2.5 mA   |
| High Impedance Leakage Current                 | -1                |                  | +1                | $\mu$ A    |   |

## SPECIFICATIONS

Table 13. General Specifications (Continued)

| Parameter                         | Min | Typ  | Max  | Unit | Test Conditions/Comments   |
|-----------------------------------|-----|------|------|------|--|
| POWER SUPPLY MONITORS             |     |      |      |      |  |
| AVDD Threshold                    |     | 5.7  |      | V    |  |
| AVSS Threshold                    |     | -1.6 |      | V    |  |
| AVCC Threshold                    |     | 4.1  |      | V    |  |
| DVCC Threshold                    |     | 2.0  |      | V    |  |
| ALDO1V8 Threshold                 |     | 1.3  |      | V    |  |
| DO_VDD Threshold                  |     | 9.5  |      | V    |  |
| POWER REQUIREMENTS                |     |      |      |      |  |
| Supply Voltages <sup>1</sup>      |     |      |      |      |  |
| AVDD                              | 6   | 24   | 28.8 | V    | Headroom requirements must be met for specific application   |
| AVSS                              | -18 | -15  | -2.5 | V    | Footroom requirements must be met for specific application   |
| DVCC                              | 2.7 | 3.3  | 5.5  | V    |  |
| AVCC                              | 4.5 | 5.0  | 5.5  | V    |  |
| DO_VDD                            | 10  |      | 35   | V    |  |
| Supply Quiescent Currents         |     |      |      |      |  |
| AVDD Current                      | 3.5 | 3.9  | 4.3  | mA   | Configured in voltage or current output mode, no load current  |
|                                   | 3.1 | 3.8  | 4.8  | mA   | Configured in any RTD or any analog or digital input mode, no load current   |
|                                   | 2.8 | 3.2  | 3.6  | mA   | Configured in digital output mode  |
| AVSS Current                      | 3.4 | 4.3  | 5.1  | mA   | Configured in any RTD or any analog or digital input mode  |
| DVCC Current                      | 0.7 | 1.4  | 1.7  | mA   | Configured in any RTD or any analog or digital input mode  |
| AVCC Current                      | 4.0 | 5.0  | 6.2  | mA   | Configured in any RTD or any analog or digital input mode  |
| DO_VDD Current                    |     | 50   |      | µA   | Configured in high Impedance mode  |
|                                   | 400 |      | 600  | µA   | Configured in any digital output mode  |
| CONFIGURATION TIMING              |     |      |      |      |  |
| Device Power-Up Time <sup>1</sup> |     | 1    |      | ms   | After all supplies are powered up  |
| Device Reset Time <sup>1</sup>    |     | 1    |      | ms   | Time taken for device reset and calibration memory upload to complete hardware or software reset events after the device is powered up (see Table 14 for pulse width specifications) |
| Use Case Switch Time <sup>1</sup> |     | 200  |      | µs   | Time in use case before changing to another use case   |
| Channel Function Enable Time      |     | 200  |      | µs   | Wait time after the CH_FUNC_SETUP register is programmed before new DAC codes can be loaded  |

<sup>1</sup> Guaranteed by design and characterization.<sup>2</sup> If the charge pump is enabled, connect the CP\_OUT pin to AVSS and ensure that there is no other source on AVSS.

## SPECIFICATIONS

## TIMING CHARACTERISTICS

## SPI Timing Specifications

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, SDO C<sub>LOAD</sub> = 30 pF, and all specifications are at T<sub>A</sub> = -40°C to +105°C, unless otherwise noted.

Table 14. SPI Timing Specifications

| Parameter <sup>1,2</sup>     | Description  | DVCC = 2.7 V to 5.5 V | Unit   |
|------------------------------|--|-----------------------|--------|
| t <sub>1</sub>               | SCLK pin cycle time                                    | 42                    | ns min |
| t <sub>2</sub>               | SCLK high time   | 17                    | ns min |
| t <sub>3</sub>               | SCLK low time  | 17                    | ns min |
| t <sub>4</sub>               | SYNC falling edge to SCLK falling edge setup time      | 21                    | ns min |
| t <sub>5</sub>               | Last SCLK falling edge to SYNC rising edge             | 21                    | ns min |
| t <sub>6</sub>               | SYNC high time   | 450                   | ns min |
| t <sub>7</sub>               | Data setup time  | 5                     | ns min |
| t <sub>8</sub>               | Data hold time   | 5                     | ns min |
| t <sub>9</sub>               | RESET pulse width                                      | 50                    | μs min |
|                              |  | 1 <sup>3</sup>        | ms max |
| t <sub>10</sub>              | SCLK rising edge to SDO valid                          | 23                    | ns max |
| t <sub>11</sub>              | SYNC falling edge to SDO valid (for readback MSB only) | 20                    | ns max |
| t <sub>12</sub>              | SYNC rising edge to SDO tristate                       | 16                    | ns max |
| t <sub>13</sub>              | SYNC rising edge to DAC output response time           | 2                     | μs typ |
| t <sub>14</sub> <sup>4</sup> | ADC_RDY pulse  | 25                    | μs typ |

<sup>1</sup> All input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 5 ns (10% to 90% of the voltage on the DVCC pin (V<sub>DVCC</sub>) and timed from a voltage level of V<sub>DVCC</sub>/2.

<sup>2</sup> Guaranteed by design and characterization; not production tested.

<sup>3</sup> Charge pump voltage decays while in reset.

<sup>4</sup> See Figure 48.

## SPI Timing Diagram

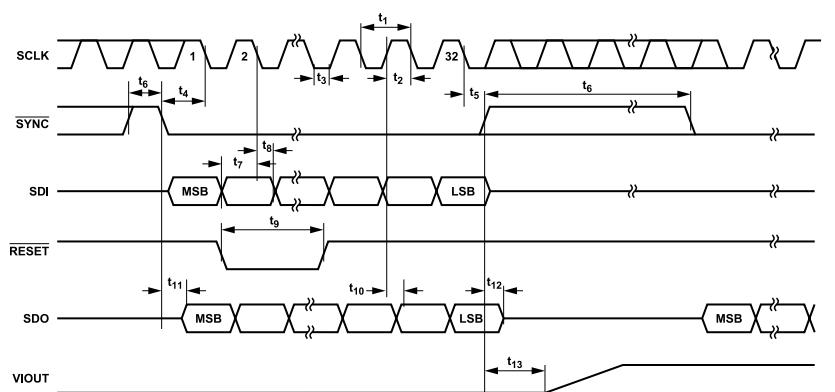


Figure 2. SPI Timing Diagram

## SPECIFICATIONS

## One-Wire Serial Interface (OWSI) Timing Specifications

AVDD = +6 V to +28.8 V, AVSS = -2.5 V to -18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, PPC\_CTRL C<sub>LOAD</sub> = 30 pF, and all specifications are at T<sub>A</sub> = -40°C to +105°C, unless otherwise noted.

Table 15. OWSI Timing Specifications

| Parameter <sup>1,2</sup> | Description   | Min  | Max  | Unit |
|--------------------------|---|------|------|------|
| t <sub>PPC1</sub>        | Bit period  | 4900 |      | ns   |
| t <sub>PPC2</sub>        | Start detect high time  | 140  | 260  | ns   |
| t <sub>PPC3</sub>        | Start detect low time   | 140  | 260  | ns   |
| t <sub>PPC4</sub>        | Start detect time (time for two successive pulses)  | 450  | 750  | ns   |
| t <sub>PPC5</sub>        | Logic low time  | 300  | 500  | ns   |
| t <sub>PPC6</sub>        | Logic high time   | 3400 | 4000 | ns   |
| t <sub>PPC7</sub>        | OWSI subordinate control start time   | 500  | 2200 | ns   |
| t <sub>PPC8</sub>        | OWSI subordinate control end time   | 2700 | 4500 | ns   |
| t <sub>PPC9</sub>        | Time when the OWSI main takes back control of the bus when there is no OWSI subordinate response        | 3400 | 3600 | ns   |
| t <sub>PPC10</sub>       | Time when the OWSI main takes back control of the bus when the OWSI subordinate responds by pulling low |      | 2700 | ns   |

<sup>1</sup> All input signals are specified with t<sub>R</sub>= fall time t<sub>F</sub> = 5 ns (10% to 90% of the voltage on the DVCC pin (V<sub>DVCC</sub>)) and timed from a voltage level of V<sub>DVCC</sub>/2.

<sup>2</sup> Guaranteed by design and characterization; not production tested.

## OWSI Timing Diagram

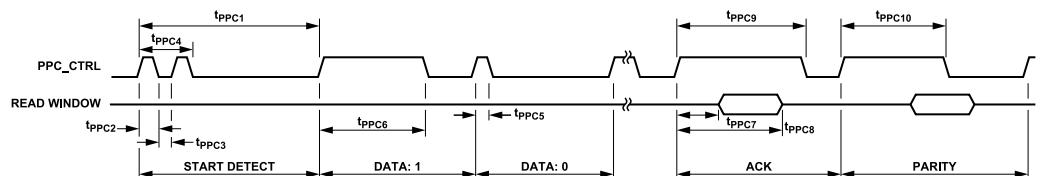


Figure 3. OWSI Timing Diagram for a Successful Transmission

Refer to the [One-Wire Serial Interface](#) section for more information.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

Table 16. Absolute Maximum Ratings

| Parameter   | Rating                                    |
|---|---|
| AVDD to AGND  | -0.3 V to +36 V                           |
| AVSS to AGND  | -20 V to +0.3 V                           |
| AVDD to AVSS  | 56 V                                      |
| DVCC to AGND  | -0.3 V to +6 V                            |
| AVCC to AGND  | -0.3 V to +6 V                            |
| DO_VDD to AGND  | -0.3 V to +40 V                           |
| REFIN and LVIN to AGND  | -0.3 V to AVCC + 0.3 V                    |
| SENSEH, SENSEHF, SENSEL, SENSELF, SENSE_EXT1, and SENSE_EXT2 to AGND                    | -50 V to +50 V                            |
| VOUT to AGND  | -50 V to +50 V                            |
| CCOMP to AGND   | -0.3 V to AVCC + 0.3 V                    |
| DO_SRC_SNS to DO_VDD  | -6 V to +0.3 V                            |
| DO_SRC_INT to DGND  | -50 V to DO_VDD                           |
| DO_SNK_SNS to DGND  | -0.3 V to AVCC + 0.3 V                    |
| DO_SNK_INT to DGND  | -0.3 V to 50 V                            |
| Digital Inputs to DGND (RESET, SYNC, SCLK, and SDI)                                     | -0.3 V to DVCC + 0.3 V                    |
| Logic Digital Outputs to DGND (GPIO_x <sup>1</sup> , SDO, ALERT, ADC_RDY, and PPC_CTRL) | -0.3 V to DVCC + 0.3 V                    |
| AGND_SENSE to AGND  | -0.3 V to +0.3 V                          |
| DGND to AGND  | -0.3 V to +0.3 V                          |
| Operating Temperature Range   | -40°C to +105°C                           |
| Storage Temperature Range   | -65°C to +150°C                           |
| Junction Temperature ( $T_J$ Maximum) <sup>2</sup>                                      | 125°C                                     |
| Reflow Profile  | JEDEC Industry Standard J-STD-020         |
| Power Dissipation   | $(T_J \text{ maximum} - T_A)/\theta_{JA}$ |

<sup>1</sup> x = A, B, C, and D.

<sup>2</sup> It is important to manage the power dissipation of the AD74115 to ensure that the maximum  $T_J$  is not violated. It is also recommended to enable the thermal shutdown function to avoid damage to the AD74115.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the junction to ambient thermal resistance.  $\theta_{JC}$  is the junction to case thermal resistance.

Table 17. Thermal Resistance

| Package Type | $\theta_{JA}$ <sup>1</sup> | $\theta_{JC}$ <sup>2</sup> | Unit |
|--------------|----------------------------|----------------------------|------|
| CP-48-13     | 30.8                       | 2.3                        | °C/W |

<sup>1</sup> Based on simulated data using a JEDEC 2S2P thermal test board with a 5 × 5 array of thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

<sup>2</sup> Measured at the exposed paddle surface with the cold plate in direct contact with the package top surface.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

## ESD Ratings for the AD74115

Table 18. AD74115, 48-Lead LFCSP

| ESD Model | Withstand Threshold | Class |
|-----------|---------------------|-------|
| HBM       | 3 kV                | 2     |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

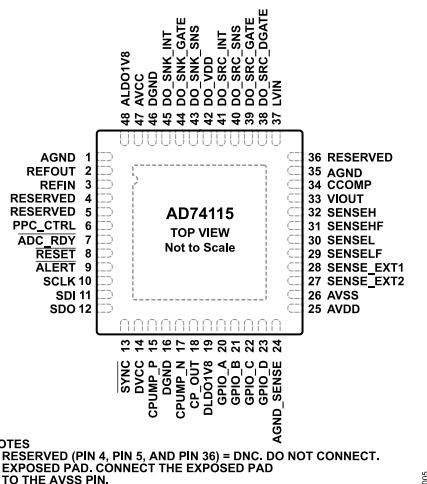


Figure 4. Pin Configuration

Table 19. Pin Function Description

| Pin No.  | Mnemonic             | Description  |
|----------|----------------------|--|
| 1        | AGND                 | Analog Ground.   |
| 2        | REFOUT <sup>1</sup>  | Internal 2.5 V Reference Output. The REFOUT pin must be connected to the REFIN pin to use the internal reference.  |
| 3        | REFIN                | 2.5 V Reference Input.   |
| 4, 5, 36 | RESERVED             | Do Not Connect (DNC).  |
| 6        | PPC_CTRL             | Single-Wire Interface Pin to Communicate with the <a href="#">ADP1034</a> . The supply voltage rails from the ADP1034 are configured by SPI writes to the AD74115 and passed to the ADP1034 through this interface.                  |
| 7        | ADC_RDY              | Active Low, Open-Drain Output. This pin asserts when a new sequence of ADC conversion results is ready to be read. Connect this pin to a pull-up resistor to the DVCC pin.   |
| 8        | RESET                | Hardware Reset Pin. Active low input. This pin resets the AD74115 to the power-on state.   |
| 9        | ALERT                | Active Low, Open-Drain Output. This pin asserts low when an alert condition occurs. Read the ALERT_STATUS register when this pin is asserted. Connect this pin to the DVCC pin via a pull-up resistor.                               |
| 10       | SCLK                 | Serial Interface Clock.  |
| 11       | SDI                  | Serial Interface Data In.  |
| 12       | SDO                  | Serial Interface Data Out.   |
| 13       | SYNC                 | Serial Interface Frame Synchronization Pin. Active low input.  |
| 14       | DVCC <sup>1</sup>    | Digital Supply. Decouple this pin with the recommended capacitor listed in <a href="#">Table 35</a> .  |
| 15       | CPUMP_P              | Charge Pump Fly Capacitor Terminal. If using the internal charge pump for unipolar operation, connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin. Pins can be left disconnected if in bipolar mode.   |
| 16       | DGND                 | Digital Ground.  |
| 17       | CPUMP_N              | Charge Pump Fly Capacitor Terminal. If using the internal charge pump for unipolar operation, connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin. Leave these pins disconnected when in bipolar mode. |
| 18       | CP_OUT               | Charge Pump Output Voltage (Equal to Negative DVCC). When using the charge pump to generate the negative supply, connect the AVSS pin to the CP_OUT pin.   |
| 19       | DLDO1V8 <sup>1</sup> | 1.8 V Digital Low Dropout (LDO) Regulator Output. Decouple this pin with the recommended capacitor shown in <a href="#">Table 35</a> . Do not use this pin externally.   |
| 20       | GPIO_A               | General-Purpose Input and Output Pin A. This pin can monitor the digital input comparator result.  |
| 21       | GPIO_B               | General-Purpose Input and Output Pin B. This pin can control the external digital output circuit.  |
| 22       | GPIO_C               | General-Purpose Input and Output Pin C. This pin can control the internal digital output circuit.  |
| 23       | GPIO_D               | General-Purpose Input and Output Pin D.  |
| 24       | AGND_SENSE           | Analog Ground Sense. Tie this pin to the I/ON screw terminal.  |
| 25       | AVDD <sup>1</sup>    | Positive Analog Supply   |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 19. Pin Function Description (Continued)

| Pin No. | Mnemonic             | Description  |
|---------|----------------------|--|
| 26      | AVSS <sup>1</sup>    | Negative Analog Supply.  |
| 27      | SENSE_EXT2           | High Voltage Sense Pin.  |
| 28      | SENSE_EXT1           | High Voltage Sense Pin   |
| 29      | SENSELF              | Filtered Low-Side Sense Pin. SENSELF can be switched to an ADC input. This pin is routed to the I/O screw terminal side of $R_{SENSE}$ through the off-chip filter.  |
| 30      | SENSEL               | Low-Side Sense Pin. SENSEL closes the loop within the voltage and current output modes. This pin is routed to the I/O screw terminal side of $R_{SENSE}$ .   |
| 31      | SENSEHF              | Filtered High-Side Sense Pin. SENSEHF can be switched to an ADC input. This pin is routed to the AD74115 side of $R_{SENSE}$ through the off-chip filter.  |
| 32      | SENSEH               | High-Side Sense Pin. SENSEH closes the loop within current output mode. This pin is routed to the AD74115 side of $R_{SENSE}$ .  |
| 33      | VIOUT                | Voltage or Current Force Pin. VIOUT provides a voltage or a current to the I/O screw terminal.   |
| 34      | CCOMP                | Compensation Capacitor Pin. CCOMP allows the AD74115 to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP pin and the I/O screw terminal.                                    |
| 35      | AGND                 | Analog Ground.   |
| 37      | LVIN                 | Low Voltage Input Pin. The voltage on LVIN can be measured by selecting the LVIN option in the diagnostics block. The measurement voltage range is 0 V to 2.5 V. For best performance, use an antialiasing filter on this pin. |
| 38      | DO_SRC_DGATE         | Smart Diode Gate Drive Pin.  |
| 39      | DO_SRC_GATE          | Sourcing Digital Output Gate Drive.  |
| 40      | DO_SRC_SNS           | Sourcing Digital Output Sense Pin. If not using the digital output function with an external FET, tie DO_SRC_SNS to DO_VDD.  |
| 41      | DO_SRC_INT           | Internal Sourcing Digital Output.  |
| 42      | DO_VDD <sup>1</sup>  | Positive Supply for Digital Output Circuit.  |
| 43      | DO_SNK_SNS           | Sinking Digital Output Sense.  |
| 44      | DO_SNK_GATE          | Sinking Digital Output Gate Drive.   |
| 45      | DO_SNK_INT           | Internal Sinking Digital Output.   |
| 46      | DGND                 | Digital Ground.  |
| 47      | AVCC <sup>1</sup>    | 5 V Analog Supply.   |
| 48      | ALDO1V8 <sup>1</sup> | 1.8 V Analog LDO Output. Do not use ALDO1V8 externally.  |
|         | Exposed Pad          | Exposed Pad. Connect the exposed pad to the AVSS pin.  |

<sup>1</sup> Connect the recommended decoupling capacitors shown in Table 35.

## TYPICAL PERFORMANCE CHARACTERISTICS

## VOLTAGE OUTPUT

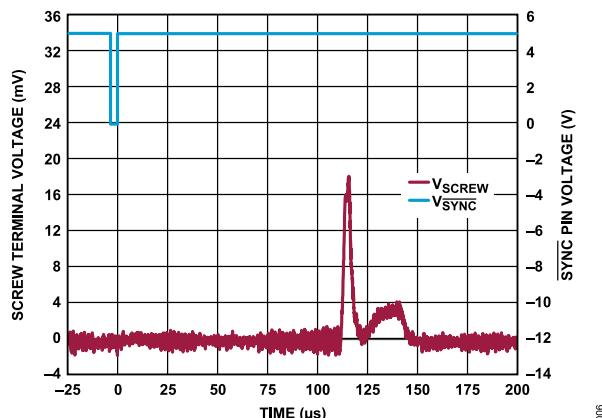


Figure 5. Screw Terminal Voltage ( $V_{SCREW}$ ) and SYNC Pin Voltage ( $V_{SYNC}$ ) vs. Time on Voltage Output Enabled

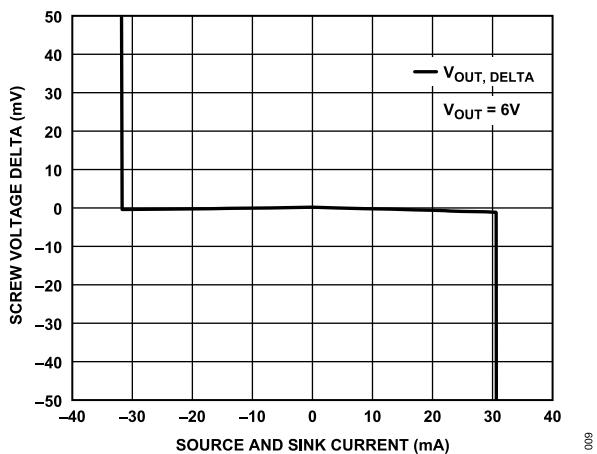


Figure 8. Output Voltage Change ( $V_{OUT, \text{DELTA}}$ ) vs. Source and Sink Current

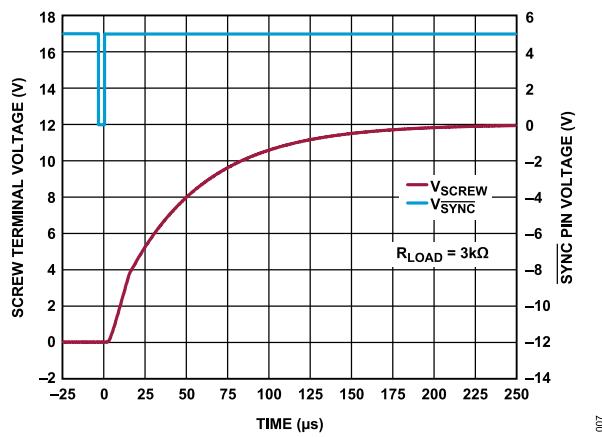


Figure 6. Full-Scale Positive Step with  $C_{COMP}$  Connected

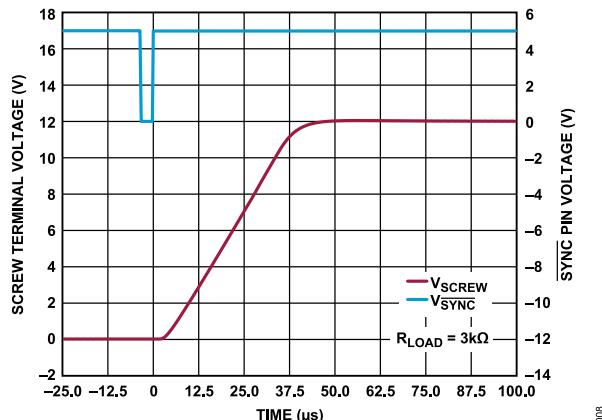


Figure 7. Full-Scale Positive Step Without  $C_{COMP}$

## TYPICAL PERFORMANCE CHARACTERISTICS

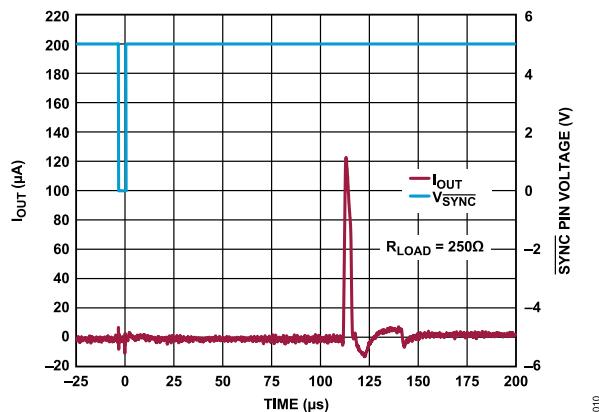
CURRENT OUTPUT ( $I_{OUT}$ )

Figure 9.  $I_{OUT}$  and SYNC Pin Voltage ( $V_{SYNC}$ ) vs. Time on Current Output Enable

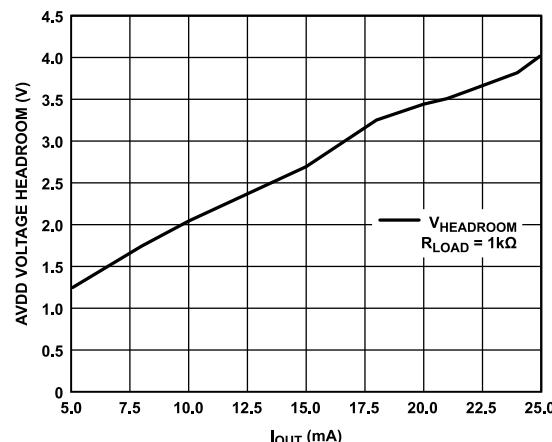


Figure 12. AVDD Voltage Headroom vs.  $I_{OUT}$

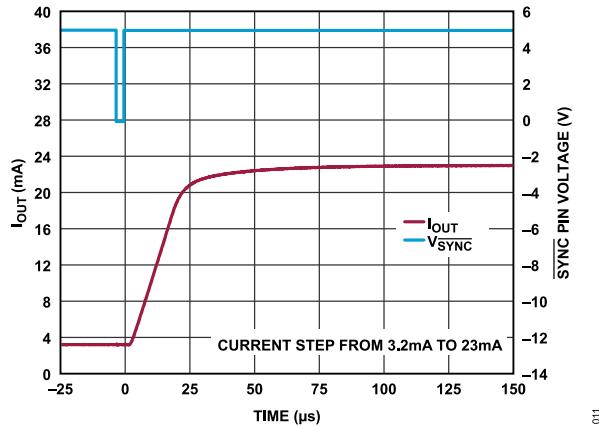


Figure 10.  $I_{OUT}$  and SYNC Pin Voltage ( $V_{SYNC}$ ) vs. Time

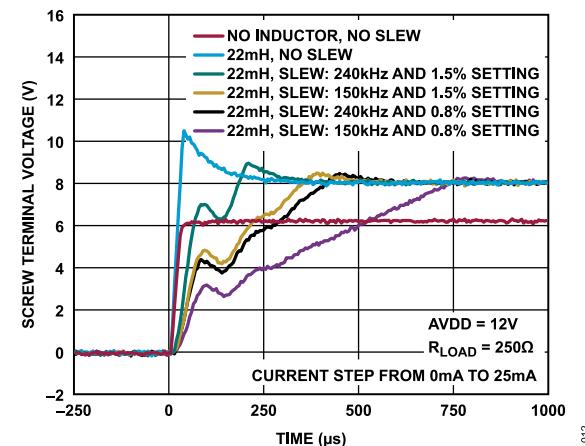


Figure 11.  $I_{OUT}$  Settling Time with Inductive Load and with and Without Slew Rate Enabled

## TYPICAL PERFORMANCE CHARACTERISTICS

## RESISTANCE MEASUREMENT

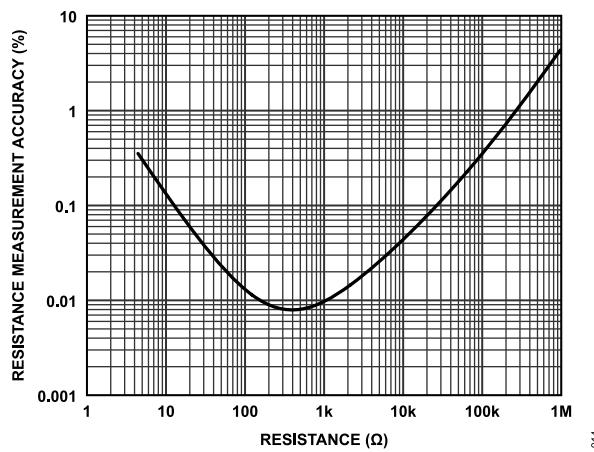


Figure 13. 2-Wire Resistance Measurement Accuracy

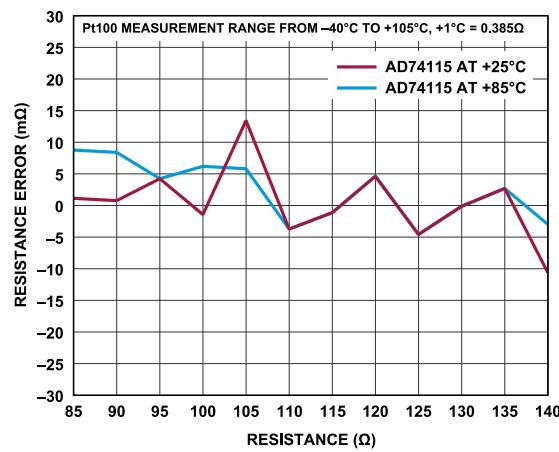


Figure 16. 4-Wire RTD Measurement Error

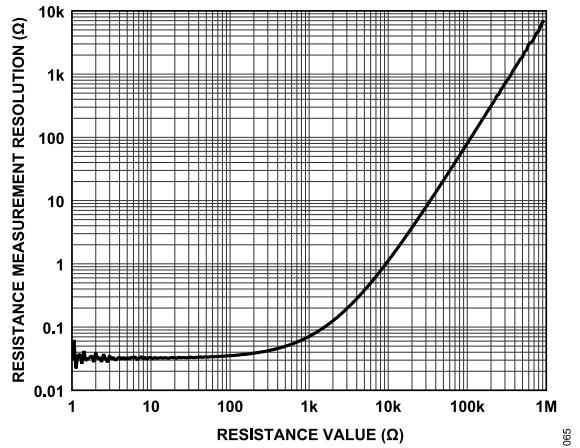


Figure 14. Resistance Measurement Resolution vs. Resistance Value

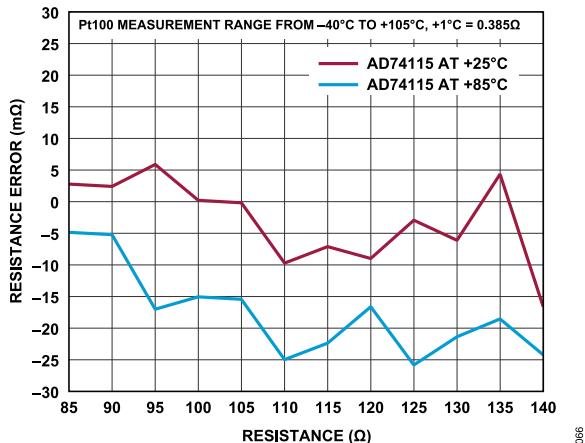
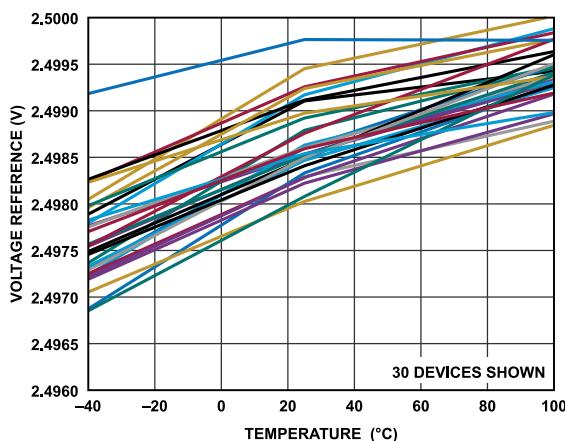


Figure 15. 3-Wire RTD Measurement Error

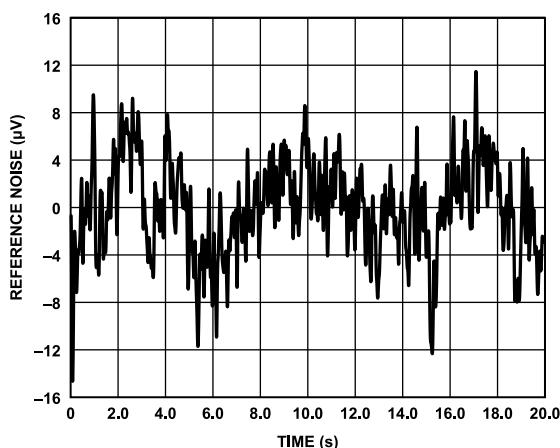
## TYPICAL PERFORMANCE CHARACTERISTICS

## REFERENCE



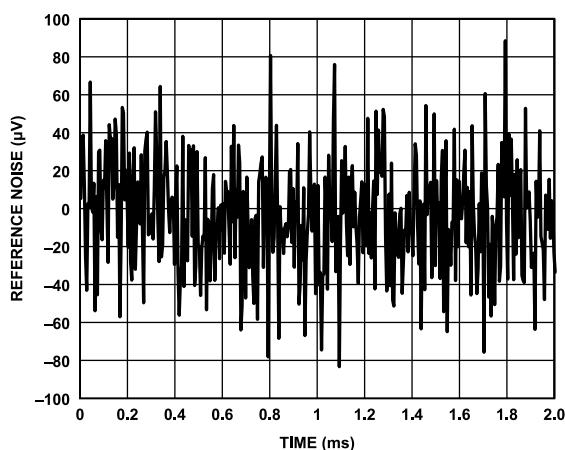
018

Figure 17. Voltage Reference vs. Temperature



019

Figure 18. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)



019

Figure 19. Peak-to-Peak Noise (100 kHz Bandwidth)

## TYPICAL PERFORMANCE CHARACTERISTICS

## ADC

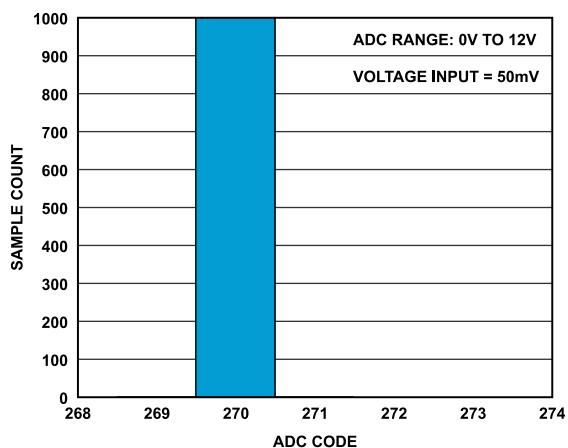


Figure 20. ADC Noise Histogram with Output Data Rate (ODR) = 10 SPS

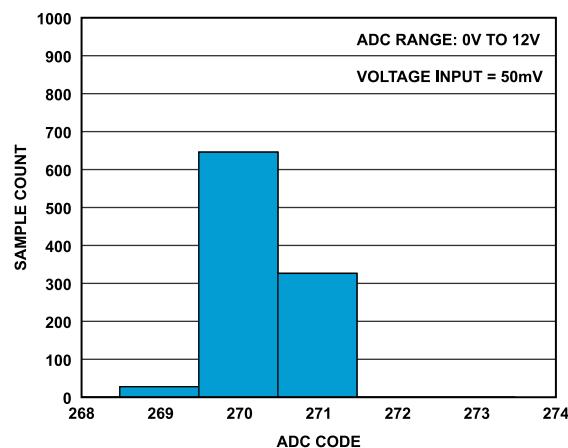


Figure 23. ADC Noise Histogram with ODR = 4.8 kSPS

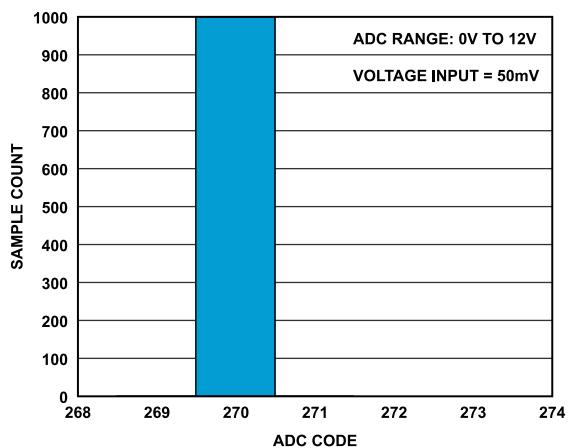


Figure 21. ADC Noise Histogram with ODR = 20 SPS

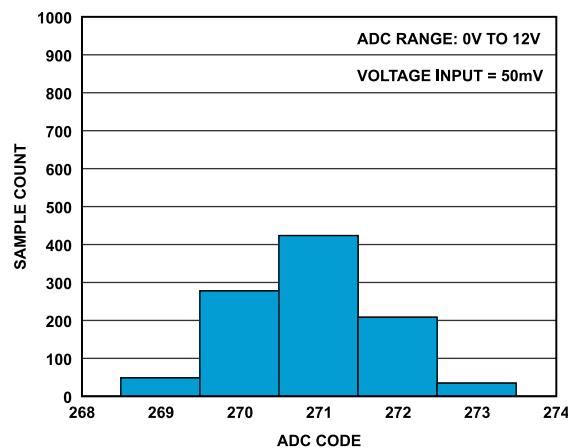


Figure 24. ADC Noise Histogram with ODR = 9.6 kSPS

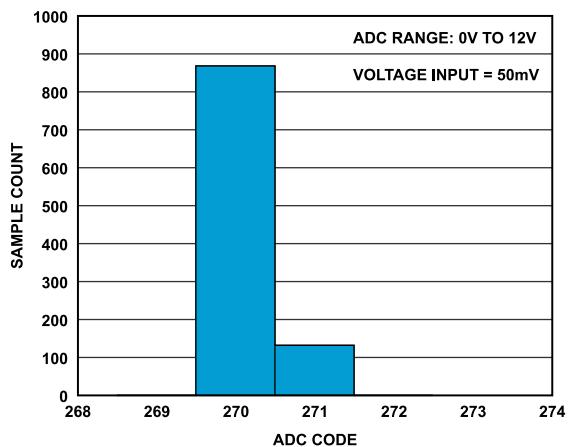


Figure 22. ADC Noise Histogram with ODR = 1.2 kSPS

## TYPICAL PERFORMANCE CHARACTERISTICS

## DIGITAL OUTPUT

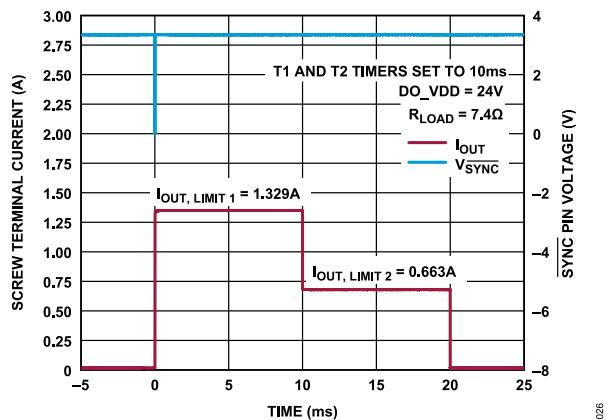
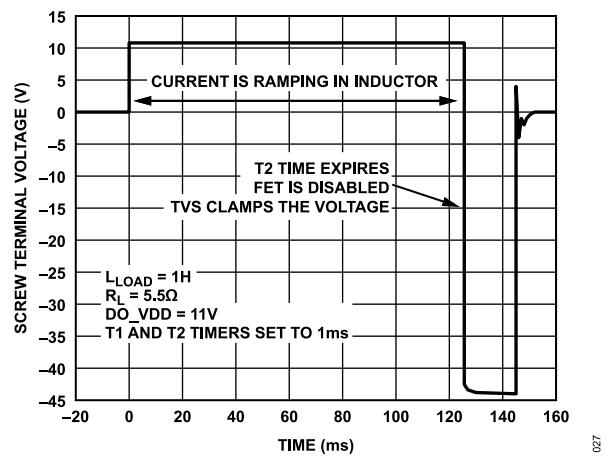


Figure 25. Digital Output Programmable Short-Circuit Activation

Figure 26. Demagnetization Strategy for Inductive Loads ( $L_{LOAD}$ )

## TYPICAL PERFORMANCE CHARACTERISTICS

## OTHERS

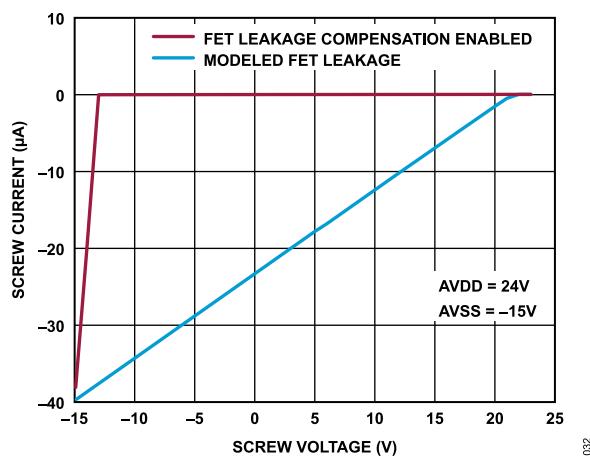


Figure 27. Function of Current Leakage Compensation

## TERMINOLOGY

### ADC Offset Error

For unipolar input ranges, ADC offset error is the deviation in LSBs from the zero-scale code (0x0000) when inputs are shorted, 0 V.

For bipolar input ranges, ADC offset error is the deviation in LSBs from the midscale code (0x8000) when inputs are shorted, 0 V.

### ADC Gain Error

Gain error applies to both unipolar and bipolar ranges. Gain error is a measure of the span error of the ADC.

For input ranges, gain error is defined as the full-scale error minus the zero-scale error. The error is expressed in ppm FSR.

### DAC Offset Error

Offset error is the deviation of the analog output from the ideal zero-scale output when the DAC output register is loaded with 0x0. The offset error is expressed in mV.

### DAC Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal midscale output of 0 V when the DAC output register is loaded with 0x2000. This error applies only to bipolar output ranges.

### DAC Gain Error

Gain error is a measure of the span error of the DAC. This error is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR.

### Total Unadjusted Error (TUE)

TUE is the maximum deviation of the output from the ideal. TUE includes INL, offset, and gain error.

## THEORY OF OPERATION

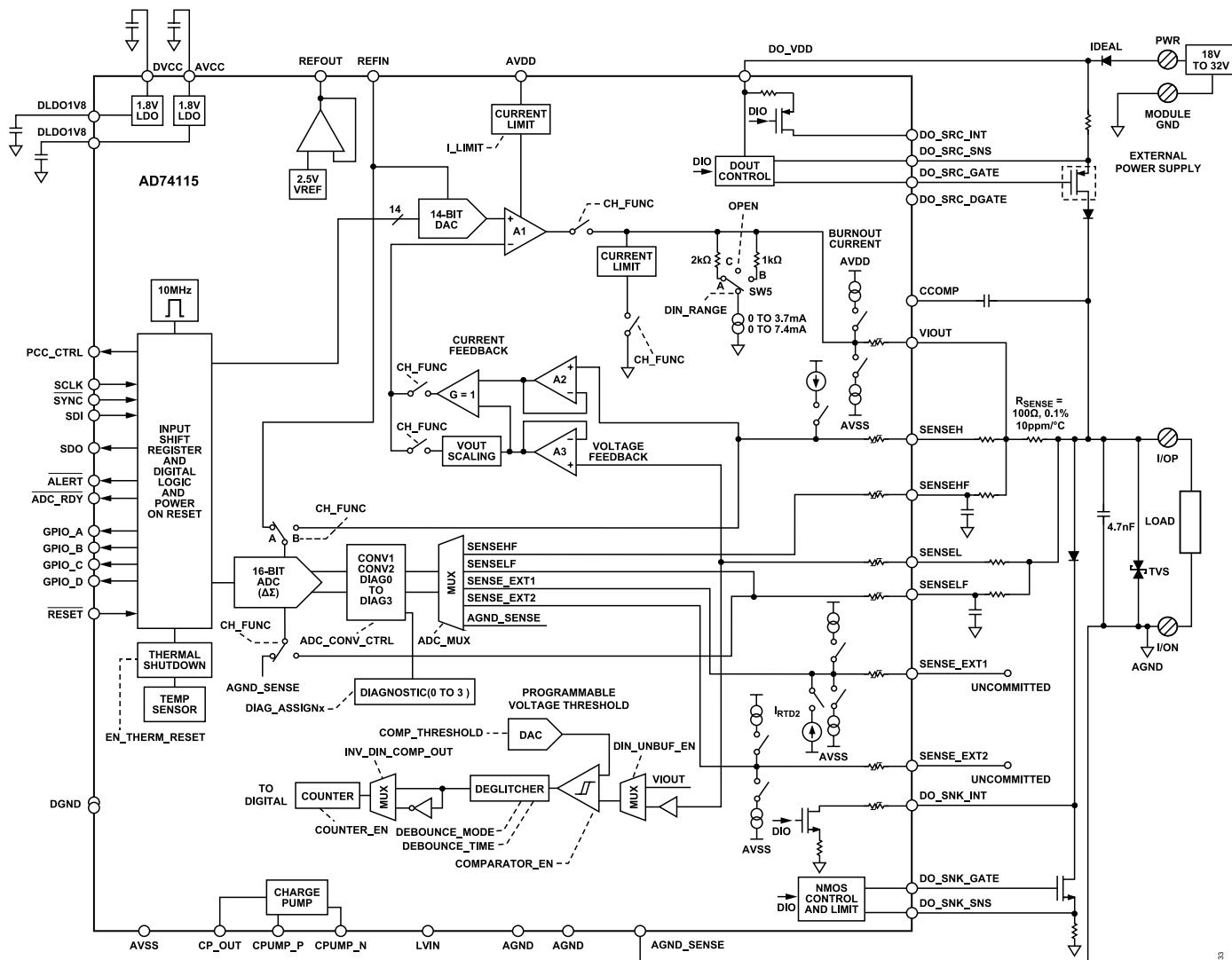


Figure 28. Detailed Functional Block Diagram

The AD74115 is a single-channel, software-configurable input and output that is designed to meet the requirements of isolated process control and factory automation applications. The device provides a fully integrated single chip solution for input and output operation. The AD74115 features a 16-bit,  $\Sigma\Delta$  ADC and a 14-bit DAC, and the device is packaged in a **7 mm × 7 mm, 48-lead LFCSP**.

The channel is configured by writing to the configuration registers. Users can refine the default configurations of each operation mode via the AD74115 register map. See [Figure 28](#) for a detailed functional block diagram of the AD74115.

## ROBUST ARCHITECTURE

The AD74115 system is robust in noisy environments and can withstand overvoltage scenarios such as miswire and surge events.

On-chip line protectors ensure that the I/O screw terminal does not provide power to the IC when brought to a higher potential than the AVDD pin.

The recommended external components shown in [Figure 28](#) and [Table 35](#), including the TVS, are selected to withstand surges on the input and output terminals.

With the recommended components, the I/O and I/ON screw terminals tolerate overvoltages up to  $dc \pm 36$  V (limited by the external TVS).

A cyclic redundancy check (CRC) function is built into the SPI to ensure error free communications in noisy environments.

## POWER SUPPLIES AND REFERENCE

Four external voltage supply rails are required to power up the AD74115:  $V_{AVDD}$ , which is the positive analog supply,  $V_{AVSS}$ , which is the negative analog supply,  $V_{AVCC}$ , which is the low voltage

## THEORY OF OPERATION

analog supply, and  $V_{DVCC}$ , which is the digital supply. See [Table 13](#) for the voltage range of the three external supplies and the associated conditions.

### Powering on the AD74115

When powering up the AD74115, apply ground connections first. After power-up, the user must wait for the device power-up time (see [Table 13](#)) before any transaction to the device can take place.

Upon initial power-up or a device reset of the AD74115, the output channel is disabled and placed in a high impedance state by default.

### Charge Pump

The AD74115 has an internal charge pump that can be enabled to provide AVSS, the negative voltage supply. When only unipolar capability is required, the charge pump can eliminate the requirement for the external AVSS supply voltage. Enable the charge pump using the CPUMP\_EN bit. For correct operation, the charge pump requires an external capacitor (CPUMP\_fly capacitor) between the CPUMP\_N pin and CPUMP\_P pin. Externally connect the CP\_OUT pin to AVSS.

If using the charge pump, take care not to apply an external supply to the AVSS pin.

When the charge pump is enabled, the  $\pm 12$  V bipolar output range is disabled.

### Reference

The AD74115 can operate with either an external or an internal reference. The reference input requires 2.5 V for the AD74115 to function correctly. The reference voltage is internally buffered before being applied to the DAC and the ADC. If using the internal reference, the REFIN pin must be tied to the REfout pin.

### DEVICE FUNCTIONS

The following sections describe the various programmable device functions of the AD74115 with block diagrams and guidelines on how to interpret the ADC results if converting with the default settings. These functions are programmed within the CH\_FUNC\_SETUP register.

Each device function is configured with default measurement settings. However, users can adjust these settings as required within the register map.

### High Impedance

High impedance is the default function upon power-up or after a device reset.

If a channel is held in high impedance for an extended time, such as when the analog input and output functions are not in use, it is recommended to enable a sinking burnout current of 1  $\mu$ A. Enable the burnout current by programming the following bits in the I\_BURNOUT\_CONFIG register:

- ▶ BRN\_VIOUT\_EN to 1
- ▶ BRN\_VIOUT\_POL to 0
- ▶ BRN\_VIOUT\_CURR to 100 binary

### Interpreting ADC Data

In high impedance mode, the ADC, by default, measures the voltage across the screw terminals (I/O<sub>P</sub> to I/O<sub>N</sub>) in a 0 V to 12 V range. Use the following equation to calculate the ADC measurement result:

$$V_{ADC} = (ADC\_CODE/65,536) \times \text{Voltage Range}$$

where:

$V_{ADC}$  is the measured voltage in volts.

$ADC\_CODE$  is the value of the ADC\_RESULT1 register.

**Voltage Range** is the measurement range of the ADC and is 12 V.

### Voltage Output

The voltage output amplifier can generate unipolar or bipolar voltages in the 0 V to +12 V and  $\pm 12$  V ranges, respectively. Each range has 14 bits of resolution. The voltage on the low-side of the  $R_{SENSE}$  is sensed on the SENSEL pin via a 2 k $\Omega$  resistor, which closes the feedback loop and maintains stability.

In voltage output mode, the output range is set to 0 V to 12 V by default. To select bipolar mode, use the following sequence:

- ▶ Write 0x2000 to the DAC\_CODE register to ensure 0 V output.
- ▶ Set the VOUT\_RANGE bit in the OUTPUT\_CONFIG register to 1 for bipolar outputs.
- ▶ Select the voltage output use case in the CH\_FUNC bits, CH\_FUNC\_SETUP register.

[Figure 29](#) shows the current, voltage, and measurement paths of the voltage output mode.

## THEORY OF OPERATION

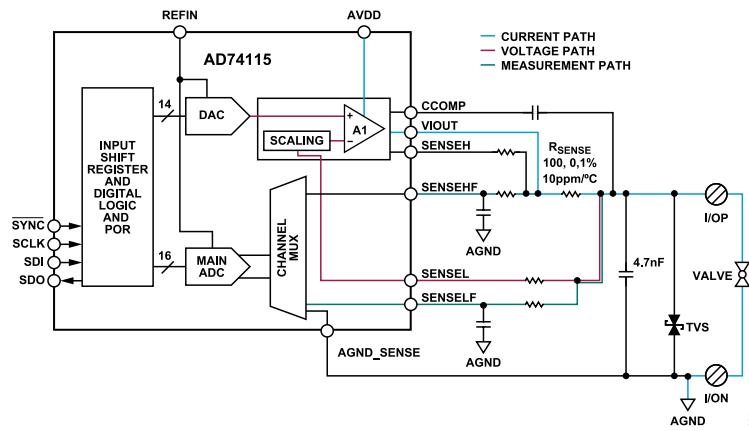


Figure 29. Voltage Output Mode Configuration

## Short-Circuit Detection

There are two available short-circuit limits that can be selected by setting the I\_LIMIT bit in the OUTPUT\_CONFIG registers. See [Table 1](#) for the specified short-circuit current values. If the selected short-circuit limit is reached on a channel, a voltage output short-circuit error is flagged for that channel, and the ALERT pin asserts.

## Interpreting ADC Data

In voltage output mode, the ADC, by default, measures the current through the  $R_{SENSE}$  in a -25 mA to +25 mA range. Use the ADC measurement result to calculate the current through the  $R_{SENSE}$  with the following equation:

$$I_{R_{SENSE}} = \frac{\left( V_{MIN} + \left( \frac{ADC\_CODE}{65,536} \times \text{Voltage Range} \right) \right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$  is the measured current in amps. A negative current indicates that the current is sourced from the AD74115. A positive current indicates that the AD74115 is sinking the current.

$V_{MIN}$  is the minimum voltage of the selected ADC range, which is -2.5 V by default.

$ADC\_CODE$  is the value of the ADC\_RESULT1 register.

$Voltage\ Range$  is the full span of the ADC range, which is 5 V.

$R_{SENSE}$  is the  $R_{SENSE}$  resistor, which is 100  $\Omega$ .

## THEORY OF OPERATION

### Current Output

In current output mode, the DAC provides a current output on the VIOUT pin that is regulated by sensing the differential voltage across  $R_{SENSE}$  by using the SENSEL and SENSEH pins.

Figure 30 shows the current, voltage, and measurement paths of the current output mode.

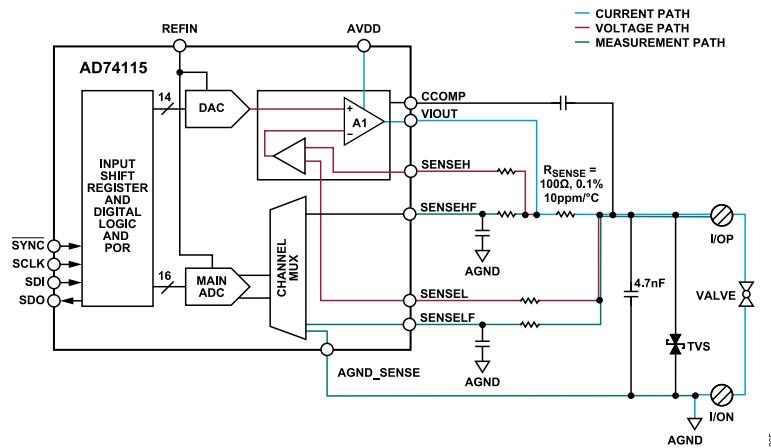


Figure 30. Current Output Mode Configuration

## THEORY OF OPERATION

### Open-Circuit Detection

In current output mode, if the headroom voltage falls below the compliance voltage (specified in [Table 2](#)), due to an open-loop circuit on the channel, a current output open-circuit error is flagged for that channel, and the **ALERT** pin asserts. If  $V_{AVDD}$  is insufficient to drive the programmed current output, the open-circuit error is flagged.

### Interpreting ADC Data

In current output mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/O/P to I/O/N) in a 0 V to 12 V range. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = (ADC\_CODE/65,536) \times \text{Voltage Range}$$

where:

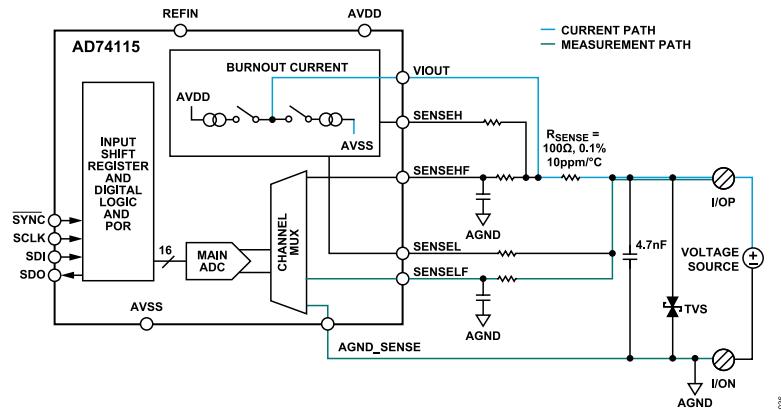


Figure 31. Voltage Input Mode Configuration

$V_{ADC}$  is the measured voltage in volts.

**ADC\_CODE** is the value of the **ADC\_RESULT1** register.

**Voltage Range** is the measurement range of the ADC and is 12 V.

### Voltage Input

In voltage input mode, the voltage across the screw terminals (I/O/P to I/O/N) is measured by the ADC via the **SENSELF** and the **AGND\_SENSE** pins. It is essential to connect the **AGND\_SENSE** pin as close as possible to the I/O/N screw terminal to ensure an accurate voltage measurement. [Figure 31](#) shows the current and measurement paths of the voltage input mode.

In voltage input mode, the voltage can be measured in a  $\pm 12$  V range. However, there is also an option to measure the I/O/P screw terminal voltage using the diagnostics function. The diagnostics function allows the voltage to be measured across the full supply rails.

## THEORY OF OPERATION

### Open-Circuit Detection

Programmable burnout currents can be used to detect an open circuit in voltage input mode (see the [Burnout Currents](#) section). Configure the VOUT pin with the required burnout current by writing to the I\_BURNOUT\_CONFIG register. If the I/O screw terminal is floating, the SENSELF pin is pulled to the supply rail, and the ADC result generates a conversion error.

### Interpreting ADC Data

In voltage input mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/O to I/ON) in a 0 V to 12 V range. A different range can be selected using the CONV1\_RANGE bits in the ADC\_CONFIG register. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = V_{MIN} + (ADC\_CODE/65,536) \times \text{Voltage Range}$$

where:

$V_{MIN}$  is the minimum input voltage of the selected ADC range and is 0 V by default.

$V_{ADC}$  is the measured voltage in volts.

ADC\_CODE is value of the ADC\_RESULT1 register.

Voltage Range is the measurement range of the ADC and is 12 V.

### Thermocouple Measurement

Voltage input mode can measure the voltage of a thermocouple when the thermocouple is connected across the screw terminals (I/O to I/ON). To accurately measure the thermocouple voltage, select the  $\pm 104$  mV input range via the ADC\_CONFIG register in voltage input mode.

### Current Input, Externally Powered

In current input, externally powered mode, the AD74115 provides a current-limited path to ground via the VOUT pin for an external current source. The 16-bit,  $\Sigma\Delta$  ADC is configured to measure the current through  $R_{SENSE}$ . The current is measured by digitizing the voltage across  $R_{SENSE}$  via the SENSEHF and the SENSELF pins. [Figure 32](#) shows the current and measurement paths of the current input, externally powered mode.

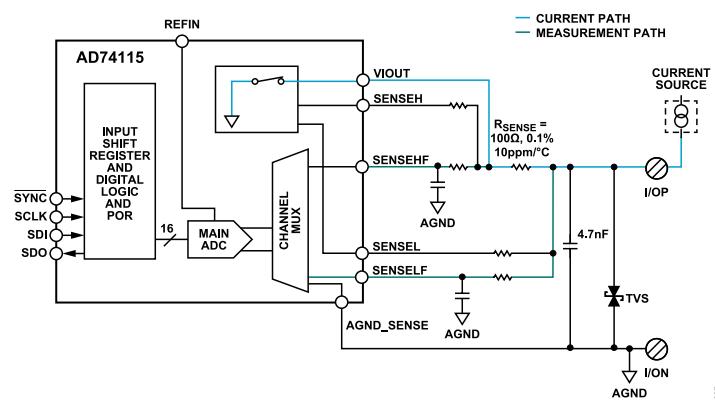


Figure 32. Current Input, Externally Powered Mode Configuration

## THEORY OF OPERATION

### Short-Circuit Protection and Detection

The maximum short-circuit limit is 35 mA in current input, externally powered mode to protect the external circuitry and to limit the power dissipated on the AD74115 device.

In current input, externally powered mode, the digital input comparator is enabled by default to detect a short-circuit condition. The digital input comparator is enabled with a threshold voltage of  $AVDD/2$ . In normal operation, the voltage on I/O/P is typically within 5 V of ground. If the current source attempts to sink more than 35 mA into the AD74115, the voltage on the SENSEL pin instantly ramps. When the voltage on the I/O/P screw terminal is more than the programmed threshold voltage, the comparator trips, setting the ANALOG\_IO\_SC bit in the ALERT\_STATUS register.

### Interpreting ADC Data

In current input mode, the ADC, by default, measures the current flowing from the I/O/P screw terminal into the AD74115 through the  $R_{SENSE}$  in a 25 mA range. Use the ADC measurement current

to calculate the current through the  $R_{SENSE}$  with the following equation:

$$I_{RSENSE} = \frac{\left( \frac{ADC\_CODE}{65,536} \right) \times Voltage\ Range}{R_{SENSE}}$$

where:

$I_{RSENSE}$  is the measured current in amps.

$ADC\_CODE$  is the value of the ADC\_RESULT1 register.

*Voltage Range* is the full span of the ADC range and is 2.5 V.

$R_{SENSE}$  is the sense resistor, which is set to 100  $\Omega$ .

### Current Input, Loop Powered

In current input loop powered mode, the AD74115 provides a current-limited voltage to the I/O/P screw terminal. The current is measured by digitizing the voltage across  $R_{SENSE}$  via the SENSEHF and the SENSELF pins. Figure 33 shows the current, voltage, and measurement paths of the current input, loop powered mode.

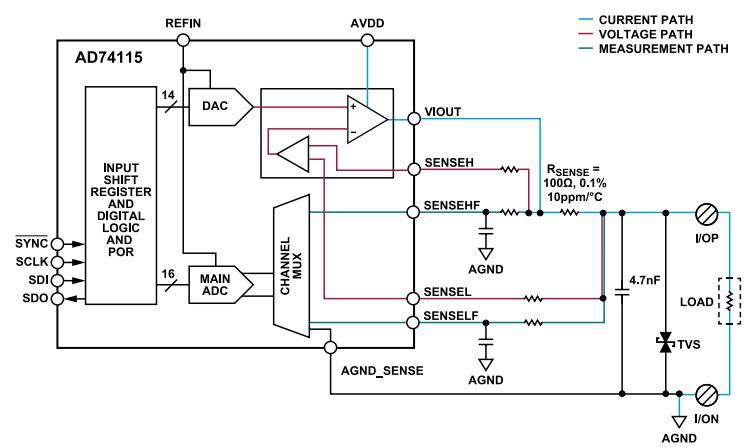


Figure 33. Current Input, Loop Powered Mode Configuration

## THEORY OF OPERATION

### Short-Circuit Protection and Detection

The current from the AD74115 is limited by the programmable DAC code.

In current input loop powered mode, the digital input comparator is enabled by default to detect a short circuit.

The digital input comparator is enabled with a threshold voltage of  $V_{AVDD}/2$  and with the output inverted. During normal operation, the voltage on I/O/P is typically within 5 V of the  $V_{AVDD}$ . If the load is short circuited to ground, the voltage on the I/O/P is pulled to ground. When the voltage on the I/O/P screw terminal falls to less than the programmed threshold level, the comparator trips low, setting the ANALOG\_IO\_SC bit in the ALERT\_STATUS register.

### Interpreting ADC Data

In current input loop, powered mode, the ADC, by default, measures the current flowing from the AD74115 into the I/O/P screw terminal through the  $R_{SENSE}$  in a 25 mA range. Use the ADC measurement result to calculate the current with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\frac{ADC\_CODE}{65,536}\right) \times Voltage\ Range}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$  is the measured current in amps.

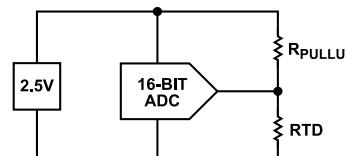
$ADC\_CODE$  is the value of the ADC\_RESULT1 register.

*Voltage Range* is the full ADC span of the ADC range and is 2.5 V.

$R_{SENSE}$  is the sense resistor, which has a value of 100  $\Omega$ .

### Resistance Measurement (2-Wire RTD)

The resistance measurement configuration biases an external 2-wire RTD with a voltage derived from a 2.5 V bias. The resultant excitation current flows through the 2 k $\Omega$  and 100  $\Omega$  resistors (shown as  $R_{PULLUP}$  in Figure 34). This configuration ensures an accurate ratiometric measurement. The 16-bit,  $\Sigma\Delta$  ADC automatically digitizes the voltage across the RTD. The low excitation current ensures that the power dissipated by the RTD is minimized, reducing self heating. See Figure 34 for an example of the RTD bias circuit.



039

Figure 34. RTD Bias Circuit

It is essential that the AGND\_SENSE pin connects to the low-side of the measured RTD. Figure 35 shows the current, voltage, and measurement paths of the resistance measurement configuration.

The resistance measurement mode can be used for 2-wire RTD measurements, but also as a diagnostic of the attached load. Load impedance can be used for load detection techniques or to help to determine the health of the load over time.

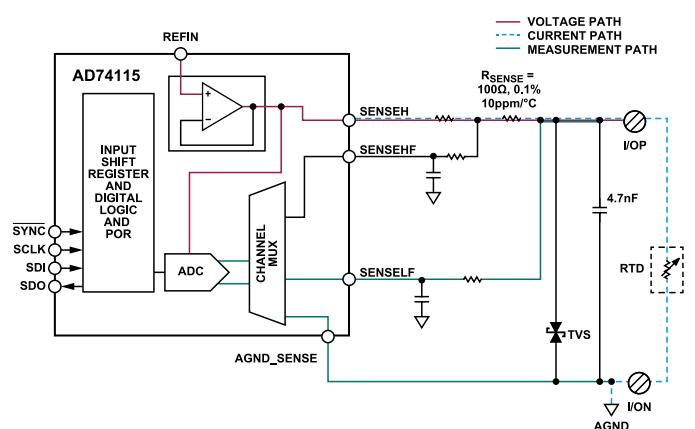


Figure 35. Resistance Measurement Configuration

## THEORY OF OPERATION

### Interpreting ADC Data

In resistance measurement mode, the 16-bit,  $\Sigma\Delta$  ADC automatically digitizes the voltage across the RTD in a 2.5 V range.

When a conversion is carried out, the ADC code reflects the ratio between the RTD and the  $R_{PULL-UP}$ . Use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{(ADC\_CODE \times R_{PULL-UP})}{(65,536 - ADC\_CODE)}$$

where:

$R_{RTD}$  is the calculated RTD resistance in ohms.

$ADC\_CODE$  is the code of the  $ADC\_RESULT1$  registers.

$R_{PULL-UP}$  has a value of  $2100\ \Omega$ .

Do not change the  $CONV1\_MUX$  bits in the settings of the  $ADC\_CONFIG$  register if in RTD mode. Changing from the default ADC mux configuration results in a void ADC result.

### 3-Wire RTD Measurements

3-wire RTD measurements are supported with the AD74115. Use the  $CH\_FUNC$  bits in the  $CH\_FUNC\_SETUP$  register to configure the channel in 3-wire or 4-wire RTD mode.

Figure 36 shows a simplified configuration of the 3-wire RTD method. Matched excitation currents,  $I_1$  and  $I_2$ , are sourced to two of the RTD leads. The third lead is connected to ground. One of the excitation currents,  $I_1$ , generates a voltage across the RTD and lead resistance  $RL_1$ . The second excitation current,  $I_2$ , generates a drop across  $RL_2$ . The resultant voltage across terminals T1 and T2 is equivalent to the voltage drop across the RTD. (It is assumed that the lead resistances are matched, that is,  $RL_1 = RL_2 = RL_3$ ).

The voltage between the T1 and T2 terminals is measured by the ADC using the  $SENSEH$  and  $SENSE\_EXT1$  pins. The full-scale

range of the ADC is determined by the voltage across the reference resistor,  $R_{REF}$ , guaranteeing a fully ratiometric measurement.

The excitation currents applied to the RTD terminals can be programmed to one of four values between  $250\ \mu A$  to  $1\ mA$  in the  $RTD3W4W\_CONFIG$  register. See Table 7 for the full list of excitation currents. Select the excitation current according to the RTD in use.

Take care that the voltage generated on the  $SENSEH$  pin ( $I_1 \times (R_{REF} + R_{RTD})$ ) is less than  $V_{AVCC}$ . The  $SENSEH$  pin voltage provides the positive reference to the ADC and must not exceed the value of  $V_{AVCC}$ .

Three measurement ranges are available in 3-wire RTD mode. These ranges are listed in Table 7. The measurement range can be configured in the  $ADC\_CONFIG$  register using the  $CONV1\_RANGE$  bits. Select the best range to suit the RTD in use.

When the 3-wire or 4-wire RTD mode is selected, the AD74115 is automatically configured to measure a 3-wire RTD in a Pt100 range. In this case, an excitation current of  $1\ mA$  is used, and the ADC measurement range is set to  $0\ V$  to  $0.625\ V$ .

If a Pt1000 measurement is required, it is recommended to use a  $500\ \mu A$  excitation current with the ADC range set to  $0\ V$  to  $12\ V$ .

For a lower resistance RTD, for example Cu10, it is recommended to use  $1\ mA$  excitation current, and the ADC range set to  $\pm 104\ mV$ .

The ADC measurement range can be changed by writing to the  $CONV1\_RANGE$  bits in the  $ADC\_CONFIG$  register. The excitation currents can be changed by writing to the  $RTD\_CURRENT$  bits in the  $RTD3W4W\_CONFIG$  register.

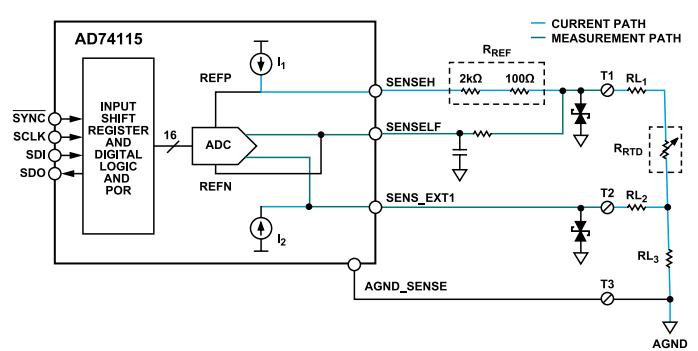


Figure 36. 3-Wire RTD Measurement Configuration

## THEORY OF OPERATION

### How to Configure a 3-Wire RTD Measurement for Pt1000 RTD

The following is an example of how to configure a 3-wire RTD measurement for the Pt1000 RTD:

- ▶ Select 3-wire or 4-wire resistance measurement in the CH\_FUNC\_SETUP register.
- ▶ Set CONV1\_MUX to SENSELF to SENSE\_EXT1 and CONV1\_RANGE to 0 V to 12 V in the ADC\_CONFIG register.
- ▶ Set RTD\_CURRENT to 500  $\mu$ A and RTD\_MODE\_SEL to 3-wire RTD mode in the RTD3W4W\_CONFIG register.
- ▶ Set CONV1\_EN and CONV\_SEQ to start continuous conversions in the ADC\_CONV\_CTRL register.

### Open-Circuit Detection

An open-circuit detect feature is available on the leads of the 3-wire RTD. The combination of excitation current and RTD and lead resistances generates voltages on the SENSEH and SENSE\_EXT1 pins. If the voltage on either of these pins exceeds the open-circuit detect voltage (shown in [Table 7](#)), an open-circuit signal is asserted in the ALERT\_STATUS register.

### Interpreting ADC Data

In 3-wire RTD mode, configure the 16-bit,  $\Sigma$ - $\Delta$  ADC to measure the voltage from SENSELF to SENSE\_EXT1. When a conversion is carried out, the ADC code reflects the ratio between  $R_{RTD}$  and  $R_{REF}$ .

When using unipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \left( \frac{ADC\_CODE + 5}{65,536 \times ADC\_GAIN} \times R_{REF} \right) + 0.2$$

where:

$R_{RTD}$  is the calculated RTD resistance in ohms.

$ADC\_CODE$  is the code of the ADC\_RESULT1 register.

$R_{REF}$  has a value of 2100  $\Omega$  (the combined value of the SENSEH and R<sub>SENSE</sub> resistors).

$ADC\_GAIN$  is the gain of the ADC in the selected ADC range.

When using the 0 V to 0.625 V range (Pt100), the  $ADC\_GAIN$  is 4.

When using the 0 V to 12 V range (Pt1000), the  $ADC\_GAIN$  is 1/4.8.

When using bipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \left( \frac{ADC\_CODE - 32,763}{32,768 \times ADC\_GAIN} \times R_{REF} \right) + 0.2$$

where:

$R_{RTD}$  is the calculated RTD resistance in ohms.

$ADC\_CODE$  is the code of the ADC\_RESULT1 register.

$R_{REF}$  has a value of 2100  $\Omega$  (the combined value of the SENSEH and R<sub>SENSE</sub> resistors).

$ADC\_GAIN$  is the gain of the ADC in the selected ADC range.

When using the  $\pm 104$  mV range (Cu10), the  $ADC\_GAIN$  is 24.

### 4-Wire RTD Measurements

4-wire RTD measurements are supported with the AD74115. Use the CH\_FUNC\_SETUP register to configure the channel in 3-wire or 4-wire RTD mode. Configure the RTD\_MODE\_SEL bit for 4-wire RTD measurements in the RTD3W4W\_CONFIG register.

[Figure 37](#) shows a simplified configuration of 4-wire RTD method. An excitation current,  $I_1$  is sourced to a single lead of the RTD via SENSEH. The fourth lead is connected to ground.

There is no current flow in second and third leads of the RTD that are connected to SENSE\_EXT2 and SENSE\_EXT1, respectively; therefore, these pins are used to sense the voltage directly across the RTD.

The full-scale range of the ADC is determined by the voltage across  $R_{REF}$ , guaranteeing a fully ratiometric measurement.

The excitation current applied to the RTD terminal can be programmed to one of four values between 250  $\mu$ A to 1 mA using the RTD\_CURRENT bits in the RTD3W4W\_CONFIG register. See [Table 7](#) for the full list of excitation currents. Select the excitation current according to the RTD in use. Take care that the voltage generated on the SENSEHF pin ( $I_1 \times (R_{REF} + R_{RTD})$ ) is less than  $V_{AVCC}$ . The SENSEHF pin voltage provides the positive reference to the ADC and must not exceed the value of  $V_{AVCC}$ .

The measurement range can be configured in the ADC\_CONFIG register using the CONV1\_RANGE bits. Select the best range to suit the RTD in use.

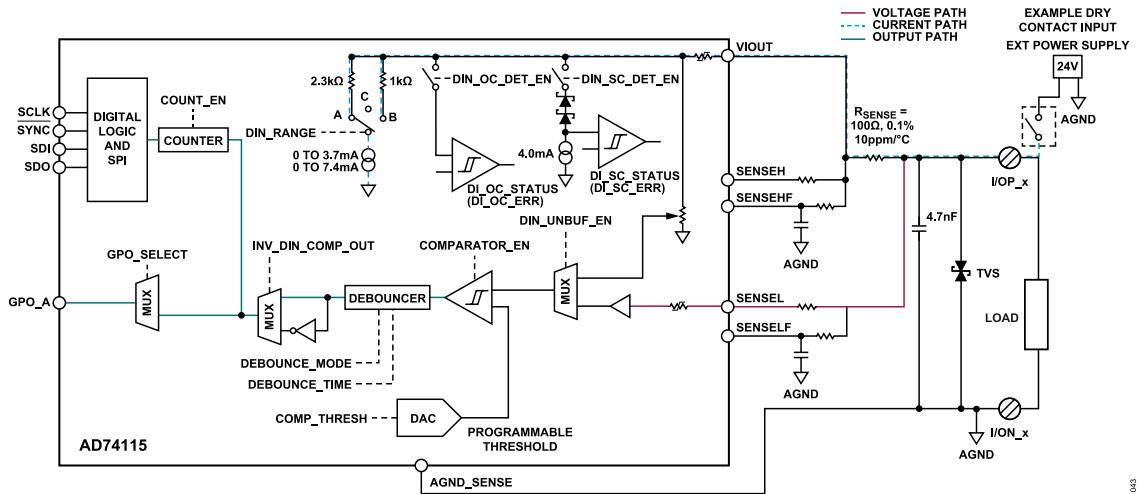


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pin is configured via the `GPIO_CONFIGx` register to drive out the debounced digital input signal.

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements while the digital input logic mode is enabled.

Figure 38 shows the current, voltage, and output paths of the digital input logic mode.



**Figure 38. Digital Input Logic Mode Configuration**

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### Digital Input Threshold Setting

The digital input thresholds are set by an internal DAC. The reference to this DAC is driven by either the  $V_{AVDD}$  or the reference voltage,  $V_{REFIN}$ . This reference is configured by writing to the DIN\_THRESH\_MODE bit within the DIN\_CONFIG2 register.

The specific threshold levels are programmed using the COMP\_THRESH bits in the DIN\_CONFIG2 register. There are seven bits available to configure the threshold, and the maximum programmable code is Decimal 98.

The following equation shows the relationship between the programmed code in the COMP\_THRESH bits and the corresponding threshold voltage when the DAC reference is set to AVDD:

$$V_{THRESH(AVDD)} = V_{AVDD} \times \left( \frac{Code - 48}{50} \right)$$

where:

$V_{THRESH(AVDD)}$  is the comparator threshold expressed in volts.  
 $V_{AVDD}$  is the AVDD supply value in volts.

Code is the decimal code loaded to the COMP\_THRESH bits.

The following equation shows the relationship between the programmed code in the COMP\_THRESH bits and the corresponding threshold voltage when the DAC reference is set to  $V_{REFIN}$ :

$$V_{THRESH(FIXED VOLTAGE)} = V_{REFIN} \times (Code - 38)/5$$

where:

$V_{THRESH(FIXED VOLTAGE)}$  is the comparator threshold expressed in volts.  
 $V_{REFIN}$  is the reference voltage.

Code is the decimal code loaded to the COMP\_THRESH bits.

### Digital Input Current Sink

The AD74115 includes a programmable current sink. The current sink is programmed via the DIN\_RANGE bit and the DIN\_SINK bits within the DIN\_CONFIG1 register. This current sink programmability enables compatibility with Type I, Type II, and Type III of the IEC 61131-2.

Program the current sink and the threshold voltages to enable compatibility with Type I and Type III of the IEC 61131-2.

For Type I and Type III, it is recommended to program the bits in the DIN\_CONFIG1 and DIN\_CONFIG2 registers as follows:

- DIN\_RANGE bit: 0x0
- DIN\_SINK bits: 0x14
- DIN\_THRESH\_MODE bit: 0x1
- COMP\_THRESH bits: 0x37

Programming these bits results in a typical current sink of 2.4 mA and a rising voltage trip point of typically 8.5 V.

For Type II, it is recommended to program the DIN\_CONFIG1 and DIN\_CONFIG2 registers as follows:

- DIN\_RANGE bit: 0x1
- DIN\_SINK bits: 0x1D
- DIN\_THRESH\_MODE bit: 0x1
- COMP\_THRESH bits: 0x37

Programming these bits result in a typical current sink of 6.96 mA and a rising voltage trip point of 8 V.

### Open-Circuit and Short-Circuit Detection

The AD74115 has open-circuit and short-circuit detection capabilities and can be configured to be compatible with IEC 61131-3D.

To use the open-circuit and short-circuit detection functions, enable the current sink by using the DIN\_RANGE bit. Set the current using the DIN\_SINK bits.

To enable the open-circuit diagnostic, use the DIN\_OC\_DET\_EN bit. An open circuit is detected if the input current is less than 0.35 mA.

To enable the short-circuit diagnostic, use the DIN\_SC\_DET\_EN bit. When the DIN\_SC\_DET\_EN bit is set, an additional 4 mA of current sink is enabled. A short-circuit fault is triggered if the 4 mA sink limit is exceeded.

Once an open-circuit or short-circuit fault is triggered, the appropriate bit is set in the ALERT\_STATUS register, and the ALERT pin is asserted.

For Type 3D diagnostics, it is recommended to program the DIN\_CONFIG1 and DIN\_CONFIG2 registers bits as follows:

- DIN\_RANGE bit: 0x0
- DIN\_SINK bits: 0xF
- DIN\_OC\_DET\_EN bit: 0x1
- DIN\_SC\_DET\_EN bit: 0x1
- DIN\_THRESH\_MODE bit: 0x1
- COMP\_THRESH bits: 0x37

Programming these bits results in a typical current sink of 1.8 mA and a rising voltage trip point of typically 8.5 V. An open-circuit detection is triggered when sinking currents are less than 220  $\mu$ A. A short-circuit detection is triggered when sinking currents are greater than typically 6.2 mA.

### Digital Input Inverter

The debounced comparator signal can pass directly to the DIN\_COMP\_OUT register. Alternatively, the signal can be inverted before being sent to the DIN\_COMP\_OUT register. To enable this inverter, set the INV\_DIN\_COMP\_OUT bit in the DIN\_CONFIG1 register.

### Digital Input Counter

A counter is available in the digital input modes, and the counter allows the user to count the debounced digital input edges. The

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counter can be programmed to count the positive edges or the negative edges, which depend on whether the digital input inverter is used. Enable the digital input counter and configure the inverter in the DIN\_CONFIG1 register. The count value is accessed in the DIN\_COUNTER register.

The counter is reset to 0 when the device is reset. When the counter reaches full scale, it rolls over to 0. The counter freezes if the COUNT\_EN bit is set to 0.

### Digital Input Data Rates

When the AD74115 is configured in digital input mode, the voltage on the SENSEL pin is buffered and monitored by the digital input comparator. [Table 9](#) shows the specified data rate.

To enable higher data rates, a high speed, unbuffered option is available to allow the comparator to monitor high speed signals. For unbuffered operation, the voltage on the VOUT pin is monitored by the digital input comparator. Refer to [Table 9](#) for the specified data rate for high speed mode. Enable the unbuffered mode by setting the DIN\_UNBUF\_EN bit in the DIN\_CONFIG2 register.

If using unbuffered mode while sourcing or sinking current to the load via the VOUT pin, consider the voltage drop across  $R_{SENSE}$  (100  $\Omega$ ) and the VOUT line protector (15  $\Omega$ ) when setting the threshold voltage.

### Debounce Function

The digital input comparator outputs are sampled at regular intervals and passed to a user-programmable debounce block.

The comparator outputs can be debounced for a user-programmable amount of time via the 5-bit DEBOUNCE\_TIME bits within the DIN\_CONFIG1 register. Set these bits to 0x00 to bypass the debouncer. [Table 20](#) shows the available programmable debounce times.

The debounce circuit has the following two modes of operation: Debounce Mode 0 and Debounce Mode 1. Both modes are programmed via the DEBOUNCE\_MODE bit in the DIN\_CONFIG1 register.

**Table 20. Digital Input Programmable Debounce Times**

| DEBOUNCE_TIME Code (Hex) | Debounce Time (ms) |
|--------------------------|--------------------|
| 00                       | Bypass             |
| 01                       | 0.0130             |
| 02                       | 0.0187             |
| 03                       | 0.0244             |
| 04                       | 0.0325             |
| 05                       | 0.0423             |
| 06                       | 0.0561             |

**Table 20. Digital Input Programmable Debounce Times (Continued)**

| DEBOUNCE_TIME Code (Hex) | Debounce Time (ms) |
|--------------------------|--------------------|
| 07                       | 0.0756             |
| 08                       | 0.1008             |
| 09                       | 0.1301             |
| 0A                       | 0.1805             |
| 0B                       | 0.2406             |
| 0C                       | 0.3203             |
| 0D                       | 0.4203             |
| 0E                       | 0.5602             |
| 0F                       | 0.7504             |
| 10                       | 1.0008             |
| 11                       | 1.3008             |
| 12                       | 1.8008             |
| 13                       | 2.4008             |
| 14                       | 3.2008             |
| 15                       | 4.2008             |
| 16                       | 5.6008             |
| 17                       | 7.5007             |
| 18                       | 10.0007            |
| 19                       | 13.0007            |
| 1A                       | 18.0006            |
| 1B                       | 24.0006            |
| 1C                       | 32.0005            |
| 1D                       | 42.0004            |
| 1E                       | 56.0003            |
| 1F                       | 75.0000            |

### Debounce Mode 0 (Default)

In this mode, the sampled comparator outputs are counted. A high sample occurrence is counted in one direction, up, whereas a low sample occurrence is counted in the opposite direction, down. The DIN\_COMP\_OUT register changes state when the programmed counter target is reached.

[Figure 39](#) shows an example of Debounce Mode 0 in operation. The debounce time is set to 100.8  $\mu$ s in the DIN\_CONFIG1 register. A clock with an approximate period of 800 ns samples the comparator signal. After the comparator signal changes state from the current debounced signal, the debounce block counter begins to count up the duration of the signal at the new state. The counting direction changes if the comparator signal reverts back to the original state. After the counter reaches the target count, the DIN\_COMP\_OUT register is updated with the state of the comparator signal.

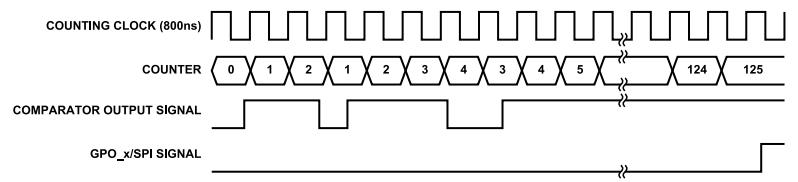
**THEORY OF OPERATION**

Figure 39. Digital Input Debounce Mode 0 Timing Example

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### Debounce Mode 1

In this mode, a counter counts the sampled comparator outputs. After a change of state occurs on the sampled comparator output, the counter increments until the programmed debounce time is reached, at which point the DIN\_COMP\_OUT register changes state, and the counter resets. If the sampled comparator output returns to the current DIN\_COMP\_OUT register value, the counter resets.

Figure 40 shows an example of Debounce Mode 1 in operation. Like Debounce Mode 0, the debounce time is set to 100.8  $\mu$ s. In Debounce Mode 1, the counter value is reset each time the comparator signal returns to the original state. The comparator output must be at the new state for the full duration of the debounce time to update the DIN\_COMP\_OUT signal.

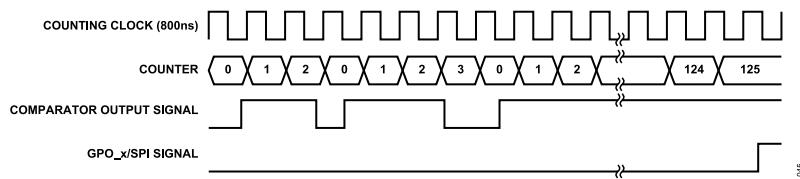


Figure 40. Digital Input Debounce Mode 1 Timing Example

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### Digital Input, Loop Powered

Like the current output mode function (see the [Current Output \(I<sub>OUT</sub>\)](#) section), the digital input, loop powered function configures the output stage to provide a high-side current output that can power an external sensor. Program the DAC\_CODE register to provide the required current source limit.

The I/O screw terminal voltage can be monitored by the digital input function. The unfiltered voltage on the SENSEL pin can be routed to the on-chip comparator. Use the DIN\_UNBUF\_EN bit in the DIN\_CONFIG2 register to bypass the input buffer if high speed digital input data rates are required. See [Table 9](#) for buffered and unbuffered data rates.

This comparator compares the voltage on the selected pin to a programmable threshold that can either be a fixed voltage or a

voltage proportional to the V<sub>AVDD</sub>. See the [Digital Input Threshold Setting](#) section for more information on the programmable threshold voltages.

The output of the comparators can be debounced (see the [Debounce Function](#) section), passed directly, or inverted to the SPI and/or to the GPIO\_A pin.

The digital input comparator outputs are monitored by reading from the DIN\_COMP\_OUT register. The comparator outputs can also be monitored with the GPIO\_A pin. The GPIO\_A pin is configured via the GPIO\_CONFIGx register to drive out the debounced comparator output signal.

[Figure 41](#) shows the current, voltage, and output paths of the digital input, loop powered mode configuration.

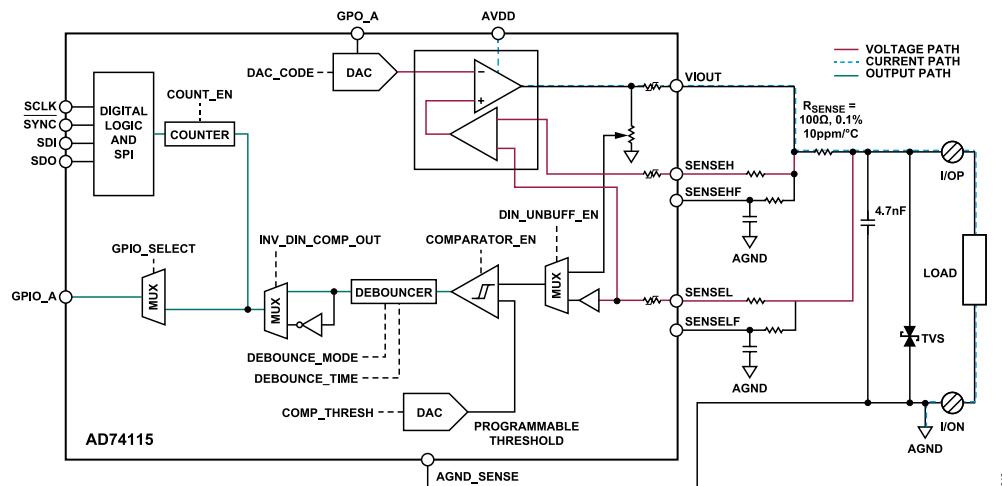


Figure 41. Digital Input, Loop Powered Configuration Mode

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### Interpreting ADC Data

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements when the digital input, loop powered mode is enabled. In digital input, loop powered mode, the ADC, by default, measures the voltage across the I/O/P to I/ON screw terminals in a 0 V to 12 V range. Use the ADC measurement result to calculate this voltage by using the following equation:

$$V_{ADC} = (ADC\_CODE/65,536) \times \text{Voltage Range}$$

where:

$V_{ADC}$  is the measured voltage in volts.

$ADC\_CODE$  is the value of the  $ADC\_RESULT1$  register.

*Voltage Range* is 12 V, the measurement range of the ADC.

### Digital Output

The AD74115 supports sourcing and sinking digital outputs. An internal digital output function is available for sourcing or sinking up to 100 mA continuous current. For currents higher than 100 mA, use the external digital output function. A push-pull feature is also available that combines both the source and sink capabilities to provide high speed, high voltage switching.

When the digital output functionality is enabled, the recommended configuration of the  $CH\_FUNC\_SETUP$  register is to set it to high impedance.

### Sourcing and Sinking Currents Greater Than 100 mA

The external sourcing digital output operates with an external, P-channel field effect transistor (PFET), and the sinking digital output operates with external N-channel FET (NFET). Push-pull mode uses both PFET and NFET. Choose the FET types to suit the application requirements. Determine the absolute current value by

the  $R_{SET}$  and short-circuit voltage values. Short-circuit voltages are indicated in the [Table 11](#).

Configure the digital output using the  $DO\_EXT\_CONFIG$  register:

- ▶ Select source, sink, or push-pull capability by using the  $DO\_EXT\_MODE$  bits.
- ▶ Select the source of the data for the digital output circuit using the  $DO\_EXT\_SRC\_SEL$  bit. The digital output data can be provided by the SPI (via the  $DO\_DATA\_EXT$  bit) or by the  $GPIO\_B$  pin for direct hardware control of the circuits.
- ▶ Configure the short-circuit timers using the  $DO\_EXT\_T1$  and  $DO\_EXT\_T2$  bits. See the [Short-Circuit Protection](#) section for more information on short-circuit functionality. Note that T1 short-circuit limits are not available in push-pull mode

Once the configuration settings are applied, provide stimulus to turn on the selected external FET. For SPI control, a new write is required to the  $DO\_EXT\_CONFIG$  register, to set the  $DO\_DATA\_EXT$  bit. Setting the  $DO\_DATA\_EXT$  to 1 turns on the selected external FET. In push-pull mode, set the bit to 0 to drive a low on the output and to 1 to drive a high on the output.

For GPIO control, configure the  $GPIO\_B$  pin to control the digital output circuit by writing 0x0004 to the  $GPIO\_CONFIG1$  register. Drive the  $GPIO\_B$  pin high to turn on the FET. In push-pull mode, set the  $GPIO\_B$  pin low for a low on the output and high for a high on the output.

If changing from one digital output function to another, first disable the digital output function before changing to the new mode (set  $DO\_EXT\_MODE$  to digital output external disable).

[Figure 42](#) shows the current and voltage paths of the sourcing digital output mode with the external FET. [Figure 43](#) shows the current and voltage paths of the sinking digital output mode with the external FETs.

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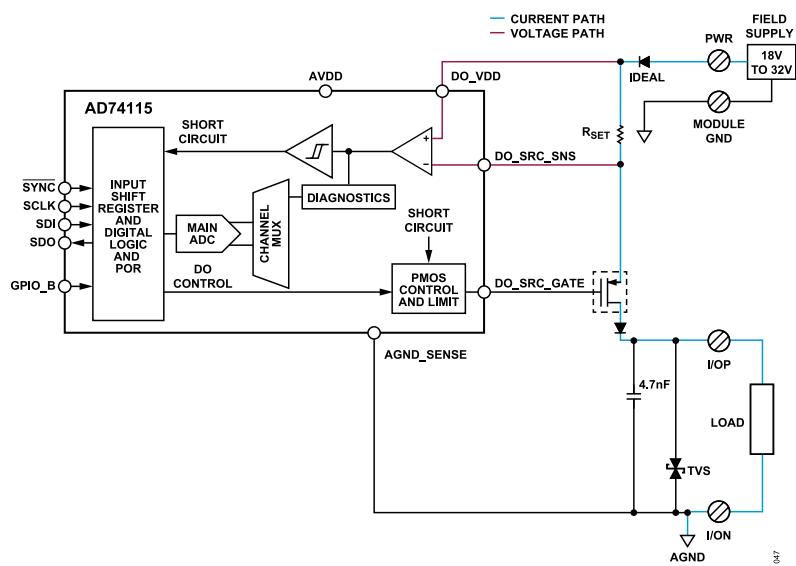


Figure 42. Digital Outputs Sourcing with External FET

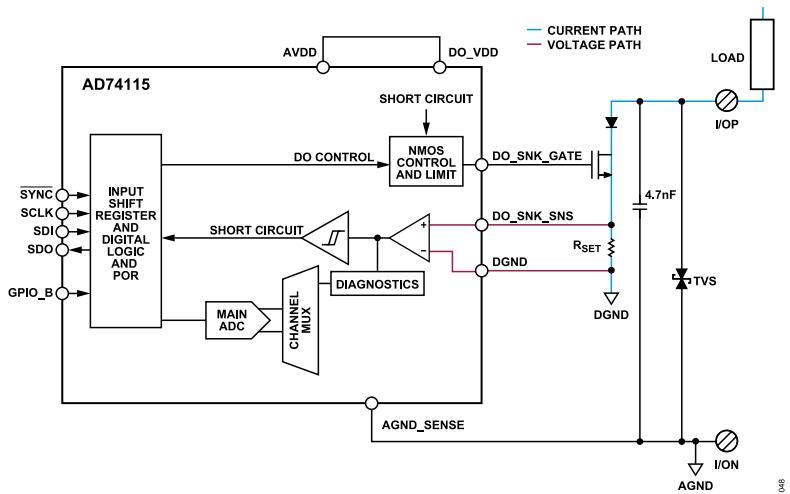


Figure 43. Digital Output Sinking with External FET

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### Smart Diode

In current sourcing applications, a blocking diode is typically placed in series with the output FETs to ensure that the digital output path is protected against reverse overvoltage conditions (when the I/O/P screw terminal voltage is greater than the DO\_VDD voltage,  $V_{DO\_VDD}$ ). This typical configuration is shown in Figure 42.

Significant power can be dissipated in this diode when the digital output circuit is sourcing high currents (for example, a 500 mA current source and a diode drop of 0.5 V generates 250 mW of power).

The AD74115 has a smart diode feature when using the external digital output function. An additional FET is connected, along with a resistor and protection Zener, as shown in Figure 44. The gate of the FET is controlled by the DO\_SRC\_DGATE pin. When the FET is disabled, the body diode of the FET conducts. When the FET is enabled, the power dissipated is calculated by  $P = I^2R$ , where  $I$  is the sourced current, and  $R$  is the  $R_{ON}$  of the FET. Typically, the power dissipation in this scenario is <50 mW.

To enable the smart diode option, set DO\_EXT\_MODE to an external source with a smart diode in the DO\_EXT\_CONFIG register.

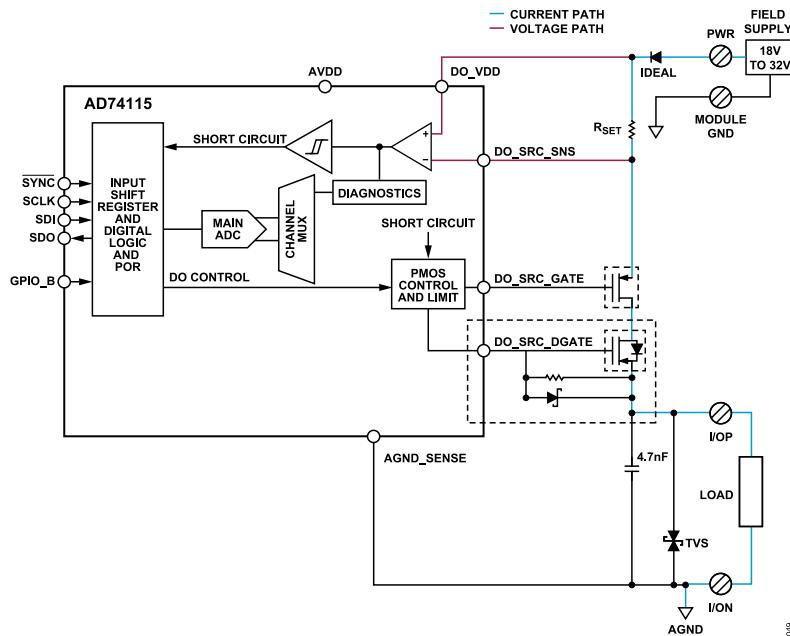


Figure 44. Smart Diode Configuration for Current Sourcing with an External FET

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## Sourcing and Sinking Currents up to 100 mA

Internal FETs are available to source or sink up to 100 mA continuous current. A 200 mA start-up current is also accommodated. Using the internal FETs to provide the digital output current eliminates the need for external FETs. Push-pull mode uses both the sourcing and sinking internal FETs. Configure the digital output using the DO\_INT\_CONFIG register:

- ▶ Select source, sink, or push-pull capability using the DO\_INT\_MODE bits.
- ▶ Select the source of the data for the digital output circuit using the DO\_INT\_SRC\_SEL bit. The digital output data can be provided by SPI (via the DO\_DATA\_INT bit) or by the GPIO\_C pin for faster output rates.
- ▶ Configure the short-circuit timers using the DO\_INT\_T1 and DO\_INT\_T2 bits. See the [Short-Circuit Detection](#) section for more information on short-circuit functionality. Note that T1 short-circuit limits are not available in push-pull mode.

Once the configuration settings are applied, a new write is required to the DO INT CONFIG register, to set the DO DATA INT bit.

Setting the `DO_DATA_INT` to 1 turns on the selected FET. In push-pull mode, set the bit to 0 to drive a low on the output and to 1 to drive a high on the output.

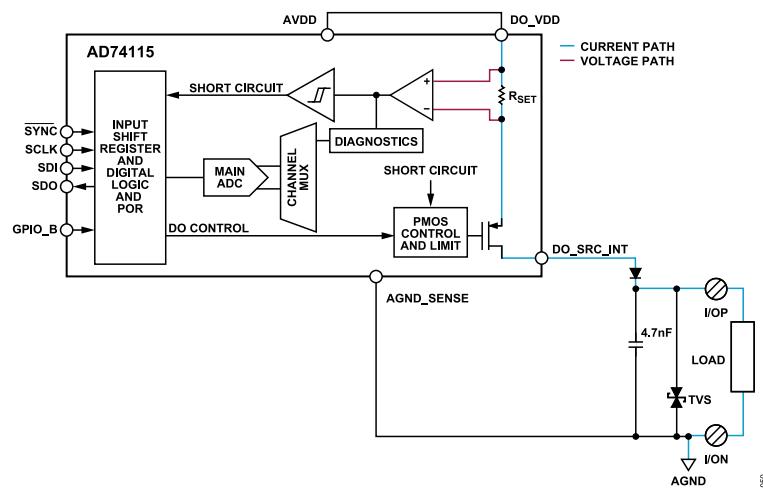
For GPIO control, configure the GPIO\_C pin to control the digital output circuit by writing 0x0004 to the GPIO\_CONFIG2 register. Drive the GPIO\_C pin high to turn on the FET. In push-pull mode, set the pin low for a low on the output and high for a high on the output.

If changing from one digital output function to another, first disable the digital output function before changing to the new mode (set DO\_INT\_MODE to digital output internal disable).

The power and isolation companion chip, [ADP1034](#), can provide the power required to operate the AD74115 in digital output mode (using the internal FETs) sourcing continuous currents up to 100 mA. The ADP1034 also accommodates the 200 mA start-up current. In this case, the AVDD pin can be externally connected to the DO\_VDD pin, eliminating the need for an additional DO\_VDD supply source.

Figure 45 shows the current and voltage paths of the digital output sourcing mode with the internal FET.

Figure 46 shows the current and voltage paths of the digital output sinking mode with the internal FET.



**Figure 45. Digital Output Sourcing Mode with the Internal FET**

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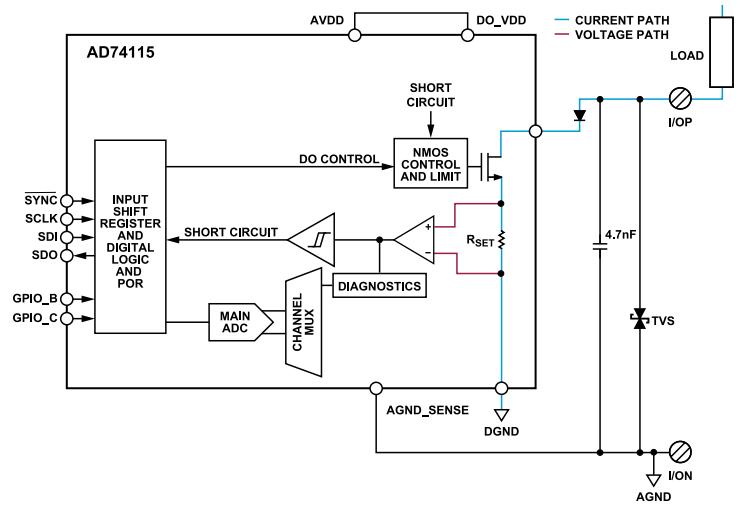


Figure 46. Digital Output Sinking Mode with the Internal FET

### Thermal Shutdown

When the internal digital output is enabled, a thermal shutdown function is automatically enabled to protect the AD74115 in short-circuit scenarios.

If the output drivers reach the disable temperature specified in [Table 11](#), the digital output is disabled. The DO\_THERM\_RESET bit is set in the ALERT\_STATUS register to indicate that thermal shutdown of the digital output circuit has occurred.

Once the die temperature reaches the specified reenabled temperature in [Table 11](#), the digital output circuit attempts to turn back on. If the high power dissipation condition persists, the die quickly reaches the disabled temperature again. Take care to manage the power dissipation to prevent multiple disable and reenable cycles on the internal digital output.

### Short-Circuit Protection

When using the external digital output, short-circuit protection is achieved using a current-limit setting resistor,  $R_{SET}$ . A short-circuit event is triggered when the voltage developed across the resistor reaches the short-circuit voltage specified in [Table 11](#). In the event of a short circuit, the DO\_EXT\_SC bit is set in the ALERT\_STATUS register, which in turn asserts the ALERT pin.

When using the internal digital output, a short circuit is triggered when the current reaches the short-circuit current limit specified in [Table 11](#). In the event of a short circuit, the DO\_INT\_SC bit is set in the ALERT\_STATUS register, which in turn asserts the ALERT pin.

There is programmability around how the short-circuit behavior operates. The two configurable short-circuit timeout times are T1 and T2.

To support charging of large current loads on initial power-on of the digital output load, a higher short-circuit current limit can be enabled for a programmable amount of time, T1. The T1 timer starts once

the digital output FET is turned on using the DO\_DATA\_INT or DO\_DATA\_EXT bit (for internal FETs or external FETs, respectively), even if no short-circuit event was triggered. If a short-circuit event occurs, the digital output FET remains on, clamped at the higher short-circuit current for the remainder of the programmed duration of T1. The short-circuit alert is not triggered during this time.

A second short-circuit limit is deployed once the T1 time elapses. Lower current limit is active for a programmable duration of time, T2. The T2 timer only starts if T1 expires and a short circuit is detected. The FET remains on during a short-circuit event, but the current is limited to the lower short-circuit current for the programmed duration of T2.

If the short circuit continues to persist after the T2 time expires, the FET automatically disables. Once disabled, the relevant digital output timeout bit is set in the ALERT\_STATUS register. The digital output is disabled, which is reflected in the DO\_EXT\_CONFIG register or the DO\_INT\_CONFIG register for the external digital output or the internal digital output, respectively.

T1 and T2 can be programmed in the DO\_EXT\_CONFIG register for external FETs or DO\_INT\_CONFIG register for internal FETs. If the higher short-circuit current limit is not required, T1 can be bypassed. See [Table 11](#) for the specified short-circuit values and T1 and T2 durations for both internal and external modes of operation.

[Figure 47](#) illustrates the operation of the two programmable timeout times along with the short-circuit current limits.

To reenable the digital output circuit after a timeout event:

- ▶ Set the DO\_DATA\_INT or DO\_DATA\_EXT bit to 0
- ▶ Choose a mode in the DO\_INT\_MODE or DO\_EXT\_MODE bits in the relevant configuration register to power on the digital output circuit

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- ▶ Set the DO\_DATA\_INT or DO\_DATA\_EXT bit back to 1 to enable the FET.

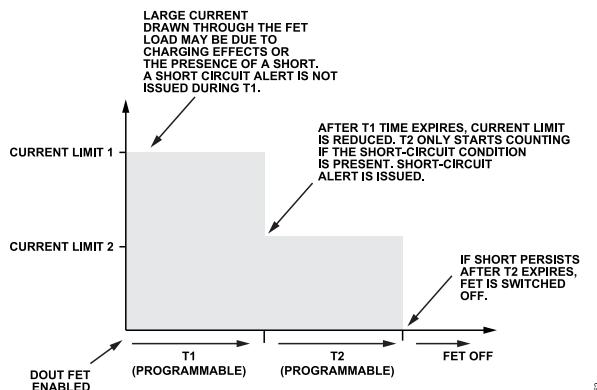


Figure 47. Digital Output Programmable Short-Circuit Control

### Current Sensing Diagnostic

A digital output, current sense diagnostic is available to monitor the current in the digital output circuit.

Select the current sense diagnostics by programming the DI-AG\_ASSIGN register.

When using external FETs, the diagnostic (Diagnostic 0 for the sinking current and Diagnostic 1 for the sourcing current) measures the voltage dropped across the external  $R_{SET}$  resistor. Consider the resistance of the selected  $R_{SET}$  when calculating the current being sourced or sinked by the digital output circuit. Note that if Diagnostic 1 is required to measure sourcing current in the external digital output circuit, and Diagnostic 0 must also be enabled in the ADC\_CONV\_CTRL register to guarantee measurement accuracy. Any diagnostic setting of choice can be selected on Diagnostic 0. Consider the additional enabled diagnostics when calculating conversion times.

When using internal FETs, the diagnostic (Diagnostic 2 for the sinking current, and Diagnostic 3 for the sourcing current) measures

the current being sourced or sinked by the digital output circuit. Use the equations in Table 28 to determine the current from the returned ADC code, which is read in the ADC\_DIAG\_RESULTx register. Note that, if Diagnostic 3 is required to measure sourcing current in the internal digital output circuit, Diagnostic 2 must also be enabled in the ADC\_CONV\_CTRL register to guarantee measurement accuracy. Any diagnostic setting of choice can be selected on Diagnostic 3. Consider the additional enabled diagnostics when calculating conversion times.

## GETTING STARTED

Power up the AD74115 as recommended in [Powering on the AD74115](#) section. After initial power-up, the ALERT pin is pulled low as a result of various bits, such as the RESET\_OCCURRED bit being set in the ALERT\_STATUS register. It is recommended to clear the ALERT\_STATUS register before continuing to use the AD74115. Write 1 to clear each bit in the ALERT\_STATUS register.

### Using Channel Functions

The channel function is selected using the CH\_FUNC\_SETUP register. Once a channel function is selected, the contents of a number of registers are updated with predefined values, which allows the user to configure the device with a minimal set of commands.

The updated settings include configuration of the ADC channel, Conversion 1. Table 21 outlines the default settings of the bits for any given channel function. In addition to the default settings described in Table 21, these bit fields are set to the following values, irrespective of the CH\_FUNC\_SETUP selection:

- ▶ RTD\_MODE\_SEL in the RTD3W4W\_CONFIG register is set to 0 (selects 3-wire RTD)
- ▶ RTD\_CURRENT in the RTD3W4W\_CONFIG register is set to 11 binary (selects 1 mA)
- ▶ DIN\_SINK in the DIN\_CONFIG1 register is set to 0 (ISINK off)
- ▶ DIN\_THRESH\_MODE in the DIN\_CONFIG2 register is set to 0 (threshold relative to AVDD)

Table 21. Register Defaults Based on Channel Function Selection

| CH_FUNC Bits (Programmed via the CH_FUNC_SETUP Register) | Defaults of the ADC_CONFIG Register |                       | Defaults of the DIN_CONFIG1 Register | Defaults of the DIN_CONFIG2 Register |
|--|-------------------------------------|-----------------------|--------------------------------------|--------------------------------------|
|  | CONV1_MUX Bits                      | CONV1_RANGE Bits      |                                      |                                      |
| 0000: High Impedance                                     | 00: SENSELF to AGND_SENSE           | 000: 0 V to 12 V      | 0: disabled                          | 0: $-0.96 \times AVDD$               |
| 0001: Voltage Output                                     | 01: SENSEHF to SENSELF              | 010: -2.5 V to +2.5 V | 0: disabled                          | 0: $-0.96 \times AVDD$               |
| 0010: Current Output                                     | 00: SENSELF to AGND_SENSE           | 000: 0 V to 12 V      | 0: disabled                          | 0: $-0.96 \times AVDD$               |
| 0011: Voltage Input                                      | 00: SENSELF to AGND_SENSE           | 000: 0 V to 12 V      | 0: disabled                          | 0: $-0.96 \times AVDD$               |
| 0100: Current Input, Externally Powered                  | 01: SENSEHF to SENSELF              | 011: -2.5 V to 0 V    | 1: enabled                           | 0x49: AVDD/2                         |
| 0101: Current Input, Loop Powered                        | 01: SENSEHF to SENSELF              | 100: 0 V to 2.5 V     | 1: enabled                           | 0x49: AVDD/2                         |

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Table 21. Register Defaults Based on Channel Function Selection (Continued)

| CH_FUNC Bits (Programmed via the CH_FUNC_SETUP Register) | Defaults of the ADC_CONFIG Register |                     | Defaults of the DIN_CONFIG1 Register | Defaults of the DIN_CONFIG2 Register |
|--|-------------------------------------|---------------------|--------------------------------------|--------------------------------------|
|  | CONV1_MUX Bits                      | CONV1_RANGE Bits    |                                      |                                      |
| 0110: 2-Wire Resistance Measurement                      | 00: SENSELF to AGND_SENSE           | 100: 0 V to 2.5 V   | 0: disabled                          | 0: $-0.96 \times \text{AVDD}$        |
| 0111: 3- or 4-wire RTD Measurement                       | 11: SENSELF to SENSE_EXT1           | 101: 0 V to 0.625 V | 0: disabled                          | 0: $-0.96 \times \text{AVDD}$        |
| 1000: Digital Input Logic                                | 00: SENSELF to AGND_SENSE           | 000: 0 V to 12 V    | 1: enabled                           | 0x49: $\text{AVDD}/2$                |
| 1001: Digital Input, Loop Powered                        | 00: SENSELF to AGND_SENSE           | 000: 0 V to 12 V    | 1: enabled                           | 0x49: $\text{AVDD}/2$                |

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### Switching Channel Functions

Take care when switching from one channel function to another. All functions must be selected for a minimum of 200  $\mu$ s before changing to another function.

The DAC\_CODE register is not reset by changing channel functions. Before changing channel functions, it is recommended to set the DAC code to 0x0000 via the DAC\_CODE register. Set the channel function to high impedance via the CH\_FUNC\_SETUP register before transitioning to the new channel function.

For  $\pm 12$  V voltage output, the DAC\_CODE can be updated to 0x2000 before the voltage output is enabled to ensure that the output stage powers up to 0 V. Refer to the [Voltage Output](#) section.

After the new channel function is configured, it is recommended to wait 200  $\mu$ s before updating the DAC code.

### ADC FUNCTIONALITY

The AD74115 provides a single, 16-bit  $\Sigma$ - $\Delta$  ADC that can be sequenced to measure up to two channel measurements and up to four diagnostics measurements for a single conversion sequence or for continuous conversions. The two channel measurements allow for various voltage and current monitoring options on the I/O/P screw terminal and the auxiliary high voltage SENSE\_EXT1 and SENSE\_EXT2 pins.

Conversion 1 is targeted at supporting the measurements required for each of the AD74115 use cases. [Table 22](#) shows the measurements available for Conversion 1. When any mode of operation is selected in the CH\_FUNC\_SETUP register, Conversion 1 is configured to a default measurement. These default measurements are described in the [Using Channel Functions](#) section.

Conversion 2 can be used for additional diagnostics measurements on the channel or to monitor other external nodes. [Table 23](#) shows the measurements available for Conversion 2.

**Table 22. Selection Options for ADC Conversion 1**

| CONV1_MUX Settings in the ADC_CONFIG Register | Measurement Selection    | Description   |
|---|--------------------------|---|
| 00  | SENSELF to AGND_SENSE    | Voltage measurement across the I/O/P and I/ON screw terminals                   |
| 01  | SENSEHF to SENSELF       | Voltage measurement across the $R_{SENSE}$ resistor                             |
| 10  | SENSE_EXT2 to SENSE_EXT1 | Voltage measurement across SENSE_EXT2 and SENSE_EXT1 for 4-wire RTD measurement |
| 11  | SENSELF to SENSE_EXT1    | Voltage measurement across SENSE_EXT1 and SENSELF for 3-wire RTD measurement    |

**Table 23. Selection Options for ADC Conversion 2**

| CONV2_MUX Settings in the ADC_CONFIG Register | Measurement Selection    | Description                                    |
|---|--------------------------|--|
| 00  | SENSE_EXT1 to AGND_SENSE | Enables single-ended monitor of SENSE_EXT1 pin |
| 01  | SENSE_EXT2 to AGND_SENSE | Enables single-ended monitor of SENSE_EXT2 pin |
| 10  | SENSE_EXT2 to SENSE_EXT1 | Enables differential measurements              |
| 11  | AGND to AGND             | Diagnostic                                     |

Each conversion has an individual conversion rate and voltage range control that can be configured in the ADC\_CONFIG register.

The ADC also provides diagnostic information on user-selectable inputs such as supplies, internal die temperature, reference, and regulators. See the [Diagnostics](#) section for more information on the diagnostics measurements.

After the measurements are configured in the ADC\_CONFIG register, enable the relevant ADC measurements via the ADC\_CONV\_CTRL register.

Select either single conversion or continuous conversion mode by setting the appropriate value to the CONV\_SEQ bits in the ADC\_CONV\_CTRL register.

In single conversion mode, the ADC sequencer starts conversions on Conversion 1 and Conversion 2 followed by the enabled diagnostics. After each enabled input is converted once, the ADC enters idle mode, and conversions are stopped.

In continuous conversion mode, the ADC channel sequencer continuously converts the enabled channel conversions and each enabled diagnostic until a command is written to stop the conversions. Exit continuous conversion mode by setting the CONV\_SEQ bits in the ADC\_CONV\_CTRL register to idle mode or power-down mode. The issued command stops conversions at the end of the current sequence.

If the measurement configuration requires a change, continuous conversions must be stopped before making the changes. Restart the continuous conversions after making the appropriate changes.

After a sequence is complete, all data results are transferred to the relevant ADC\_RESULT1, ADC\_RESULT2, and ADC\_DIAG\_RESULTn registers and the  $\overline{ADC\_RDY}$  pin is asserted.

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### Auxiliary Sense Pins

The SENSE\_EXT1 and SENSE\_EXT2 pins are uncommitted high voltage sense pins that can be measured with the ADC. These pins can be used for a number of functions.

The SENSE\_EXT1 and SENSE\_EXT2 pins can be used for single-ended or differential voltage measurements using ADC Conversion 2. An appropriate antialiasing filter can be added to the pin being measured. See [Table 35](#) for example components. Use the ADC result to calculate the voltage measured on the relevant sense pin by using the following equation:

$$V_{ADC} = V_{MIN} + (ADC\_CODE/65,536) \times \text{Voltage Range}$$

where:

$V_{MIN}$  is the minimum input voltage of the selected ADC range.

$V_{ADC}$  is the measured voltage in volts.

$ADC\_CODE$  is value of the ADC\_RESULT2 register.

*Voltage Range* is the selected measurement range of the ADC.

SENSE\_EXT1 is required for 3-wire RTD measurements. See the [3-Wire RTD Measurements](#) section for more detail. SENSE\_EXT1 and SENSE\_EXT2 are required for 4-wire RTD measurements. See the [4-Wire RTD Measurements](#) section for more details.

If either SENSE\_EXT1 or SENSE\_EXT2 pins are unused for an extended time, it is recommended to enable a sinking burnout current of 1  $\mu$ A. Enable the burnout current on SENSE\_EXT1 by programming the following bits in the I\_BURNOUT\_CONFIG register:

- ▶ BRN\_SENEXT1\_EN to 1
- ▶ BRN\_SENEXT1\_POL to 0
- ▶ BRN\_SENEXT1\_CURR to 100 binary

Enable the burnout current on SENSE\_EXT2 by programming the following bits in the I\_BURNOUT\_CONFIG register:

- ▶ BRN\_SENEXT2\_EN to 1
- ▶ BRN\_SENEXT2\_POL to 0
- ▶ BRN\_SENEXT2\_CURR to 100 binary

### ADC Transfer Function

[Table 24](#) shows the ideal input voltage for zero-scale, midscale, and full-scale codes for each of the available voltage ranges when measuring voltages with the on-board ADC.

Currents through the external  $R_{SENSE}$  resistor are determined by measuring the voltage across  $R_{SENSE}$ . Set the CONV1\_MUX bits to measure between SENSEHF and SENSELF. [Table 25](#) shows the ideal input currents for zero-scale, midscale, and full-scale codes using each available voltage range (to calculate current, measured voltage is divided by the  $R_{SENSE}$  value, 100  $\Omega$ .)

If the voltage measured by the ADC is either more than full scale or less than zero scale, an ADC\_ERR bit is set in the ALERT\_STATUS registers, asserting the ALERT pin. In this case, the ADC output reads 0xFFFF or 0x0000, respectively. The ADC\_ERR bit can be masked via the ALERT\_MASK register (optional) if these alerts are not required.

**Table 24. Ideal Output Code to Input Voltage Relationship**

| Input Voltage Range | Input Voltage for Selected ADC Codes <sup>1</sup> |           |                   |
|---------------------|---|-----------|-------------------|
|                     | 0x0   | 0x8000    | 0xFFFF            |
| 0 V to +12 V        | 0 V   | +6 V      | 12 V – 1 LSB      |
| $\pm 12$ V          | -12 V   | 0 V       | 12 V – 1 LSB      |
| $\pm 2.5$ V         | -2.5 V  | 0 V       | 2.5 V – 1 LSB     |
| 0 V to +2.5 V       | 0 V   | +1.25 V   | 2.5 V – 1 LSB     |
| -2.5 V to 0 V       | 0 V   | -1.25 V   | -2.5 V – 1 LSB    |
| $\pm 104.16$ mV     | -104.16 mV  | 0 V       | 104.16 mV – 1 LSB |
| 0 V to +0.625 V     | 0 V   | +0.3125 V | 0.625 V – 1 LSB   |

<sup>1</sup> 1 LSB = (Full Scale – Zero Scale)/65,536.

**Table 25. Ideal Output Code to Input Current Relationship**

| Input Voltage Range | Input Current for Selected ADC Codes <sup>1</sup> |         |                          | Sourcing or Sinking |
|---------------------|---|---------|--------------------------|---------------------|
|                     | 0x0   | 0x8000  | 0xFFFF                   |                     |
| $\pm 2.5$ V         | -25 mA (Sinking)                                  | 0 mA    | 25 mA – 1 LSB (sourcing) | Sink and source     |
| 0 V to +2.5 V       | 0 mA  | 12.5 mA | 25 mA – 1 LSB            | Sourcing            |
| -2.5 V to 0 V       | 0 mA  | 12.5 mA | 25 mA – 1 LSB            | Sinking             |

<sup>1</sup> 1 LSB = (Full Scale – Zero Scale)/65,536.

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### Saving Power When Using the ADC

Each of the high voltage sense pins available for measurement by the ADC (SENSEHF, SENSELF, SENSE\_EXT1, and SENSE\_EXT2) has a high voltage buffer that is powered up by default. The typical current drawn from each of these buffers is specified in [Table 13](#).

If any of the sense pins are not required for measurement by the ADC, the high voltage buffer associated with that pin can be put in standby mode to save total power consumption by the AD74115. Configure the AD74115 into the desired channel function and put any of the high voltage sense pin buffers in standby. Buffers are put into standby by setting the appropriate bit in the PWR\_OPTIM\_CONFIG register. Wait for the appropriate power-up time, specified in [Table 13](#), when taking the buffers out of standby mode.

For optimal performance, power up the buffers before starting the conversion sequence.

Do not update the PWR\_OPTIM\_CONFIG settings while an ADC conversion sequence is taking place.

### ADC Conversion Rates

The ADC on the AD74115 is available at precision conversion and fast conversion subsets of values. The ADC conversions rates must be configured in one subset of values at a time.

The precision conversion subset includes the following subset of conversion rates: 10 SPS, 20 SPS, 1.2 kSPS, and 4.8 kSPS. In addition, 50 Hz and 60 Hz rejection is provided on the 10 SPS and 20 SPS conversion rates.

The fast conversion subset allows the user to configure the device conversion rates without filtering. Fast conversion rates are 1.2 kSPS, 4.8 kSPS, and 9.6 kSPS.

Configure each of the channel conversion rates via the ADC\_CONFIG register. The conversion rate of the diagnostics inputs is set via the ADC\_CONV\_CTRL register. One conversion rate selection applies to all diagnostic inputs.

The time it takes for a sequence of conversions to complete is dependent on several factors, such as the number of selected inputs, the selected conversion rates, and whether single or continuous mode conversions are enabled. Conversions are clocked by an on-chip oscillator. [Table 26](#) outlines the various components required to estimate a complete conversion time for any given sequence.

For single conversions, consider the following time components when calculating the overall sequence time:

**Table 26. Conversion Times Components**

| Conversion Rate | ADC and/or Buffer Power-Up Time (μs) | SPI Transfer Time (μs), 42 ns SCLK | Start-Up Pipeline Delay (μs) | Single ADC Conversion Time | Channel Switch Time, Multiple Enabled Conversions (μs) |
|-----------------|--------------------------------------|------------------------------------|------------------------------|----------------------------|--|
| 9.6 kSPS        | 100                                  | 1.99                               | 55                           | 104.17 μs                  | 24.4   |

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers, if previously powered down.
- The initial pipeline delay before the first conversion.
- The conversion time for each ADC conversion.

[Figure 48](#) shows the timing breakdown of a single conversion example. In this example, the ADC and high voltage buffers are in a power-down state before a single conversion on the channel is enabled, and continuous conversions are initiated with a 4.8 kSPS conversion rate.

The time to the first complete conversion (the SYNC pin falling edge to the ADC\_RDY pin falling edge) is 391.32 μs and is calculated by adding the SPI transfer time, the ADC and high voltage buffer power-up time, the pipeline delay time, and the conversion rate on the channel at 4.8 kSPS (208.33 μs). The time between conversions (the ADC\_RDY pin falling edge to the ADC\_RDY pin falling edge) is 208.33 μs.

For multiple conversions, consider the following components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers, if previously powered down.
- An initial pipeline delay before the first conversion.
- The conversion time required for each ADC conversion.
- The channel switch time for each time the selected ADC channel is switched.

[Figure 49](#) shows an example of the timing breakdown for a multichannel conversion. In this example, Conversion 1, Conversion 2, Diagnostic 1, and Diagnostic 2 are all enabled. Continuous conversions are initiated with a 20 SPS conversion rate. In this example, the ADC is in idle mode, and the high voltage buffers are powered up.

The time it takes for the first complete conversion (SYNC falling edge to ADC\_RDY falling edge), is 200.190 ms and is calculated by adding the SPI transfer time, the pipeline delay time, and the conversion time on Conversion 1 at 20 SPS, followed by adding the channel switch time and conversion time for the remaining three conversions.

The time between all subsequent conversion sequences (the ADC\_RDY pin falling edge to the ADC\_RDY pin falling edge) is 200.134 ms and is calculated by adding the channel switch time with the conversion time for the four selected ADC inputs.

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Table 26. Conversion Times Components (Continued)

| Conversion Rate | ADC and/or Buffer Power-Up Time (μs) | SPI Transfer Time (μs),<br>42 ns SCLK | Start-Up Pipeline Delay (μs) | Single ADC Conversion Time | Channel Switch Time, Multiple Enabled Conversions (μs) |
|-----------------|--------------------------------------|---------------------------------------|------------------------------|----------------------------|--|
| 4.8 kSPS        | 100                                  | 1.99                                  | 81                           | 208.33 μs                  | 24.4   |
| 1.2 kSPS        | 100                                  | 1.99                                  | 81                           | 833.33 μs                  | 24.4   |
| 20 SPS          | 100                                  | 1.99                                  | 87                           | 50 ms                      | 33.6   |
| 10 SPS          | 100                                  | 1.99                                  | 5000                         | 100 ms                     | 5024   |

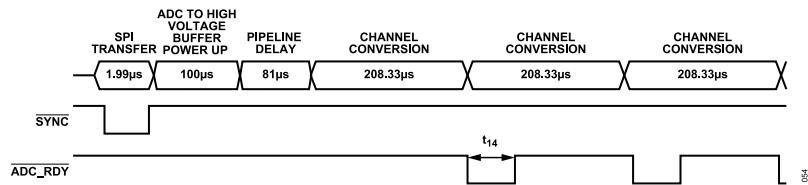


Figure 48. Single Measurement, Continuous Conversions Timing Diagram

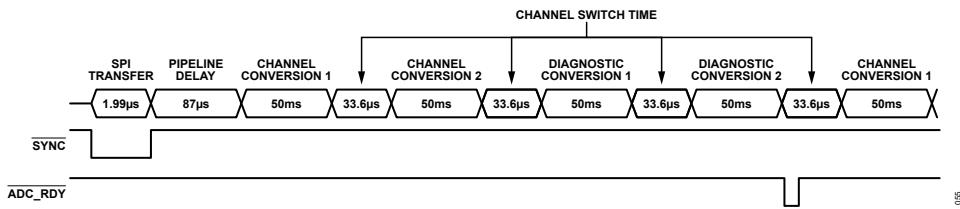


Figure 49. Multiple Measurements, Continuous Conversions Timing Diagram

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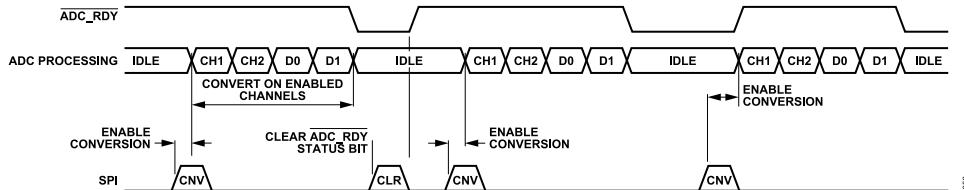
### ADC\_RDY Functionality

The ADC\_RDY pin asserts low at the end of a sequence of conversions for either single conversion or continuous conversion mode.

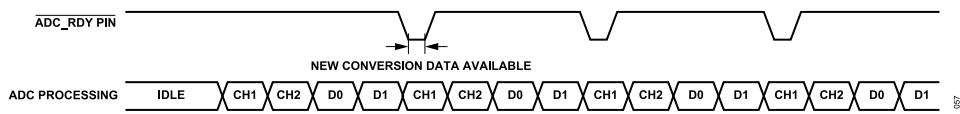
The ADC\_RDY pin deasserts in any of the following scenarios:

- ▶ After a 1 is written to the ADC\_DATA\_RDY status bit in the LIVE\_STATUS register
- ▶ After 24  $\mu$ s in continuous mode
- ▶ After writing to the ADC\_CONV\_CTRL register

See [Figure 50](#) and [Figure 51](#) for timing diagrams of the ADC\_RDY pin in single and continuous conversion modes.



**Figure 50.** ADC\_RDY Functionality in Single Conversion Mode



**Figure 51.** ADC\_RDY Functionality in Continuous Conversion Mode

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### ADC Noise

Table 27 shows the peak-to-peak noise of the AD74115 for each of the output data rates and voltage ranges. These numbers are

typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel.

Table 27. Peak-to-Peak Noise in LSBs per Voltage Range and Output Data Rate (Inputs Shorted)

| Output Data Rate | +12 V Range (LSBs) | ±12 V Range (LSBs) | +2.5 V Range (LSBs) | ±2.5 V Range (LSBs) | +0.625 V Range (LSBs) | ±104 mV Range (LSBs) |
|------------------|--------------------|--------------------|---------------------|---------------------|-----------------------|----------------------|
| 10 SPS           | 0.1                | 0.07               | 0.16                | 0.08                | 0.3                   | 0.7                  |
| 20 SPS           | 0.2                | 0.1                | 0.2                 | 0.1                 | 0.5                   | 1.0                  |
| 1.2 kSPS         | 1.1                | 0.5                | 1.4                 | 0.7                 | 3.0                   | 8.9                  |
| 4.8 kSPS         | 2.7                | 1.4                | 3.6                 | 1.8                 | 8.5                   | 18.1                 |
| 9.6 kSPS         | 6.0                | 3.0                | 7.2                 | 3.6                 | 17.9                  | 33.3                 |

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## Diagnostics

The AD74115 has a diagnostic function that allows the ADC to measure various on-chip voltages. These diagnostic voltages are scaled to be measurable within the ADC range.

The diagnostics inputs are independent of the two available channel measurements of the AD74115. The DIAG\_ASSIGN register assigns the voltage measurements to each diagnostic input. Select a diagnostic input to be measured by the ADC by enabling that input in the ADC\_CONV\_CTRL register. Users can also select the conversion rate via the ADC\_CONV\_CTRL register. The follow-

ing three conversion rates are available for selection within the ADC\_CONV\_CTRL register: 9.6 kSPS, 4.8 kSPS, and 20 SPS. In addition, 50 Hz and 60 Hz rejection is provided on the 20 SPS conversion rate.

**Table 28** shows a full list of available diagnostics, and the equations required to calculate the diagnostic value.

In the equations listed in **Table 28**, DIAG\_CODE is the ADC result code read from the ADC\_DIAG\_RESULTn registers, and the voltage range is the ADC measurement range and is 2.5 V.

**Table 28. User-Selectable Diagnostics<sup>1</sup>**

| Diagnostic  | Formula to Interpret ADC Result   | Measurement Range  |
|---|---|--|
| V <sub>AGND</sub>   | $V_{AGND} = \frac{DIAG\_CODE}{65,536} \times 2.5$                           | 0 V to 2.5 V   |
| Temperature Sensor (Internal Die Temperature Measurement)/°C                      | $Temperature = \left( \frac{DIAG\_CODE - 2034}{8.95} \right) - 40$          | See <b>Table 16</b> for recommended maximum junction temperature                       |
| Voltage on AVDD Pin (V <sub>AVDD</sub> )  | $V_{AVDD} = \frac{DIAG\_CODE}{65,536} \times 50$                            | 0 V to 50 V  |
| Voltage on DLDO1V8 Pin (V <sub>DLDO1V8</sub> )                                    | $V_{DLDO1V8} = \frac{DIAG\_CODE}{65,536} \times 7.5$                        | 0 V to 7.5 V   |
| Voltage on AVSS Pin (V <sub>AVSS</sub> )  | $V_{AVSS} = \left( \frac{DIAG\_CODE}{65,536} \times 31.017 \right) - 20$    | -20 V to +11 V   |
| Voltage on REFOUT Pin (V <sub>REFOUT</sub> )                                      | $V_{REFOUT} = \frac{DIAG\_CODE}{65,536} \times 3.125$                       | 0 V to 3.125 V   |
| Voltage on AVCC Pin (V <sub>AVCC</sub> )  | $V_{AVCC} = \frac{DIAG\_CODE}{65,536} \times 17.5$                          | 0 V to 17.5 V  |
| Voltage on ALDO1V8 Pin (V <sub>ALDO1V8</sub> )                                    | $V_{ALDO1V8} = \frac{DIAG\_CODE}{65,536} \times 5.825$                      | 0 V to 5.825 V   |
| Voltage on DVCC Pin (V <sub>DVCC</sub> )  | $V_{DVCC} = \frac{DIAG\_CODE}{65,536} \times 8.25$                          | 0 V to 8.25 V  |
| Voltage on SENSEL Pin (V <sub>SENSEL</sub> )                                      |   |  |
| DIN_THRESH_MODE Bit = 0   | $V_{SENSEL} = \left( \frac{DIAG\_CODE}{65,536} \times 60 \right) - AVDD$    | -AVDD to +60 V - AVDD  |
| DIN_THRESH_MODE Bit = 1   | $V_{SENSEL} = \left( \frac{DIAG\_CODE}{65,536} \times 50 \right) - 20$      | -20 V to +30 V   |
| Voltage on LVIN Pin (V <sub>LVIN</sub> )  | $V_{LVIN} = \frac{DIAG\_CODE}{65,536} \times 2.5$                           | 0 V to 2.5 V   |
| Voltage on SENSE_EXT1 Pin (V <sub>SENSE_EXT1</sub> )                              | $V_{SENSE\_EXT1} = \left( \frac{DIAG\_CODE}{65,536} \times 50 \right) - 20$ | -20 V to +30 V   |
| Voltage on SENSE_EXT2 Pin (V <sub>SENSE_EXT2</sub> )                              | $V_{SENSE\_EXT2} = \left( \frac{DIAG\_CODE}{65,536} \times 50 \right) - 20$ | -20 V to +30 V   |
| Voltage on DO_VDD Pin (V <sub>DO_VDD</sub> )                                      | $V_{DO\_VDD} = \frac{DIAG\_CODE}{65,536} \times 49.2$                       | 0 V to 49.2 V  |
| Voltage Across R <sub>SET</sub> in External Digital Output Sourcing Mode          | $V_{RSET} = \frac{DIAG\_CODE}{65,536} \times 0.3125$                        | 0 V to 0.3125 V (equivalent to 2.08 A when using recommended 0.15 Ω external resistor) |
| Voltage Across R <sub>SET</sub> in External Digital Output Sinking Mode           | $V_{RSET} = \frac{DIAG\_CODE}{65,536} \times 2.5$                           | 0 V to 2.5 V (equivalent to 16 A when using recommended 0.15 Ω external resistor)      |
| Current Flowing Through R <sub>SET</sub> in Internal Digital Output Sourcing Mode | $I_{RSET} = \left( \frac{DIAG\_CODE}{65,536} \times 0.3125 \right) / 1.38$  | 0 mA to 226 mA   |
| Current Flowing Through R <sub>SET</sub> in Internal Digital Output Sinking Mode  | $I_{RSET} = \left( \frac{DIAG\_CODE}{65,536} \times 2.5 \right) / 1.38$     | 0 mA to 1.8 A  |

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### DAC FUNCTIONALITY

The AD74115 contains a 14-bit DAC. The DAC core is a 14-bit string DAC. The architecture structure consists of a string of resistors, each with a value of R. The digital input code that is loaded to the DAC\_CODE register determines which node on the string the voltage is tapped off from and fed into the output amplifier. This architecture is inherently monotonic and linear.

There are two sources for the code loaded to the DAC. The typical option is to load a code to the DAC from the DAC\_CODE register. The second option is to enable slewing to control the rate at which the DAC code is loaded to the DAC.

*Table 29. Ideal DAC Input Code to Output Relationship*

| DAC Code |      |      |      |                                  | Analog Output                         |  |
|----------|------|------|------|----------------------------------|---------------------------------------|--|
| MSBs     |      | LSBs |      | ±12 V                            | 0 V to 12 V                           | 0 mA to 25 mA                          |
| 0000     | 0000 | 0000 | 0000 | -12 V                            | 0 V                                   | 0 mA                                   |
| 0000     | 0000 | 0000 | 0001 | $24 \times (1/16,384) - 12$      | $12 \times (1/16,384)$                | $25 \text{ mA} \times (1/16,384)$      |
| 0010     | 0000 | 0000 | 0000 | 0 V                              | 6 V                                   | 12.5 mA                                |
| 0011     | 1111 | 1111 | 1110 | $24 \times (16,382/16,384) - 12$ | $12 \text{ V} \times (16,382/16,384)$ | $25 \text{ mA} \times (16,382/16,384)$ |
| 0011     | 1111 | 1111 | 1111 | $24 \times (16,383/16,384) - 12$ | $12 \text{ V} \times (16,383/16,384)$ | $25 \text{ mA} \times (16,383/16,384)$ |

The code loaded to the DAC from either of the two sources is also loaded to the DAC\_ACTIVE register. The DAC\_ACTIVE register contains the current code loaded to the DAC, irrespective of the code source.

### DAC Transfer Function

*Table 29* shows the input code to ideal analog output relationship for each of the available output ranges.

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### Digital Linear Slew Rate Control

The digital linear slew rate control feature of the AD74115 controls the rate at which the output transitions to the new value. This slew rate control feature is available for both the current and voltage outputs.

When the slew rate control feature is disabled, the output value transitions at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the digital slew rate control feature via the OUTPUT\_CONFIG register.

After the digital slew rate control feature is enabled, the output steps digitally at a rate defined by the user in the OUTPUT\_CON-

FIG register. The SLEW\_LIN\_STEP bits dictate the number of codes per increment, and the SLEW\_LIN\_RATE bits dictate the rate at which the codes are updated. [Table 30](#) shows the typical programmable slew rates for a zero-scale to full-scale (or full-scale to zero-scale) DAC update that is available on the AD74115.

The DAC\_ACTIVE register can monitor the progress of slewing to a target DAC code. This register contains the code that is currently loaded to the DAC.

If the digital slewing is disabled before the end code in the DAC\_CODE register is reached, the value remains at the DAC\_ACTIVE value and does not ramp to the end code.

**Table 30. Programmable Slew Times for a Zero-Scale to Full-Scale Code Update**

| Update Slew Rate, Programmable via SLEW_LIN_RATE Bits (kHz) | Step Size (% of Full-Scale DAC Voltage), Programmable via SLEW_LIN_STEP Bits <sup>1</sup> |             |              |              |
|---|---|-------------|--------------|--------------|
|   | 0.8%  | 1.5%        | 6.1%         | 22.2%        |
| 4   | 31.3 ms   | 16.7 ms     | 4.1 ms       | 1.1 ms       |
| 64  | 2.0 ms  | 1.0 ms      | 256 $\mu$ s  | 70.4 $\mu$ s |
| 150   | 833 $\mu$ s   | 444 $\mu$ s | 109 $\mu$ s  | 30.0 $\mu$ s |
| 240   | 521 $\mu$ s   | 277 $\mu$ s | 68.3 $\mu$ s | 18.8 $\mu$ s |

<sup>1</sup> These are theoretical values. The final slew rate is limited by the  $C_{LOAD}$  value.

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### Driving Inductive Loads

It is recommended to use the digital slew rate control when driving inductive loads greater than approximately 4 mH. Controlling the output slew rate minimizes ringing when stepping the output current by minimizing the current rate of change (di/dt). See the  $I_{OUT}$  typical performance of the settling time with an inductive load with and without the slew rate enabled in the [Figure 11](#).

### RESET FUNCTION

After the AD74115 is reset, all registers are reset to the default state, and the calibration memory is refreshed. The device is configured in high impedance mode. A reset can be initiated in several ways.

The hardware reset is initiated by pulsing the  $\overline{RESET}$  pin low. The  $\overline{RESET}$  pulse width must comply with the specifications in [Table 14](#).

A software reset is initiated by writing the 0x15FA code (Software Reset Key 1) followed by the 0xAF51 code (Software Reset Key 2) to the  $CMD\_KEY$  register.

A reset can also be initiated via the thermal reset function, which is described in the [Thermal Alert and Thermal Reset](#) section.

If the  $V_{DLDO1V8}$  or the  $V_{DVCC}$  drop below the specified power supply monitors threshold highlighted in [Table 13](#) the internal power-on reset function resets the AD74115. The device does not come out of reset until the  $V_{DLDO1V8}$  and the  $V_{DVCC}$  rise above these voltage levels.

After a reset cycle completes, the  $RESET\_OCCURRED$  bit is set in the  $ALERT\_STATUS$  register. If an SPI transfer is attempted before the reset cycle is complete (see [Table 13](#) for typical reset time), the  $CAL\_MEM\_ERR$  bit in the  $SUPPLY\_ALERT\_STATUS$  register is also set to indicate that the calibration memory is not fully refreshed. After the reset time elapses, clear these bits in the  $ALERT\_STATUS$  register before continuing to use the device.

### FAULTS AND ALERTS

The AD74115 is equipped with several fault monitors to detect an error condition.

If an alert or fault condition occurs, the  $\overline{ALERT}$  pin asserts. To determine the source of the alert condition, read the  $ALERT\_STATUS$  register. This register contains a latched bit for each alert condition.

After the error condition is removed, clear the activated flag by writing 1 to the location of the corresponding bits in the  $ALERT\_STATUS$  register (write 0xFFFF to the  $ALERT\_STATUS$  register to clear all alert bits). Alerts asserted in  $SUPPLY\_ALERT\_STATUS$  must be cleared before the  $ALERT\_STATUS$  register.

The  $LIVE\_STATUS$  register is a live representation of the error conditions. The bits in this register are not latched and clear automatically when the error condition is no longer present.

The  $ALERT\_MASK$  register prevents error conditions from activating the  $\overline{ALERT}$  pin.

### Channel Faults

The AD74115 is equipped with multiple open-circuit and short-circuit faults in the various functions as described in the [Device Functions](#) section. Manage faults as these faults appear and reset the channel, if necessary, to avoid overheating the device.

### Power Supply Monitors

The AD74115 includes six power supply monitors to detect a supply failure. If any of the supplies fall to less than the defined threshold detailed in [Table 13](#), the corresponding bit is set in the  $ALERT\_STATUS$  register.

### Thermal Alert and Thermal Reset

If the AD74115 die temperature reaches the alert temperature described in [Table 13](#), a high temperature error bit (TEMP\_ALERT) is set in the  $ALERT\_STATUS$  register to alert the user of the increasing die temperature.

The device can also be configured to reset at higher die temperatures. To reset the device at higher temperatures, enable the thermal reset function by setting the  $EN\_THERM\_RST$  bit in the  $THERM\_RST$  register. After this bit is set, the device goes through a full reset after the die temperature reaches the reset temperature described in [Table 13](#).

### Burnout Currents

Burnout currents are used to verify the integrity of an attached sensor and to ensure that it has not gone open circuit before taking a measurement from it. The AD74115 can be enabled to provide a user programmable, current source that can be programmed to a fixed value between 50 nA and 10  $\mu$ A. Burnout currents are available on the  $V_{IOUT}$  (to monitor the I/O screw terminal),  $SENSE\_EXT1$ , and  $SENSE\_EXT2$  pins and can be programmed to source or sink current.

The burnout current sources are disabled on power up. Program the burnout current using the bits in the  $I\_BURNOUT\_CONFIG$  register. The full list of available current settings can be found in [Table 13](#).

The current source can be enabled at all times or alternatively enabled when needed for diagnostic purposes. When a burnout current source is enabled, the selected current is switched onto the selected pin, and it flows in the external load.

### FET LEAKAGE COMPENSATION

A software configurable input and output solution can include a precision analog input and output capability along with a high current, digital output capability on a single screw terminal. In this case, the external FET used in the digital output function may

## THEORY OF OPERATION

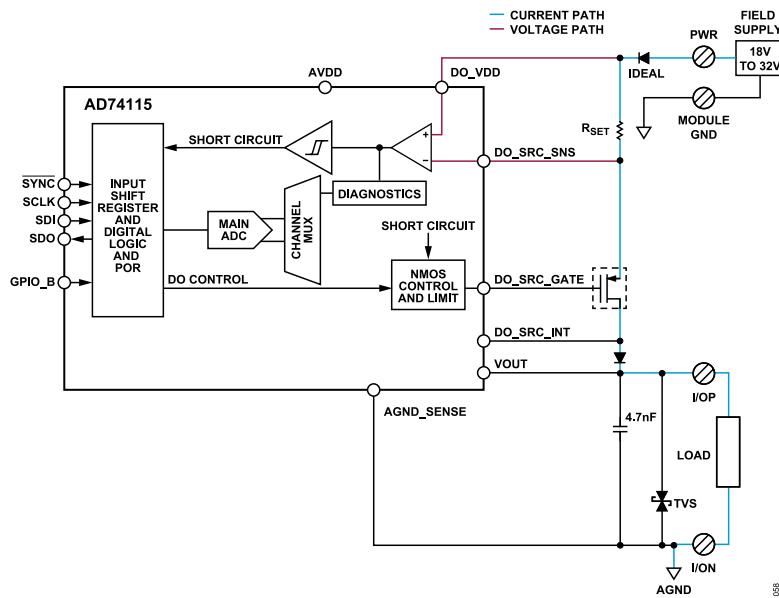
contribute off-leakage to the screw terminal when not in use. This leakage can affect the accuracy of the analog functions, especially to RTD measurements.

The AD74115 has a FET leakage compensation feature that provides an alternative path to the FET leakage to prevent it from flowing in the I/O screw terminal.

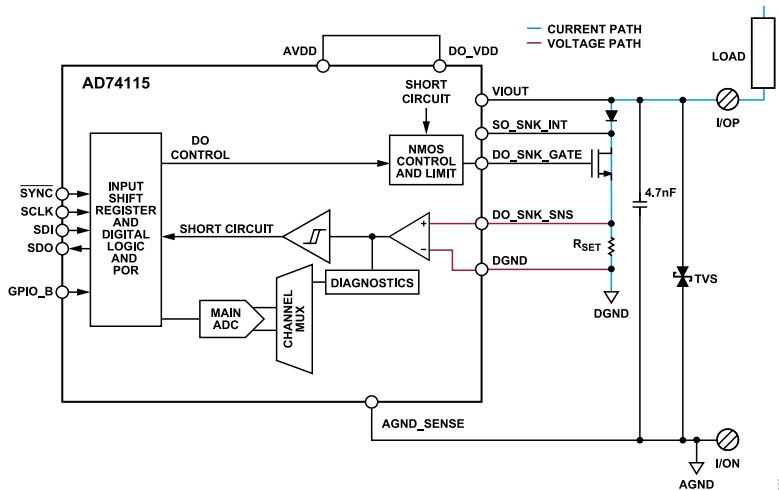
To enable this feature, configure the FET\_LKG\_COMP register. Set the FET\_SRC\_LKG\_COMP\_EN bit for sourcing digital output and set the FET\_SNK\_LKG\_COMP\_EN bit for sinking digital output.

For sourcing the digital output, connect the DO\_SRC\_INT pin to the drain of the FET as shown in [Figure 52](#). Similarly, for sinking the digital output, connect the DO\_SNK\_INT pin to the drain of the sinking FET as shown in [Figure 53](#).

The FET leakage compensation feature can be used if the specified leakage of the chosen external FET is expected to contribute error to the precision analog measurements like the current input or 3-wire and 4-wire RTD measurements. This feature is not recommended for use in 2-wire RTD mode.



**Figure 52. Configuration for Digital Output Sourcing with FET Leakage Compensation**



**Figure 53. Configuration for Digital Output Sinking with FET Leakage Compensation**

## THEORY OF OPERATION

### GPIO\_X PINS

The AD74115 has four GPIO pins. Each GPIO\_x pin can be configured in several ways:

- ▶ In high impedance
- ▶ As a logic high or low output
- ▶ As a logic input

In addition, GPIO\_A can be used to monitor the digital input comparator, GPIO\_B can be used to control the external digital output circuits, and GPIO\_C can be used to control the internal digital output circuits.

By default, a weak pull-down is enabled on the GPIO\_x pins. Disable the weak pull-down if configuring any of the GPIO\_x pins as logic inputs or outputs. To disable the pull-down, set the GP\_WK\_PD\_EN bit to 0 in the relevant GPIO\_CONFIGx register.

The GPIO\_x configuration can be set via the GPIO\_SELECT bits within the GPIO\_CONFIGx registers. When configuring the GPIO\_x pins as logic outputs, the data of the pins can be written to the GPO\_DATA bit in the GPIO\_CONFIGx registers.

### SPI

The AD74115 is controlled over a versatile 4-wire SPI with an 8-bit CRC that operates at clock speeds of up to 24 MHz (refer the  $t_1$  parameter in [Table 14](#)) and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

### SPI Write

The input shift register is 32 bits wide, and data is loaded into the device MSB first under the control of SCLK. Data is clocked in on the falling edge of SCLK. [Table 31](#) shows the structure of an SPI write frame.

**Table 31. Writing to a Register**

| MSB              | LSB      |         |
|------------------|----------|---------|
| [D31:D24]        | [D23:D8] | [D7:D0] |
| Register address | Data     | CRC     |

### SPI Read

Two SPI frames are required to read a register location. In the first frame, the address of the register to be read is written to the READ\_SELECT register. [Table 32](#) shows the structure of the first SPI frame.

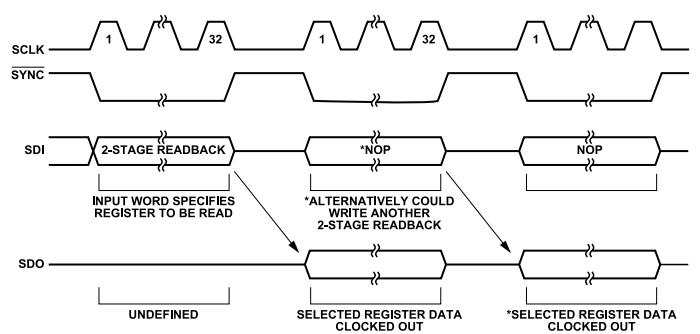
**Table 32. First Frame of a Readback Sequence**

| MSB       | LSB              |         |
|-----------|------------------|---------|
| [D31:D24] | [D23:D8]         | [D7:D0] |
| 0x64      | Readback address | CRC     |

The second SPI frame consists of either a no operation (NOP) command or a write to any other register. The data is shifted out, MSB first, on the SDO pin.

- ▶ The MSB (Bit 31) is always set to 1 to allow the SPI main to detect if the SDO line is stuck low. This MSB is timed off the falling SYNC edge. All other bits are clocked out on the SCLK rising edge.
- ▶ The contents of the selected register are available in Bits[D23:D8].
- ▶ Bits[D30:D24] provide status information on the SDO pin. The contents of these bits is determined by setting the SPI\_RD\_RET\_INFO bit in the READ\_SELECT register. [Table 33](#) and [Table 34](#) show the content available for each SPI\_RD\_RET\_INFO setting.
- ▶ An 8-bit CRC is returned in Bits[D7:D0].

[Figure 54](#) shows the timing diagram of the two-stage readback.



**Figure 54. 2-Stage Readback Timing Diagram**

**Table 33. SDO Contents for a Read Operation When the SPI\_RD\_RET\_INFO Bit = 0**

| MSB | LSB                |           |         |
|-----|--------------------|-----------|---------|
| D31 | [D30:D24]          | [D23:D8]  | [D7:D0] |
| 1   | READBACK_ADDR[6:0] | Read data | CRC     |

**THEORY OF OPERATION****Table 34. SDO Contents for a Read Operation When the SPI\_RD\_RET\_INFO Bit = 1**

| MSB |     |       |              |     |     |     |              |           |         | LSB |
|-----|-----|-------|--------------|-----|-----|-----|--------------|-----------|---------|-----|
| D31 | D30 | D29   | D28          | D27 | D26 | D25 | D24          | [D23:D8]  | [D7:D0] |     |
| 1   | 0   | ALERT | ADC_DATA_RDY | 0   | 0   | 0   | DIN_COMP_OUT | Read data | CRC     |     |

## THEORY OF OPERATION

### Auto Readback

Auto readback allows the user to read from the same register during every SPI transaction. To enable auto readback, set the AUTO\_RD\_EN bit in the READ\_SELECT register. If auto readback is enabled, the contents of the address written to the READBACK\_ADDR bits are output on the SDO lines during each SPI transfer.

### Burst Read Mode

The AD74115 incorporates a burst read mode that allows sequential reading of multiple registers on the SDO pin as long as there are sufficient SCLKs.

To read back data from multiple registers, the  $\overline{\text{SYNC}}$  line must be kept low after the second frame of a 2-stage readback (see the [SPI Read](#) section). The AD74115 increments through the register addresses clocking out the 32-bit contents until the  $\overline{\text{SYNC}}$  pin is returned high. An SPI\_ERR error is reported if the transaction does not end with  $32 + (n \times 24)$  SCLK rising edges, where  $n$  is the number of transactions.

Here is an example of how to complete a repeated burst read of the two ADC result registers:

1. Enable auto readback (to allow the SDO to return the register address in each SPI transaction).
2. Set the READBACK\_ADDR bits in the READ\_SELECT register to 0x44 to read the first of the ADC results registers.
3. Provide a NOP command. The contents of the ADC\_RESULT1 register are clocked out on the SDO pin, along with the CRC
4. Keep the  $\overline{\text{SYNC}}$  pin low to provide an additional 24 clocks to allow for the 16 bits of data from the ADC\_RESULT2 register to be clocked out along with the CRC.
5. Return  $\overline{\text{SYNC}}$  high.
6. To continue reading from these registers, repeat from Step 3.

[Figure 55](#) shows the contents on the SDO line when burst reading the ADC results registers. The data appearing on the SDO includes 7 bits of the register address (when the SPI\_RD\_RET\_INFO is set to 0), the 16-bit data of ADC\_RESULT1, and the 8-bit CRC. When the  $\overline{\text{SYNC}}$  pin is kept low and the clocks are applied, the data from the next sequential address (ADC\_RESULT2) is clocked out.

A register can be removed from the burst read sequence by deselecting it in the BURST\_READ\_SEL register.

Writes to the register map are not supported in streaming mode.

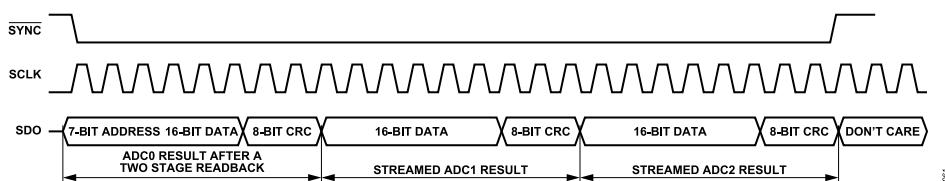


Figure 55. Burst Read Mode SDO Contents

## THEORY OF OPERATION

### SPI CRC

To ensure that data is received correctly in noisy environments, the AD74115 has a CRC implemented in the SPI. This CRC is based on an 8-bit CRC. The device controlling the AD74115 generates an 8-bit frame check sequence using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This frame check sequence is added to the end of the data-word, and the 32-bit data-word is sent to the AD74115 before taking the **SYNC** pin high.

A frame 32 bits wide containing the 24 data bits and 8 CRC bits must be supplied by the user. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the SPI\_ERR status bit in the ALERT\_STATUS register is asserted, and the ALERT pin goes low.

An 8-bit CRC is also provided with the data read during a register readback that can be used by the host microcontroller to verify that there are no SPI errors during the read transaction.

Clear the SPI\_ERR bit in the ALERT\_STATUS register by setting it to 1. Once the alert bit clears, the ALERT pin is deasserted (assuming that there are no other active alerts). The SPI CRC error can be masked by writing to the relevant bit in the ALERT\_MASK register.

### SPI SCLK Count Feature

An SCLK count feature is built into the SPI diagnostics. Only SPI frames with exactly 32 SCLK falling edges are accepted by the SPI as a valid write. In burst read mode, the number of SCLK rising edges must equal  $32 + (n \times 24)$ , where n is the number of transactions.

SPI frames of lengths other than the valid cases previously listed are ignored, and the SPI\_ERR bit asserts in the ALERT\_STATUS register. Mask the SPI\_ERR bit via the ALERT\_MASK register.

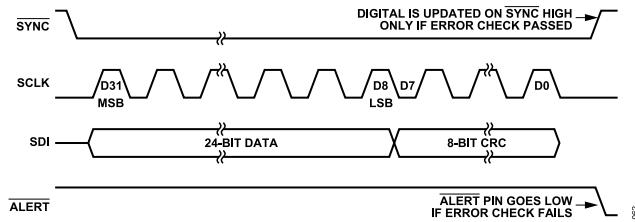


Figure 56. CRC Timing

## APPLICATIONS INFORMATION

### POWER AND ISOLATION

The AD74115 is designed to operate with a companion power and isolation chip. The [ADP1034](#) provides programmable power control (PPC) to the analog supply (AVDD) so that  $V_{AVDD}$  can be software controlled. The ADP1034 also provides fixed power supply voltages to the following AD74115 supply pins: AVSS, AVCC, and DVCC.

The ADP1034 is controlled by the AD74115 via the PPC\_CTRL pin using an OWSI. The host controller issues commands to adjust the AVDD supply voltage to the PPC\_TX register. In turn, the AD74115 passes the required  $V_{AVDD}$  changes to the ADP1034 using the OWSI. Once the ADP1034 receives a command to modify  $V_{AVDD}$ , it updates the  $V_{AVDD}$  accordingly.

Choose the PPC\_TX register code based on the following equation:

$$PPC\_CODE = 252 \times \left( \frac{V_{AVDD}}{V_{AVDD\_MAX}} \right) - 1$$

where:

$PPC\_CODE$  is the code that must be programmed to the PPC\_TX register for the desired  $V_{AVDD}$  value.

$V_{AVDD}$  is the desired  $V_{AVDD}$  supply voltage.

$V_{AVDD\_MAX}$  is the maximum voltage that can be generated by the ADP1034 with the selected feedback resistors. Refer to the ADP1034 data sheet for more information.

The AVDD supply from the ADP1034 can be dynamically changed as the load requirement and selected use case changes. Any changes must be done in a coordinated manner. If the voltage on the I/O screw terminal is expected to increase due to a change in conditions,  $V_{AVDD}$  must be adjusted first. If the voltage on the I/O screw terminal is expected to decrease due to the change in conditions,  $V_{AVDD}$  must be adjusted after the change in load, current, or selected use case.

The diagnostics function can confirm that the voltage is set on the AVDD pin. Select AVDD in one of the available diagnostics in the DIAG\_ASSIGN register. Enable an ADC conversion using the ADC\_CONFIG register and read the diagnostics result using the relevant ADC\_DIAG\_RESULTx register.

The ADP1034 provides digital isolation to the AD74115 SPI pins (SCLK, SYNC, SDO, and SDI). Isolation is available for two other digital output pins and one digital input pin. The block diagram in [Figure 58](#) shows that the RESET, ADC\_RDY, and ALERT pins are isolated using the ADP1034.

Refer to the ADP1034 data sheet for more information.

### One-Wire Serial Interface

Programmable power control is implemented via an OWSI between the AD74115 and the ADP1034.

The AD74115 acts as the OWSI main, using the PPC\_CTRL pin. An OWSI transaction requires a number of elements, as shown in [Figure 57](#). OWSI timing specifications are listed in [Table 15](#). The OWSI frame is broken into bit periods as start event, data bits, acknowledge (ACK) bit, and parity. Each timing specification is defined from the start of that bit period.

A start sequence is defined by two successive rising edge pulses. Once the start command is transmitted, 16 data bits follow to make up the address, data, and CRC bits. Finally, an acknowledge sequence is required from the OWSI subordinate. The acknowledge is comprised of two bits: an ACK bit and a parity bit.

The AD74115 pulls the OWSI bus high at the start of the ACK and parity bit periods. The OWSI bus is sampled by the AD74115 for a fixed time during the ACK and parity bits during which the OWSI subordinate can drive the bus low. Refer to [Figure 3](#) for a detailed view of the OWSI timing and to [Table 15](#) for the appropriate timing specifications.

During a successful transaction, the OWSI subordinate remains high during the ACK bit and drives the bus low during the parity bit.

If the transaction is not successful, the OWSI subordinate drives the bus low during the ACK bit and remains high during the parity bit.

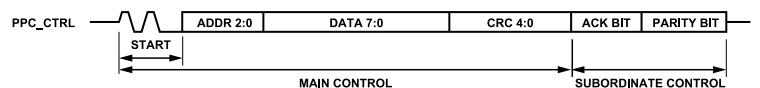


Figure 57. OWSI Write with Acknowledge

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### OWSI CRC

To ensure that data is received correctly in noisy environments, the AD74115 has a CRC implemented in the OWSI. This CRC is based on a 5-bit CRC. The AD74115 generates a 5-bit frame check sequence using the following polynomial:

$$C(x) = x^5 + x^2 + 1$$

This 5-bit frame check sequence is added to the end of the 11-bit data-word, and the full 16-bit word is sent to the subordinate device before expecting an acknowledge sequence.

Subordinate device check if the corresponding CRC is valid and responds with an acknowledge sequence. If the CRC check is not valid, the no acknowledge (NOACK) sequence is issued, and data is ignored.

The AD74115 asserts the PPC\_TX\_ACK\_ERR bit in the PPC\_ACTIVE register when NOACK sequence is noticed. The PPC\_ERR bit is also asserted in the ALERT\_STATUS register.

Clear the PPC\_ERR bit (ALERT\_STATUS register) by writing a 1, which returns the ALERT pin high (assuming that there are no other active alerts). The PPC\_ERR error bit can be masked by writing to the relevant bit in the ALERT\_MASK register.

### SYSTEM LEVEL BLOCK DIAGRAM

Figure 58 shows the connectivity between the AD74115 and the ADP1034. Figure 58 shows a fully isolated solution for a single-

channel software configurable input and output. The  $V_{AVDD}$ ,  $V_{AVCC}$ ,  $V_{DVCC}$ , and  $V_{AVSS}$  supply voltages for the AD74115 are provided by the ADP1034. The AVDD supply voltage can be dynamically controlled from the host controller using the programmable power control function. Refer to the [Power and Isolation](#) section for more information on the programmable power control feature using the ADP1034.

The output power available from the ADP1034 is dependent on the input supply voltage to the VINP pin of the ADP1034. The total power required to be delivered to the AD74115 and to the end load must be considered when choosing the system supply voltage. Refer to the ADP1034 for more information on power delivery.

The connectivity shown in Figure 58 allows the AD74115 to operate in bipolar mode with all of the modes of operation of the device that can be delivered on two screw terminals. An external field supply is only required if digital output currents greater than 100 mA are required with this configuration. The SENSE\_EXT1 and SENSE\_EXT2 pins on the AD74115 can also be connected to additional screw terminals for 3-wire and 4-wire measurements, if required.

## APPLICATIONS INFORMATION

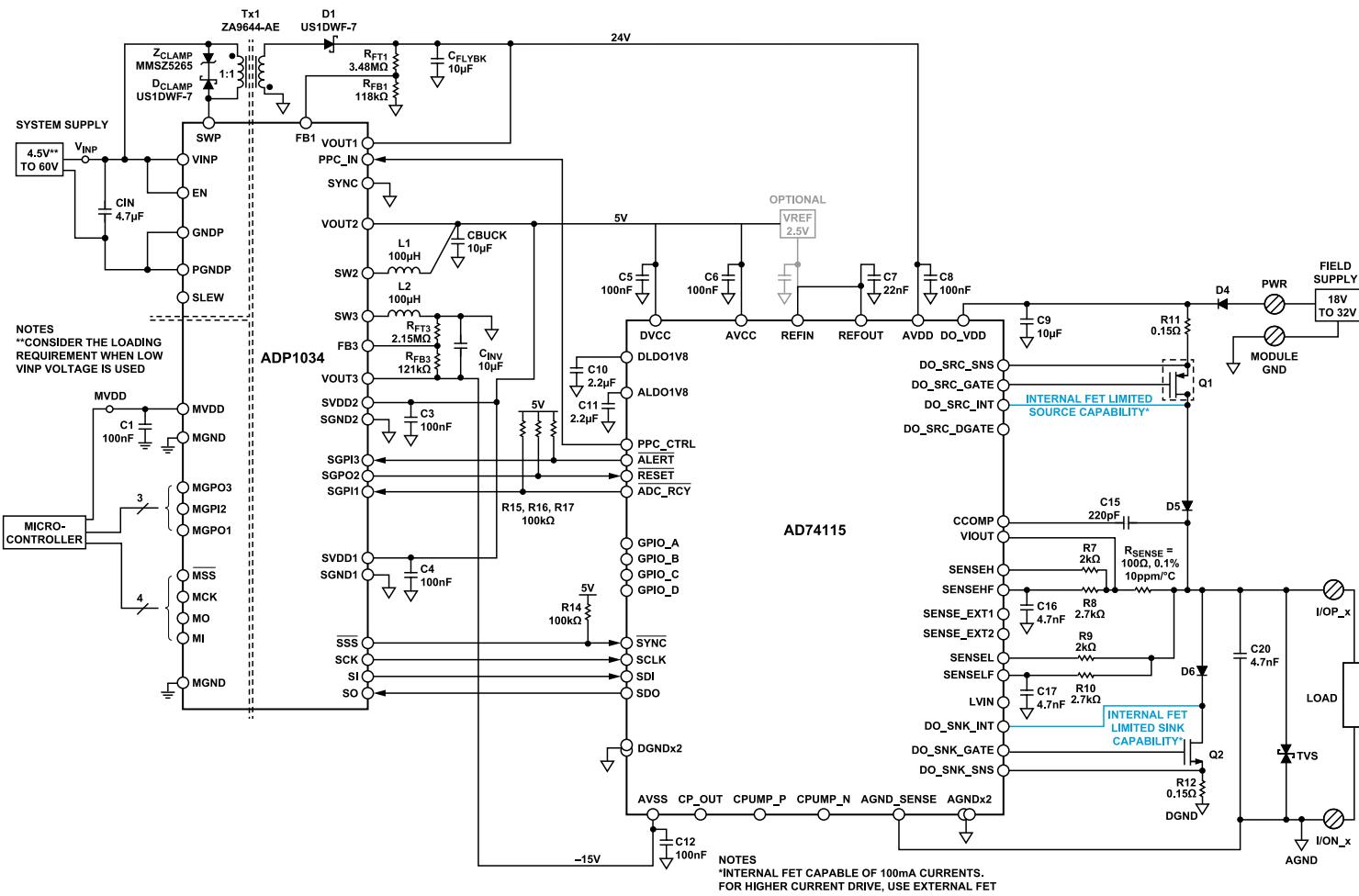


Figure 58. AD74115 and ADP1034 System Level Diagram

## APPLICATIONS INFORMATION

## EXTERNAL COMPONENTS

Table 35 lists the external components that are recommended to operate the AD74115.

Table 35. External Components

| Component                             | Value     |                |       | Suggested Component <sup>1</sup> | Notes/Comments  |
|---------------------------------------|-----------|----------------|-------|----------------------------------|---|
|                                       | Min       | Typical        | Max   |                                  |   |
| Decoupling                            |           |                |       |                                  |   |
| AVDD Decoupling                       |           | 10 $\mu$ F     |       | 50                               | Generic   |
|                                       |           | 0.1 $\mu$ F    |       | 50                               | Generic   |
| AVSS Decoupling                       |           | 10 $\mu$ F     |       | 50 <sup>2</sup>                  | Generic   |
|                                       |           | 100 nF         |       | 50 <sup>1</sup>                  | Generic   |
| AVCC Decoupling                       |           | 10 $\mu$ F     |       | 16                               | Generic   |
|                                       |           | 100 nF         |       |                                  | Generic   |
| DVCC Decoupling                       |           | 10 $\mu$ F     |       | 16                               | Generic   |
|                                       |           | 0.1 $\mu$ F    |       | 16                               | Generic   |
| DO_VDD                                |           | 10 $\mu$ F     |       | 100                              | Generic   |
| ALDO1V8 Decoupling                    | 1 $\mu$ F | 2.2 $\mu$ F    |       | 6.3                              | GRM21BR70J225MA01   |
| DLDO1V8 Decoupling                    | 1 $\mu$ F | 2.2 $\mu$ F    |       | 6.3                              | GRM21BR70J225MA01   |
| REFOUT Decoupling                     |           | 22.0 nF        | 50 nF | 6.3                              | Generic   |
| Charge Pump                           |           |                |       |                                  | When using the charge pump, connect CP_OUT to AVSS.   |
| Fly Capacitor                         |           | 330 nF         |       | 10                               | GRM188R71A334KA61<br>Connect this capacitor between the CPUMP_P and CPUMP_N pins.   |
| Analog Input and Output               |           |                |       |                                  |   |
| CCOMP Pin Compensation                |           | 220 pF         |       | 100                              | Generic<br>This pin is recommended for a total C <sub>LOAD</sub> > 14 nF and tied between the CCOMP pin and the I/O/P screw terminal. |
| SENSEHF Filter Capacitor <sup>3</sup> |           | 4.7 nF         |       | 100                              | Generic   |
| SENSEHF Filter Resistor <sup>3</sup>  |           | 2.7 k $\Omega$ |       | Generic                          | 1% accuracy.  |
| SENSELF Filter Capacitor <sup>3</sup> |           | 4.7 nF         |       | 100                              | Generic   |
| SENSELF Filter Resistor <sup>3</sup>  |           | 2.7 k $\Omega$ |       | Generic                          | 1% accuracy.  |
| SENSEH Precision                      |           | 2 k $\Omega$   |       | Generic                          | Generic<br>The SENSEH resistor accuracy directly affects RTD specifications.  |
| SENSEL                                |           | 2 k $\Omega$   |       | Generic                          | 1% accuracy.  |
| R <sub>SENSE</sub>                    |           | 100 $\Omega$   |       | Generic                          | R <sub>SENSE</sub> accuracy directly affects current output, current input, and RTD accuracy.   |
| Screw Terminal                        |           |                |       |                                  |   |
| Load Capacitor                        |           | 4.7 nF         |       | 100                              | Generic   |
| 36 V TVS                              |           |                |       | 36                               | SMBJ36CA<br>It is recommended to use low leakage TVS.   |

## APPLICATIONS INFORMATION

Table 35. External Components (Continued)

| Component                       | Value          |         |         | Suggested Component <sup>1</sup> | Notes/Comments  |
|---------------------------------|----------------|---------|---------|----------------------------------|---|
|                                 | Min            | Typical | Max     |                                  |   |
| Digital Output                  |                |         |         | Generic                          |   |
| External FETs                   |                |         |         | Generic                          |   |
| PFET for Sourcing Only          |                |         | 100     | Si7113ADN                        | Suitable for sourcing designs.  |
| NFET for Sinking Only           |                |         | 100     | SiA416DJ                         | Suitable for sinking designs.   |
| External Sense Resistor         | 0.15 $\Omega$  |         |         | Generic                          | Choose the $R_{SENSE}$ value based on the desired current resolution and range. |
| Smart Diode FET                 |                |         | 100     | Si7113ADN                        |   |
| Smart Diode 5 V Zener           |                |         | Generic | Generic                          |   |
| Smart Diode Resistor            | 10 k $\Omega$  |         | Generic | Generic                          |   |
| Blocking Diode                  | 1 A            |         | Generic | MSE1PB                           |   |
| High Voltage Auxiliary Inputs   |                |         |         |                                  |   |
| SENSE_EXT1                      |                |         |         |                                  |   |
| 36 V TVS                        |                |         |         | Generic                          |   |
| Filter Resistor <sup>3,4</sup>  | 2.7 k $\Omega$ |         |         | Generic                          | Optional.   |
| Filter Capacitor <sup>3,4</sup> | 4.7 nF         |         | 100     | Generic                          | Optional.   |
| SENSE_EXT2                      |                |         |         |                                  |   |
| 36 V TVS                        |                |         |         | Generic                          |   |
| Filter Resistor <sup>3,4</sup>  | 2.7 k $\Omega$ |         |         | Generic                          | Optional.   |
| Filter Capacitor <sup>3,4</sup> | 4.7 nF         |         | Generic | Generic                          | Optional.   |

<sup>1</sup> Use recommended components or ones that are similar.

<sup>2</sup> Voltage rating can be reduced if charge pump is used instead of the external supply.

<sup>3</sup> Antialiasing filter values provide a compromise in performance for all use cases and conditions. These values can be adjusted to optimize for specific design conditions.

<sup>4</sup> Not recommended for 3-wire and 4-wire resistance measurements.

## BOARD DESIGN AND LAYOUT CONSIDERATIONS

This section outlines the critical board design and layout considerations for the AD74115.

To guarantee stability for the SENSEL pin, limit the capacitance to ground between the SENSEL pin and the required 2 k $\Omega$  resistor to <10 pF.

To guarantee stability for the SENSEH pin, limit the capacitance to ground between the SENSEH pin and the required 2 k $\Omega$  resistor to <10 pF.

To guarantee stability for the CCOMP pin, limit the capacitance to ground between the CCOMP pin and the C<sub>COMP</sub> capacitor (if required) to <10 pF.

For correct operation of the programmable power control interface, limit the capacitance to ground on the PPC\_CTRL pin to 30 pF.

To optimize thermal performance, design the AD74115 boards with a minimum of four layers and with multiple thermal vias connecting the paddle to the bottom layer of the board. See the JEDEC JESD-51 specifications for more details. Users are recommended to thermally connect the exposed pad of the AD74115 to the thermal vias.

When grounding the AD74115 pins, it is recommended to connect the AGND pins and DGND pins to a single ground plane. The I/ON screw terminal must also be tied to this ground plane.

Track the SENSEH, SENSEHF, SENSEL, and SENSELF pins directly to the pad of the R<sub>SENSE</sub> resistor.

Track the DO\_SRC\_SNS and DO\_SNK\_SNS pins directly to the pad of the external R<sub>SET</sub> resistors.

The AGND\_SENSE pin senses the voltage at the I/ON screw terminal and provides this voltage as an input to the ADC. It is not recommended to directly connect the AGND\_SENSE pin to ground. Instead, users must route a single trace from the AGND\_SENSE pin to the I/ON screw terminal. This connection can be done by connecting the AGND\_SENSE pin to the I/ON screw terminal on the AD74115 board.

## REGISTER MAP

Table 36 summarizes the register map for the AD74115 with information on how to read and write to and from the registers. R indicates read only access, R/W indicates read and write access, R/W1C indicates read, write, or clear, and W indicates write only access.

Table 36. Register Summary

| Address      | Name                | Description   | Reset  | Access |
|--------------|---------------------|---|--------|--------|
| 0x00         | NOP                 | NOP Register  | 0x0000 | R      |
| 0x01         | CH_FUNC_SETUP       | Function Setup Register                                 | 0x0000 | R/W    |
| 0x02         | ADC_CONFIG          | ADC Configuration Register                              | 0x2400 | R/W    |
| 0x03         | PWR_OPTIM_CONFIG    | Power Optimization Configuration Register               | 0x001F | R/W    |
| 0x04         | DIN_CONFIG1         | Digital Input Configuration Register 1                  | 0x000B | R/W    |
| 0x05         | DIN_CONFIG2         | Digital Input Configuration Register 2                  | 0x0000 | R/W    |
| 0x06         | OUTPUT_CONFIG       | Output Configuration Register                           | 0x0000 | R/W    |
| 0x07         | RTD3W4W_CONFIG      | 3-Wire and 4-Wire RTD Configuration Register            | 0x0001 | R/W    |
| 0x08         | DO_INT_CONFIG       | Digital Output with Internal FET Configuration Register | 0x2E00 | R/W    |
| 0x09         | DO_EXT_CONFIG       | Digital Output with External FET Configuration Register | 0x2E00 | R/W    |
| 0x0A         | I_BURNOUT_CONFIG    | Burnout Currents Configuration Register                 | 0x0000 | R/W    |
| 0x0B         | DAC_CODE            | DAC Code Register                                       | 0x0000 | R/W    |
| 0x0D         | DAC_ACTIVE          | DAC Active Code Register                                | 0x0000 | R      |
| 0x35 to 0x38 | GPIO_CONFIGx        | GPIO_x Configuration Register                           | 0x0008 | R/W    |
| 0x39         | FET_LKG_COMP        | FET Leakage Compensation Register                       | 0x0000 | R/W    |
| 0x3A         | CHARGE_PUMP         | Charge Pump Configuration Register                      | 0x0000 | R/W    |
| 0x3B         | ADC_CONV_CTRL       | ADC Conversion Control Register                         | 0x0000 | R/W    |
| 0x3C         | DIAG_ASSIGN         | Diagnostics Select Register                             | 0x0000 | R/W    |
| 0x40         | DIN_COMP_OUT        | Digital Input Level Register                            | 0x0000 | R      |
| 0x41         | ALERT_STATUS        | Alert Status Register                                   | 0x0001 | R/W    |
| 0x42         | LIVE_STATUS         | Live Status Register                                    | 0x0000 | R/W    |
| 0x44         | ADC_RESULT1         | ADC Conversion 1 Result Register                        | 0x0000 | R      |
| 0x46         | ADC_RESULT2         | ADC Conversion 2 Result Register                        | 0x0000 | R      |
| 0x53 to 0x56 | ADC_DIAG_RESULTx    | Diagnostic Results Registers                            | 0x0000 | R      |
| 0x57         | DIN_COUNTER         | Digital Input Counter Register                          | 0x0000 | R      |
| 0x5B         | SUPPLY_ALERT_STATUS | Supply Alert Status Register                            | 0x0000 | R/W    |
| 0x5F         | ALERT_MASK          | Alert Mask Register for ALERT_STATUS                    | 0x0000 | R/W    |
| 0x60         | SUPPLY_ALERT_MASK   | Alert Mask Register for SUPPLY_ALERT_STATUS             | 0x0000 | R/W    |
| 0x64         | READ_SELECT         | Readback Select Register                                | 0x0000 | R/W    |
| 0x65         | BURST_READ_SEL      | Select the Registers Read in Burst Mode                 | 0x03FF | R/W    |
| 0x66         | PPC_TX              | PPC Transmit Register                                   | 0x00FF | R/W    |
| 0x6E         | PPC_ACTIVE          | PPC Status Register                                     | 0x00FF | R      |
| 0x77         | THERM_RST           | Thermal Reset Enable Register                           | 0x0000 | R/W    |
| 0x78         | CMD_KEY             | Command Register  | 0x0000 | W      |
| 0x79 to 0x7A | SCRATCH             | Scratch or Spare Register                               | 0x0000 | R/W    |
| 0x7B         | SILICON_REV         | Silicon Revision Register                               | 0x0001 | R      |
| 0x7C         | SILICON_ID0         | Silicon ID 0  | 0x0000 | R      |
| 0x7D         | SILICON_ID1         | Silicon ID 1  | 0x0000 | R      |
| 0x7E         | SILICON_ID2         | Silicon ID 2  | 0x0000 | R      |
| 0x7F         | SILICON_ID3         | Silicon ID 3  | 0x0000 | R      |

## REGISTER MAP

### SOFTWARE CONFIGURABLE INPUT AND OUTPUT REGISTERS

Use the following registers to configure the input and output functionality and to take measurements from the AD74115.

#### NOP Register

Address: 0x00, Reset: 0x0000, Name: NOP

Read only register. Writing to this register results in a no operation (NOP) command.

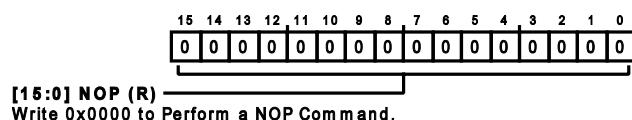


Table 37. Bit Descriptions for NOP

| Bits   | Bit Name | Description                            | Reset | Access |
|--------|----------|--|-------|--------|
| [15:0] | NOP      | Write 0x0000 to Perform a NOP Command. | 0x0   | R      |

#### Function Setup Register

Address: 0x01, Reset: 0x0000, Name: CH\_FUNC\_SETUP

Write to this register to select the function. When CH\_FUNC\_SETUP is programmed, some fields in the ADC\_CONFIG, OUTPUT\_CONFIG, DIN\_CONFIG1, DIN\_CONFIG2 and RTD3W4W\_CONFIG registers can change.

When changing the function, the high impedance function must be programmed first, before programming the new function.

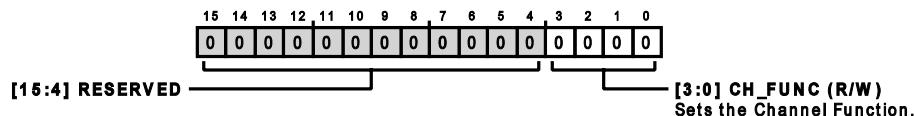


Table 38. Bit Descriptions for CH\_FUNC\_SETUP

| Bits   | Bit Name | Description   | Reset | Access |
|--------|----------|---|-------|--------|
| [15:4] | RESERVED | Reserved.   | 0x0   | R      |
| [3:0]  | CH_FUNC  | Sets the Channel Function. The default state on initial power-up or reset is high impedance. Values other than those listed as follows select the high impedance function.<br>0000: high impedance. The ADC is functional in this mode.<br>0001: voltage output. Force voltage, measure current.<br>0010: current output. Force current, measure voltage.<br>0011: voltage input. Measures the voltage between the I/O and I/ON screw terminals.<br>0100: current input, externally powered.<br>0101: current input, loop powered.<br>0110: 2-wire resistance measurement.<br>0111: 3-wire or 4-wire resistance measurement.<br>1000: digital input logic.<br>1001: digital input, loop powered.<br>Others: reserved. | 0x0   | R/W    |

#### ADC Configuration Register

Address: 0x02, Reset: 0x2400, Name: ADC\_CONFIG

## REGISTER MAP

This register selects the ADC configuration for the input and output channel. Disable ADC conversions before making any changes to the ADC\_CONFIG register.

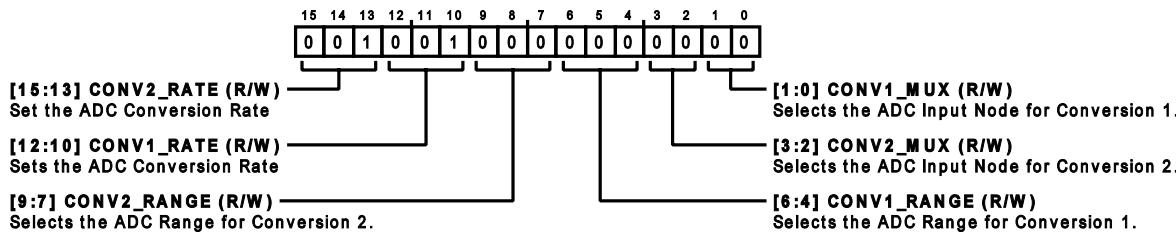


Table 39. Bit Descriptions for ADC\_CONFIG

| Bits    | Bit Name    | Description   | Reset | Access |
|---------|-------------|---|-------|--------|
| [15:13] | CONV2_RATE  | Set the ADC Conversion Rate. Values other than those listed in this table select the 20 SPS rate.<br>000: 10 SPS. Provides 50 Hz and 60 Hz noise rejection.<br>001: 20 SPS. Provides 50 Hz and 60 Hz noise rejection.<br>010: 1.2 kSPS.<br>011: 4.8 kSPS.<br>100: 9.6 kSPS.   | 0x1   | R/W    |
| [12:10] | CONV1_RATE  | Sets the ADC Conversion Rate. Values other than those listed in this table select the 20 SPS rate.<br>000: 10 SPS. Provides 50 Hz and 60 Hz noise rejection.<br>001: 20 SPS. Provides 50 Hz and 60 Hz noise rejection.<br>010: 1.2 kSPS.<br>011: 4.8 kSPS.<br>100: 9.6 kSPS.  | 0x1   | R/W    |
| [9:7]   | CONV2_RANGE | Selects the ADC Range for Conversion 2. Values outside of those listed in this table select the 0 V to 12 V range.<br>000: 0 V to 12 V.<br>001: -12 V to +12 V.<br>010: -2.5 V to +2.5 V.<br>011: -2.5 V to 0 V.<br>100: 0 V to 2.5 V.<br>101: 0 V to 0.625 V.<br>110: -104 mV to +104 mV.  | 0x0   | R/W    |
| [6:4]   | CONV1_RANGE | Selects the ADC Range for Conversion 1. Values outside of those listed in this table select the 0 V to 12 V range. Note that these bits can change when the CH_FUNC_SETUP register is programmed.<br>000: 0 V to 12 V.<br>001: -12 V to +12 V.<br>010: -2.5 V to +2.5 V.<br>011: -2.5 V to 0 V.<br>100: 0 V to 2.5 V.<br>101: 0 V to 0.625 V.<br>110: -104 mV to +104 mV. | 0x0   | R/W    |
| [3:2]   | CONV2_MUX   | Selects the ADC Input Node for Conversion 2.<br>00: SENSE_EXT1 to AGND_SENSE.<br>01: SENSE_EXT2 to AGND_SENSE.<br>10: SENSE_EXT2 to SENSE_EXT1.<br>11: AGND to AGND.  | 0x0   | R/W    |
| [1:0]   | CONV1_MUX   | Selects the ADC Input Node for Conversion 1. These bits can change when the CH_FUNC_SETUP register is programmed.<br>00: SENSELF to AGND_SENSE.   | 0x0   | R/W    |

## REGISTER MAP

Table 39. Bit Descriptions for ADC\_CONFIG (Continued)

| Bits | Bit Name | Description  | Reset | Access |
|------|----------|--|-------|--------|
|      |          | 01: SENSEHF to SENSELF.<br>10: SENSE_EXT2 to SENSE_EXT1.<br>11: SENSELF to SENSE_EXT1. |       |        |

## Power Optimization Configuration Register

Address: 0x03, Reset: 0x001F, Name: PWR\_OPTIM\_CONFIG

This register contains some settings to allow for power optimization of the channel.

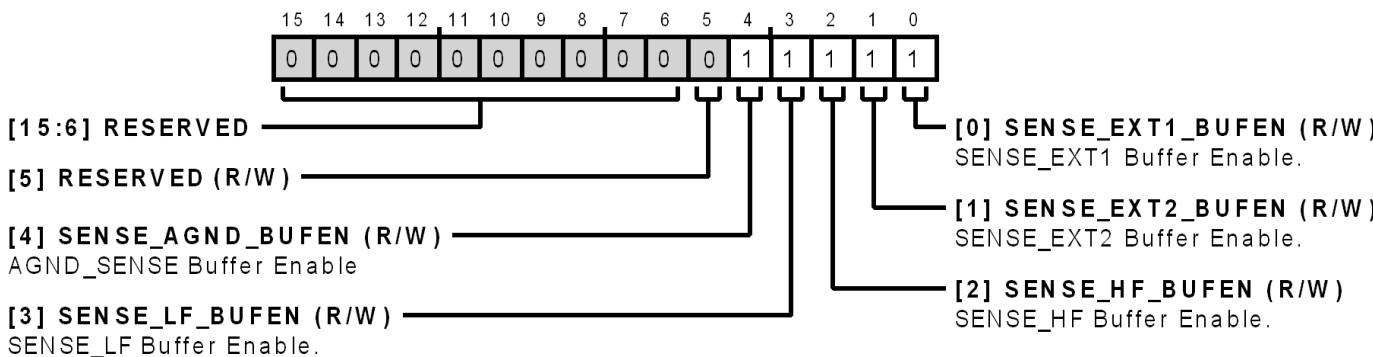


Table 40. Bit Descriptions for PWR\_OPTIM\_CONFIG

| Bits   | Bit Name         | Description  | Reset | Access |
|--------|------------------|--|-------|--------|
| [15:5] | RESERVED         | Reserved.  | 0x0   | R      |
| 4      | SENSE_AGND_BUFEN | AGND_SENSE Buffer Enable.<br>0: the sense AGND buffer is in low power mode.<br>1: the sense AGND buffer is in full power mode. | 0x1   | R/W    |
| 3      | SENSE_LF_BUFEN   | SENSE_LF Buffer Enable.<br>0: the SENSE_LF buffer is in low power mode.<br>1: the SENSE_LF buffer is in full power mode.       | 0x1   | R/W    |
| 2      | SENSE_HF_BUFEN   | SENSE_HF Buffer Enable.<br>0: the SENSE_HF buffer is in low power mode.<br>1: the SENSE_HF buffer is in full power mode.       | 0x1   | R/W    |
| 1      | SENSE_EXT2_BUFEN | SENSE_EXT2 Buffer Enable.<br>0: the SENSE_EXT2 buffer is in low power mode.<br>1: the SENSE_EXT2 buffer is in full power mode. | 0x1   | R/W    |
| 0      | SENSE_EXT1_BUFEN | SENSE_EXT1 Buffer Enable.<br>0: the SENSE_EXT1 buffer is in low power mode.<br>1: the SENSE_EXT1 buffer is in full power mode. | 0x1   | R/W    |

## Digital Input Configuration Register 1

Address: 0x04, Reset: 0x000B, Name: DIN\_CONFIG1

This register (along with DIN\_CONFIG2) is used to configure the digital input function of the channel.

## REGISTER MAP

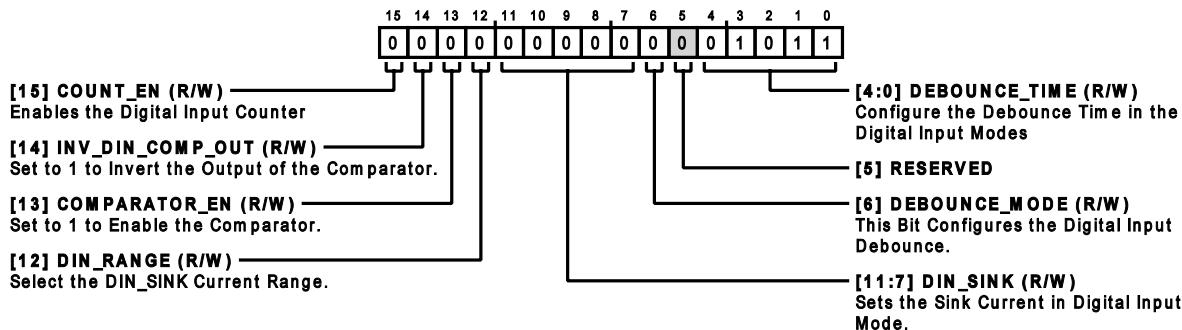


Table 41. Bit Descriptions for DIN\_CONFIG1

| Bits   | Bit Name         | Description  | Reset | Access |
|--------|------------------|--|-------|--------|
| 15     | COUNT_EN         | Enables the Digital Input Counter. If INV_DIN_COMP_OUT is 0, the positive edges of the debounced inputs are counted. If INV_DIN_COMP_OUT is 1, the negative edges of debounced inputs are counted. The count is reflected in the DIN_COUNTER register.   | 0x0   | R/W    |
| 14     | INV_DIN_COMP_OUT | Set to 1 to Invert the Output of the Comparator.   | 0x0   | R/W    |
| 13     | COMPARATOR_EN    | Set to 1 to Enable the Comparator. This bit can change when the CH_FUNC_SETUP register is programmed.  | 0x0   | R/W    |
| 12     | DIN_RANGE        | Select the DIN_SINK Current Range.<br>0: Range 0. Range from 0 mA to 3.7 mA in steps of 120 $\mu$ A and $\sim$ 2 k $\Omega$ of series resistance.<br>1: Range 1. Range from 0 mA to 7.4 mA in steps of 240 $\mu$ A and $\sim$ 1 k $\Omega$ of series resistance.   | 0x0   | R/W    |
| [11:7] | DIN_SINK         | Sets the Sink Current in Digital Input Mode. Configure these bits to program the current sink as defined by the DIN_RANGE bit. Set DIN_SINK to 0x0 to switch off the current sink. Note that these bits are set to 0 when the corresponding CH_FUNC_SETUP register is written, irrespective of the function.         | 0x0   | R/W    |
| 6      | DEBOUNCE_MODE    | This Bit Configures the Digital Input Debounce.<br>0: Debounce Mode 0. Integrator method is used. A counter increments when the signal is asserted and decrements when the signal is deasserted.<br>1: Debounce Mode 1. A simple counter increments while a signal is asserted and resets when the signal deasserts. | 0x0   | R/W    |
| 5      | RESERVED         | Reserved.  | 0x0   | R      |
| [4:0]  | DEBOUNCE_TIME    | Configure the Debounce Time in the Digital Input Modes. Reset value: 240 $\mu$ s. Set the bits to 0x0 to bypass the debounce circuit.  | 0xB   | R/W    |

## Digital Input Configuration Register 2

Address: 0x05, Reset: 0x0000, Name: DIN\_CONFIG2

This register (along with DIN\_CONFIG1) is used to configure the digital input function of the channel.

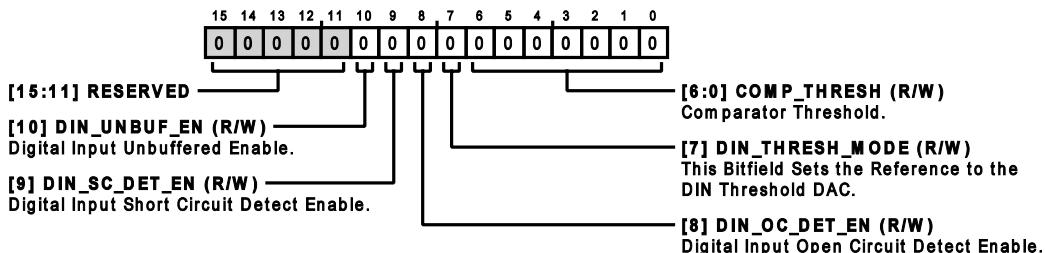


Table 42. Bit Descriptions for DIN\_CONFIG2

| Bits    | Bit Name | Description | Reset | Access |
|---------|----------|-------------|-------|--------|
| [15:11] | RESERVED | Reserved.   | 0x0   | R      |

## REGISTER MAP

Table 42. Bit Descriptions for DIN\_CONFIG2 (Continued)

| Bits  | Bit Name        | Description  | Reset | Access |
|-------|-----------------|--|-------|--------|
| 10    | DIN_UNBUF_EN    | Digital Input Unbuffered Enable.   | 0x0   | R/W    |
| 9     | DIN_SC_DET_EN   | Digital Input Short Circuit Detect Enable (when configured for IEC 61131 Type 3D diagnostics, as described in the <a href="#">Digital Input Logic</a> section).  | 0x0   | R/W    |
| 8     | DIN_OC_DET_EN   | Digital Input Open Circuit Detect Enable (when configured for IEC 61131 Type 3D diagnostics, as described in the <a href="#">Digital Input Logic</a> section).   | 0x0   | R/W    |
| 7     | DIN_THRESH_MODE | This Bitfield Sets the Reference to the DIN Threshold DAC.<br>0: the threshold scales with AVDD. The threshold range is from $-0.96 \times AVDD$ to AVDD.<br>1: fixed threshold. Threshold is from -19 V to +30 V. | 0x0   | R/W    |
| [6:0] | COMP_THRESH     | Comparator Threshold. DIN comparator threshold.  | 0x0   | R/W    |

## Output Configuration Register

Address: 0x06, Reset: 0x0000, Name: OUTPUT\_CONFIG

This register configures the output settings of the channel.

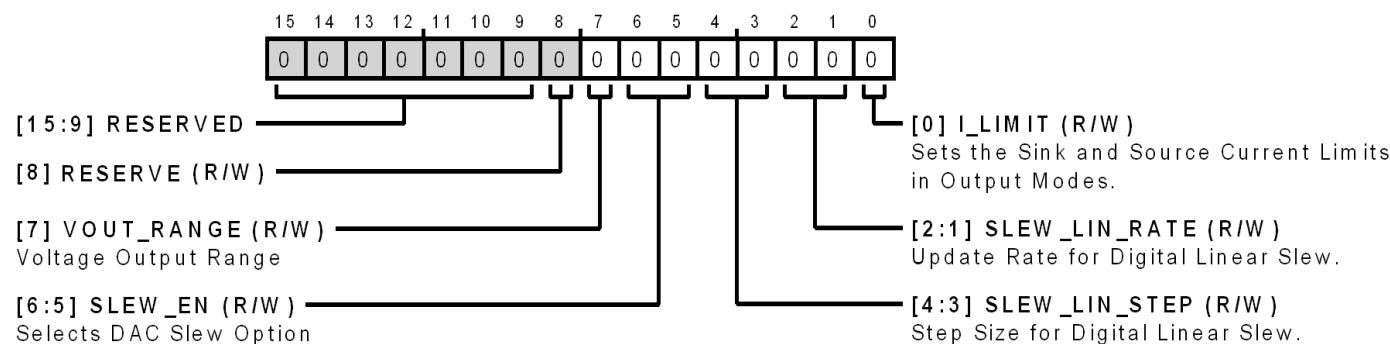


Table 43. Bit Descriptions for OUTPUT\_CONFIG

| Bits   | Bit Name      | Description   | Reset | Access |
|--------|---------------|---|-------|--------|
| [15:8] | RESERVED      | Reserved.   | 0x0   | R      |
| 7      | VOUT_RANGE    | Voltage Output Range.<br>0: 0 to 12 V.<br>1: -12 V to +12 V.  | 0x0   | R/W    |
| [6:5]  | SLEW_EN       | Selects DAC Slew Option.<br>00: slewing disabled. Slew stops immediately when disabled, there are no further updates to the DAC code.<br>01: enable linear slew on the DAC output.<br>Others: reserved.   | 0x0   | R/W    |
| [4:3]  | SLEW_LIN_STEP | Step Size for Digital Linear Slew.<br>00: voltage step size of 0.8% of full-scale DAC voltage.<br>01: voltage step size of 1.5% of full-scale DAC voltage.<br>10: voltage step size of 6.1% of full-scale DAC voltage.<br>11: voltage step size of 22.2% of full-scale DAC voltage. | 0x0   | R/W    |
| [2:1]  | SLEW_LIN_RATE | Update Rate for Digital Linear Slew.<br>00: update at a rate of 4 kHz.<br>01: update at a rate of 64 kHz.<br>10: update at a rate of 150 kHz.<br>11: update at a rate of 240 kHz.   | 0x0   | R/W    |
| 0      | I_LIMIT       | Sets the Sink and Source Current Limits in Output Modes. These are typical current limits.<br>0: Current-Limit 0. $V_{OUT}$ : 32 mA source or sink. $I_{OUT}$ : 4 mA sink.  | 0x0   | R/W    |

## REGISTER MAP

Table 43. Bit Descriptions for OUTPUT\_CONFIG (Continued)

| Bits | Bit Name | Description  | Reset | Access |
|------|----------|--|-------|--------|
|      |          | 1: Current-Limit 1. $V_{OUT}$ : 16 mA source or sink. $I_{OUT}$ : 1 mA sink. |       |        |

## 3-Wire and 4-Wire RTD Configuration Register

Address: 0x07, Reset: 0x0001, Name: RTD3W4W\_CONFIG

This register configures the 3-wire and 4-wire RTD measurements.

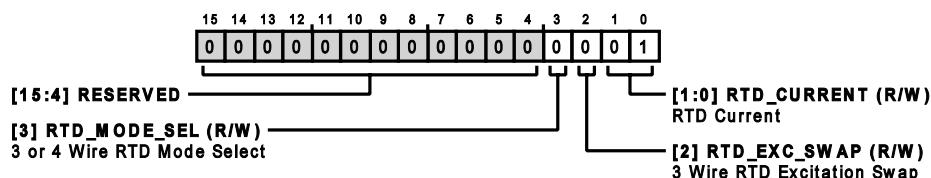


Table 44. Bit Descriptions for RTD3W4W\_CONFIG

| Bits   | Bit Name     | Description  | Reset | Access |
|--------|--------------|--|-------|--------|
| [15:4] | RESERVED     | Reserved.  | 0x0   | R      |
| 3      | RTD_MODE_SEL | 3-Wire or 4-Wire RTD Mode Select.<br>0: 3-Wire RTD Mode.<br>1: 4-Wire RTD Mode.  | 0x0   | R/W    |
| 2      | RTD_EXC_SWAP | 3-Wire RTD Excitation Swap. This field is only used for 3-wire RTD.  | 0x0   | R/W    |
| [1:0]  | RTD_CURRENT  | RTD Current. Values other than those listed as follows select a current of 250 $\mu$ A.<br>00: 250 $\mu$ A.<br>01: 500 $\mu$ A.<br>10: 750 $\mu$ A.<br>11: 1 mA. | 0x1   | R/W    |

## Digital Output with Internal FET Configuration Register

Address: 0x08, Reset: 0x2E00, Name: DO\_INT\_CONFIG

This register configures the settings for the internal digital output function. When the digital output functionality is enabled, the recommended configuration of the CH\_FUNC\_SETUP register is to set it to high impedance.

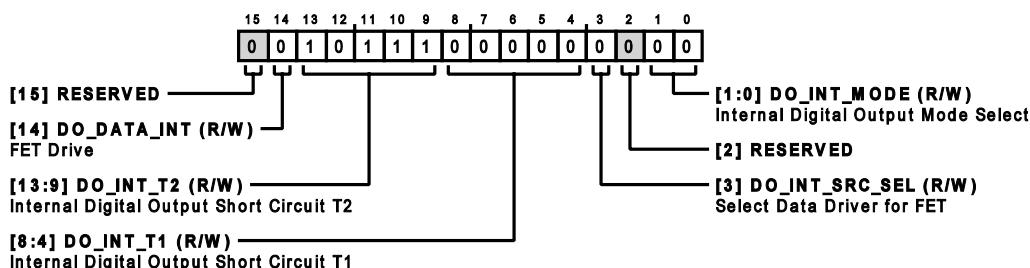


Table 45. Bit Descriptions for DO\_INT\_CONFIG

| Bits | Bit Name    | Description   | Reset | Access |
|------|-------------|---|-------|--------|
| 15   | RESERVED    | Reserved.   | 0x0   | R      |
| 14   | DO_DATA_INT | FET Drive.<br>0: source or sink mode, switch off the FET. Push-pull mode: sink current.<br>1: source or sink mode, switch on the FET. Push-pull mode: source current. | 0x0   | R/W    |

## REGISTER MAP

Table 45. Bit Descriptions for DO\_INT\_CONFIG (Continued)

| Bits   | Bit Name  | Description   | Reset | Access |
|--------|-----------|---|-------|--------|
| [13:9] | DO_INT_T2 | <p>Internal Digital Output Short-Circuit T2. Set these bits to program the T2 short-circuit duration. If a short-circuit event duration exceeds this time, the DO_EXT_TIMEOUT alert bit is asserted in the ALERT_STATUS register. Setting this register to 0 results in the minimum timer count and activation of the T2 timer when a short-circuit is detected.</p> <p>00: T2 18.699 µs.<br/> 01: T2 18.699 µs.<br/> 02: T2 24.39 µs.<br/> 03: T2 32.52 µs.<br/> 04: T2 42.276 µs.<br/> 05: T2 56.097 µs.<br/> 06: T2 75.609 µs.<br/> 07: T2 100.812 µs.<br/> 08: T2 130.08 µs.<br/> 09: T2 180.486 µs.<br/> 10: T2 240.648 µs.<br/> 11: T2 320.322 µs.<br/> 12: T2 420.321 µs.<br/> 13: T2 560.157 µs.<br/> 14: T2 750.399 µs.<br/> 15: T2 1.000803 ms.<br/> 16: T2 1.3008 ms.<br/> 17: T2 1.800795 ms.<br/> 18: T2 2.400789 ms.<br/> 19: T2 3.200781 ms.<br/> 20: T2 4.200771 ms.<br/> 21: T2 5.600757 ms.<br/> 22: T2 7.500738 ms.<br/> 23: T2 10.000713 ms.<br/> 24: T2 13.000683 ms.<br/> 25: T2 18.000633 ms.<br/> 26: T2 24.000573 ms.<br/> 27: T2 32.000493 ms.<br/> 28: T2 42.000393 ms.<br/> 29: T2 56.000253 ms.<br/> 30: T2 100.000626 ms.<br/> 31: T2 disabled.</p> | 0x17  | R/W    |
| [8:4]  | DO_INT_T1 | <p>Internal Digital Output Short-Circuit T1. Set these bits to program the T1 short-circuit duration. Setting this register to 0 results in the timer being disabled and immediate activation of the T2 timer when a short-circuit is detected. Note T1 is not available in push-pull mode of operation.</p> <p>00: T1 bypass.<br/> 01: T1 18.699 µs.<br/> 02: T1 24.39 µs.<br/> 03: T1 32.52 µs.<br/> 04: T1 42.276 µs.<br/> 05: T1 56.097 µs.<br/> 06: T1 75.609 µs.<br/> 07: T1 100.812 µs.<br/> 08: T1 130.08 µs.<br/> 09: T1 180.486 µs.</p>   | 0x0   | R/W    |

## REGISTER MAP

Table 45. Bit Descriptions for DO\_INT\_CONFIG (Continued)

| Bits  | Bit Name       | Description   | Reset | Access |
|-------|----------------|---|-------|--------|
|       |                | 10: T1 240.648 $\mu$ s.<br>11: T1 320.322 $\mu$ s.<br>12: T1 420.321 $\mu$ s.<br>13: T1 560.157 $\mu$ s.<br>14: T1 750.399 $\mu$ s.<br>15: T1 1.000803 ms.<br>16: T1 1.3008 ms.<br>17: T1 1.800795 ms.<br>18: T1 2.400789 ms.<br>19: T1 3.200781 ms.<br>20: T1 4.200771 ms.<br>21: T1 5.600757 ms.<br>22: T1 7.500738 ms.<br>23: T1 10.000713 ms.<br>24: T1 13.000683 ms.<br>25: T1 18.000633 ms.<br>26: T1 24.000573 ms.<br>27: T1 32.000493 ms.<br>28: T1 42.000393 ms.<br>29: T1 56.000253 ms.<br>30: T1 75.000063 ms.<br>31: T1 100.000626 ms.  |       |        |
| 3     | DO_INT_SRC_SEL | Select Data Driver for FET.<br>1: the GPIO_x pin is configured to drive the FET. Note that when this bit is set, configure the GPIO_CONFIG2 register as an input to the digital output circuit.<br>0: direct software control of the FET. When under software control, the FET is controlled via DO_DATA_INT.   | 0x0   | R/W    |
| 2     | RESERVED       | Reserved.   | 0x0   | R      |
| [1:0] | DO_INT_MODE    | Internal Digital Output Mode Select. Note that, if the DO_INT_TIMEOUT bit in the ALERT_STATUS register is set, the digital output function disables. The DO_INT_MODE automatically configures to select digital output internal disable mode. When switching between digital output modes, ensure that the digital output internal disable mode is the intermediate step.<br>00: digital output internal disable.<br>01: digital output internal source.<br>10: digital output internal sink.<br>11: digital output internal push-pull. DO_INT_SRC_SEL determines the data source. A 0 from data source enables the FET sinking current, and a 1 from the data source enables the FET sourcing current. | 0x0   | R/W    |

## Digital Output with External FET Configuration Register

Address: 0x09, Reset: 0x2E00, Name: DO\_EXT\_CONFIG

This register configures the settings for the external digital output function. When the digital output functionality is enabled, the recommended configuration of the CH\_FUNC\_SETUP register is to set it to high impedance.

## REGISTER MAP

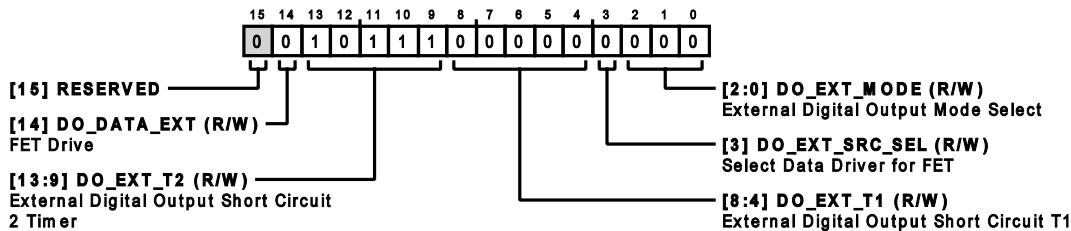


Table 46. Bit Descriptions for DO\_EXT\_CONFIG

| Bits   | Bit Name    | Description  | Reset | Access |
|--------|-------------|--|-------|--------|
| 15     | RESERVED    | Reserved.  | 0x0   | R      |
| 14     | DO_DATA_EXT | FET Drive.<br>0: switch off the FET.<br>1: switch on the FET.  | 0x0   | R/W    |
| [13:9] | DO_EXT_T2   | External Digital Output Short-Circuit 2 Timer. Set these bits to program the T2 short-circuit duration. If a short-circuit event duration exceeds this time, the DO_EXT_TIMEOUT alert bit is asserted in the ALERT_STATUS register. Setting this register to 0 results in the minimum timer count and activation of the T2 timer when a short circuit is detected. Take care when setting T2 to infinity because this can cause thermal damage to the selected external FET.<br>00: T2 100.812 µs.<br>01: T2 100.812 µs.<br>02: T2 100.812 µs.<br>03: T2 100.812 µs.<br>04: T2 100.812 µs.<br>05: T2 100.812 µs.<br>06: T2 100.812 µs.<br>07: T2 100.812 µs.<br>08: T2 130.08 µs.<br>09: T2 180.486 µs.<br>10: T2 240.648 µs.<br>11: T2 320.322 µs.<br>12: T2 420.321 µs.<br>13: T2 560.157 µs.<br>14: T2 750.399 µs.<br>15: T2 1.000803 ms.<br>16: T2 1.3008 ms.<br>17: T2 1.800795 ms.<br>18: T2 2.400789 ms.<br>19: T2 3.200781 ms.<br>20: T2 4.200771 ms.<br>21: T2 5.600757 ms.<br>22: T2 7.500738 ms.<br>23: T2 10.000713 ms.<br>24: T2 13.000683 ms.<br>25: T2 18.000633 ms.<br>26: T2 24.000573 ms.<br>27: T2 32.000493 ms.<br>28: T2 42.000393 ms.<br>29: T2 56.000253 ms.<br>30: T2 100.000626 ms.<br>31: T2 disabled. | 0x17  | R/W    |

## REGISTER MAP

Table 46. Bit Descriptions for DO\_EXT\_CONFIG (Continued)

| Bits  | Bit Name       | Description  | Reset | Access |
|-------|----------------|--|-------|--------|
| [8:4] | DO_EXT_T1      | <p>External Digital Output Short-Circuit T1. Set these bits to program the T1 short-circuit duration. Setting this register to 0 results in the timer being disabled and immediate activation of the T2 timer when a short circuit is detected. Note T1 is not available in push-pull mode of operation.</p> <p>00: T1 bypass.</p> <p>01: T1 100.812 µs.</p> <p>02: T1 100.812 µs.</p> <p>03: T1 100.812 µs.</p> <p>04: T1 100.812 µs.</p> <p>05: T1 100.812 µs.</p> <p>06: T1 100.812 µs.</p> <p>07: T1 100.812 µs.</p> <p>08: T1 130.08 µs.</p> <p>09: T1 180.486 µs.</p> <p>10: T1 240.648 µs.</p> <p>11: T1 320.322 µs.</p> <p>12: T1 420.321 µs.</p> <p>13: T1 560.157 µs.</p> <p>14: T1 750.399 µs.</p> <p>15: T1 1.000803 ms.</p> <p>16: T1 1.3008 ms.</p> <p>17: T1 1.800795 ms.</p> <p>18: T1 2.400789 ms.</p> <p>19: T1 3.200781 ms.</p> <p>20: T1 4.200771 ms.</p> <p>21: T1 5.600757 ms.</p> <p>22: T1 7.500738 ms.</p> <p>23: T1 10.000713 ms.</p> <p>24: T1 13.000683 ms.</p> <p>25: T1 18.000633 ms.</p> <p>26: T1 24.000573 ms.</p> <p>27: T1 32.000493 ms.</p> <p>28: T1 42.000393 ms.</p> <p>29: T1 56.000253 ms.</p> <p>30: T1 75.000063 ms.</p> <p>31: T1 100.000626 ms.</p> | 0x0   | R/W    |
| 3     | DO_EXT_SRC_SEL | <p>Select Data Driver for FET.</p> <p>1: the GPIO_x pin is configured to drive the FET. Note that when this bit is set, configure the GPIO_CONFIG1 register as an input to the digital output circuit.</p> <p>0: direct software control of the FET. When under software control, the FET is controlled via DO_DATA_EXT.</p>   | 0x0   | R/W    |
| [2:0] | DO_EXT_MODE    | <p>External Digital Output Mode Select. Note that, if the DO_EXT_TIMEOUT bit in the ALERT_STATUS register is set, the digital output function disables. The DO_EXT_MODE automatically configures to select digital output external disable mode. When switching between digital output modes, ensure that the digital output external disable mode is the intermediate step.</p> <p>000: digital output external disable.</p> <p>001: external source.</p> <p>010: external sink.</p> <p>011: external push-pull. DO_EXT_SRC_SEL determines the data source. A 0 from the data source enables the FET sinking, and a 1 from the data source enables the FET sourcing.</p> <p>100: external source with smart diode.</p>  | 0x0   | R/W    |

## REGISTER MAP

## Burnout Currents Configuration Register

Address: 0x0A, Reset: 0x0000, Name: I\_BURNOUT\_CONFIG

This register configures the burnout currents for the VOUT, SENSE\_EXT1, and SENSE\_EXT2 pins.

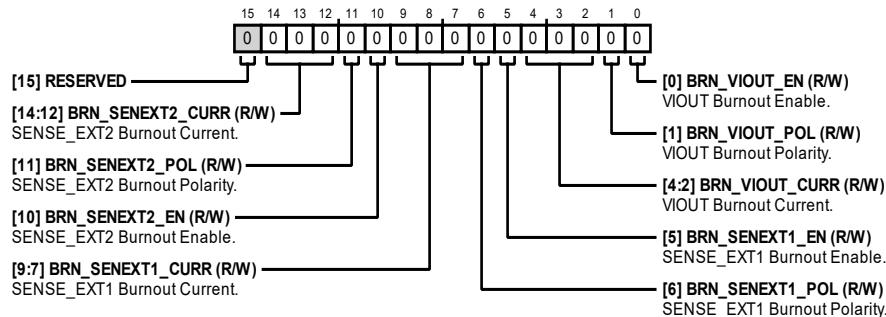


Table 47. Bit Descriptions for I\_BURNOUT\_CONFIG

| Bits    | Bit Name         | Description   | Reset | Access |
|---------|------------------|---|-------|--------|
| 15      | RESERVED         | Reserved.   | 0x0   | R      |
| [14:12] | BRN_SENEXT2_CURR | SENSE_EXT2 Burnout Current.<br>000: burnout current disabled.<br>001: 50 nA.<br>011: 500 nA.<br>100: 1 $\mu$ A.<br>110: 10 $\mu$ A.<br>Others: reserved | 0x0   | R/W    |
| 11      | BRN_SENEXT2_POL  | SENSE_EXT2 Burnout Polarity.<br>0: sinking current.<br>1: sourcing current.   | 0x0   | R/W    |
| 10      | BRN_SENEXT2_EN   | SENSE_EXT2 Burnout Enable.  | 0x0   | R/W    |
| [9:7]   | BRN_SENEXT1_CURR | SENSE_EXT1 Burnout Current.<br>000: burnout current disabled.<br>001: 50 nA.<br>011: 500 nA.<br>100: 1 $\mu$ A.<br>110: 10 $\mu$ A.<br>Others: reserved | 0x0   | R/W    |
| 6       | BRN_SENEXT1_POL  | SENSE_EXT1 Burnout Polarity.<br>0: sinking current.<br>1: sourcing current.   | 0x0   | R/W    |
| 5       | BRN_SENEXT1_EN   | SENSE_EXT1 Burnout Enable.  | 0x0   | R/W    |
| [4:2]   | BRN_VIOUT_CURR   | VOUT Burnout Current.<br>000: burnout current disabled.<br>100: 1 $\mu$ A.<br>110: 10 $\mu$ A.<br>Others: reserved                                      | 0x0   | R/W    |
| 1       | BRN_VIOUT_POL    | VOUT Burnout Polarity.<br>0: sinking current.<br>1: sourcing current.   | 0x0   | R/W    |
| 0       | BRN_VIOUT_EN     | VOUT Burnout Enable.  | 0x0   | R/W    |

## REGISTER MAP

### DAC Code Register

Address: 0x0B, Reset: 0x0000, Name: DAC\_CODE

This register is used to set the DAC code for the output functions. The DAC\_CODE register is not reset by changing channel functions.

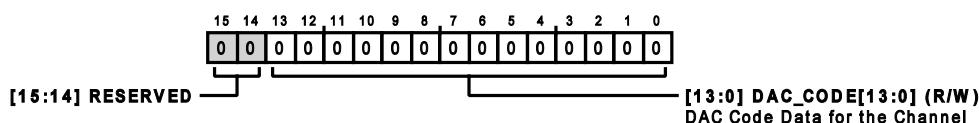


Table 48. Bit Descriptions for DAC\_CODE

| Bits    | Bit Name       | Description                    | Reset | Access |
|---------|----------------|--------------------------------|-------|--------|
| [15:14] | RESERVED       | Reserved.                      | 0x0   | R      |
| [13:0]  | DAC_CODE[13:0] | DAC Code Data for the Channel. | 0x0   | R/W    |

### DAC Active Code Register

Address: 0x0D, Reset: 0x0000, Name: DAC\_ACTIVE

This register displays the current value of the code loaded to the DAC. If slewling is enabled, this register reflects the current slew step.

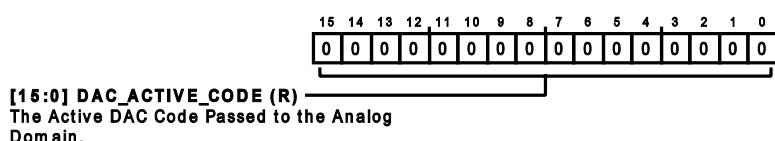


Table 49. Bit Descriptions for DAC\_ACTIVE

| Bits   | Bit Name        | Description  | Reset | Access |
|--------|-----------------|--|-------|--------|
| [15:0] | DAC_ACTIVE_CODE | The Active DAC Code Passed to the Analog Domain. Current code loaded to the DAC. | 0x0   | R      |

### GPIO\_A Configuration Register

Address: 0x35, Reset: 0x0008, Name: GPIO\_CONFIG0

The four GPIO\_x registers configure the four GPIO\_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP\_WK\_PD\_EN bit.

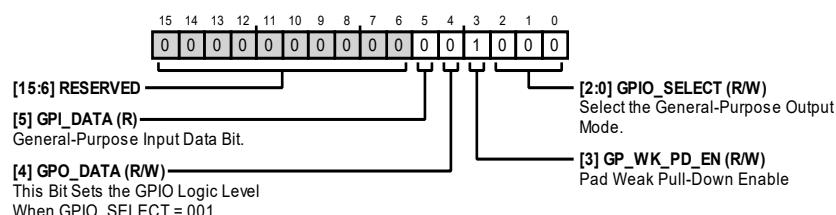


Table 50. Bit Descriptions for GPIO\_CONFIG0

| Bits   | Bit Name    | Description   | Reset | Access |
|--------|-------------|---|-------|--------|
| [15:6] | RESERVED    | Reserved.   | 0x0   | R      |
| 5      | GPI_DATA    | General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.   | 0x0   | R      |
| 4      | GPO_DATA    | This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001.<br>0: drive a logic low on GPIO_x pin.<br>1: drive a logic high on GPIO_x pin. | 0x0   | R/W    |
| 3      | GP_WK_PD_EN | Pad Weak Pull-Down Enable.<br>0: disable weak pull-down.  | 0x1   | R/W    |

## REGISTER MAP

Table 50. Bit Descriptions for GPIO\_CONFIG0 (Continued)

| Bits  | Bit Name    | Description   | Reset | Access |
|-------|-------------|---|-------|--------|
| [2:0] | GPIO_SELECT | <p>1: enable weak pull-down.</p> <p>Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option.</p> <p>000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled.</p> <p>001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled.</p> <p>010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA.</p> <p>011: configured as an input. The GPIO_x output driver is configured in high impedance state.</p> <p>100: configured to monitor the output of the digital input comparator.</p> <p>Others: reserved.</p> | 0x0   | R/W    |

## GPIO\_B Configuration Register

Address: 0x36, Reset: 0x0008, Name: GPIO\_CONFIG1

The four GPIO\_x registers configure the four GPIO\_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP\_WK\_PD\_EN bit.

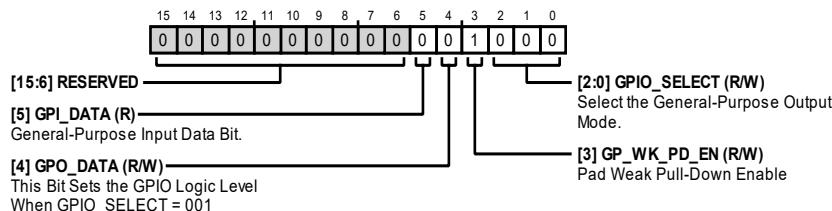


Table 51. Bit Descriptions for GPIO\_CONFIG1

| Bits   | Bit Name    | Description   | Reset | Access |
|--------|-------------|---|-------|--------|
| [15:6] | RESERVED    | Reserved.   | 0x0   | R      |
| 5      | GPI_DATA    | General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.   | 0x0   | R      |
| 4      | GPO_DATA    | This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001.<br>0: drive a logic low on GPIO_x pin.<br>1: drive a logic high on GPIO_x pin.   | 0x0   | R/W    |
| 3      | GP_WK_PD_EN | Pad Weak Pull-Down Enable.<br>0: disable weak pull-down.<br>1: enable weak pull-down.   | 0x1   | R/W    |
| [2:0]  | GPIO_SELECT | <p>Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option.</p> <p>000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled.</p> <p>001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled.</p> <p>010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA.</p> <p>011: configured as an input. GPIO_x output driver is configured in high impedance state.</p> <p>100: configured to drive the external digital output FET.</p> <p>Others: reserved.</p> | 0x0   | R/W    |

## GPIO\_C Configuration Register

Address: 0x37, Reset: 0x0008, Name: GPIO\_CONFIG2

The four GPIO\_x registers configure the four GPIO\_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP\_WK\_PD\_EN bit.

## REGISTER MAP

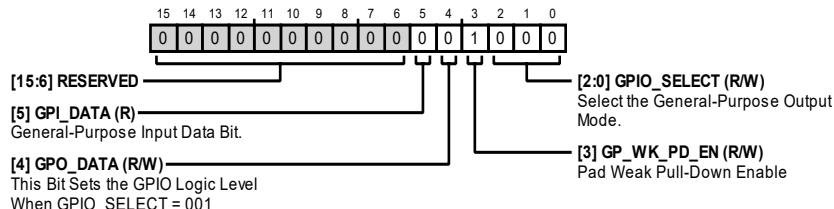


Table 52. Bit Descriptions for GPIO\_CONFIG2

| Bits   | Bit Name    | Description  | Reset | Access |
|--------|-------------|--|-------|--------|
| [15:6] | RESERVED    | Reserved.  | 0x0   | R      |
| 5      | GPI_DATA    | General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.  | 0x0   | R      |
| 4      | GPO_DATA    | This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001.<br>0: drive a logic low on GPIO_x pin.<br>1: drive a logic high on GPIO_x pin.  | 0x0   | R/W    |
| 3      | GP_WK_PD_EN | Pad Weak Pull-Down Enable.<br>0: disable weak pull-down.<br>1: enable weak pull-down.  | 0x1   | R/W    |
| [2:0]  | GPIO_SELECT | Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option.<br>000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled.<br>001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled.<br>010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA.<br>011: configured as an input. GPIO_x output driver is configured in high impedance state.<br>100: configured to drive internal digital output FET.<br>Others: reserved. | 0x0   | R/W    |

## GPIO\_D Configuration Register

Address: 0x38, Reset: 0x0008, Name: GPIO\_CONFIG3

The four GPIO\_x registers configure the four GPIO\_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP\_WK\_PD\_EN bit.

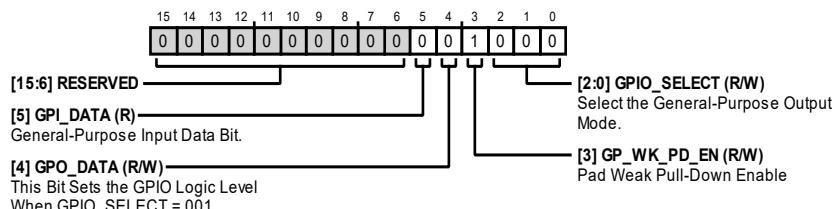


Table 53. Bit Descriptions for GPIO\_CONFIG3

| Bits   | Bit Name    | Description   | Reset | Access |
|--------|-------------|---|-------|--------|
| [15:6] | RESERVED    | Reserved.   | 0x0   | R      |
| 5      | GPI_DATA    | General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.   | 0x0   | R      |
| 4      | GPO_DATA    | This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001.<br>0: drive a logic low on GPIO_x pin.<br>1: drive a logic high on GPIO_x pin. | 0x0   | R/W    |
| 3      | GP_WK_PD_EN | Pad Weak Pull-Down Enable.<br>0: disable weak pull-down.<br>1: enable weak pull-down.   | 0x1   | R/W    |

## REGISTER MAP

Table 53. Bit Descriptions for GPIO\_CONFIG3 (Continued)

| Bits  | Bit Name    | Description   | Reset | Access |
|-------|-------------|---|-------|--------|
| [2:0] | GPIO_SELECT | Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option.<br>000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled.<br>001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled.<br>010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPO_DATA.<br>011: configured as an input. GPIO_x output driver is configured in high impedance state.<br>100: the GPIO_x output driver is off. The GPIO_x pad input buffer is disabled.<br>Others: reserved. | 0x0   | R/W    |

## FET Leakage Compensation Register

Address: 0x39, Reset: 0x0000, Name: FET\_LKG\_COMP

This register enables compensation for leakage in the external digital output FETs. This feature can be enabled during precision analog input and output measurements. Only use this register when the DO\_INT\_MODE is programmed to digital output internal disable, and the DO\_EXT\_MODE is programmed to digital output external disable.

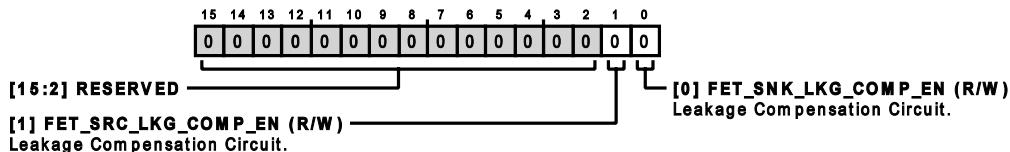


Table 54. Bit Descriptions for FET\_LKG\_COMP

| Bits   | Bit Name            | Description   | Reset | Access |
|--------|---------------------|---|-------|--------|
| [15:2] | RESERVED            | Reserved.   | 0x0   | R      |
| 1      | FET_SRC_LKG_COMP_EN | Leakage Compensation Circuit. Enables the source FET leakage compensation circuit.<br>0: leakage compensation circuit off.<br>1: leakage compensation circuit on. | 0x0   | R/W    |
| 0      | FET_SNK_LKG_COMP_EN | Leakage Compensation Circuit. Enable the sink FET leakage compensation circuit.<br>0: leakage compensation circuit off.<br>1: leakage compensation circuit on.    | 0x0   | R/W    |

## Charge Pump Configuration Register

Address: 0x3A, Reset: 0x0000, Name: CHARGE\_PUMP

The internal charge pump is enabled in this register when the unipolar capability is required.

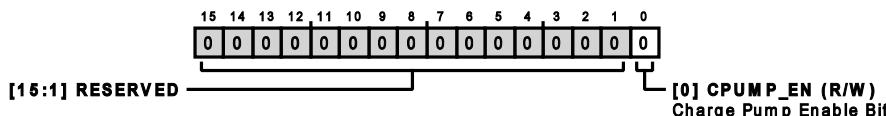


Table 55. Bit Descriptions for CHARGE\_PUMP

| Bits   | Bit Name | Description  | Reset | Access |
|--------|----------|--|-------|--------|
| [15:1] | RESERVED | Reserved.  | 0x0   | R      |
| 0      | CPUMP_EN | Charge Pump Enable Bit.<br>0: disable charge pump.<br>1: enable charge pump. | 0x0   | R/W    |

## REGISTER MAP

### ADC Conversion Control Register

Address: 0x3B, Reset: 0x0000, Name: ADC\_CONV\_CTRL

This register controls the ADC conversions that must be performed.

Disable ADC conversions before making any changes to the ADC\_CONV\_CTRL register.

If enabling a sequence of conversions, ensure that any previous sequence has completed. Ensure that the ADC\_BUSY bit in the LIVE\_STATUS register is 0 before enabling the next sequence.

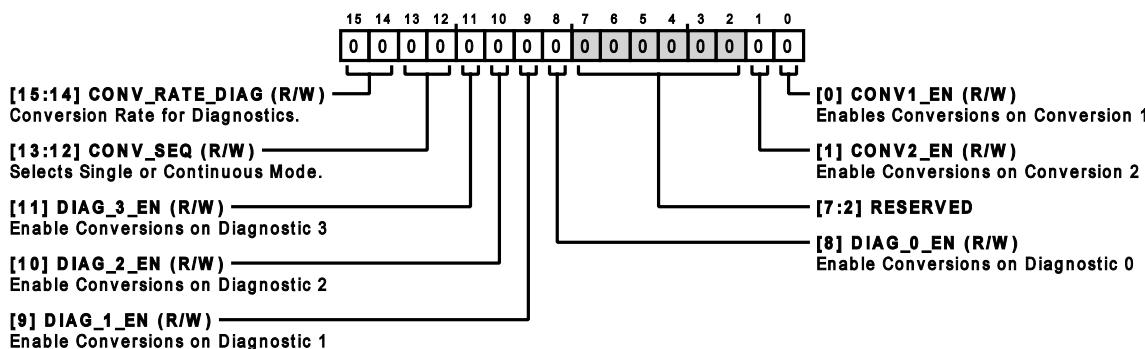


Table 56. Bit Descriptions for ADC\_CONV\_CTRL

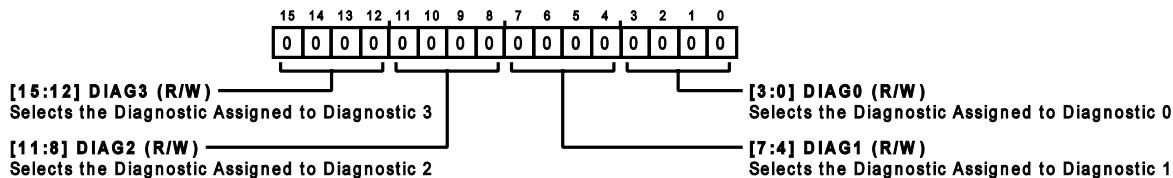
| Bits    | Bit Name       | Description   | Reset | Access |
|---------|----------------|---|-------|--------|
| [15:14] | CONV_RATE_DIAG | Conversion Rate for Diagnostics. A value outside of those listed as follows selects a rate of 20 SPS.<br>00: sampling rate of 20 SPS and provides 50 Hz and 60 Hz noise rejection.<br>01: sampling rate of 4.8 kSPS.<br>10: sampling rate of 9.6 kSPS.  | 0x0   | R/W    |
| [13:12] | CONV_SEQ       | Selects Single or Continuous Mode.<br>00: put ADC in standby mode. If converting continuously, stop conversions at the end of the current sequence and leave the ADC powered up.<br>01: start single sequence conversion. Perform a single conversion on each enabled channel and diagnostic. Once complete, ADC moves to the idle state.<br>10: start continuous conversions. Sequences continuously through the enabled channels and diagnostics. Once conversions are stopped, the sequencer waits until the end of the current sequence before moving to idle or ADC power down.<br>11: stop continuous conversions or power down the ADC. The ADC is powered down and takes 100 $\mu$ s to power up if subsequent conversions are requested. | 0x0   | R/W    |
| 11      | DIAG_3_EN      | Enable Conversions on Diagnostic 3.   | 0x0   | R/W    |
| 10      | DIAG_2_EN      | Enable Conversions on Diagnostic 2.   | 0x0   | R/W    |
| 9       | DIAG_1_EN      | Enable Conversions on Diagnostic 1.   | 0x0   | R/W    |
| 8       | DIAG_0_EN      | Enable Conversions on Diagnostic 0.   | 0x0   | R/W    |
| [7:2]   | RESERVED       | Reserved.   | 0x0   | R      |
| 1       | CONV2_EN       | Enable Conversions on Conversion 2.   | 0x0   | R/W    |
| 0       | CONV1_EN       | Enables Conversions on Conversion 1.  | 0x0   | R/W    |

### Diagnostics Select Register

Address: 0x3C, Reset: 0x0000, Name: DIAG\_ASSIGN

This register assigns diagnostics to the four available diagnostics inputs.

## REGISTER MAP

Table 57. Bit Descriptions for **DIAG\_ASSIGN**

| Bits    | Bit Name | Description  | Reset | Access |
|---------|----------|--|-------|--------|
| [15:12] | DIAG3    | Selects the Diagnostic Assigned to Diagnostic 3.<br>0000: assign AGND to Diagnostic 3.<br>0001: assign the temperature sensor to Diagnostic 3.<br>0010: assign DVCC to Diagnostic 3.<br>0011: assign AVCC to Diagnostic 3.<br>0100: assign ALDO1V8 to Diagnostic 3.<br>0101: assign DLDO1V8 to Diagnostic 3.<br>0110: assign REFOUT to Diagnostic 3.<br>0111: assign AVDD to Diagnostic 3.<br>1000: assign AVSS to Diagnostic 3.<br>1001: assign LVIN to Diagnostic 3.<br>1010: assign SENSEL to Diagnostic 3.<br>1011: assign SENSE_EXT1 to Diagnostic 3.<br>1100: assign SENSE_EXT2 to Diagnostic 3.<br>1101: assign DO_VDD to Diagnostic 3.<br>1110: assign AGND to Diagnostic 3.<br>1111: measure sourcing current from the internal digital output. | 0x0   | R/W    |
| [11:8]  | DIAG2    | Selects the Diagnostic Assigned to Diagnostic 2.<br>0000: assign AGND to Diagnostic 2.<br>0001: assign the temperature sensor to Diagnostic 2.<br>0010: assign DVCC to Diagnostic 2.<br>0011: assign AVCC to Diagnostic 2.<br>0100: assign ALDO1V8 to Diagnostic 2.<br>0101: assign DLDO1V8 to Diagnostic 2.<br>0110: assign REFOUT to Diagnostic 2.<br>0111: assign AVDD to Diagnostic 2.<br>1000: assign AVSS to Diagnostic 2.<br>1001: assign LVIN to Diagnostic 2.<br>1010: assign SENSEL to Diagnostic 2.<br>1011: assign SENSE_EXT1 to Diagnostic 2.<br>1100: assign SENSE_EXT2 to Diagnostic 2.<br>1101: assign DO_VDD to Diagnostic 2.<br>1110: assign AGND to Diagnostic 2.<br>1111: measure sinking current from the internal digital output.  | 0x0   | R/W    |
| [7:4]   | DIAG1    | Selects the Diagnostic Assigned to Diagnostic 1.<br>0000: assign AGND to Diagnostic 1.<br>0001: assign the temperature sensor to Diagnostic 1.<br>0010: assign DVCC to Diagnostic 1.<br>0011: assign AVCC to Diagnostic 1.<br>0100: assign ALDO1V8 to Diagnostic 1.<br>0101: assign DLDO1V8 to Diagnostic 1.<br>0110: assign REFOUT to Diagnostic 1.   | 0x0   | R/W    |

## REGISTER MAP

Table 57. Bit Descriptions for DIAG\_ASSIGN (Continued)

| Bits  | Bit Name | Description   | Reset | Access |
|-------|----------|---|-------|--------|
|       |          | 0111: assign AVDD to Diagnostic 1.<br>1000: assign AVSS to Diagnostic 1.<br>1001: assign LVIN to Diagnostic 1.<br>1010: assign SENSEL to Diagnostic 1.<br>1011: assign SENSE_EXT1 to Diagnostic 1.<br>1100: assign SENSE_EXT2 to Diagnostic 1.<br>1101: assign DO_VDD to Diagnostic 1.<br>1110: assign AGND to Diagnostic 1.<br>1111: measure sourcing current from the external digital output.  |       |        |
| [3:0] | DIAG0    | Selects the Diagnostic Assigned to Diagnostic 0.<br>0000: assign AGND to Diagnostic 0.<br>0001: assign the temperature sensor to Diagnostic 0.<br>0010: assign DVCC to Diagnostic 0.<br>0011: assign AVCC to Diagnostic 0.<br>0100: assign ALDO1V8 to Diagnostic 0.<br>0101: assign DLDO1V8 to Diagnostic 0.<br>0110: assign REFOUT to Diagnostic 0.<br>0111: assign AVDD to Diagnostic 0.<br>1000: assign AVSS to Diagnostic 0.<br>1001: assign LVIN to Diagnostic 0.<br>1010: assign SENSEL to Diagnostic 0.<br>1011: assign SENSE_EXT1 to Diagnostic 0.<br>1100: assign SENSE_EXT2 to Diagnostic 0.<br>1101: assign DO_VDD to Diagnostic 0.<br>1110: assign AGND to Diagnostic 0.<br>1111: measure sinking current from the external digital output. | 0x0   | R/W    |

## Digital Input Level Register

Address: 0x40, Reset: 0x0000, Name: DIN\_COMP\_OUT

This register reflects the debounced output of the digital input comparator.

The I/O/P screw terminal voltage is compared to a programmed threshold voltage. The output of this comparison is fed into a programmable debounce circuit.

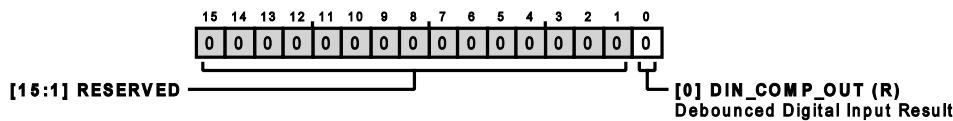


Table 58. Bit Descriptions for DIN\_COMP\_OUT

| Bits   | Bit Name     | Description                     | Reset | Access |
|--------|--------------|---------------------------------|-------|--------|
| [15:1] | RESERVED     | Reserved.                       | 0x0   | R      |
| 0      | DIN_COMP_OUT | Debounced Digital Input Result. | 0x0   | R      |

## Alert Status Register

Address: 0x41, Reset: 0x0001, Name: ALERT\_STATUS

## REGISTER MAP

This register contains the alert status of the alert status bits. Once the alert condition has been removed, write 1 to clear any of the bits in this register.

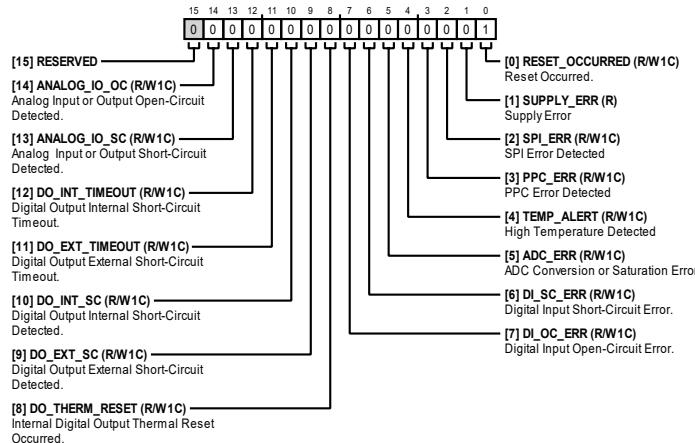


Table 59. Bit Descriptions for ALERT\_STATUS

| Bits | Bit Name       | Description  | Reset | Access |
|------|----------------|--|-------|--------|
| 15   | RESERVED       | Reserved.  | 0x0   | R      |
| 14   | ANALOG_IO_OC   | Analog Input or Output Open-Circuit Detected. This bit is asserted if an open circuit is detected in any of the analog input or output functions.  | 0x0   | R/W1C  |
| 13   | ANALOG_IO_SC   | Analog Input or Output Short-Circuit Detected. This bit is asserted if a short circuit is detected in any of the analog input or output functions.   | 0x0   | R/W1C  |
| 12   | DO_INT_TIMEOUT | Digital Output Internal Short-Circuit Timeout. Digital output internal is disabled.  | 0x0   | R/W1C  |
| 11   | DO_EXT_TIMEOUT | Digital Output External Short-Circuit Timeout. Digital output external is disabled.  | 0x0   | R/W1C  |
| 10   | DO_INT_SC      | Digital Output Internal Short-Circuit Detected. Note that this interrupt does not assert while the digital output FET is in the T1 period of operation.  | 0x0   | R/W1C  |
| 9    | DO_EXT_SC      | Digital Output External Short-Circuit Detected. Note that this interrupt does not assert while the digital output FET is in the T1 period of operation.  | 0x0   | R/W1C  |
| 8    | DO_THERM_RESET | Internal Digital Output Thermal Reset Occurred.  | 0x0   | R/W1C  |
| 7    | DI_OC_ERR      | Digital Input Open-Circuit Error.  | 0x0   | R/W1C  |
| 6    | DI_SC_ERR      | Digital Input Short-Circuit Error.   | 0x0   | R/W1C  |
| 5    | ADC_ERR        | ADC Conversion or Saturation Error.  | 0x0   | R/W1C  |
| 4    | TEMP_ALERT     | High Temperature Detected. This bit asserts if the die temperature reaches 115°C.  | 0x0   | R/W1C  |
| 3    | PPC_ERR        | PPC Error Detected. This bit is asserted if a programmable power control command results in either the PPC_TX_BUSY_ERR or the PPC_TX_ACK_ERR asserting in the PPC_ACTIVE register.   | 0x0   | R/W1C  |
| 2    | SPI_ERR        | SPI Error Detected. This bit is asserted if an SPI transaction does not contain the correct number of SCLKs or if a CRC error is detected.   | 0x0   | R/W1C  |
| 1    | SUPPLY_ERR     | Supply Error. Read the SUPPLY_ALERT_STATUS register to determine the source of this error. This bit is set if any of the fields in the SUPPLY_ALERT_STATUS register are set and the corresponding fields in SUPPLY_ALERT_MASK are 0. This bit clears when all bit fields in SUPPLY_ALERT_STATUS are 0 or masked. | 0x0   | R      |
| 0    | RESET_OCCURRED | Reset Occurred. This bit is asserted after a reset event that asserts the ALERT pin. Write a 1 to this bit to clear the flag. Note that a mask bit is not provided for this bit.   | 0x1   | R/W1C  |

## Live Status Register

Address: 0x42, Reset: 0x0000, Name: LIVE\_STATUS

This register contains the live status of some of the status bits. The bits are not latched and directly reflect the status bits.

## REGISTER MAP

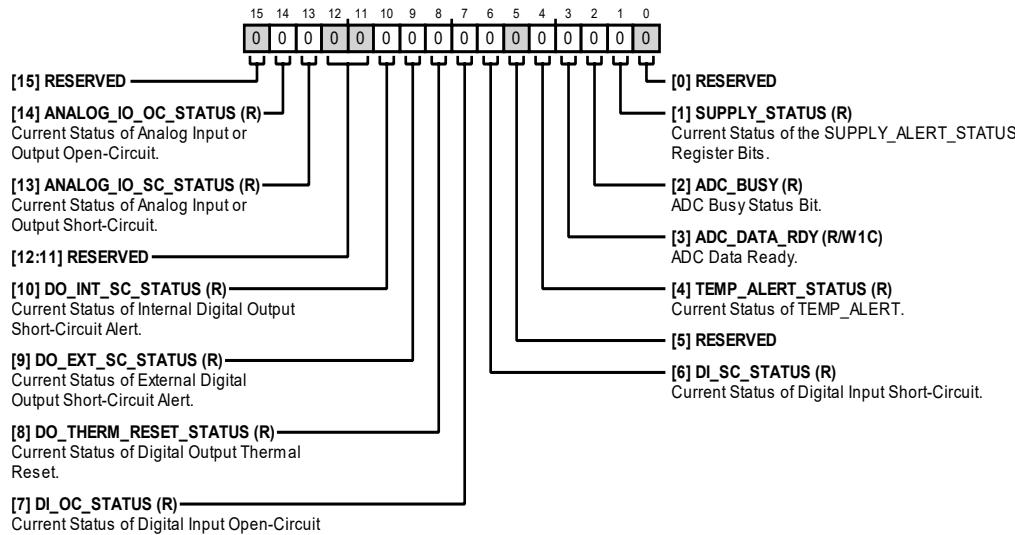


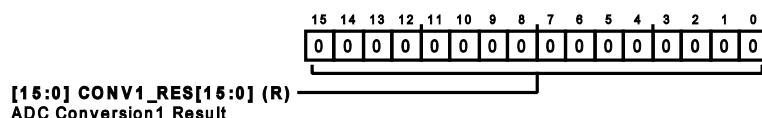
Table 60. Bit Descriptions for LIVE\_STATUS

| Bits    | Bit Name              | Description   | Reset | Access |
|---------|-----------------------|---|-------|--------|
| 15      | RESERVED              | Reserved.   | 0x0   | R      |
| 14      | ANALOG_IO_OC_STATUS   | Current Status of Analog Input or Output Open-Circuit.  | 0x0   | R      |
| 13      | ANALOG_IO_SC_STATUS   | Current Status of Analog Input or Output Short-Circuit.   | 0x0   | R      |
| [12:11] | RESERVED              | Reserved.   | 0x0   | R      |
| 10      | DO_INT_SC_STATUS      | Current Status of Internal Digital Output Short-Circuit Alert. Note: This interrupt does not assert during the T1 short-circuit time.   | 0x0   | R      |
| 9       | DO_EXT_SC_STATUS      | Current Status of External Digital Output Short-Circuit Alert. Note: This interrupt does not assert during the T1 short-circuit time.   | 0x0   | R      |
| 8       | DO_THERM_RESET_STATUS | Current Status of Digital Output Thermal Reset.   | 0x0   | R      |
| 7       | DI_OC_STATUS          | Current Status of Digital Input Open-Circuit.   | 0x0   | R      |
| 6       | DI_SC_STATUS          | Current Status of Digital Input Short-Circuit.  | 0x0   | R      |
| 5       | RESERVED              | Reserved.   | 0x0   | R      |
| 4       | TEMP_ALERT_STATUS     | Current Status of TEMP_ALERT. If the die temperature is at or above typically 115°C, this bit is asserted.  | 0x0   | R      |
| 3       | ADC_DATA_RDY          | ADC Data Ready. In continuous conversion mode, the ADC_RDY pin returns high after 24 µs, but the ADC_DATA_RDY status bit stays asserted until a user writes 1 to clear the bit. | 0x0   | R/W1C  |
| 2       | ADC_BUSY              | ADC Busy Status Bit. This bit resets to 1 as the ADC is initially in a power-up state.  | 0x0   | R      |
| 1       | SUPPLY_STATUS         | Current Status of the SUPPLY_ALERT_STATUS Register Bits.  | 0x0   | R      |
| 0       | RESERVED              | Reserved.   | 0x0   | R      |

## ADC Conversion 1 Result Register

Address: 0x44, Reset: 0x0000, Name: ADC\_RESULT1

This register contains the 16 bits of the ADC conversion result.



## REGISTER MAP

Table 61. Bit Descriptions for ADC\_RESULT1

| Bits   | Bit Name        | Description             | Reset | Access |
|--------|-----------------|-------------------------|-------|--------|
| [15:0] | CONV1_RES[15:0] | ADC Conversion1 Result. | 0x0   | R      |

### ADC Conversion 2 Result Register

Address: 0x46, Reset: 0x0000, Name: ADC\_RESULT2

This register contains the 16 bits of the ADC conversion result.

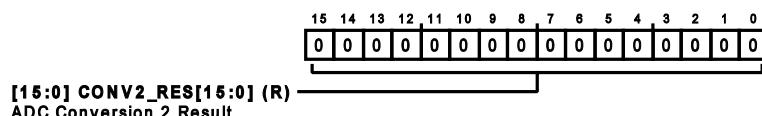


Table 62. Bit Descriptions for ADC\_RESULT2

| Bits   | Bit Name        | Description              | Reset | Access |
|--------|-----------------|--------------------------|-------|--------|
| [15:0] | CONV2_RES[15:0] | ADC Conversion 2 Result. | 0x0   | R      |

### Diagnostic Results Registers

Address: 0x53 to 0x56, Reset: 0x0000, Name: ADC\_DIAG\_RESULTx

These four registers contain the 16-bit diagnostic conversion results.

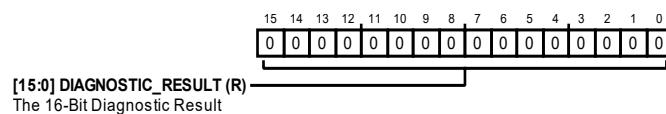


Table 63. Bit Descriptions for ADC\_DIAG\_RESULTx

| Bits   | Bit Name          | Description                   | Reset | Access |
|--------|-------------------|-------------------------------|-------|--------|
| [15:0] | DIAGNOSTIC_RESULT | The 16-Bit Diagnostic Result. | 0x0   | R      |

### Digital Input Counter Register

Address: 0x57, Reset: 0x0000, Name: DIN\_COUNTER

This register reflects the digital input counter value when the COUNT\_EN bit in DIN\_CONFIG1 register is set. This count is allowed to roll over from full scale back to 0; therefore, read this register often enough to avoid unexpected roll-over.

Note that, when the enable signal is low, the count is frozen.

The INV\_DIN\_COMP\_OUT bit inverts the deglitched output allowing the counter increment edge to be modified.

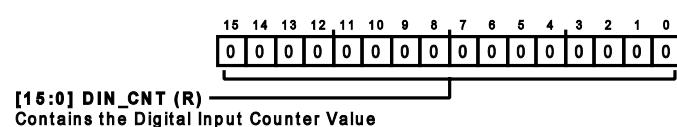


Table 64. Bit Descriptions for DIN\_COUNTER

| Bits   | Bit Name | Description   | Reset | Access |
|--------|----------|---|-------|--------|
| [15:0] | DIN_CNT  | Contains the Digital Input Counter Value. This counter is enabled when the COUNT_EN bit within the DIN_CONFIG1 register is set. When the enable signal is low, the count is frozen. This count is allowed to roll over by design, as in normal operation, and its update rate must be slow. Read the counter often enough to avoid unexpected roll over. The INV_DIN_COMP_OUT bit inverts the deglitched output allowing the counter increment edge to be modified. | 0x0   | R      |

## REGISTER MAP

## Supply Alert Status Register

Address: 0x5B, Reset: 0x0000, Name: SUPPLY\_ALERT\_STATUS

This register contains the supply alert status bits. Once the alert condition has been removed, write 1 to clear the bits in this register.

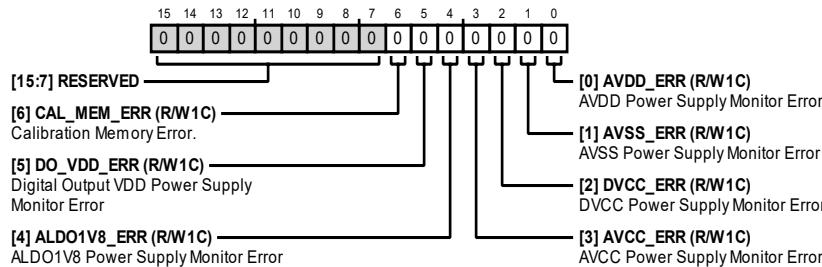


Table 65. Bit Descriptions for SUPPLY\_ALERT\_STATUS

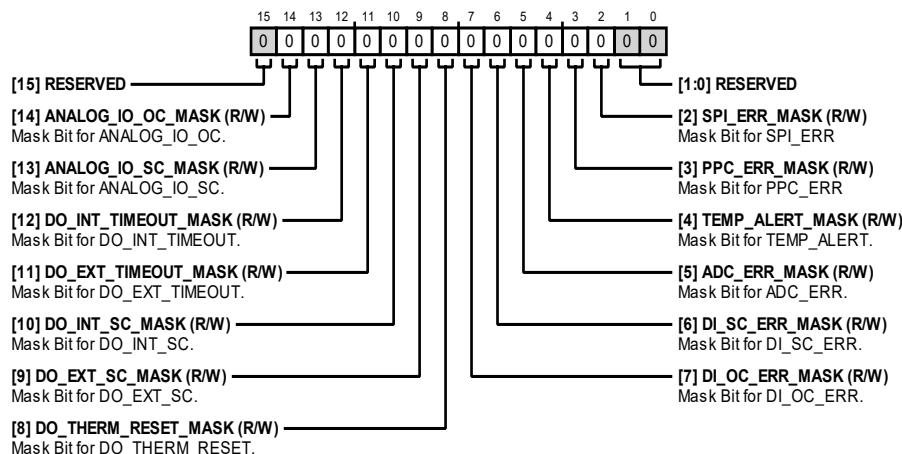
| Bits   | Bit Name    | Description   | Reset | Access |
|--------|-------------|---|-------|--------|
| [15:7] | RESERVED    | Reserved.   | 0x0   | R      |
| 6      | CAL_MEM_ERR | Calibration Memory Error. This flag asserts when a calibration memory CRC error or an uncorrectable error correcting code (ECC) error is detected on calibration memory upload, or when there is an attempted SPI access to a register when the memory refresh has not completed. (Do not address this device until the one time programmable (OTP) memory is uploaded.) If this bit is asserted, it is recommended to reset the device and check the supplies. | 0x0   | R/W1C  |
| 5      | DO_VDD_ERR  | Digital Output VDD Power Supply Monitor Error. This bit is asserted when digital output VDD falls below 9.3 V.  | 0x0   | R/W1C  |
| 4      | ALDO1V8_ERR | ALDO1V8 Power Supply Monitor Error. This bit is asserted when ALDO1V8 falls below 1.4 V.  | 0x0   | R/W1C  |
| 3      | AVCC_ERR    | AVCC Power Supply Monitor Error. This bit is asserted when AVCC falls below 4.1 V.  | 0x0   | R/W1C  |
| 2      | DVCC_ERR    | DVCC Power Supply Monitor Error. This bit is asserted when DVCC falls below 1.9 V.  | 0x0   | R/W1C  |
| 1      | AVSS_ERR    | AVSS Power Supply Monitor Error. This bit is asserted when AVSS goes above -1.6V.   | 0x0   | R/W1C  |
| 0      | AVDD_ERR    | AVDD Power Supply Monitor Error. This bit is asserted when AVDD falls below 5.5 V.  | 0x0   | R/W1C  |

## Alert Mask Register for ALERT\_STATUS

Address: 0x5F, Reset: 0x0000, Name: ALERT\_MASK

This register is used to mask specific status bits from activating the ALERT pin. The position of mask bits in this register line up the corresponding status bits in the ALERT\_STATUS register. To mask a specific alert condition, set the corresponding mask bit to 1.

Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT\_STATUS register.



## REGISTER MAP

Table 66. Bit Descriptions for ALERT\_MASK

| Bits  | Bit Name            | Description                  | Reset | Access |
|-------|---------------------|------------------------------|-------|--------|
| 15    | RESERVED            | Reserved.                    | 0x0   | R      |
| 14    | ANALOG_IO_OC_MASK   | Mask Bit for ANALOG_IO_OC.   | 0x0   | R/W    |
| 13    | ANALOG_IO_SC_MASK   | Mask Bit for ANALOG_IO_SC.   | 0x0   | R/W    |
| 12    | DO_INT_TIMEOUT_MASK | Mask Bit for DO_INT_TIMEOUT. | 0x0   | R/W    |
| 11    | DO_EXT_TIMEOUT_MASK | Mask Bit for DO_EXT_TIMEOUT. | 0x0   | R/W    |
| 10    | DO_INT_SC_MASK      | Mask Bit for DO_INT_SC.      | 0x0   | R/W    |
| 9     | DO_EXT_SC_MASK      | Mask Bit for DO_EXT_SC.      | 0x0   | R/W    |
| 8     | DO_THERM_RESET_MASK | Mask Bit for DO_THERM_RESET. | 0x0   | R/W    |
| 7     | DI_OC_ERR_MASK      | Mask Bit for DI_OC_ERR.      | 0x0   | R/W    |
| 6     | DI_SC_ERR_MASK      | Mask Bit for DI_SC_ERR.      | 0x0   | R/W    |
| 5     | ADC_ERR_MASK        | Mask Bit for ADC_ERR.        | 0x0   | R/W    |
| 4     | TEMP_ALERT_MASK     | Mask Bit for TEMP_ALERT.     | 0x0   | R/W    |
| 3     | PPC_ERR_MASK        | Mask Bit for PPC_ERR.        | 0x0   | R/W    |
| 2     | SPI_ERR_MASK        | Mask Bit for SPI_ERR.        | 0x0   | R/W    |
| [1:0] | RESERVED            | Reserved.                    | 0x0   | R      |

## Alert Mask Register for SUPPLY\_ALERT\_STATUS

Address: 0x60, Reset: 0x0000, Name: SUPPLY\_ALERT\_MASK

This register is used to mask specific SUPPLY\_ALERT\_STATUS bits from activating the ALERT pin. The position of mask bits in this register line up the corresponding status bits in the SUPPLY\_ALERT\_STATUS register. To mask a particular alert, set the corresponding mask bit to 1. Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT\_STATUS register.

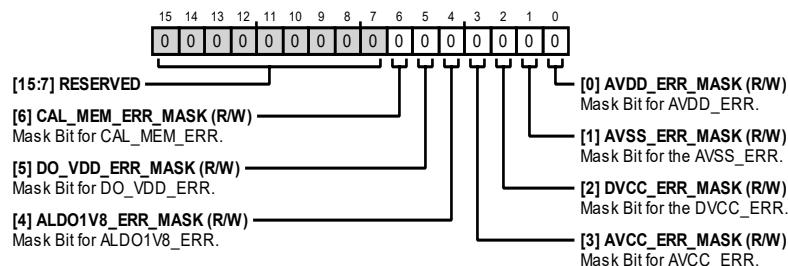


Table 67. Bit Descriptions for SUPPLY\_ALERT\_MASK

| Bits   | Bit Name         | Description                | Reset | Access |
|--------|------------------|----------------------------|-------|--------|
| [15:7] | RESERVED         | Reserved.                  | 0x0   | R      |
| 6      | CAL_MEM_ERR_MASK | Mask Bit for CAL_MEM_ERR.  | 0x0   | R/W    |
| 5      | DO_VDD_ERR_MASK  | Mask Bit for DO_VDD_ERR.   | 0x0   | R/W    |
| 4      | ALDO1V8_ERR_MASK | Mask Bit for ALDO1V8_ERR.  | 0x0   | R/W    |
| 3      | AVCC_ERR_MASK    | Mask Bit for AVCC_ERR.     | 0x0   | R/W    |
| 2      | DVCC_ERR_MASK    | Mask Bit for the DVCC_ERR. | 0x0   | R/W    |
| 1      | AVSS_ERR_MASK    | Mask Bit for the AVSS_ERR. | 0x0   | R/W    |
| 0      | AVDD_ERR_MASK    | Mask Bit for AVDD_ERR.     | 0x0   | R/W    |

## Readback Select Register

Address: 0x64, Reset: 0x0000, Name: READ\_SELECT

This register selects the address of the register required to be read back and determines the contents of the SPI readback frame.

## REGISTER MAP

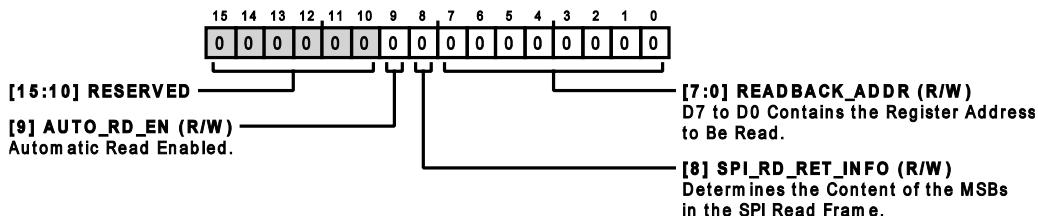


Table 68. Bit Descriptions for READ\_SELECT

| Bits    | Bit Name        | Description  | Reset | Access |
|---------|-----------------|--|-------|--------|
| [15:10] | RESERVED        | Reserved.  | 0x0   | R      |
| 9       | AUTO_RD_EN      | Automatic Read Enabled. When this bit is set to 1, read data is returned on the SDO on every SPI access. The location read is determined by READBACK_ADDR.   | 0x0   | R/W    |
| 8       | SPI_RD_RET_INFO | Determines the Content of the MSBs in the SPI Read Frame. When this bit is set to 0, READBACK_ADDR[6:0] is returned in Bits[30:24] of any subsequent SPI read. When this bit is set to 1, the ADC_RDY and ALERT flags and the four DIN outputs are returned in Bits[30:24] of any subsequent SPI read. | 0x0   | R/W    |
| [7:0]   | READBACK_ADDR   | D7 to D0 Contains the Register Address to Be Read.   | 0x0   | R/W    |

## Select the Registers Read in Burst Mode

Address: 0x65, Reset: 0x03FF, Name: BURST\_READ\_SEL

This register can be used to select which registers are returned on a burst read that includes any of the ALERT\_STATUS, LIVE\_STATUS, ADC\_RESULTx, ADC\_DIAG\_RESULTx, and DIN\_COUNTER registers.

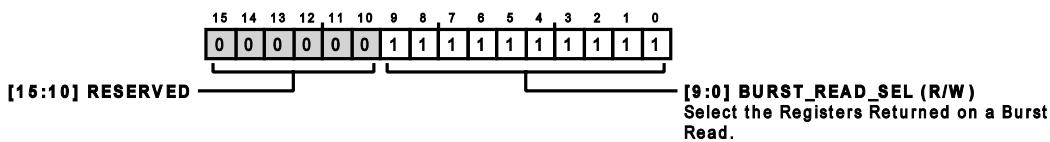


Table 69. Bit Descriptions for BURST\_READ\_SEL

| Bits    | Bit Name       | Description   | Reset | Access |
|---------|----------------|---|-------|--------|
| [15:10] | RESERVED       | Reserved.   | 0x0   | R      |
| [9:0]   | BURST_READ_SEL | <p>Select the Registers Returned on a Burst Read. If a bit corresponding to a register is 0, that register is skipped during the burst read.</p> <p>Bit 0: enable burst read of the ALERT_STATUS register.</p> <p>Bit 1: enable burst read of the LIVE_STATUS register.</p> <p>Bit 2: enable burst read of the ADC_RESULT1 register.</p> <p>Bit 3: enable burst read of the ADC_RESULT2 register.</p> <p>Bit 4: enable burst read of the ADC_DIAG_RESULT0 register.</p> <p>Bit 5: enable burst read of the ADC_DIAG_RESULT1 register.</p> <p>Bit 6: enable burst read of the ADC_DIAG_RESULT2 register.</p> <p>Bit 7: enable burst read of the ADC_DIAG_RESULT3 register.</p> <p>Bit 8: enable burst read of the DIN_COUNTER register.</p> <p>Bit 9: enable burst read of the SUPPLY_ALERT_STATUS register.</p> <p>Read data for all registers outside of those previously listed always return on a burst read if the burst read includes the register. Note that the starting address location of a burst read is always returned even if its corresponding BURST_READ_SEL bit is 0. Burst reads can start at DIN_COMP_OUT to include this as the first register in a burst read. However, DIN_COMP_OUT does not have a corresponding BURST_READ_SEL bit.</p> | 0x3FF | R/W    |

## REGISTER MAP

### PPC Transmit Register

Address: 0x66, Reset: 0x00FF, Name: PPC\_TX

Programmable power control voltage configuration register. This register allows the power supply voltage generated by the ADP1034 to be configured via the OWSI to adjust the AD74115 power supply, AVDD.

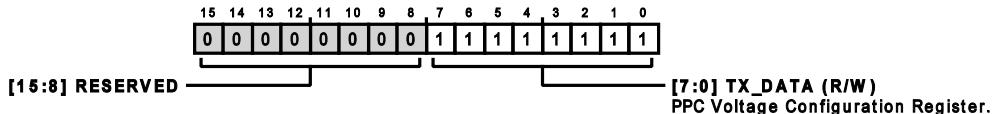


Table 70. Bit Descriptions for PPC\_TX

| Bits   | Bit Name | Description  | Reset | Access |
|--------|----------|--|-------|--------|
| [15:8] | RESERVED | Reserved.  | 0x0   | R      |
| [7:0]  | TX_DATA  | PPC Voltage Configuration Register. These bits reset to the maximum power supply voltage that matches the ADP1034 configuration. Note that once these bits are updated, further writes are blocked until the transmission completes. | 0xFF  | R/W    |

### PPC Status Register

Address: 0x6E, Reset: 0x00FF, Name: PPC\_ACTIVE

This read only register provides status information on the OWSI transactions.

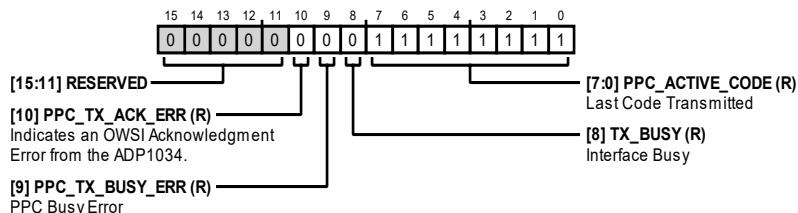


Table 71. Bit Descriptions for PPC\_ACTIVE

| Bits    | Bit Name        | Description   | Reset | Access |
|---------|-----------------|---|-------|--------|
| [15:11] | RESERVED        | Reserved.   | 0x0   | R      |
| 10      | PPC_TX_ACK_ERR  | Indicates an OWSI Acknowledgment Error from the ADP1034. This bit is set if a second attempt to write to the ADP1034 is not acknowledged. When the ADP1034 does not acknowledge an initial data transfer, the OWSI controller attempts a second OWSI transfer to the PPC. If this second transfer is not successful, this bit asserts. This flag is cleared when the PPC_ERR bit is programmed to 1 in the ALERT_STATUS register. | 0x0   | R      |
| 9       | PPC_TX_BUSY_ERR | PPC Busy Error. This bit indicates that a write to the PPC_TX register was blocked because the TX_BUSY bit is set. This flag is cleared when PPC_ERR is programmed to 1 in the ALERT_STATUS register.   | 0x0   | R      |
| 8       | TX_BUSY         | Interface Busy. Indicates that TX_DATA is in the process or waiting to be transmitted. Do not attempt a write to TX_DATA while this bit is set. This bit deasserts once TX_DATA is transmitted.   | 0x0   | R      |
| [7:0]   | PPC_ACTIVE_CODE | Last Code Transmitted. These bits reflect the last successfully transmitted data to the ADP1034.  | 0xFF  | R      |

## REGISTER MAP

## Thermal Reset Enable Register

Address: 0x77, Reset: 0x0000, Name: THERM\_RST

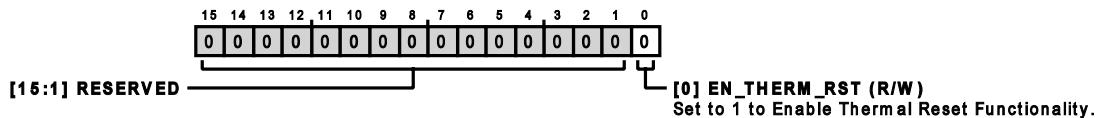


Table 72. Bit Descriptions for THERM\_RST

| Bits   | Bit Name     | Description  | Reset | Access |
|--------|--------------|--|-------|--------|
| [15:1] | RESERVED     | Reserved.  | 0x0   | R      |
| 0      | EN_THERM_RST | Set to 1 to Enable Thermal Reset Functionality. If the die temperature reaches typically 140°C, a thermal reset event triggers a digital reset, which is detected via a change in the ALERT pin and the RESET_OCCURRED flag. | 0x0   | R/W    |

## Command Register

Address: 0x78, Reset: 0x0000, Name: CMD\_KEY

This register is used to issue specific commands to the device.

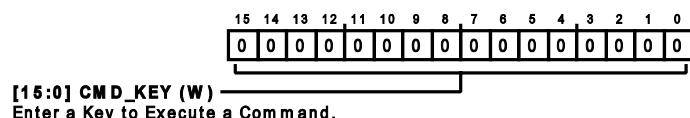


Table 73. Bit Descriptions for CMD\_KEY

| Bits   | Bit Name | Description   | Reset | Access |
|--------|----------|---|-------|--------|
| [15:0] | CMD_KEY  | Enter a Key to Execute a Command.<br>0x15FA: Software Reset Key 1. To trigger a software reset, write to this key followed by Software Reset Key 2. The SPI writes must be back to back.<br>0xAF51: Software Reset Key 2. To trigger a software reset, write to Software Reset Key 1 followed by this key. The SPI writes must be back to back.<br>The CAL_MEM_ERR bit asserts if there is an SPI access while the fuses are being uploaded. Therefore, it is possible to determine when the fuse upload has completed by repeatedly reading and clearing the CAL_MEM_ERR bit until it does not assert on an SPI access. Note that the oscillator trim bits are passed from the shadow register to the active register (connected to oscillator) upon completion of the ECC in the user mode. In test mode, oscillator trim bits pass directly to the active register during fuse reading. Therefore, it is recommended to upload fuses in user mode only to avoid errant trim bits being passed to the oscillator. | 0x0   | W      |

## Scratch or Spare Register

Address: 0x79 to 0x7A (Increments of 1), Reset: 0x0000, Name: SCRATCHx

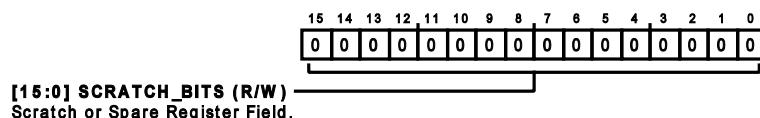


Table 74. Bit Descriptions for SCRATCHx

| Bits   | Bit Name     | Description                      | Reset | Access |
|--------|--------------|----------------------------------|-------|--------|
| [15:0] | SCRATCH_BITS | Scratch or Spare Register Field. | 0x0   | R/W    |

## REGISTER MAP

### Silicon Revision Register

Address: 0x7B, Reset: 0x0001, Name: SILICON\_REV

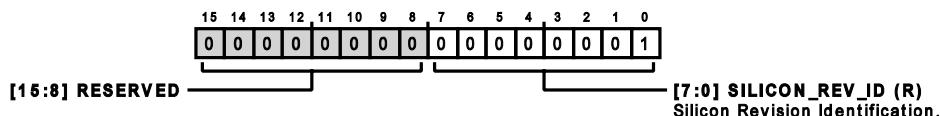


Table 75. Bit Descriptions for SILICON\_REV

| Bits   | Bit Name       | Description                      | Reset | Access |
|--------|----------------|----------------------------------|-------|--------|
| [15:8] | RESERVED       | Reserved.                        | 0x0   | R      |
| [7:0]  | SILICON_REV_ID | Silicon Revision Identification. | 0x1   | R      |

### Silicon ID 0 Register

Address: 0x7C, Reset: 0x0000, Name: SILICON\_ID0

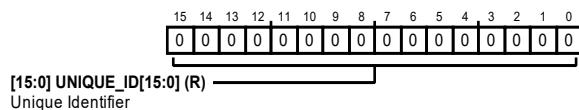


Table 76. Bit Descriptions for SILICON\_ID0

| Bits   | Bit Name        | Description       | Reset | Access |
|--------|-----------------|-------------------|-------|--------|
| [15:0] | UNIQUE_ID[15:0] | Unique Identifier | 0x0   | R      |

### Silicon ID 1 Register

Address: 0x7D, Reset: 0x0000, Name: SILICON\_ID1

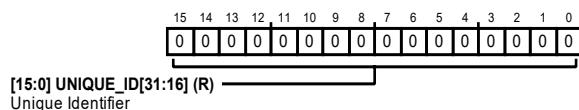


Table 77. Bit Descriptions for SILICON\_ID1

| Bits   | Bit Name         | Description       | Reset | Access |
|--------|------------------|-------------------|-------|--------|
| [15:0] | UNIQUE_ID[31:16] | Unique Identifier | 0x0   | R      |

### Silicon ID 2 Register

Address: 0x7E, Reset: 0x0000, Name: SILICON\_ID2

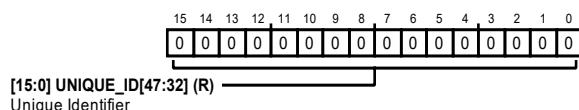


Table 78. Bit Descriptions for SILICON\_ID2

| Bits   | Bit Name         | Description       | Reset | Access |
|--------|------------------|-------------------|-------|--------|
| [15:0] | UNIQUE_ID[47:32] | Unique Identifier | 0x0   | R      |

**REGISTER MAP****Silicon ID 3 Register**

Address: 0x7F, Reset: 0x0000, Name: SILICON\_ID3

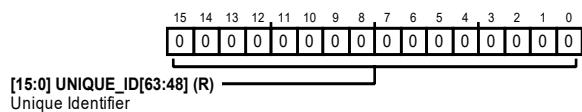


Table 79. Bit Descriptions for SILICON\_ID3

| Bits   | Bit Name         | Description       | Reset | Access |
|--------|------------------|-------------------|-------|--------|
| [15:0] | UNIQUE_ID[63:48] | Unique Identifier | 0x0   | R      |

## OUTLINE DIMENSIONS

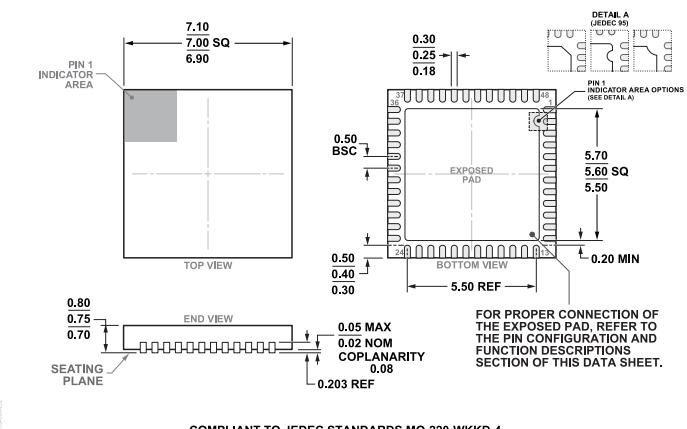


Figure 59. 48-Lead Lead Frame Chip Scale Package [LFCSP]

7 mm x 7 mm and 0.75 mm Package Height

(CP-48-13)

Dimensions shown in millimeters

Updated: November 12, 2022

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                             | Packing Quantity | Package Option |
|--------------------|-------------------|---|------------------|----------------|
| AD74115BCPZ        | -40°C to +105°C   | 48-Lead LFCSP (7 mm x 7 mm x 0.75 mm with EPAD) | Tray, 260        | CP-48-13       |
| AD74115BCPZ-RL7    | -40°C to +105°C   | 48-Lead LFCSP (7 mm x 7 mm x 0.75 mm with EPAD) | Reel, 750        | CP-48-13       |

<sup>1</sup> Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model <sup>1</sup> | Description      |
|--------------------|------------------|
| EVAL-AD74115-ARDZ  | Evaluation Board |

<sup>1</sup> Z = RoHS Compliant Part.

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