

MAX32670/MAX32671

High-Reliability, Ultra-Low-Power Microcontroller Powered by Arm Cortex-M4 Processor with FPU for Industrial and IoT

General Description

In the Darwin family, the MAX32670/MAX32671 are ultra-low-power, cost-effective, high-reliability 32-bit microcontrollers enabling designs with complex sensor processing without compromising battery life. They combine a flexible and versatile power management unit with the powerful Arm® Cortex®-M4 processor with a floating point unit (FPU). The MAX32670/MAX32671 also offer legacy designs an easy and cost optimal upgrade path from 8- or 16-bit microcontrollers.

The devices integrate up to 384KB of flash and 160KB of SRAM to accommodate application and sensor code. Error correction coding (ECC), capable of single error correction and double error detection (SEC-DED), is implemented over the entire flash, RAM, and cache to ensure ultra-reliable code execution for demanding applications. Additional features such as the two windowed watchdog timers with fully flexible and independent clocking have been added to further enhance reliable operation. Brown-out detection ensures proper operation during power-down/power-up events and unexpected supply transients.

Multiple high-speed peripherals such as 3.4MHz I²C, 50MHz SPI, and 4MBd UARTs are included to maximize communication bandwidth. In addition, a low-power UART is available for operation in the lowest power sleep modes to facilitate wakeup on activity without any loss of data. A total of six timers with I/O capability are provided, including two low-power timers to enable pulse counting, capture/compare, and PWM generation even in the lowest power sleep modes. All of this capability is packaged in a tiny form factor: 5mm x 5mm, 40-pin TQFN-EP.

Applications

- Smart Sensor Controller
- Industrial Sensors
- Optical Communication Modules
- Secure Radio Modem Controller
- Battery-Powered Medical Devices
- System Housekeeping Controller
- Algorithm Coprocessor

Ordering Information appears at end of data sheet.

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Benefits and Features

- High-Efficiency Microcontroller for Low-Power, High-Reliability Devices
 - Arm Cortex-M4 Core with FPU up to 100MHz
 - 384KB Flash Memory with Error Correction
 - 160KB SRAM (128KB with ECC Enabled), Optionally Preserved in Lowest Power Modes
 - 16KB Unified Cache with ECC
 - UART Bootloader
 - Dual- or Single-Supply Operation
 - Ultra-Low 0.9V to 1.1V V_{CORE} Supply Voltage
 - Internal LDO Operation from 1.7V to 3.6V Single Supply
 - Wide Operating Temperature: -40°C to +105°C
- Flexible Clocking Schemes
 - Internal High-Speed 100MHz Oscillator
 - Internal Low-Power 7.3728MHz and Ultra-Low-Power 80kHz Oscillators
 - 16MHz to 32MHz Oscillator (External Crystal Required)
 - 32.768kHz Oscillator (External Crystal Required)
 - External Clock Input for the Core
 - External Clock Input for the LPUART and LPTMR
- Power Management Maximizes Uptime for Battery Applications
 - 44µA/MHz Active at 0.9V up to 12MHz
 - 50µA/MHz Active at 1.1V up to 100MHz
 - 2.6µA Full Memory Retention Power in BACKUP Mode at V_{DD} = 1.8V
 - 350nA Ultra-Low-Power RTC at V_{DD} = 1.8V
 - Wake from LPUART or LPTMR
- Optimal Peripheral Mix Provides Platform Scalability
 - Up to 31 General-Purpose I/O Pins
 - Up to Three SPI Master/Slave (up to 50MHz)
 - Up to Three 4-Wire UART
 - One Low-Power UART (LPUART)
 - Up to Three I²C Master/Slave 3.4Mbps High Speed
 - 8-Channel Standard DMA Controller
 - Up to Four 32-Bit Timers (TMR)
 - Up to Two Low-Power 32-Bit Timers (LPTMR)
 - Two Windowed Watchdog Timers
 - One I²S Slave for Digital Audio Interface
- Security and Integrity
 - Available Secure Boot
 - AES 128/192/256 Hardware Acceleration Engine
 - 32-Bit CRC Acceleration Engine

Simplified Block Diagram

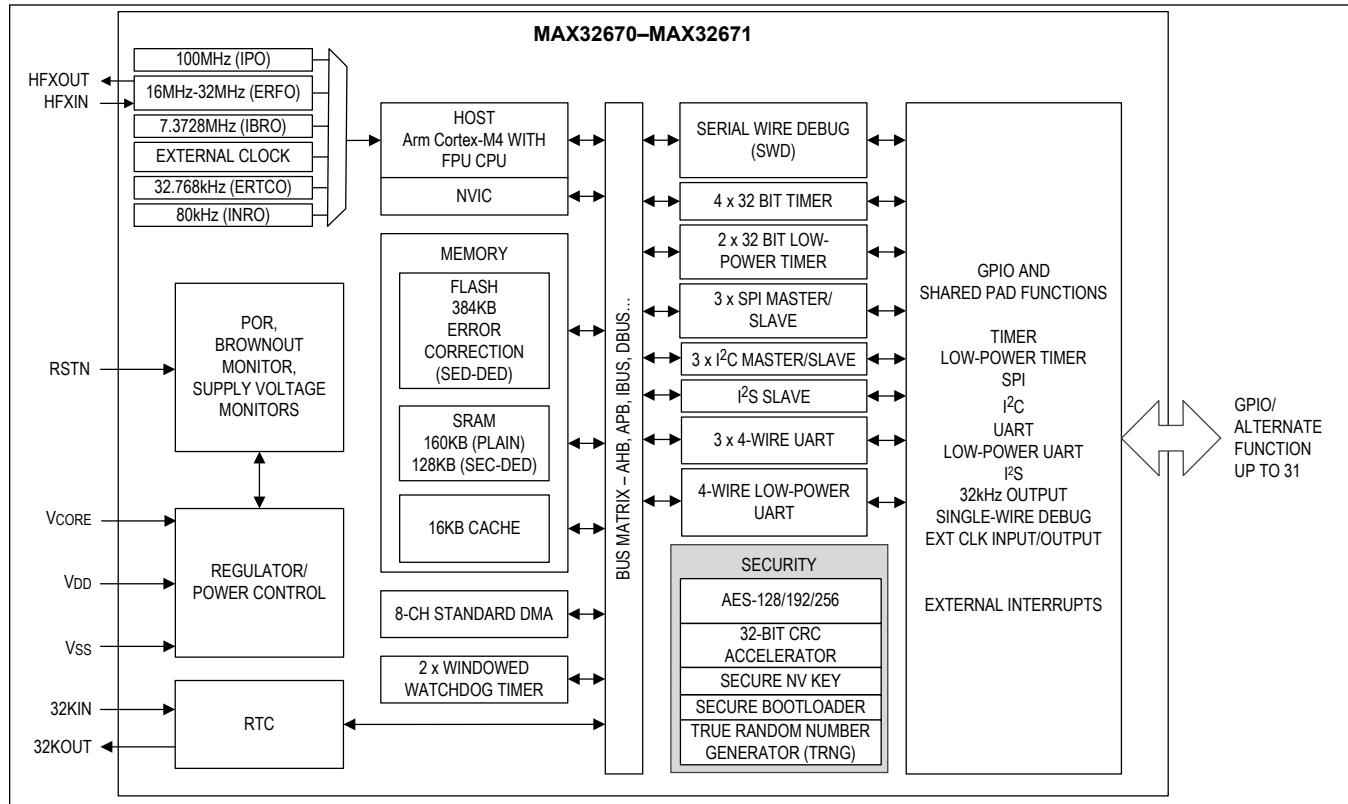


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Absolute Maximum Ratings

(All voltages with respect to V_{SS} , unless otherwise noted.)	
V_{CORE}	-0.3V to +1.21V
V_{DD}	-0.3V to +3.63V
$HFXIN, HFXOUT$	-0.2V to V_{COREV}
32KIN, 32KOUT, RSTN, GPIO	-0.3V to V_{DD} + 0.3V
Total Current into All GPIO Combined (sink)	100mA
V_{SS}	100mA
Output Current (sink) by Any GPIO Pin	25mA

Output Current (source) by Any GPIO Pin	-25mA
Continuous Package Power Dissipation 40 TQFN-EP (multilayer board) $T_A = +70^\circ\text{C}$ (derate $35.7\text{mW}/^\circ\text{C}$ above $+70^\circ\text{C}$)	2857.10mW
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

40 TQFN-EP

Package Code	T4055+1
Outline Number	21-0140
Land Pattern Number	90-0016
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](#). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](#).

Electrical Characteristics

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER / BOTH SINGLE-SUPPLY OPERATION AND DUAL-SUPPLY OPERATION						
Supply Voltage	V_{DD}		1.71	1.8	3.63	V
Supply Voltage, Core	V_{CORE}	Dual-supply operation	OVR = [00]	0.855	0.9	0.945
			OVR = [01]	0.95	1.0	1.05
			Default OVR = [10]	1.045	1.1	1.155
		No power supply connection for single supply operation	—	—	—	
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}	1.58	1.71	—	V
		Monitors V_{CORE} during dual-supply operation	0.77	—	0.845	
Power-on-Reset Voltage	V_{POR}	Monitors V_{DD}	—	1.4	—	V
		Monitors V_{CORE} during dual-supply operation	—	0.58	—	

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER / SINGLE-SUPPLY OPERATION (V_{DD} ONLY)						
V _{DD} Current ACTIVE Mode	IDD_DACTS	Dynamic, IPO enabled, total current into V_{DD} pin, $V_{DD} = 3.3\text{V}$, CPU in ACTIVE mode, executing CoreMark®, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(MAX)} = 100\text{MHz}$	57.5		
		OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(MAX)} = 50\text{MHz}$	55.7			
		OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(MAX)} = 12\text{MHz}$	52.2			
		OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(MAX)} = 100\text{MHz}$	56.9			
		OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(MAX)} = 50\text{MHz}$	55.3			
		OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(MAX)} = 12\text{MHz}$	52			
		OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(MAX)} = 100\text{MHz}$	43			
		OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(MAX)} = 50\text{MHz}$	40.7			
		OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(MAX)} = 12\text{MHz}$	37.5			

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDD_FACTS	Dynamic, IPO enabled, total current into V_{DD} pin, $V_{DD} = 1.8\text{V}$, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(\text{MAX})} = 100\text{MHz}$		42.4		µA
		OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(\text{MAX})} = 50\text{MHz}$		40.5		
		OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(\text{MAX})} = 12\text{MHz}$		38.2		
	Fixed, IPO enabled, total current into V_{DD} pin, $V_{DD} = 3.3\text{V}$, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See Temperature Variance		735		
		OVR = [01], internal regulator set to 1.0V. See Temperature Variance		659		
		OVR = [00], internal regulator set to 0.9V. See Temperature Variance		563		
	Fixed, IPO enabled, total current into V_{DD} pin, $V_{DD} = 1.8\text{V}$, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See Temperature Variance		754		
		OVR = [01], internal regulator set to 1.0V. See Temperature Variance		663		
		OVR = [00], internal regulator set to 0.9V. See Temperature Variance		538		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Current SLEEP Mode	IDD_DSLPS	Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, f _{SYS_CLK(MAX)} = 100MHz	30		µA/MHz
			OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz	28.8		
			OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz	28.0		
		Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, f _{SYS_CLK(MAX)} = 100MHz	36.4		
			OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz	28.5		
			OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz	28.1		
	IDD_DSLP0	Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, f _{SYS_CLK(MAX)} = 100MHz	13.4		
			OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz	11.8		
			OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz	10.6		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I _{DD_FSLPS}	Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, f _{SYS_CLK(MAX)} = 100MHz		14.6		µA
		OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz		11.7		
		OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz		10.5		
	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See Temperature Variance		735		
		OVR = [01], internal regulator set to 1.0V. See Temperature Variance		659		
		OVR = [00], internal regulator set to 0.9V. See Temperature Variance		563		
	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See Temperature Variance		754		
		OVR = [01], internal regulator set to 1.0V. See Temperature Variance		633		
		OVR = [00], internal regulator set to 0.9V. See Temperature Variance		538		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Fixed Current, DEEPSLEEP Mode	I _{DD_FDSLPS}	Standby state with full data retention and 160KB SRAM retained	V _{DD} = 3.3V. See Temperature Variance	4.0		µA
			V _{DD} = 1.8V. See Temperature Variance	3.7		
V _{DD} Fixed Current, BACKUP Mode	I _{DD_FBKUS}	V _{DD} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled. See Temperature Variance	0.38		µA
			20KB SRAM retained. See Temperature Variance	1.08		
			40KB SRAM retained. See Temperature Variance	1.4		
			80KB SRAM retained. See Temperature Variance	1.9		
			160KB SRAM retained. See Temperature Variance	2.8		
		V _{DD} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled. See Temperature Variance	0.15		
			20KB SRAM retained. See Temperature Variance	0.86		
			40KB SRAM retained. See Temperature Variance	1.2		
			80KB SRAM retained. See Temperature Variance	1.7		
			160KB SRAM retained. See Temperature Variance	2.58		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, STORAGE Mode	I _{DD_FSTOS}	$V_{DD} = 3.3\text{V}$. See Temperature Variance	0.3			μA
		$V_{DD} = 1.8\text{V}$. See Temperature Variance	0.11			
SLEEP Mode Resume Time	t _{SLP_ONS}			2.1		μs
DEEPSLEEP Mode Resume Time	t _{DSL_ONS}	fast_wk_en = 1		89		μs
		fast_wk_en = 0		129		
BACKUP Mode Resume Time	t _{BKU_ONS}	Includes system initialization and ROM execution time		1.25		ms
STORAGE Mode Resume Time	t _{STO_ONS}	Includes system initialization and ROM execution time		1.5		ms

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER / DUAL-SUPPLY OPERATION (V_{DD} AND V_{CORE})						
V_{CORE} Current, ACTIVE Mode	I _{CORE_DACTD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{CORE} = 1.1\text{V}$, $f_{SYS_CLK(\text{MAX})} = 100\text{MHz}$	56.7		$\mu\text{A}/\text{MHz}$
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [01], $V_{CORE} = 1.0\text{V}$, $f_{SYS_CLK(\text{MAX})} = 50\text{MHz}$	55.3		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [00], $V_{CORE} = 0.9\text{V}$, $f_{SYS_CLK(\text{MAX})} = 12\text{MHz}$	48.9		
	I _{CORE_FACTD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{CORE} = 1.1\text{V}$, $f_{SYS_CLK(\text{MAX})} = 100\text{MHz}$	42.2		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [01], $V_{CORE} = 1.0\text{V}$, $f_{SYS_CLK(\text{MAX})} = 50\text{MHz}$	40.5		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [00], $V_{CORE} = 0.9\text{V}$, $f_{SYS_CLK(\text{MAX})} = 12\text{MHz}$	35.7		
	I _{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{CORE} = 1.1\text{V}$. See Temperature Variance	311		μA
		Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [01], $V_{CORE} = 1.0\text{V}$. See Temperature Variance	209		
		Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [00], $V_{CORE} = 0.9\text{V}$. See Temperature Variance	106		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Current, ACTIVE Mode	I _{DD_DACTD}	Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], f _{SYS_CLK(MAX)} = 100MHz		0.449	μA/MHz
		OVR = [01], f _{SYS_CLK(MAX)} = 50MHz		0.457		
		OVR = [00], f _{SYS_CLK(MAX)} = 12MHz		0.473		
		Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], f _{SYS_CLK(MAX)} = 100MHz		0.209	
			OVR = [01], f _{SYS_CLK(MAX)} = 50MHz		0.214	
			OVR = [00], f _{SYS_CLK(MAX)} = 12MHz		0.233	
		Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], f _{SYS_CLK(MAX)} = 100MHz		0.448	
			OVR = [01], f _{SYS_CLK(MAX)} = 50MHz		0.456	
			OVR = [00], f _{SYS_CLK(MAX)} = 12MHz		0.474	
		Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], f _{SYS_CLK(MAX)} = 100MHz		0.207	
			OVR = [01], f _{SYS_CLK(MAX)} = 50MHz		0.214	
			OVR = [00], f _{SYS_CLK(MAX)} = 12MHz		0.226	

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDD_FACTD		Fixed, IPO enabled, total current into V_{DD} pin, $V_{DD} = 3.3\text{V}$, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{CORE} = 1.1\text{V}$. See Temperature Variance	391		μA
			OVR = [01], $V_{CORE} = 1.0\text{V}$. See Temperature Variance	390		
			OVR = [00], $V_{CORE} = 0.9\text{V}$. See Temperature Variance	387		
		Fixed, IPO enabled, total current into V_{DD} pin, $V_{DD} = 1.8\text{V}$, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{CORE} = 1.1\text{V}$. See Temperature Variance	372		
			OVR = [01], $V_{CORE} = 1.0\text{V}$. See Temperature Variance	372		
			OVR = [00], $V_{CORE} = 0.9\text{V}$. See Temperature Variance	369		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CORE} Current, SLEEP Mode	$I_{\text{CORE_DSLPD}}$	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{\text{CORE}} = 1.1\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 100\text{MHz}$		29.8	$\mu\text{A/MHz}$
			OVR = [01], $V_{\text{CORE}} = 1.0\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 50\text{MHz}$		28.7	
			OVR = [00], $V_{\text{CORE}} = 0.9\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 12\text{MHz}$		26.3	
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR = [10], $V_{\text{CORE}} = 1.1\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 100\text{MHz}$		13.0	
			OVR = [01], $V_{\text{CORE}} = 1.0\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 50\text{MHz}$		11.7	
			OVR = [00], $V_{\text{CORE}} = 0.9\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 12\text{MHz}$		9.0	
	$I_{\text{CORE_FSLPD}}$	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD} , outputs source/sink 0mA	OVR [10], $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance		311	μA
			OVR [01], $V_{\text{CORE}} = 1.0\text{V}$. See Temperature Variance		209	
			OVR [00], $V_{\text{CORE}} = 0.9\text{V}$. See Temperature Variance		106	

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Current, SLEEP Mode	I _{DD_DSLPD}	Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V, f _{SYS_CLK(MAX)} = 100MHz	0.001		μA/MHz
			OVR = [01], V _{CORE} = 1.0V, f _{SYS_CLK(MAX)} = 50MHz	0.001		
			OVR = [00], V _{CORE} = 0.9V, f _{SYS_CLK(MAX)} = 12MHz	0.001		
		Dynamic, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V, f _{SYS_CLK(MAX)} = 100MHz	0.001		
			OVR = [01], V _{CORE} = 1.0V, f _{SYS_CLK(MAX)} = 50MHz	0.001		
			OVR = [00], V _{CORE} = 0.9V, f _{SYS_CLK(MAX)} = 12MHz	0.001		
	I _{DD_FSLPD}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V. See Temperature Variance	391		μA
			OVR = [01], V _{CORE} = 1.0V. See Temperature Variance	390		
			OVR = [00], V _{CORE} = 0.9V. See Temperature Variance	387		
		Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V. See Temperature Variance	372		
			OVR = [01], V _{CORE} = 1.0V. See Temperature Variance	372		
			OVR = [00], V _{CORE} = 0.9V. See Temperature Variance	369		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CORE} Fixed Current, DEEPSLEEP Mode	I _{CORE_FDSLP} D	V _{DD} = 3.3V, V _{CORE} = 1.1V. See Temperature Variance	10.5			µA
		V _{DD} = 3.3V, V _{CORE} = 0.855V. See Temperature Variance	4			
		V _{DD} = 1.8V, V _{CORE} = 1.1V. See Temperature Variance	10.5			
		V _{DD} = 1.8V, V _{CORE} = 0.855V. See Temperature Variance	4			
V _{DD} Fixed Current, DEEPSLEEP Mode	I _{DD_FDSLP}	V _{DD} = 3.3V, V _{CORE} = 1.1V. See Temperature Variance	0.36			µA
		V _{DD} = 3.3V, V _{CORE} = 0.855V. See Temperature Variance	0.36			
		V _{DD} = 1.8V, V _{CORE} = 1.1V. See Temperature Variance	0.149			
		V _{DD} = 1.8V, V _{CORE} = 0.855V. See Temperature Variance	0.149			

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CORE} Fixed Current, BACKUP Mode	$I_{\text{CORE_FBKUD}}$	0KB SRAM retained, RTC disabled, retention regulator disabled	$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	0.3		μA
			$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.19		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	0.297		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.187		
		20KB SRAM retained with RTC disabled	$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	1.37		
			$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.6		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	1.37		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.6		
		40KB SRAM retained with RTC disabled	$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	2.39		
			$V_{\text{DD}} = 3.3\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.99		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 1.1\text{V}$. See Temperature Variance	2.39		
			$V_{\text{DD}} = 1.8\text{V}$, $V_{\text{CORE}} = 0.855\text{V}$. See Temperature Variance	0.99		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	80KB SRAM retained with RTC disabled	$V_{DD} = 3.3\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		4.15		
		$V_{DD} = 3.3\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		1.6		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		4.15		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		1.6		
	160KB SRAM retained with RTC disabled	$V_{DD} = 3.3\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		7.4		
		$V_{DD} = 3.3\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		2.7		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		7.4		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		2.7		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Fixed Current, BACKUP Mode	I _{DD_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V. See Temperature Variance		0.36	µA
			V _{DD} = 3.3V, V _{CORE} = 0.855V. See Temperature Variance		0.36	
			V _{DD} = 1.8V, V _{CORE} = 1.1V. See Temperature Variance		0.15	
			V _{DD} = 1.8V, V _{CORE} = 0.855V. See Temperature Variance		0.15	
		20KB SRAM retained with RTC disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V. See Temperature Variance		0.36	
			V _{DD} = 3.3V, V _{CORE} = 0.855V. See Temperature Variance		0.36	
			V _{DD} = 1.8V, V _{CORE} = 1.1V. See Temperature Variance		0.15	
			V _{DD} = 1.8V, V _{CORE} = 0.855V. See Temperature Variance		0.15	
		40KB SRAM retained with RTC disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V. See Temperature Variance		0.36	
			V _{DD} = 3.3V, V _{CORE} = 0.855V. See Temperature Variance		0.36	
			V _{DD} = 1.8V, V _{CORE} = 1.1V. See Temperature Variance		0.15	
			V _{DD} = 1.8V, V _{CORE} = 0.855V. See Temperature Variance		0.15	

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	80KB SRAM retained with RTC disabled	$V_{DD} = 3.3\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.36		μA
		$V_{DD} = 3.3\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.36		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.15		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.15		
	160KB SRAM retained with RTC disabled	$V_{DD} = 3.3\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.36		
		$V_{DD} = 3.3\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.36		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.15		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.15		
V_{CORE} Fixed Current, STORAGE Mode	I_{CORE_FSTOD}	$V_{DD} = 3.3\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.25		μA
		$V_{DD} = 3.3\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.14		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 1.1\text{V}$. See Temperature Variance		0.25		
		$V_{DD} = 1.8\text{V}$, $V_{CORE} = 0.855\text{V}$. See Temperature Variance		0.14		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Fixed Current, STORAGE Mode	I _{DD_FSTOD}	V _{DD} = 3.3V; V _{CORE} = 1.1V. See Temperature Variance	0.32			μA
		V _{DD} = 3.3V; V _{CORE} = 0.855V. See Temperature Variance	0.31			
		V _{DD} = 1.8V; V _{CORE} = 1.1V. See Temperature Variance	0.11			
		V _{DD} = 1.8V; V _{CORE} = 0.855V. See Temperature Variance	0.11			
SLEEP Mode Resume Time	t _{SLP_OND}		2.1			μs
DEEPSLEEP Mode Resume Time	t _{DSE_OND}	fast_wk_en = 1	81			μs
		fast_wk_en = 0	129			
BACKUP Mode Resume Time	t _{BKU_OND}	Includes system initialization and ROM execution time	1.25			ms
STORAGE Mode Resume Time	t _{STO_OND}	Includes system initialization and ROM execution time	1.5			ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO, RSTN	V _{IL_GPIO}	Pin configured as GPIO		0.3 × V _{DD}		V
Input High Voltage for All GPIO, RSTN	V _{IH_GPIO}	Pin configured as GPIO	0.7 × V _{DD}			V
Output Low Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V _{OL_GPIO}	V _{DD} = 1.71V, I _{OL} = 1mA, DS[1:0] = 00 (Note 1)	0.2	0.4		V
		V _{DD} = 1.71V, I _{OL} = 2mA, DS[1:0] = 10 (Note 1)	0.2	0.4		
		V _{DD} = 1.71V, I _{OL} = 4mA, DS[1:0] = 01 (Note 1)	0.2	0.4		
		V _{DD} = 1.71V, I _{OL} = 6mA, DS[1:0] = 11 (Note 1)	0.2	0.4		
Output Low Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V _{OL_I2C}	V _{DD} = 1.71V, I _{OL} = 2mA, DS = 0 (Note 1)	0.2	0.4		V
		V _{DD} = 1.71V, I _{OL} = 10mA, DS = 1 (Note 1)	0.2	0.4		
Output High Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V _{OH_GPIO}	V _{DD} = 1.71V, I _{OH} = 1mA, DS[1:0] = 00 (Note 1)	V _{DD} - 0.4			V
		V _{DD} = 1.71V, I _{OH} = 2mA, DS[1:0] = 10 (Note 1)	V _{DD} - 0.4			
		V _{DD} = 1.71V, I _{OH} = 4mA, DS[1:0] = 01 (Note 1)	V _{DD} - 0.4			
		V _{DD} = 1.71V, I _{OH} = 6mA, DS[1:0] = 11 (Note 1)	V _{DD} - 0.4			
Output High Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V _{OH_I2C}	V _{DD} = 1.71V, I _{OH} = 2mA, DS = 0 (Note 1)	V _{DD} - 0.4			V
		V _{DD} = 1.71V, I _{OH} = 10mA, DS = 1 (Note 1)	V _{DD} - 0.4			

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined I_{OL} , All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH} , All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	$V_{IN} = 0\text{V}$, internal pull-up disabled	-500		+500	nA
Input Leakage Current High	I_{IH}	$V_{IN} = 3.6\text{V}$, internal pull-down disabled	-500		+500	nA
Input Pull-Up Resistor to RSTN	R_{PU_VDD}	Pull up to $V_{DD} = V_{RST}$, RSTN at V_{IH}		18.7		$\text{k}\Omega$
		Pull up to $V_{DD} = 3.63\text{V}$, RSTN at V_{IH}		10.0		
Input Pull-Up Resistor for All GPIO	R_{PU}	Device pin configured as GPIO, pull up to $V_{DD} = V_{RST}$, device pin at V_{IH}		18.7		$\text{k}\Omega$
		Device pin configured as GPIO, pull up to $V_{DD} = 3.63\text{V}$, device pin at V_{IH}		10.0		
Input Pull-Down Resistor for All GPIO	R_{PD}	Device pin configured as GPIO, pull down to V_{SS} , $V_{DD} = V_{RST}$, device pin at V_{IL}		17.6		$\text{k}\Omega$
		Device pin configured as GPIO, pull down to V_{SS} , $V_{DD} = 3.63\text{V}$, device pin at V_{IL}		8.8		
CLOCKS						
System Clock Frequency	f_{SYS_CLK}				100	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS_CLK}$		μs
Internal Primary Oscillator (IPO)	f_{IPO}	Default OVR = [10]		100		MHz
External RF Oscillator (XRFO)	f_{XRFO}	Required crystal characteristics: $C_L = 12\text{pF}$, $\text{ESR} \leq 50\Omega$, $C_0 \leq 7\text{pF}$, temperature stability $\pm 20\text{ppm}$, initial tolerance $\pm 20\text{ppm}$	16	32		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nano-Ring Oscillator (INRO)	f_{INRO}	Measured at $V_{DD} = 1.8\text{V}$		70		kHz
External RTC Oscillator (XRTCO)	f_{XRTCO}	32.768kHz watch crystal, $C_L = 6\text{pF}$, $\text{ESR} < 90\text{k}\Omega$, $C_0 < 2\text{pF}$		32.768		kHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled		0.35		μA
RTC Power-Up Time	t_{RTC_ON}			250		ms
External Clock Input Frequency	f_{EXT_CLK}	EXT_CLK1 selected		50		MHz
		EXT_CLK2 selected		1		

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase	30			ms
	t_{P_ERASE}	Page erase	30			
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, $f_{FLC_CLK} = 1\text{MHz}$		42		μs
Flash Endurance			10			
Data Retention	t_{RET}	$T_A = +125^\circ\text{C}$	10			years

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	$f_{SYS_CLK} = 100\text{MHz}$, $f_{MCK(MAX)} = f_{SYS_CLK}/2$		50		MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}			$t_{MCK}/2$		ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}			$t_{MCK}/2$		ns
MOSI Output Valid to Sample Edge	t_{MOV}			$t_{MCK}/2$		ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}			50		MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SS _x Inactive	t_{SSD}			10		ns
SS _x Inactive Time	t_{SSH}			$1/f_{SCK}$		μs
MISO Hold Time After SS _x Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I²C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD-MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0	100		kHz
Low Period SCL Clock	t_{LOW}		4.7			μs
High Time SCL Clock	t_{HIGH}		4.0			μs
Setup Time for Repeated Start Condition	$t_{SU;STA}$			4.7		μs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			μs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			μs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			μs
Data Valid Time	$t_{VD;DAT}$		3.45			μs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			μs
FAST-MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0	400		kHz
Low Period SCL Clock	t_{LOW}		1.3			μs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Time SCL Clock	t_{HIGH}		0.6			μs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			μs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			μs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			μs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			μs
Data Valid Time	$t_{VD;DAT}$		0.9			μs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			μs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$	80			ns
Pulse Width Suppressed by Input Filter	t_{SP}		75			ns
SCL Clock Frequency	f_{SCL}		0	1000		kHz
Low Period SCL Clock	t_{LOW}		0.5			μs
High Time SCL Clock	t_{HIGH}		0.26			μs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			μs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			μs
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		10			ns
Rise Time for SDA and SCL	t_R		50			ns
Fall Time for SDA and SCL	t_F		30			ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			μs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			μs
Data Valid Time	$t_{VD;DAT}$		0.45			μs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			μs

Electrical Characteristics—I²S Slave

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

GPIO Drive Strength: Note 1: When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.71V.

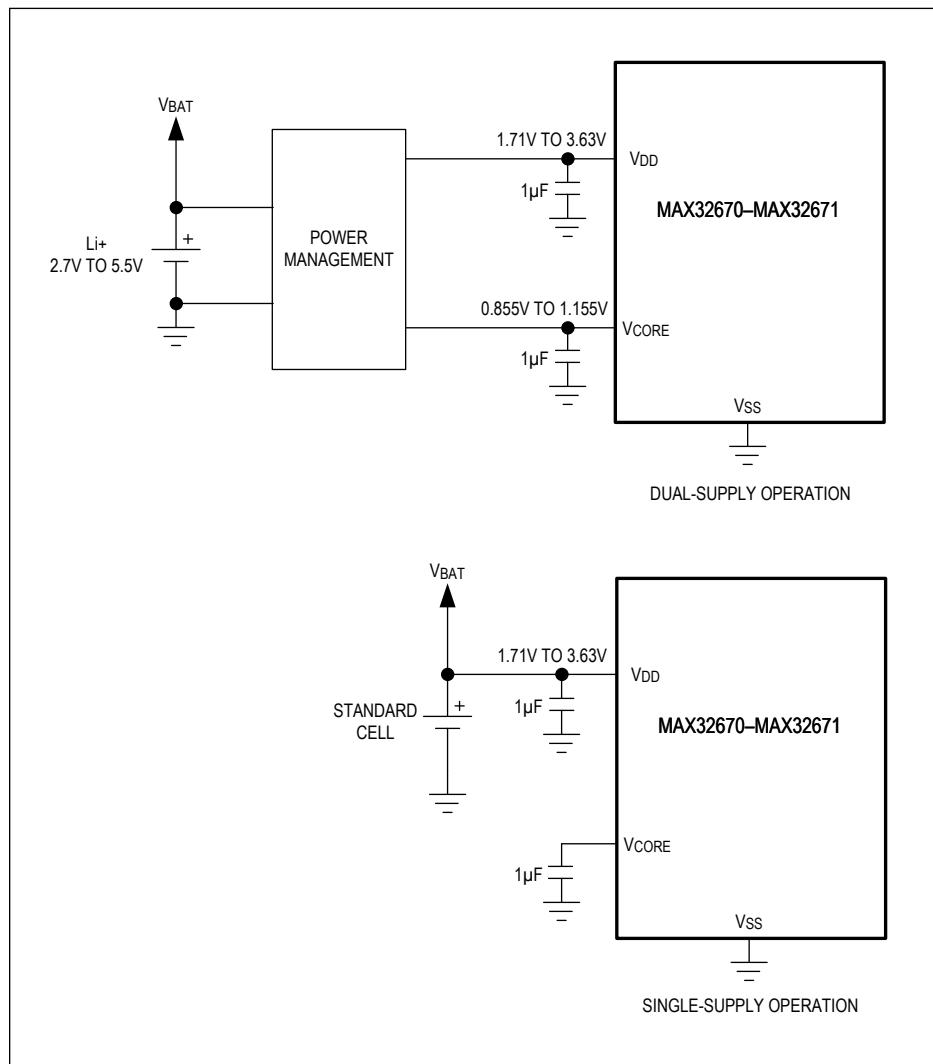


Figure 1. Power-Supply Operational Modes

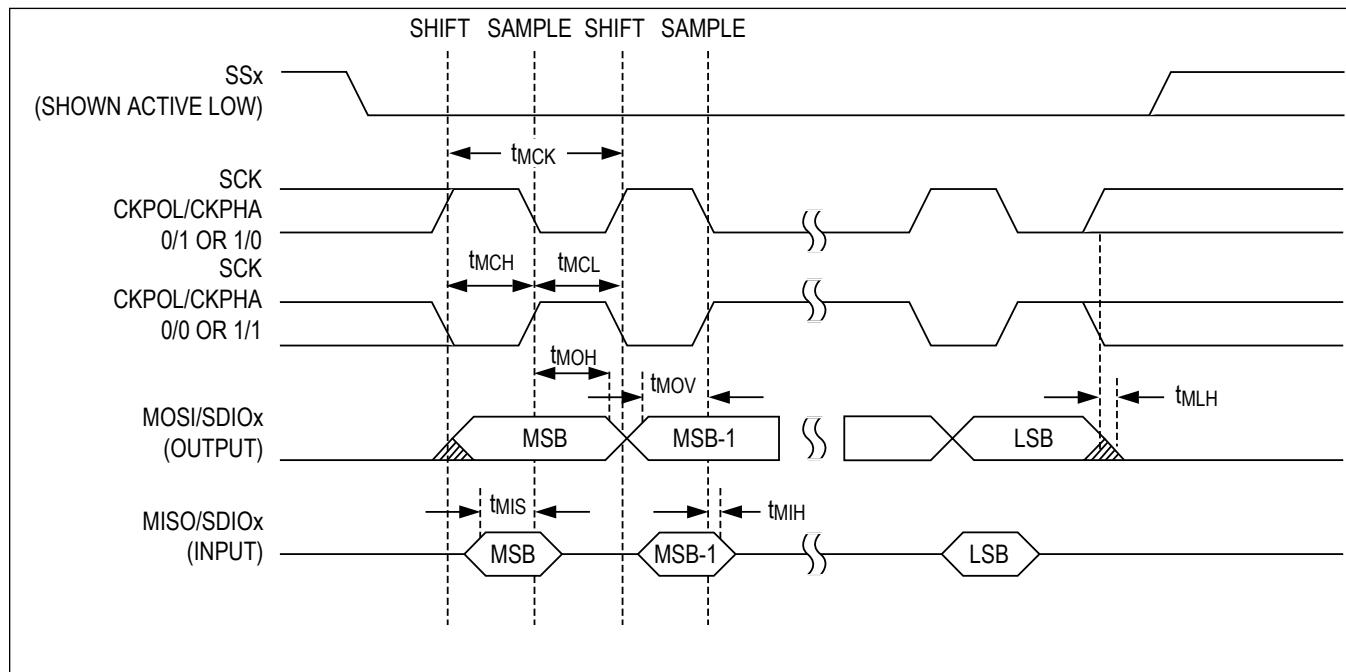


Figure 2. SPI Master Mode Timing Diagram

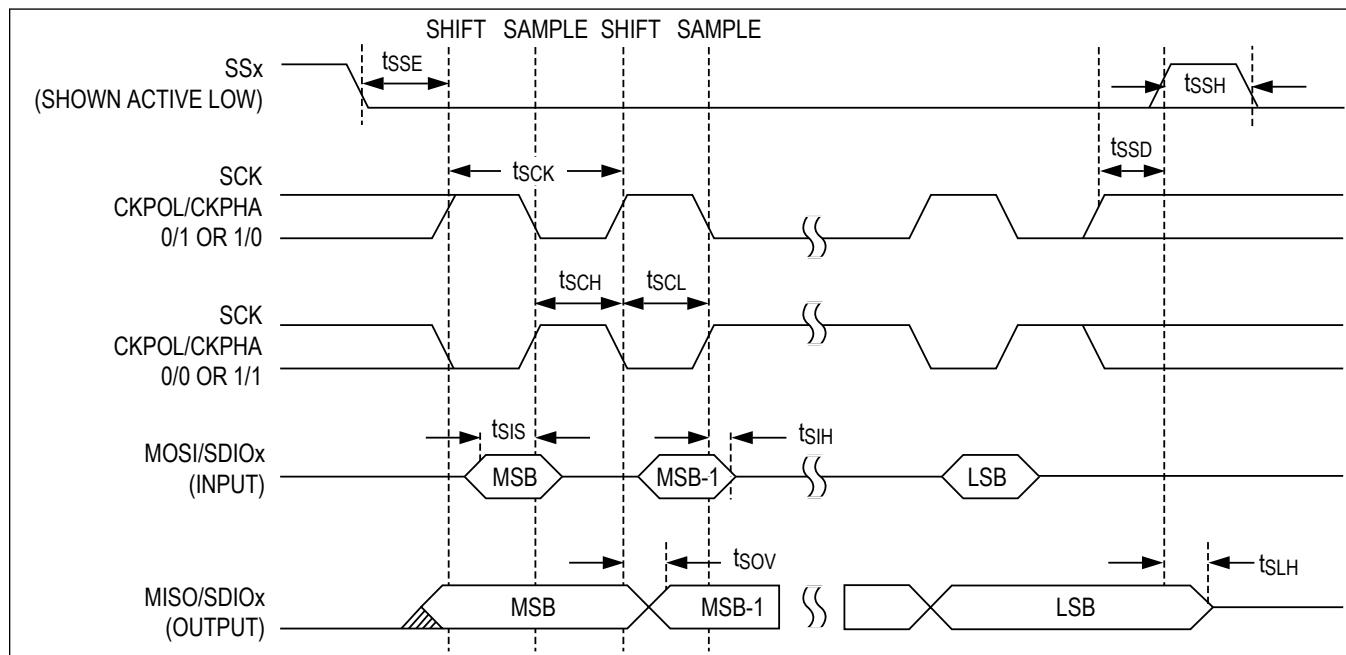
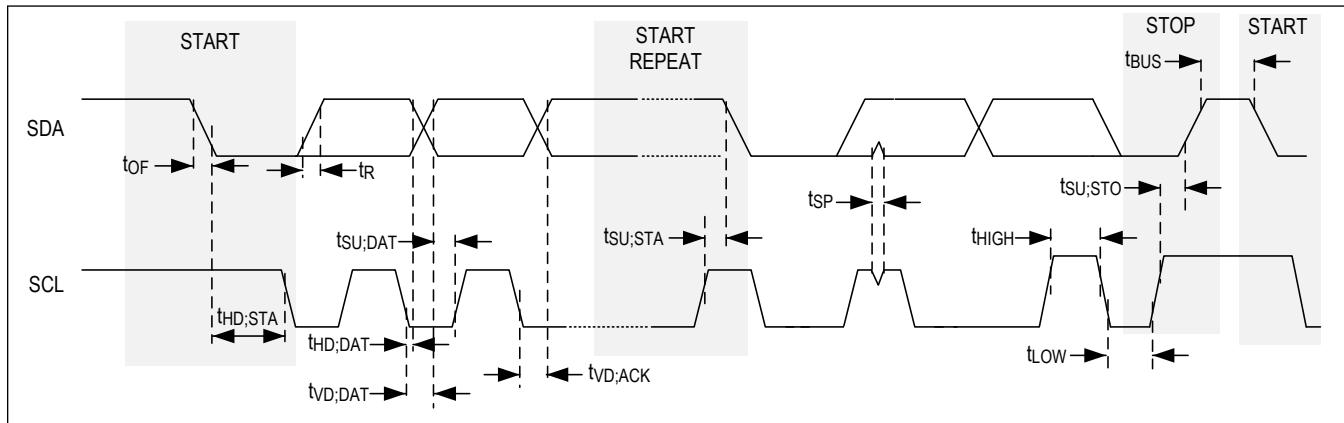
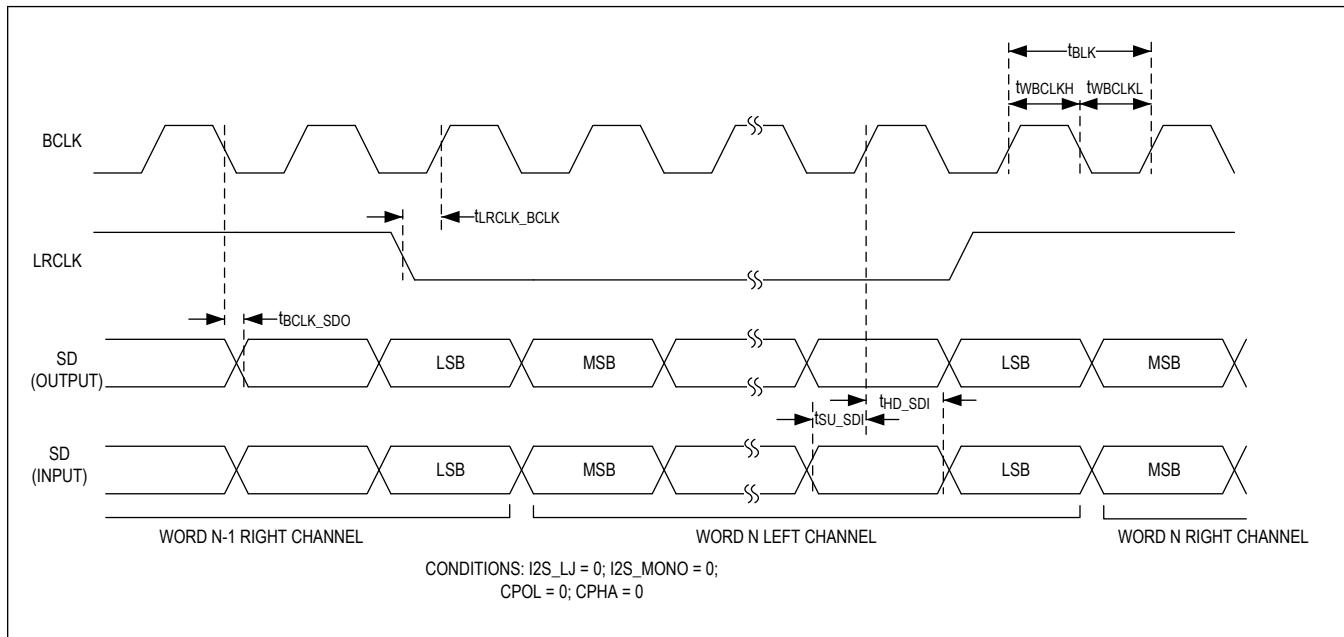
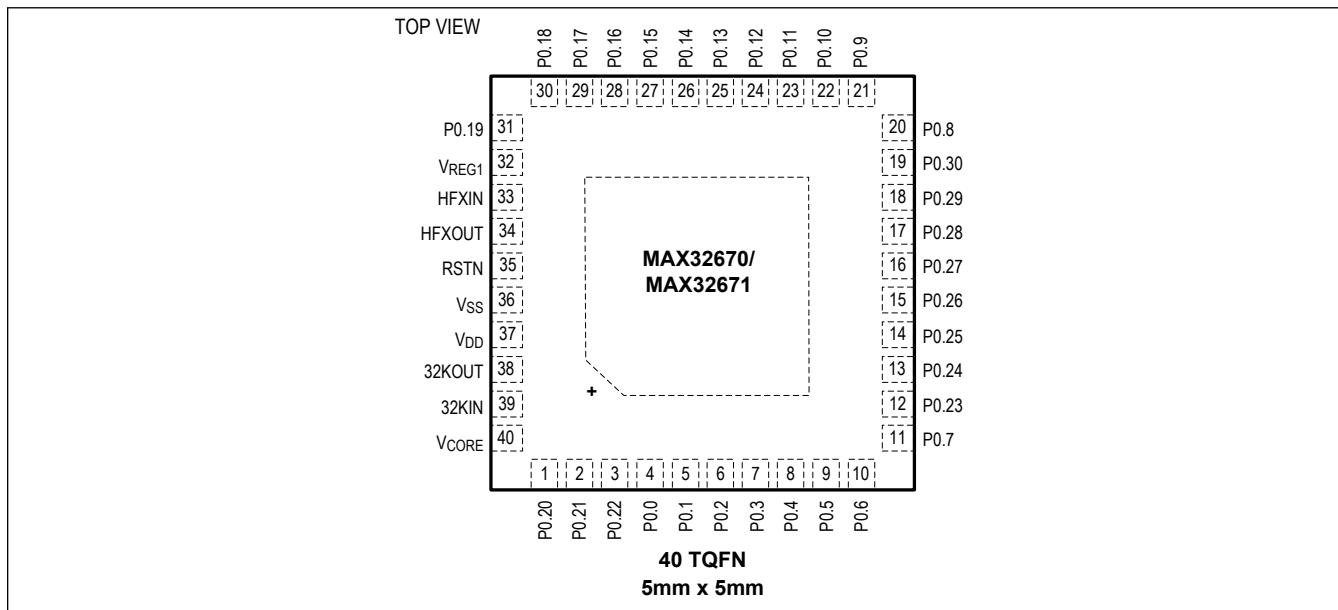


Figure 3. SPI Slave Mode Timing Diagram

Figure 4. I²C Timing DiagramFigure 5. I²S Timing Diagram

Pin Configuration

40 TQFN



Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER (See the Applications Information section for bypass capacitor recommendations.)							
40	V _{CORE}	—	—	—	—	—	Digital Power-Supply Input. Bypass with 100nF to V _{SS} and 1μF with 10mΩ to 150mΩ ESR to V _{SS} .
32	V _{REG1}	—	—	—	—	—	Bypass with 4.7nF to V _{SS} . Do not connect this device pin to any other external circuitry.
37	V _{DD}	—	—	—	—	—	Power-Supply Input. Bypass with 100nF to V _{SS} and 1μF with 10mΩ to 150mΩ ESR to V _{SS} .
36	V _{SS}	—	—	—	—	—	Digital Ground
RESET AND CONTROL							
35	RSTN	—	—	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pull-up to the V _{DD} supply.

40 TQFN

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
CLOCK							
38	32KOUT	—	—	—	—	—	32kHz Crystal Oscillator Output. Refer to the MAX32670/MAX32671 User Guide for determination of the required external stability capacitors.
39	32KIN	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the MAX32670/MAX32671 User Guide for determination of the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
33	HFXIN	—	—	—	—	—	RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square-wave source. See the Electrical Characteristics table for details of the crystal requirements.
34	HFXOUT	—	—	—	—	—	RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See the Electrical Characteristics table for details of the crystal requirements.
GPIO AND ALTERNATE FUNCTION (See the Applications Information section for GPIO and Alternate Function Matrices.)							
4	P0.0	P0.0	SWDIO	—	TMR0C_IA	—	Single-Wire Debug I/O; Timer0 Port Map C Input.
5	P0.1	P0.1	SWDCLK	—	TMR0C_O	—	Single-Wire Debug Clock; Timer0 Port Map C Output. This device pin also controls the behavior of the device when exiting a reset event. See Applications Information for details.
6	P0.2	P0.2	SPI0_MISO	UART1B_RX	TMR1C_IA	—	SPI0 Master In Slave Out; UART1 Port Map B Rx; Timer1 Port Map C Input
7	P0.3	P0.3	SPI0_MOSI	UART1B_TX	TMR1C_OA	—	SPI0 Master Out Slave In; UART1 Port Map B Tx; Timer1 Port Map C Output
8	P0.4	P0.4	SPI0_SCK	UART1B_CTS	TMR2C_IA	—	SPI0 Serial Clock; UART1 Port Map B CTS; Timer2 Port Map C Input
9	P0.5	P0.5	SPI0_SS0	UART1B_RTS	TMR2C_OA	DIV_CLK_OUTA	SPI0 Slave Select 0; UART1 Port Map B RTS; Timer2 Port Map C Output; Divided Clock Output Port Map A

40 TQFN

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
10	P0.6	P0.6	I2C0_SCL	LPTMR0B_IA	TMR3C_IA	—	I2C0 Serial Clock; Low-Power Timer0 Port Map B Input; Timer3 Port Map C Input
11	P0.7	P0.7	I2C0_SDA	LPTMR0B_OA	TMR3C_OA	—	I2C0 Serial Data; Low-Power Timer0 Port Map B Output; Timer3 Port Map C Output
20	P0.8	P0.8	UART0A_RX	I2S0_SDO	TMR0C_IA	—	UART0 Port Map A Rx; I2S0 Serial Data Output; Timer0 Port Map C Input. This device pin also controls the behavior of the device when exiting a reset event. See Applications Information for details.
21	P0.9	P0.9	UART0A_TX	I2S0_LRCLK	TMR0C_OA	—	UART0 Port Map A Tx; I2S0 Left/Right Clock; Timer0 Port Map C Output
22	P0.10	P0.10	UART0A_CTS	I2S0_BCLK	TMR1C_IA	DIV_CLK_OUTB	UART0 Port Map A CTS; I2S0 Bit Clock; Timer1 Port Map C Input; Divided Clock Output Port Map B
23	P0.11	P0.11	UART0A_RTS	I2S0_SDI	TMR1C_OA	—	UART0 Port Map A RTS; I2S0 Serial Data Input; Timer1 Port Map C Output
24	P0.12	P0.12	I2C1_SCL	EXT_CLK2	TMR2C_IA	EXT_CLK1	I2C1 Serial Clock; Low-Power External Clock Input; Timer2 Port Map C Input; External Clock Input
25	P0.13	P0.13	I2C1_SDA	32KCAL	TMR2C_OA	SPI1_SS0	I2C1 Serial Data; 32.768kHz Calibration Output; Timer2 Port Map C Output; SPI1 Slave Select 0
26	P0.14	P0.14	SPI1_MISO	UART2B_RX	TMR3C_IA	—	SPI1 Master In Slave Out; UART2 Port Map B Rx; Timer3 Port Map C Input
27	P0.15	P0.15	SPI1_MOSI	UART2B_TX	TMR3C_OA	—	SPI1 Master Out Slave In; UART2 Port Map B Tx; Timer3 Port Map C Output
28	P0.16	P0.16	SPI1_SCK	UART2B_CTS	TMR0C_IA	—	SPI1 Serial Clock; UART2 Port Map B CTS; Timer0 Port Map C Input
29	P0.17	P0.17	SPI1_SS0	UART2B_RTS	TMR0C_OA	—	SPI1 Slave Select 0; UART2 Port Map B RTS; Timer0 Port Map C Output
30	P0.18	P0.18	I2C2_SCL	—	TMR1C_IA	—	I2C2 Serial Clock; Timer1 Port Map C Input
31	P0.19	P0.19	I2C2_SDA	—	TMR1C_OA	—	I2C2 Serial Data; Timer1 Port Map C Output
1	P0.20	P0.20	CM4_RX	—	TMR2C_IA	SWDCLKB	CM4 Rx Event Input; Timer2 Port Map C Input; Single-Wire Debug Clock Port Map B
2	P0.21	P0.21	CM4_TX	—	TMR2C_OA	—	CM4 Tx Event Output; Timer2 Port Map C Output

40 TQFN

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
3	P0.22	P0.22	LPTMR1A_IA	—	TMR3C_IA	SWDIOB	Low-Power Timer1 Port Map A Input; Timer3 Port Map C Input; Single-Wire Debug Port Map B I/O
12	P0.23	P0.23	LPTMR1A_OA	—	TMR3C_OA	—	Low-Power Timer1 Port Map A Output; Timer3 Port Map C Output
13	P0.24	P0.24	LPUART0_CTS	UART0B_RX	TMR0C_IA	—	Low-Power UART0 CTS; UART0 Port Map B Rx; Timer0 Port Map C Input
14	P0.25	P0.25	LPUART0_RTS	UART0B_TX	TMR0C_OA	—	Low-Power UART0 RTS; UART0 Port Map B Tx; Timer0 Port Map C Output
15	P0.26	P0.26	LPUART0_RX	UART0B_TS	TMR1C_IA	—	Low-Power UART0 Rx; UART0 Port Map B CTS; Timer1 Port Map C Input
16	P0.27	P0.27	LPUART0_TX	UART0B_RTS	TMR1C_OA	—	Low-Power UART0 Tx; UART0 Port Map B RTS; Timer1 Port Map C Output
17	P0.28	P0.28	UART1A_RX	—	TMR2C_IA	—	UART1 Port Map A Rx; Timer2 Port Map C Input
18	P0.29	P0.29	UART1A_TX	—	TMR2C_OA	—	UART1 Port Map A Tx; Timer2 Port Map C Output
19	P0.30	P0.30	UART1A_TS	—	TMR3C_IA	—	UART1 Port Map A CTS; Timer3 Port Map C Input

Detailed Description

The MAX32670/MAX32671 are ultra-low-power, cost-effective, high-reliability 32-bit microcontrollers enabling designs with complex sensor processing without compromising battery life. They combine a flexible and versatile power management unit with the powerful Arm Cortex-M4 processor with FPU. They also offer legacy designs an easy and cost optimal upgrade path from 8- or 16-bit microcontrollers. ECC (capable of SEC-DED) for both flash and SRAM provides extremely reliable code execution. The devices integrate up to 384KB of flash memory and 160KB (128KB with ECC) of SRAM to accommodate application and sensor code.

The devices feature five powerful and flexible power modes. They can operate from a single-supply battery or a dual-supply typically provided by a PMIC. The I²C ports support standard-mode, fast-mode, fast-mode plus, and high-speed mode, operating up to 3400kbps. The SPI ports can run up to 50MHz in both master and slave mode, and three UARTs can run up to 4000kBd. One low-power UART can run up to 1000kBd. Four general-purpose 32-bit timers, two low-power 32-bit timers, two windowed watchdog timers, and a real-time clock (RTC) are also provided. An I²S interface provides digital audio streaming to a codec.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 processor with FPU combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 processor with FPU supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed or unsigned data, with or without saturation

Memory

Internal Flash Memory

384KB of internal flash memory with error correction provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 160KB SRAM provides low-power retention of application information in all power modes except STORAGE. For enhanced system reliability, the SRAM can be configured as 128KB with ECC SEC-DED. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data-retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Clocking Scheme

Multiple clock sources can be selected as the system clock:

- Internal primary oscillator (IPO) at a nominal frequency of 100MHz
- Internal nanoring oscillator at 80kHz
- External RTC oscillator at 32.768kHz (ERTCO) (external crystal required)
- Internal baud rate oscillator at 7.3728MHz (IBRO)
- External RF oscillator at 16MHz to 32MHz (ERFO) (external crystal required)
- External square-wave clock up to 50MHz
- External square-wave clock up to 1MHz for LPTMR0, LPTMR1, and LPUART

An external 32.768kHz time base is required when using the RTC.

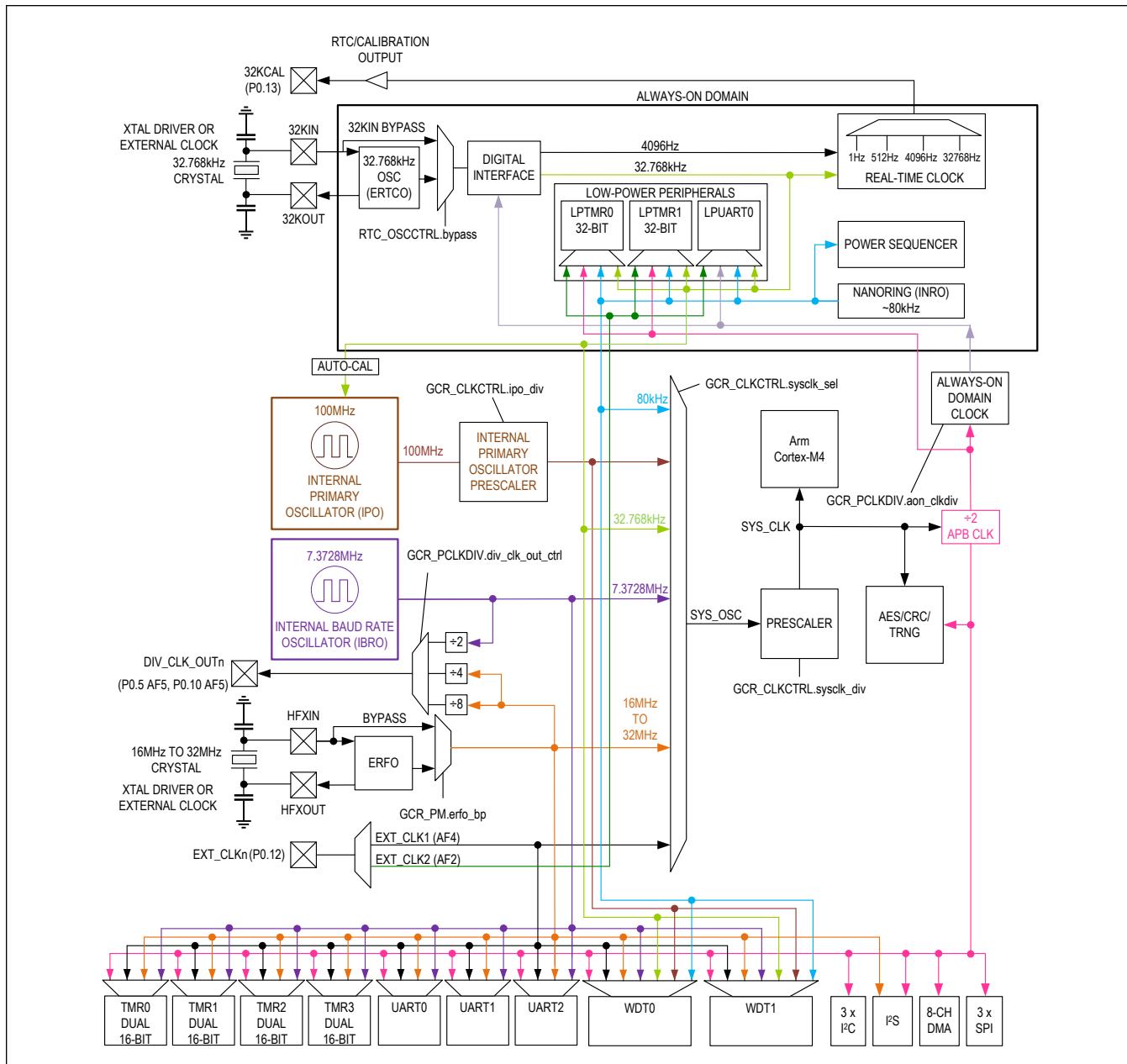


Figure 6. Clocking Scheme

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the [Electrical Characteristics](#) tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled and configured as a level-

or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32670/MAX32671 provide up to 31 GPIOs for the 40-pin TQFN.

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 8 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit

The power management unit (PMU) provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wakeup of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU Active mode.

SLEEP Mode

This mode allows for lower power consumption operation than ACTIVE mode. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause transition to the ACTIVE mode. This mode corresponds to the Arm Cortex-M4 processor with FPU Sleep mode.

DEEPSLEEP Mode

In this mode, CPU and critical peripheral configuration settings and all volatile memory are preserved.

The device status is as follows:

- The CPU is powered down. The system state and all SRAM is retained.
- The GPIO pins retain their state.
- The transition from DEEPSLEEP to ACTIVE mode is faster than the transition from BACKUP mode because system

initialization is not required.

- The system oscillators are all disabled to provide additional power savings over SLEEP mode.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

This mode corresponds to the Arm Cortex-M4 with FPU DeepSleep mode.

BACKUP Mode

This mode places the CPU in a static, low-power state. BACKUP mode supports the same wake-up sources as DEEPSLEEP mode.

The device status is as follows:

- The CPU is powered down.
- SRAM retention as per [Table 1](#). Each of the RAM blocks can be retained.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

Table 1. BACKUP Mode RAM Retention

RAM BLOCK	RAM SIZE WITHOUT ECC (KB)	RAM SIZE WITH ECC (KB)
SYSRAM0	20	16
SYSRAM1	20	16
SYSRAM2	40	32
SYSRAM3	80	64

STORAGE Mode

The device status is as follows:

- The CPU is powered off.
- All peripherals are powered off.
- Wake-up from GPIO interrupt.
- RTC can be enabled.
- No SRAM retention.

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed between 244µs and 12 days. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the [Electrical Characteristics](#) table.

An RTC calibration feature provides the ability for user-software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ± 127 ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Windowed Watchdog Timer (WWDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed watchdog timer (WWDT), which detects runaway code or system unresponsiveness.

The WWDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WWDT must be periodically reset by the application software. Failure to reset the WWDT within the user-configurable timeout period

indicates that the application software is not operating correctly and results in a WWDT timeout. A WWDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WWDT to be reset within a specific window of time.

The WWDT supports multiple clock options:

- 100MHz IPO
- 16MHz to 32MHz ERFO (external crystal required)
- 7.3728MHz IBRO
- 80kHz INRO
- 32.768kHz ERTCO (external crystal required)
- External square-wave clock up to 50MHz
- PCLK

The MAX32670/MAX32671 provide two instances of the windowed watchdog timer (WWDT0 and WWDT1).

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating or capture
- Timer output pin
- TMR0–TMR3 can be configured as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32670/MAX32671 provide six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, and LPTMR1). LPTMR0 and LPTMR1 are capable of operation in the low-power SLEEP, DEEPSLEEP, and BACKUP modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See [Table 2](#) for individual timer features.

Table 2. Timer Configuration Options

INSTANCE	SINGLE 32 BIT	DUAL 16 BIT	POWER MODE	CLOCK SOURCE							
				AOD_PCLK	PCLK	IBRO	ERFO	INRO	ERTCO	EXT_CLK1	EXT_CLK2
TMR0	YES	YES	ACTIVE SLEEP	NO	YES	YES	YES	NO	NO	YES	NO
TMR1	YES	YES	ACTIVE SLEEP	NO	YES	YES	YES	NO	NO	YES	NO
TMR2	YES	YES	ACTIVE SLEEP	NO	YES	YES	YES	NO	NO	YES	NO
TMR3	YES	YES	ACTIVE SLEEP	NO	YES	YES	YES	NO	NO	YES	NO
LPTMR0	YES	NO	ACTIVE SLEEP	YES	NO	NO	NO	YES	YES	NO	YES
			DEEPSLEEP BACKUP	NO							
LPTMR1	YES	NO	ACTIVE SLEEP	YES	NO	NO	NO	YES	YES	NO	YES

Table 2. Timer Configuration Options (continued)

			DEEPSLEEP BACKUP	NO							
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Serial Peripherals**I²C Interface (I²C)**

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support Standard-mode, Fast-mode, Fast-mode Plus and high-speed mode I²C speeds. It provides the following features:

- Master or slave mode operation
 - Supports up to four different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
 - Standard-mode: 100kbps
 - Fast-mode: 400kbps
 - Fast-mode Plus: 1000kbps
 - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32670/MAX32671 provide three instances of the I²C peripheral (I²C0, I²C1, and I²C2).

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, and 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32670/MAX32671 provide three instances of the SPI peripheral (SPI0, SPI1, and SPI2). See [Table 3](#) for configuration options.

Table 3. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES	MAXIMUM FREQUENCY MASTER MODE (MHz)	MAXIMUM FREQUENCY SLAVE MODE (MHz)
		40 TQFN		

Table 3. SPI Configuration Options (continued)

SPI0	3 wire, 4 wire	1	50	50
SPI1	3 wire, 4 wire	1	50	50
SPI2	3 wire, 4 wire	1	50	50

I²S Interface (I²S)

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Master and slave mode operation
- Support for 4 channels
- 8-, 16-, 24-, and 32-bit frames
- Receive and transmit DMA support
- Wakeup on FIFO status (full/empty/threshold)
- Pulse density modulation support for receive channel
- Word select polarity control
- First bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32670/MAX32671 provide one instance of the I²S peripheral (I²S0).

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32670/MAX32671 provide four instances of the UART peripheral (UART0, UART1, UART2, and LPUART0). LPUART0 is capable of operation in the low-power SLEEP, DEEPSLEEP, and BACKUP modes. See [Table 4](#) for configuration options.

Table 4. UART Configuration Options

INSTANCE	POWER MODE	CLOCK SOURCE							
		AOD_PCLK	PCLK	IBRO	ERFO	INRO	ERTCO	EXT_CLK1	EXT_CLK2
UART0	ACTIVE	NO	YES	YES	YES	NO	NO	YES	NO

Table 4. UART Configuration Options (continued)

UART1	ACTIVE	NO	YES	YES	YES	NO	NO	YES	NO
UART2	ACTIVE	NO	YES	YES	YES	NO	NO	YES	NO
LPUART0	ACTIVE/SLEEP	YES	NO	NO	NO	YES	YES	NO	YES
	DEEPSLEEP/BACKUP	NO							

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers that can be used for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This is helpful in thwarting replay attacks or key search approaches. An effective true random number generator (TRNG) must be continuously updated by a high-entropy source.

The provided TRNG is continuously driven by a physically-unpredictable entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Analog Devices for details of compliance with specific standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Bootloader

The bootloader allows loading and verification of program memory through a serial interface. Features include:

- Bootloader interface through UART
- Program loading of Motorola® SREC format files
- Permanent lock state prevents altering or erasing program memory
- Access to the USN for device or customer application identification
- Disable SWD interface to block debug access port functionality

Secure Boot

The optional secure boot feature ensures software integrity by automatically comparing program memory against a stored HMAC SHA-256 hash value after every reset. Programs that fail the integrity check indicate corrupted or modified program memory and are prevented from executing any instructions.

Devices with the secure boot feature also provide an optional challenge/response that authenticates before executing bootloader commands.

Debug and Development Interface (SWD)

The serial wire debug interface is used for code loading and in-circuit emulation (ICE) debug activities. All devices in mass production have the debugging/development interface enabled.

Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The [Pin Descriptions](#) table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the [Pin Descriptions](#) table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins which recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

Bootloader Activation

The bootloader starts if the [Table 5](#) pins are in their active state before exiting any reset and remain active until the bootloader sends the first command prompt. If the pins are not in their active state, the device will perform a secure boot and, if successful, will begin execution of the application code. The design must ensure that the activation pins and the RSTN pin are available to the host so it can activate the bootloader.

Table 5. Bootloader Activation Summary

ACTIVATION PINS	
UART0_RX (Active Low)	SWDCLK (Active Low)

Typical Fixed Current Consumption Temperature Variance

Single-Supply ACTIVE Mode

Table 6. Single-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Current ACTIVE Mode	I _{DD_FACTS}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	634	735	863	1127	1477	µA
			OVR = [01], internal regulator set to 1.0V	544	659	760	956	1241	µA
			OVR = [00], internal regulator set to 0.9V	474	563	654	819	1063	µA
	I _{DD_VDD1.8V}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	618	754	847	1099	1435	µA
			OVR = [01], internal regulator set to 1.0V	525	633	734	961	1242	µA

Table 6. Single-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode (continued)

			OVR = [00], internal regulator set to 0.9V	455	538	626	815	1052	µA
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Single-Supply SLEEP Mode**Table 7. Single-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Current SLEEP Mode	I _{DD_FSLPS}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	634	735	863	1127	1477	µA
			OVR = [01], internal regulator set to 1.0V	544	659	760	956	1241	µA
			OVR = [00], internal regulator set to 0.9V	474	563	654	819	1063	µA
		Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	618	754	847	1099	1435	µA
			OVR = [01], internal regulator set to 1.0V	525	633	734	961	1242	µA
			OVR = [00], internal regulator set to 0.9V	455	538	626	815	1052	µA

Single-Supply DEEPSLEEP Mode**Table 8. Single-Supply Operation Fixed V_{DD} Current Consumption DEEPSLEEP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Fixed Current DEEPSLEEP Mode	I _{DD_FDSLPS}	Standby state with full data retention and 160KB SRAM retained	V _{DD} = 3.3V	1.44	4	9.7	24.7	49	µA
			V _{DD} = 1.8V	1.3	3.7	9.3	24.2	48.3	µA

Single-Supply BACKUP Mode**Table 9. Single-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	

Table 9. Single-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode (continued)

V _{DD} Fixed Current BACKUP Mode	I _{DD_FBKUS}	V _{DD} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.28	0.38	0.57	1	1.75	µA
			20KB SRAM retained	0.64	1.08	1.96	4.3	8.2	µA
			40KB SRAM retained	0.72	1.4	2.84	6.6	12.8	µA
			80KB SRAM retained	0.89	1.9	4.1	9.9	19.5	µA
			160KB SRAM retained	1.2	2.8	6.1	15.2	30.3	µA
		V _{DD} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.13	0.15	0.22	0.48	1	µA
			20KB SRAM retained	0.49	0.86	1.64	3.8	7.5	µA
			40KB SRAM retained	0.58	1.2	2.5	6.1	12.1	µA
			80KB SRAM retained	0.75	1.7	3.7	9.4	18.7	µA
			160KB SRAM retained	1.06	2.58	5.8	14.7	29.7	µA

Single-Supply STORAGE Mode**Table 10. Single-Supply Operation Fixed V_{DD} Current Consumption STORAGE Mode**

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V _{DD} Fixed Current STORAGE Mode	I _{DD_FSTOS}	V _{DD} = 3.3V	0.23	0.33	0.51	0.96	1.68	µA
		V _{DD} = 1.8V	0.094	0.11	0.19	0.45	0.94	µA

Dual-Supply ACTIVE Mode**Table 11. Dual-Supply Operation Fixed V_{CORE} Current Consumption ACTIVE Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{CORE} Current ACTIVE Mode	I _{CORE_FACTD}	Fixed, IPO enabled, total current into V _{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V	222	311	410	663	996	µA
			OVR = [01], V _{CORE} = 1.0V	131	209	310	483	760	µA
			OVR = [00], V _{CORE} = 0.9V	54	106	171	317	52	µA

Dual-Supply ACTIVE Mode**Table 12. Dual-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Current ACTIVE Mode	I _{DD_FACTD}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	360	391	406	424	441	µA

Table 12. Dual-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode (continued)

		Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [01], internal regulator set to 1.0V	360	390	406	424	441	μA
			OVR = [00], internal regulator set to 0.9V	356	387	402	420	437	μA
			OVR = [10], internal regulator set to 1.1V	341	372	388	406	422	μA
			OVR = [01], internal regulator set to 1.0V	341	372	387	405	421	μA
			OVR = [00], internal regulator set to 0.9V	338	369	384	401	417	μA

Dual-Supply SLEEP Mode**Table 13. Dual-Supply Operation Fixed V_{CORE} Current Consumption SLEEP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{CORE} Current SLEEP Mode	I _{CORE_FSLPD}	Fixed, IPO enabled, total current into V _{CORE} pin, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V	222	311	410	663	996	μA
			OVR = [01], V _{CORE} = 1.0V	131	209	310	483	760	μA
			OVR = [00], V _{CORE} = 0.9V	54	106	171	317	523	μA

Dual-Supply SLEEP Mode**Table 14. Dual-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Current SLEEP Mode	I _{DD_FSLPD}	Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V	360	391	406	424	441	μA
			OVR = [01], V _{CORE} = 1.0V	360	390	406	424	441	μA
			OVR = [00], V _{CORE} = 0.9V	356	387	402	420	437	μA

Table 14. Dual-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode (continued)

		Fixed, IPO enabled, total current into V _{DD} pin, V _{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DD} , outputs source/sink 0mA	OVR = [10], V _{CORE} = 1.1V	341	372	388	406	422	µA
			OVR = [01], V _{CORE} = 1.0V	341	372	387	405	421	µA
			OVR = [00], V _{CORE} = 0.9V	338	369	384	401	417	µA

Dual-Supply DEEPSLEEP Mode

Table 15. Dual-Supply Operation Fixed V_{CORE} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V _{CORE} Fixed Current, DEEPSLEEP Mode	I _{CORE_FDSLPD}	V _{DD} = 3.3V, V _{CORE} = 1.1V	4.9	10.5	20	43	78	µA
		V _{DD} = 3.3V, V _{CORE} = 0.855V	1.26	4	9.8	25	49	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	4.9	10.5	20	43.6	78.9	µA
		V _{DD} = 1.8V, V _{CORE} = 0.855V	1.25	4	9.8	25	49	µA

Dual-Supply DEEPSLEEP Mode

Table 16. Dual-Supply Operation Fixed V_{DD} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V _{DD} Fixed Current, DEEPSLEEP Mode	I _{DD_FDSLPD}	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.262	0.36	0.531	0.965	1.67	µA
		V _{DD} = 3.3V, V _{CORE} = 0.855V	0.254	0.36	0.532	0.964	1.69	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	0.127	0.149	0.22	0.48	0.99	µA
		V _{DD} = 1.8V, V _{CORE} = 0.855V	0.127	0.149	0.22	0.48	0.99	µA

Dual-Supply BACKUP Mode

Table 17. Dual-Supply Operation Fixed V_{CORE} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{CORE} Fixed Current, BACKUP Mode	I _{CORE_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.115	0.3	0.856	2.6	5.7	µA

Table 17. Dual-Supply Operation Fixed VCORE Current Consumption BACKUP Mode (continued)

			$V_{DD} = 3.3V$, $V_{CORE} = 0.855V$	0.058	0.19	0.626	2.06	4.67	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 1.1V$	0.11	0.297	0.86	2.6	5.7	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 0.855V$	0.058	0.187	0.623	2.05	4.69	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 1.1V$	0.595	1.37	2.93	7.1	13.8	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 0.855V$	0.177	0.6	1.64	4.6	9.7	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 1.1V$	0.59	1.37	2.93	7.1	13.9	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 0.855V$	0.179	0.6	1.65	4.6	9.7	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 1.1V$	1.07	2.39	4.86	11.2	21.1	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 0.855V$	0.3	0.99	2.55	6.95	14.2	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 1.1V$	1.07	2.39	4.9	11.2	21.3	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 0.855V$	0.3	0.99	2.56	7	14.3	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 1.1V$	1.97	4.15	7.9	17.1	31.5	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 0.855V$	0.52	1.6	3.9	10.2	20.5	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 1.1V$	1.99	4.15	7.9	17.2	31.7	μA
			$V_{DD} = 1.8V$, $V_{CORE} = 0.855V$	0.52	1.6	3.9	10.2	20.6	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 1.1V$	3.7	7.4	13.2	27.2	49	μA
			$V_{DD} = 3.3V$, $V_{CORE} = 0.855V$	0.94	2.7	6.2	15.7	31.2	μA

Table 17. Dual-Supply Operation Fixed V_{CORE} Current Consumption BACKUP Mode (continued)

			V _{DD} = 1.8V, V _{CORE} = 1.1V	3.71	7.4	13.3	27.3	49.3	µA
			V _{DD} = 1.8V, V _{CORE} = 0.855V	0.947	2.7	6.3	15.7	31.3	µA

Dual-Supply BACKUP Mode**Table 18. Dual-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode**

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V _{DD} Fixed Current, BACKUP Mode	I _{DD_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 3.3V, V _{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 1.8V, V _{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V _{DD} = 1.8V, V _{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		20KB SRAM retained with RTC disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 3.3V, V _{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 1.8V, V _{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V _{DD} = 1.8V, V _{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		40KB SRAM retained with RTC disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 3.3V, V _{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 1.8V, V _{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V _{DD} = 1.8V, V _{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		80KB SRAM retained with RTC disabled	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA

Table 18. Dual-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode (continued)

160KB SRAM retained with RTC disabled			V _{DD} = 3.3V, V _{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V _{DD} = 1.8V, V _{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V _{DD} = 1.8V, V _{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		V _{DD} = 3.3V, V _{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA	
			0.26	0.36	0.53	0.97	1.7	µA	
			0.13	0.15	0.22	0.48	0.99	µA	
			0.13	0.15	0.22	0.48	0.99	µA	

Dual-Supply STORAGE Mode**Table 19. Dual-Supply Operation Fixed V_{CORE} Current Consumption STORAGE Mode**

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V _{CORE} Fixed Current, STORAGE Mode	I _{CORE_FSTOD}	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.064	0.25	0.8	2.58	5.71	µA
		V _{DD} = 3.3V, V _{CORE} = 1.1V	0.009	0.14	0.57	2.02	4.68	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	0.064	0.25	0.8	2.57	5.72	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	0.007	0.139	0.57	2.03	4.67	µA

Dual-Supply STORAGE Mode**Table 20. Dual-Supply Operation Fixed V_{DD} Current Consumption STORAGE Mode**

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V _{DD} Fixed Current, STORAGE Mode	I _{DD_FSTOD}	V _{DD} = 3.3V, V _{CORE} = 1.1V	0.22	0.32	0.49	0.93	1.66	µA
		V _{DD} = 3.3V, V _{CORE} = 1.1V	0.21	0.31	0.48	0.92	1.64	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	0.092	0.11	0.19	0.44	0.95	µA
		V _{DD} = 1.8V, V _{CORE} = 1.1V	0.092	0.11	0.19	0.44	0.95	µA

Ordering Information

PART	FLASH (KB)	SRAM (KB)	BOOTLOADER	SECURE BOOT	PIN-PACKAGE
MAX32670GTL+	384	160	YES	NO	40 TQFN
MAX32670GTL+T	384	160	YES	NO	40 TQFN
MAX32671GTL+*	384	160	YES	YES	40 TQFN
MAX32671GTL+T*	384	160	YES	YES	40 TQFN

T = Tape and reel. Full reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	5/20	Added MAX32671 and updated Pin Descriptions .	1–44
2	5/21	Updated Pin Descriptions . Updated Simplified Block Diagram . Added Bootloader and Secure Boot descriptions. Added new Bootloader Activation description in Applications Information . Added ERTCO stability capacitor requirements. Updated the Clocking Scheme . Changed the ERFO frequency range.	1, 2, 23, 32–35, 36, 39, 42–44
3	5/22	Updated Benefits and Features , the POWER section of the Electrical Characteristics table, and the Pin Description table. Removed UART speed indication. Updated the Bootloader Activation section in Applications Information. Added temperature variance Table 6 through Table 20 to the Applications Information section.	1, 8–14, 16–26, 36–38, 45, 48–55

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