*Click **here** to ask an associate for production status of specific part numbers.*

MAX20098

Versatile Automotive 36V 2.2MHz Buck Controller with 3.5µA I_Q

General Description

The MAX20098 is an automotive 2.2MHz synchronous step-down controller IC with 3.5µA IQ. This IC operates with an input-voltage supply from 3.5V to 42V and can operate in dropout condition by running at 99% (typ) duty cycle. It is intended for applications with mid- to high- power requirements that operate at a wide input voltage range such as during automotive cold-crank or engine stop-start conditions.

The step-down controller operates at up to 2.2MHz frequency to allow small external components, reduced output ripple, and to guarantee no AM band interference. The switching frequency is resistor adjustable (220kHz to 2.2MHz). FSYNC input programmability enables three frequency modes for optimized performance: forced fixed-frequency operation, skip mode with ultra-low quiescent current, and synchronization to an external clock. The IC also provides a SYNC output to enable two controllers to operate in parallel. The IC has a factory-programmable spread-spectrum option for frequency modulation to minimize EMI interference.

The PGOOD output indicates when the voltage is within regulation range. Protection features include cycle-by- cycle current limit and thermal shutdown. The MAX20098 is specified for operation over the -40°C to +125°C auto- motive temperature range.

Applications

- Infotainment Systems
- USB Hub
- General-Purpose Point-of-Load (POL)

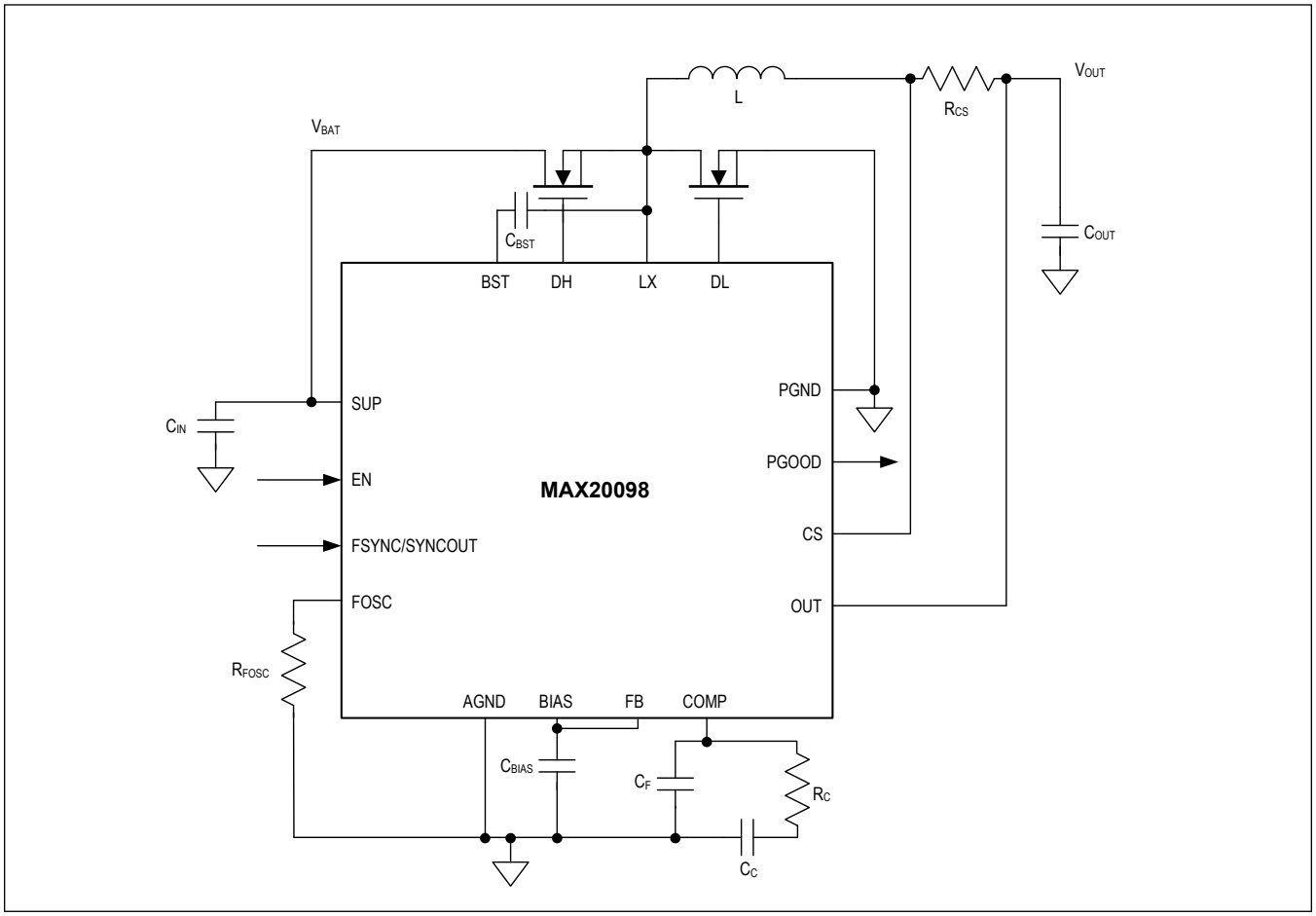
Benefits and Features

- Meets Stringent Automotive OEM Module Power Consumption and Performance Specifications
  - 3.5µA Quiescent Current in Skip Mode at V_{OUT} = 3.3V
  - Fixed 5.0V/3.3V or Adjustable 1V to 10V Output
  - ±1.1% Output-Voltage Accuracy for 5V Fixed Setting
- Enables Crank-Ready Designs
  - Wide Input Supply Range from 3.5V to 42V
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 50ns (typ) Minimum On-Time Allows
  - Skip-Free Operation for 3.3V Output from Car Battery at 2.2MHz
  - Spread-Spectrum Option
  - Frequency-Synchronization Input
  - Resistor-Programmable Frequency Between 220kHz and 2.2MHz
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - 2MHz Step-Down Controller
  - Current-Mode Controller with Forced-Continuous and Skip Modes
  - 16-Pin Side-Wettable (SW) TQFN-EP Package
  - 20A Reference Design Available
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection
  - Output Overvoltage and Undervoltage Monitoring
  - -40°C to +125°C Grade 1 Automotive Temperature Range
  - AEC-Q100 Qualified

Ordering Information appears at end of data sheet.

19-100089; Rev 16; 10/21

Simplified Block Diagram



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Absolute Maximum Ratings

SUP, EN, LX to PGND ..... -0.3V to +42V
OUT to AGND..... -0.3V to +12V
CS to OUT ..... -0.3V to +0.3V
BST to LX ..... -0.3V to +6V
FSYNC, FSYNCOUT, FOSC, COMP, FB to AGND.....-0.3V to to V_{BIAS} + 0.3V
BIAS to AGND ..... -0.3V to +6V
PGOOD to AGND..... -0.3V to +6V
DL to PGND ..... -0.3V to to V_{BIAS} + 0.3V
DH to LX ..... -0.3V to to V_{BST} + 0.3V
Continuous Power Dissipation (T_A = +70°C).....-40ºC to +125ºC
16 SW TQFN (derate 23.09mW/°C above +70°C) 1847mW
Operating Temperature Range (Note 5).....-40ºC to +125ºC
Junction Temperature.....+150ºC
Storage Temperature Range .....-40ºC to +150ºC

Note 1: Switching nodes (LX to PGND, BST to LX, DH to LX, DL to PGND) are self-protected for transient voltages (<50ns) of up to -5V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SW TQFN-EP

Package Type	16 SW TQFN
Package Code	T1633Y+5C
Outline Number	21-100150
Land Pattern Number	90-100064
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient Thermal Resistance (θ_{JA})	43.30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	4.0°C/W

Note:Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, C_{IN} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 2* and *Note 5*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-DOWN CONVERTER						
Supply Voltage Range	V_{SUP}	Normal operation (*Note 3*)	3.5		36	V
		t < 1s			42	
Output Overvoltage Threshold		Detected with respect to V_{FB} rising		107		%
		Detected with respect to V_{FB} falling		105		
Output Overvoltage-Threshold Debounce					5	µs

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 2 and Note 5))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{SUP}	V_{EN} = 0V		1	5	µA
		V_{EN} = 14V, V_{OUT} = 5V, no switching		5	11	
		V_{EN} = 14V, V_{OUT} = 3.3V, no switching		3.5	7	
		V_{EN} = 14V, MAX20098ATEG/VY+, no switching		81	150	
Fixed-Output Voltage	V_{OUT}	V_{FB} = VBIAS, V_{OUT} = 5V, PWM mode	4.945	5	5.055	V
		V_{FB} = VBIAS, V_{OUT} = 5V, skip mode	4.9	5	5.1	
		V_{FB} = VBIAS, V_{OUT} = 3.3V, PWM mode	3.234	3.3	3.366	
		V_{FB} = VBIAS, V_{OUT} = 3.3V, skip mode	3.234	3.3	3.366	
Output-Voltage Adjustable Range			1		10	V
Regulated Feedback Voltage	V_{FB}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB}	T_A = +25ºC		0.01	1	µA
Feedback Line-Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.01		%/V
Transconductance (from FB to COMP)	$g_{m,EA}$	V_{FB} = 1V, V_{BIAS} = 5V	220	500	650	µS
Dead Time		DL low to DH rising		15		ns
		DH low to DL rising		15		
Maximum Duty Cycle			97			%
Minimum On-Time	$t_{ON,MIN}$			50		ns
PWM Switching-Frequency Range	f_{SW}	Programmable	0.22		2.2	MHz
Switching Frequency		R_{FOSC} = 12kΩ, V_{BIAS} = 5V, 3.3V	2	2.2	2.4	MHz
CS Current-Limit Voltage Threshold	V_{LIMIT}	V_{CS} - V_{OUT}; V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	71	80	89	mV
Soft-Start Ramp Time		Fixed soft-start time regardless of frequency		5.4		ms
LX Leakage Current		V_{IN} = 6V, V_{LX} = $V_{PGND\_}$ or V_{IN}, T_A = +25°C		0.01		µA
DH Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		1.5		Ω
DH Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1		Ω
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		1.5		Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1		Ω
PGOOD Threshold	P_{GOOD_H}	% of V_{OUT} rising		95		%
	P_{GOOD_F}	% of V_{OUT} falling	91	93	95	
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = +25°C		0.01	1	µA

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, C_{IN} = 4.7µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 2 and Note 5))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD Debounce Time		Fault detection, rising and falling		32		µs
PGOOD Timeout		Default 0ms	0.5			ms
FSYNC INPUT						
FSYNC Frequency Range		FOSC = 2.2MHz, minimum sync pulse > (1/FSYNC - 1/FOSC)	1.8		2.6	MHz
		FOSC = 400kHz, minimum sync pulse > (1/ FSYNC - 1/FOSC)	320		480	kHz
		Minimum sync-in pulse	100			ns
FSYNC Switching Thresholds		High threshold	1.4			V
		Low threshold			0.4	
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.5	V
		V_{BIAS} falling	2.6	2.8		
Switchover Operating Range			3.2		5.5	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 4)		165		°C
Thermal Shutdown Hysteresis		(Note 4)		20		°C
ENABLE LOGIC INPUT						
High Threshold		EN	1.8			V
Low Threshold		EN			0.8	V
EN_ Input Bias Current		EN input only, T_A = +25ºC		0.01	1	µA
SYNCOUT OUTPUT						
SYNCOUT Low Voltage		I_{SINK} = 5mA			0.4	V
SYNCOUT Leakage Current		T_A = +25ºC			1	µA
SPREAD-SPECTRUM INPUT						
Spread Spectrum				±6		% of FOSC

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

Note 3: During initial startup, V_{SUP} rising must cross 4.5V. The normal operating range is then valid.

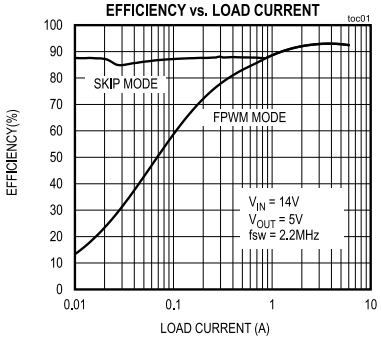
Note 4: Guaranteed by design; not production tested

Note 5: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

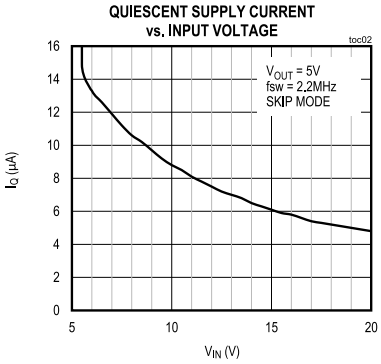
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

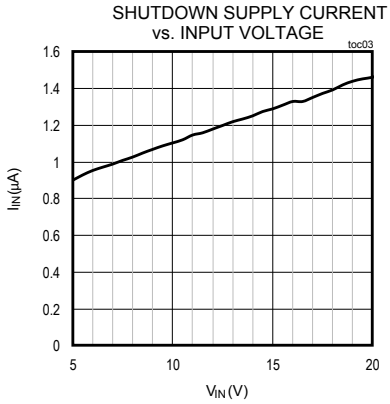
EFFICIENCY vs. LOAD CURRENT



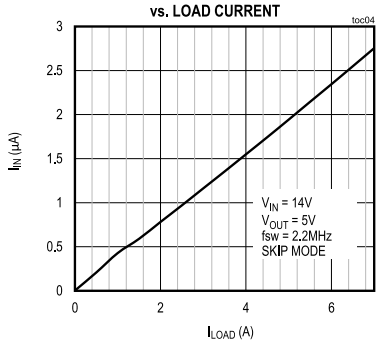
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE



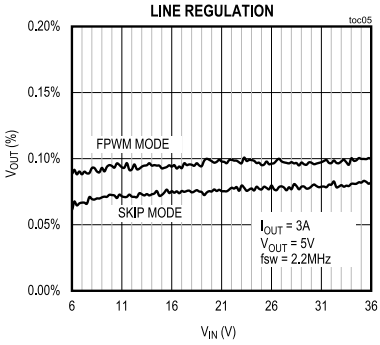
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



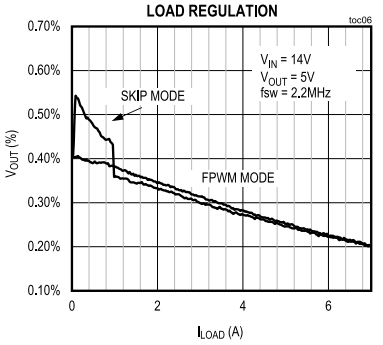
SUPPLY CURRENT vs. LOAD CURRENT



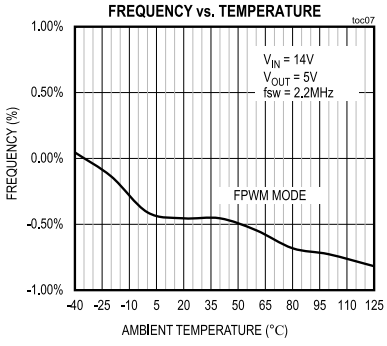
LINE REGULATION



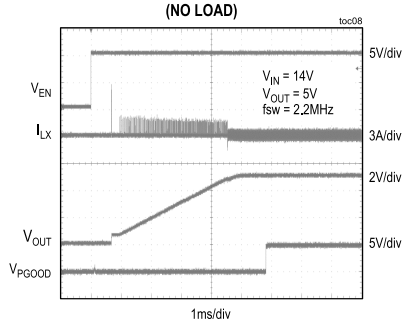
LOAD REGULATION



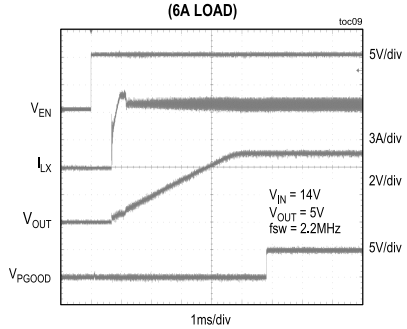
FREQUENCY vs. TEMPERATURE



STARTUP WAVEFORM (NO LOAD)



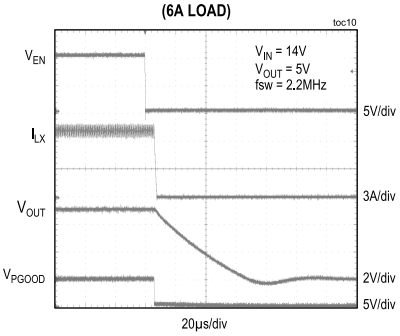
STARTUP WAVEFORM (6A LOAD)



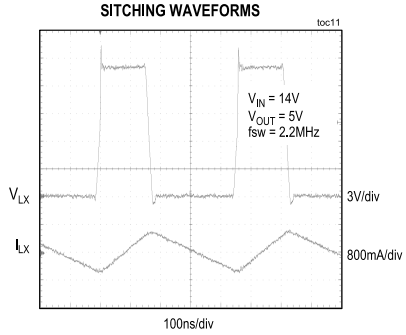
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

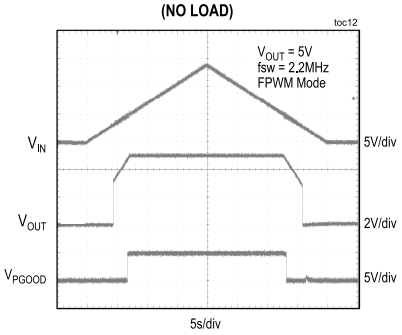
SHUTDOWN WAVEFORM (6A LOAD)



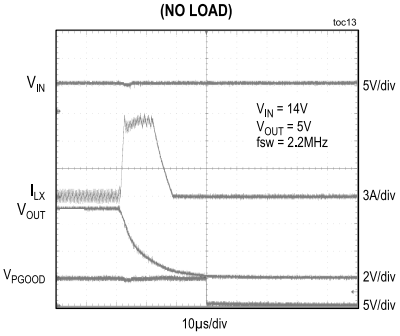
STEADY-STATE SITCHING WAVEFORMS



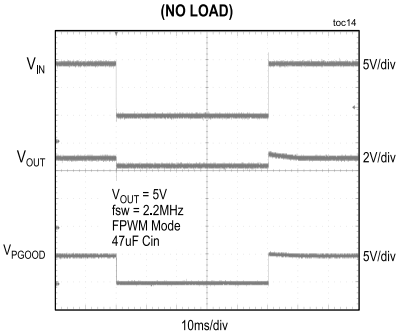
SLOW VIN RAMP (NO LOAD)



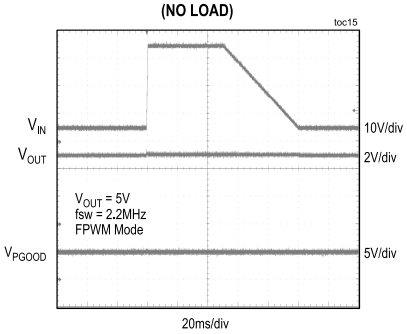
SHORT-CIRCUIT RESPONSE (NO LOAD)



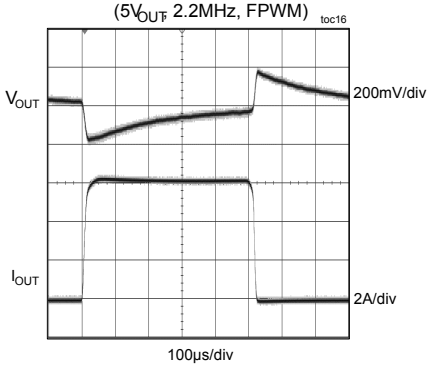
UNDERVOLTAGE PULSE (NO LOAD)



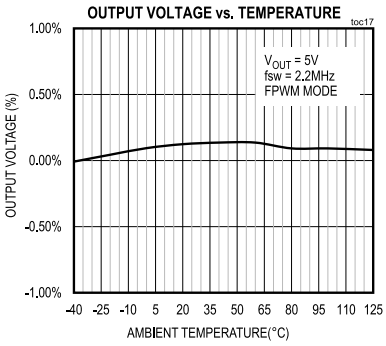
LOAD-DUMP TEST (NO LOAD)



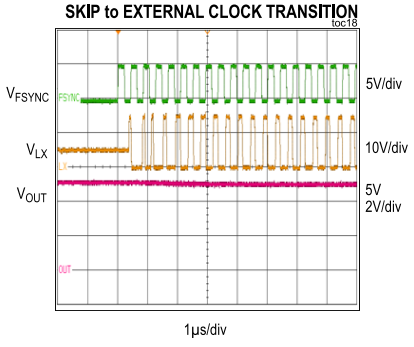
LOADSTEP TEST (5V_{OUT}, 2.2MHz, FPWM)



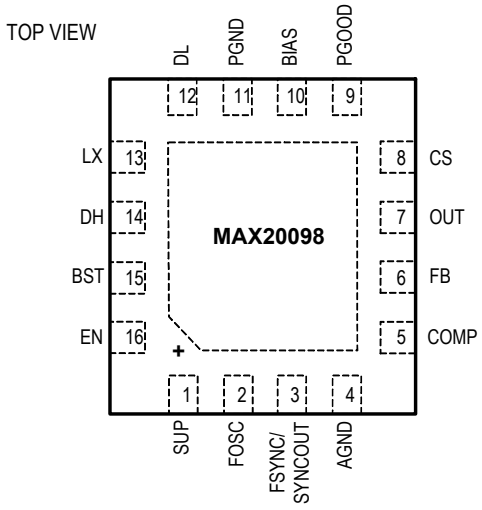
OUTPUT VOLTAGE vs. TEMPERATURE



SKIP to EXTERNAL CLOCK TRANSITION



Pin Configuration



SW TQFN
(3mm x 3mm)

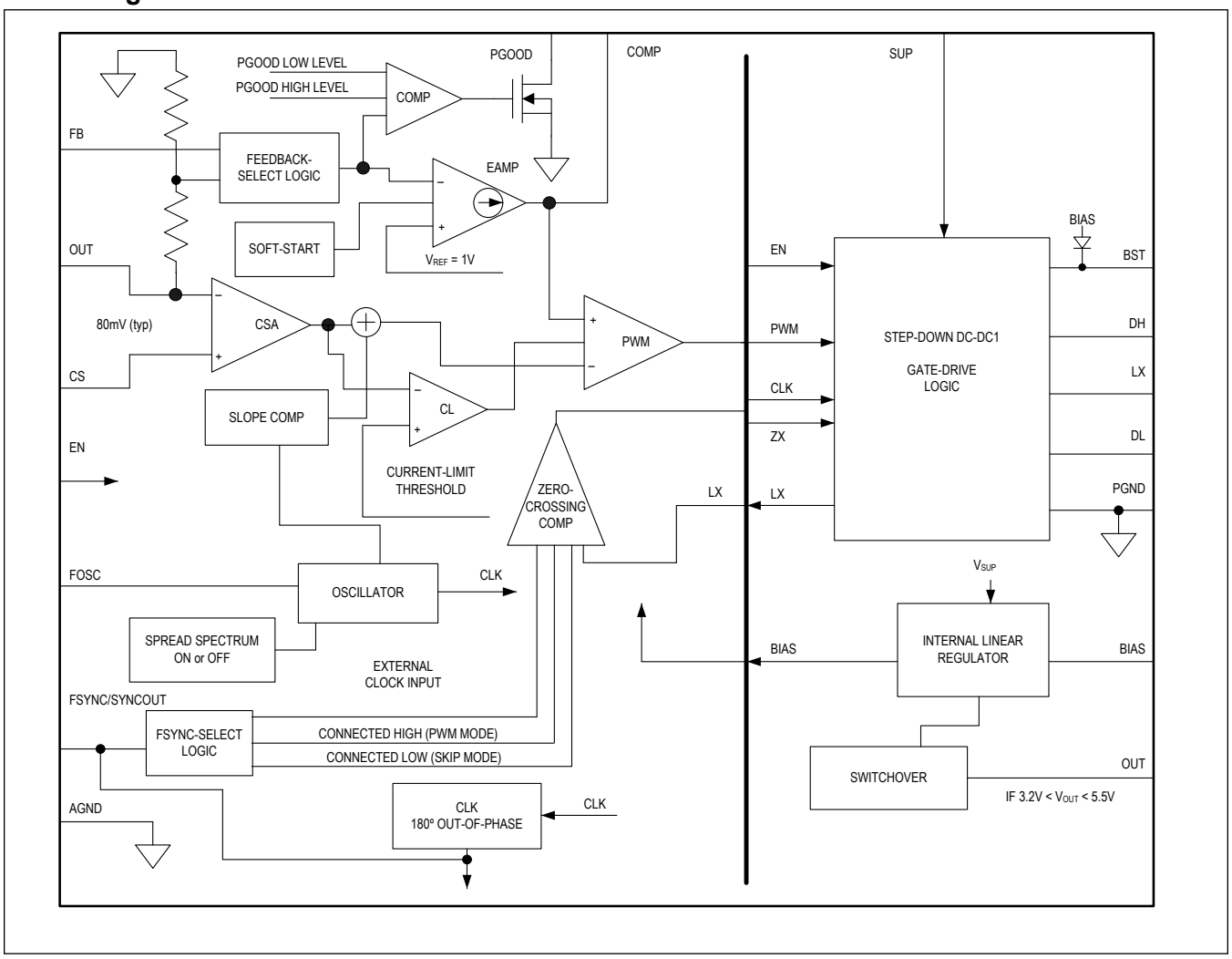
Pin Description

PIN	NAME	FUNCTION
1	SUP	Supply Input. Bypass SUP with enough capacitors to minimize input ripple.
2	FOSC	Frequency-Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC controller.
3	FSYNC/ SYNCOUT	External Clock-Synchronization Input. Synchronization to the controller operating-frequency ratio is 1. See the *Electrical Characteristics* table for frequency range and the *Switching Frequency/ External Synchronization* section for additional information. Connect FSYNC to AGND to enable skip mode of operation. Connect to BIAS or an external clock to enable forced-PWM mode of operation. Factory option allows synchronous output to allow controllers to operate in parallel.
4	AGND	Signal Ground for the IC
5	COMP	Buck Controller Error-Amplifier Output. Connect an RC network to COMP to compensate the buck controller.
6	FB	Feedback Input for Buck Controller. Connect FB to BIAS for the fixed output, or to a resistive divider between OUT and AGND to adjust the output voltage between 1V and 10V. In adjustable mode, FB regulates to 1V (typ). See the *Setting the Output Voltage* section.
7	OUT	Output Sense and Negative Current-Sense Input for Buck Controller. When using the internal preset feedback-divider (FB = BIAS), the controller uses OUT to sense the output voltage. Connect OUT to the negative terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT and CS)* and *Current-Sense Measurement* sections.
8	CS	Positive Current-Sense Input for Buck Controller. Connect CS to the positive terminal of the current sense element. See the *Current Limiting and Current-Sense Inputs (OUT and CS)* and *Current-Sense Measurement* sections.
9	PGOOD	Open-Drain Power-Good Output for Buck Controller. PGOOD is low if OUT is more than 7% (typ) below the normal regulation point. PGOOD asserts low during soft-start and in shutdown. PGOOD becomes high impedance when OUT is in regulation. To obtain a logic signal, pull up PGOOD with an external resistor connected to a positive voltage lower than 5.5V.

Pin Description (continued)

PIN	NAME	FUNCTION
10	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 2.2µF minimum value. BIAS provides the power to the internal circuitry and external loads. See the *Fixed 5V Linear Regulator (BIAS)* section.
11	PGND	Power Ground for the Controller
12	DL	Low-Side Gate-Driver Output. DL output voltage swings from V_{PGND} to V_{BIAS}.
13	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
14	DH	High-Side Gate-Driver Output. DH output voltage swings from V_{LX} to V_{BST}.
15	BST	Boost Flying-Capacitor Connection. Connect a ceramic capacitor between BST and LX. See the *High-Side Gate-Driver Supply (BST)* section. When the switching frequency is greater than 1MHz, connect a high-voltage Schottky diode between BIAS and BST.
16	EN	High-Voltage Tolerant, Active-High Digital-Enable Input for the Controller
EP	-	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Block Diagram



Detailed Description

The MAX20098 is an automotive 2.2MHz synchronous step-down controller IC with 3.5µA I_Q, and a fixed output voltage, or an adjustable 1V to 10V output voltage. In skip mode, with no load, the total supply current is reduced to 3.5µA (typ). When the controller is disabled, the total current drawn is further reduced to 1µA (typ). Connect EN directly to V_{BAT}, or to a power-supply sequencing logic.

Fixed 5V Linear Regulator (BIAS)

The internal circuitry of the IC requires a 5V bias supply. An internal 5V linear regulator (BIAS) generates this supply. Bypass BIAS with a 2.2µF or greater ceramic capacitor to guarantee stability under the full-load condition.

The BIAS linear regulator can source up to 100mA for internal logic, DH, and DL drivers. The estimation of the internal current requirements for the ICs:

$I_{BIAS} = I_{CC} + f_{SW} \times (Q_{GDH} + Q_{GDL})$ = 20mA to 50mA (typ) for 400kHz

where I_{CC} is the internal supply current (5mA, typ), f_{SW} is the switching frequency. Q_{GDH} is the gate charge of the upper MOSFET, and Q_{GDL} is the gate charge of the lower MOSFET. Q_G ($Q_G = Q_{GDH} + Q_{GDL}$) is the MOSFET's total gate charge (specification limits at V_{GS} = 5V). The BIAS linear regulator is not intended for powering external loads.

Switchover

Switchover typically occurs during skip mode to reduce operating current, but this skip mode switchover can be disabled by using the ATEG version of the MAX20098. This IC also offers an option to force switchover at all times, when possible.

When switchover occurs, BIAS internally switches to OUT and the internal linear regulator turns off. This configuration has several advantages:

- Reduces the internal power dissipation of the IC
- Improves low-load efficiency as the internal supply current is scaled down proportionally to the duty cycle
- Switchover occurs when the output voltage is between 3.2V and 5.5V; when voltage is outside this range, the internal BIAS LDO is used

Undervoltage Lockout (UVLO)

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.8V (typ) UVLO falling threshold. Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and EN enables the buck controller, the controller start switching and the output voltages begin to ramp up using soft-start.

Buck Controller

The IC provides a buck controller with synchronous rectification. The step-down controller uses a PWM, current-mode control scheme. External MOSFETs allow for optimized load-current design. Output-current sensing provides an accurate current limit with a sense resistor, or power dissipation can be reduced by using lossless current sensing across the inductor.

Soft-Start

Once the buck controller is enabled by driving EN high, the soft-start circuitry gradually ramps up the reference voltage during soft-start time (t_{SSTART} = 5.4ms (typ)) to reduce the input surge currents during startup. Before the device can begin the soft-start, the following conditions must be met:

V_{BIAS} exceeds the 3.5V (max) undervoltage lockout threshold V_{EN} goes logic-high

Switching Frequency/External Synchronization

The IC provides an internal oscillator, adjustable from 220kHz to 2.2MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. To set the switching frequency, connect a resistor (R_{FOSC}) from FOSC to AGND .

$$R_{FOSC} = \frac{400kHz \times 66k\Omega}{FOSC}$$

where FOSC is in Hz and R_{FOSC} is in Ω.

The IC can be synchronized to an external clock by connecting the external clock signal to FSYNC. A rising edge on FSYNC resets the internal clock. Keep the FSYNC frequency ±20% of the internal frequency. The ICs can be used in parallel for multiphase operation when high power is required. Multiphase operation includes one master and one or more slave ICs. Synchronization is achieved by connecting the master IC's clock output SYNCOUT to the slave IC's clock input FSYNC. Contact the factory for SYNCOUT options.

Light-Load-Efficiency Skip Mode (V_{FSYNC} = 0V)

Drive FSYNC low to enable skip mode. In skip mode, the IC stops switching until the FB voltage drops below the reference voltage. Once the FB voltage has dropped below the reference voltage, the IC begins switching until the inductor current reaches 30% of the maximum current defined by the inductor DCR or output shunt resistor.

Forced-PWM Mode (V_{FSYNC})

Driving FSYNC high prevents the IC from entering skip mode by disabling the zero-crossing detection of the inductor current. This forces the low-side gate-driver waveform to constantly be the complement of the high-side gate-driver waveform, so the inductor current reverses at light loads and discharges the output capacitor. The benefit of forced-PWM mode is to keep the switching frequency constant under all load conditions; however, forced- frequency operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions. Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Maximum Duty-Cycle Operation

The IC has a maximum duty cycle of 97% (min). The internal logic of the IC looks for approximately 10 consecutive high-side FET ON pulses and decides to turn on the low-side FET for 150ns (typ) every 12µs. The input voltage at which the IC enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the IC enters dropout can be approximated as:

$$V_{IN} = [V_{OUT} + (I_{OUT} \times R_{ON\_H})] / 0.97$$

Note: The above equation does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the R_{ON_H} max number from the data sheet of the respective high-side MOSFET used.

Spread Spectrum

The IC features enhanced EMI performance. It performs ±6% dithering of the switching frequency to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent emission limits. All of this is controlled by a pin on the IC. When using an external clock source (e.g., driving the FSYNC input with an external clock), spread spectrum is disabled.

MOSFET Gate Drivers (DH and DL)

The DH high-side n-channel MOSFET drivers are powered from capacitors at BST, while the low-side drivers (DL) are powered by the 5V linear regulator (BIAS). During BIAS switchover, the gate drive may be as low as 3.2V. V_{GS} should be considered when low BIAS voltage is expected. Choose $V_{GS(TH)}$ carefully. A shoot-through protection circuit monitors the gate-to-source voltage of the external MOSFETs to prevent a MOSFET from turning on until the complementary switch is fully off. There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the protection circuits to work properly. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver) It may be necessary to decrease the slew rate for the gate drivers to reduce switching noise or to compensate for low-gate-charge capacitors. For the low-side drivers, use 1nF to 5nF gate capacitors from DL to PGND. For the high-side drivers, connect a small 1Ω to 5Ω resistor between BST and the bootstrap capacitor.

High-Side Gate-Driver Supply (BST)

The high-side MOSFET is turned on by closing an internal switch between BST and DH and transferring the bootstrap

capacitor's (at BST) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor. When the switching frequency range is greater than 1MHz, connect a high-voltage diode between BIAS and BST.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values (C_{BST} in the *Typical Application Circuit*) according to:

$CBST = QG/\Delta V_{BST}$

where QG is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV to 300mV) when determining C_{BST}. The boost capacitor should be a low-ESR ceramic capacitor; a minimum value of 100nF works in most cases.

Current Limiting and Current-Sense Inputs (OUT and CS)

The current-limit circuit uses differential current-sense inputs (OUT and CS) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (V_{LIMIT} = 80mV (typ)), the PWM controller turns off the high-side MOSFET. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current; therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (VOUT/VIN). For the most accurate current sensing, use a current-sense shunt resistor (R_{CS}) between the inductor and the output capacitor. Connect CS to the inductor side of R_{CS} and OUT to the capacitor side. Dimension R_{CS} such that the maximum inductor current (I_L (max) = I_{LOAD} (max) + 1/2 I_{RIPPLE} (peak-to-peak) induces a voltage of V_{LIMIT} across R_{CS}, including all tolerances. For higher efficiency, the current can also be measured directly across the inductor. This method could cause up to 30% error over the entire temperature range and requires a filter network in the current-sense circuit. See the *Current-Sense Measurement* section.

Voltage Monitoring (PGOOD)

The IC includes a power monitoring signal (PGOOD) to facilitate power-supply sequencing and supervision. PGOOD can be used to enable circuits that are supplied by the IC's output voltage rail, or to turn on subsequent supplies. The PGOOD signal features hysteresis, it stays low until output voltage rises to 95% of the nominal value and is pulled low only when output voltage falls to 93% of the nominal value. PGOOD also asserts low during soft-start and soft-discharge. PGOOD goes high impedance when the output voltage is at its nominal value (range). Connect a 10kΩ pullup resistor from PGOOD to a relevant logic rail to level shift the signal.

Thermal-Overload, Overcurrent, Overvoltage, and Undervoltage Behavior

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature exceeds +165°C, an internal thermal sensor shuts down the IC, allowing it to cool. The thermal sensor turns on the IC again after the junction temperature cools by 20°C.

Overcurrent Protection

If the inductor current on the IC exceeds the maximum current limit programmed at CS and OUT, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. Choose the components so they can withstand the short-circuit current if required.

Overvoltage Protection

The IC limits the output voltage of the buck converters by turning off the high-side gate driver at approximately 108% of the regulated output voltage. The output voltage needs to come back in regulation before the high-side gate driver starts switching again.

Design Procedure

Effective Input Voltage Range in the Buck Converter

Although the IC can operate from input supplies up to 36V (42V transients) and regulate down to 1V, the minimum voltage conversion ratio (V_{OUT}/V_{IN}) might be limited by the minimum controllable on-time. For proper fixed- frequency PWM operation and optimal efficiency, buck 1 and buck 2 should operate in continuous conduction during normal operating conditions. For continuous conduction, set the typical voltage conversion ratio following Equation:

$$\frac{V_{OUT}}{V_{IN}} > 50ns \times f_{SW}$$

where f_{SW} is the switching frequency in hertz. If the desired voltage conversion does not meet the above condition, pulse skipping occurs to decrease the effective duty cycle. Decrease the switching frequency if constant switching frequency is required. The same is true for the maximum voltage-conversion ratio.

The maximum voltage-conversion ratio is limited by the maximum duty cycle of 97% and the maximum allowed output voltage of 10V.

$$\frac{V_{OUT}}{V_{IN} - V_{DROP}} < 0.97$$

where $V_{DROP} = I_{OUT} (R_{ON,HS} + R_{DCR})$ is the sum of the parasitic voltage drops in the high-side path. During low-drop operation, the IC reduces f_{SW} to ~80kHz. In practice, the above condition should be met with adequate margin for good load-transient response.

Setting the Output Voltage

Connect FB to BIAS to enable the fixed buck-controller output voltages (5V and 3.3V) set by a preset internal resistive voltage-divider connected between the feedback (FB) and AGND. To externally adjust the output voltage between 1V and 10V, connect a resistive divider from the output (OUT) to FB to AGND (see the *Typical Application Circuit*. Calculate RFB with:

$$R_{FB2} = R_{FB1} \times [(\frac{V_{OUT}}{V_{FB}}) - 1]$$

where V_{FB} = 1V (typ) (see the *Electrical Characteristics* table), R_{FB2}, R_{FB1} are top and bottom resistors in the feedback divider.

DC output-accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold, V_{FB} = 1V (typ). When the inductor conducts continuously (continuous conduction mode), the IC regulates the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output-ripple voltage.

In discontinuous-conduction mode (skip or STDBY active and $I_{OUT} < I_{LOAD(SKIP)}$), the IC regulates the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold.

Inductance

The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient-response requirements:

- Lower inductor values increase LIR, which minimizes size and cost and improves transient response at the cost of reduced efficiency due to higher peak currents.
- Higher inductance values decrease LIR, which increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value, as shown in the following Equation:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions).

To avoid instability for >50% duty cycle cases, the inductance must satisfy the slope compensation criterion:

$$V_{SLOPE} f_{SW} > \frac{V_{OUT}}{2 \times L_{MIN2}} A_{VCS} R_{CS}$$

where A_{VCS} is the current sense amplifier gain (typical 13V/V). V_{SLOPE} is V_{OUT} dependent and is given by the equation below:

$$V_{SLOPE} = 105mV \text{ for } 0V < V_{OUT} \le 3V$$
$$= 210mV \text{ for } 3V < V_{OUT} \le 5.5V$$
$$= 420mV \text{ for } 5.5V < V_{OUT}$$

Select the larger of L_{MIN1} and L_{MIN2} as L_{MIN}.

Peak Inductor Current

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current, in addition to half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is calculated as follows:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz. Once the peak current and the inductance are known, the inductor can be selected. The saturation current should be larger than I_{PEAK} or at least in a range where the inductance does not degrade significantly. The MOSFETs are required to handle the same range of current without dissipating too much power.

MOSFET Selection

The step-down controller drives two external logic-level n-channel MOSFETs as the circuit-switch elements. The key selection parameters to choose these MOSFETs include the items in the following sections.

Threshold Voltage

All n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V. If the internal regulator is bypassed (e.g., buck output = 3.3V), then the n-channel MOSFETs should be chosen to have guaranteed on-resistance at that gate-to-source voltage.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

All MOSFETs must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions

Current Capability

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V, or V_{GS} = 3.3V when the internal linear regulator is bypassed. For load currents below ~3A, dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the BST path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Current-Sense Measurement

For the best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor between the inductor and output, as shown in Figure 1. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement. Alternatively, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by

connecting a series RC circuit across the inductor (Figure 2) with an equivalent time constant.

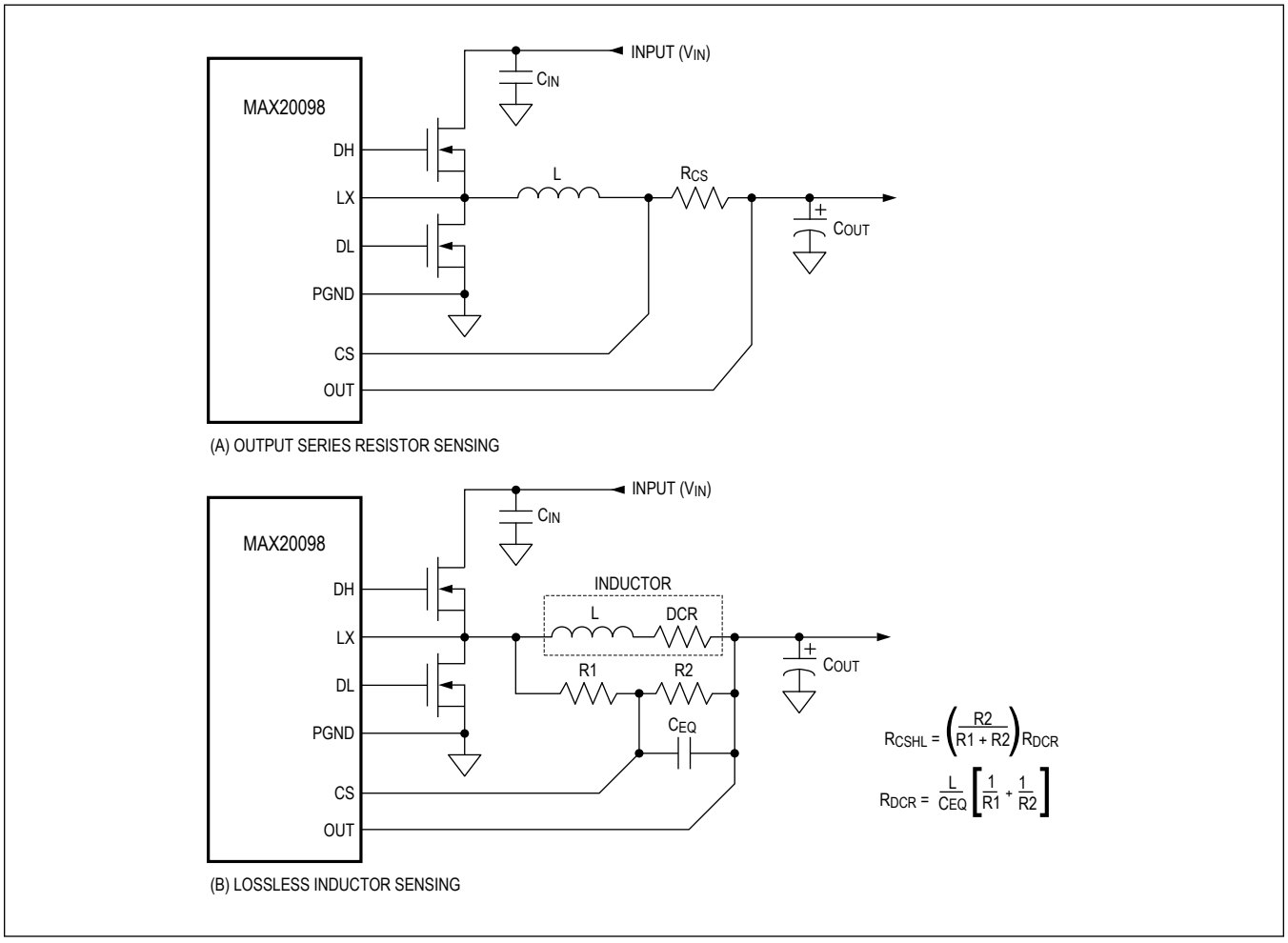


Figure 1. Current-Sense Configurations

$$R_{CSHL} = (\frac{R2}{R1 + R2})R_{DCR}$$

and

$$R_{DCR} = \frac{L}{C_{EQ}}(\frac{1}{R1} + \frac{1}{R2})$$

where R_{CSHL} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistor. Use the inductance and R_{DCR} values provided by the inductor manufacturer. If DCR sense is the preferred current-sense method, then the recommended resistor value for R1 (Figure 2) is ≤ 1kΩ.

Carefully follow the *PCB Layout Recommendations* to ensure the noise and DC errors do not corrupt the differential current-sense signals seen by CS and OUT. Place the sense resistor close to the IC with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Input Capacitor

The discontinuous input current of the buck converter causes large input-ripple currents and therefore the input capacitor must be carefully chosen to withstand the input-ripple current and the input-voltage ripple kept within design requirements. When using two MAX20098 in parallel, the 180° ripple-phase operation increases the frequency of the

input-capacitor ripple current to twice the individual converter switching frequency. When using ripple phasing, the worst-case input-capacitor ripple current is when the converter with the highest output current is on.

The input-voltage ripple is composed of ΔV_Q (caused by capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and ESR required for a specific ripple.

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2})}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times (\frac{V_{OUT}}{V_{IN}})}{(\Delta V_Q \times f_{SW})} \times (1 - D)$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current in amps, ΔI_{P-P} is the peak-to-peak inductor current in amps, f_{SW} is the switching frequency in MHz, and L is the inductor value in µH. The internal 5V linear regulator (BIAS) includes an output UVLO with hysteresis to avoid unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the undervoltage-lockout threshold during transient loading.

Output Capacitor

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from

causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

The total voltage sag (V_{SAG}) can be calculated as shown:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}((V_{IN} \times D_{MAX}) - (V_{OUT})}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as shown in the following equation:

$$V_{SOAR} = \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

ESR Considerations

The output-filter capacitor must have low enough equivalent series resistance (ESR) to meet output-ripple and load-transient requirrements, yet have high enough ESR to satisfy stability requirements. When using high Capacitance low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the output capacitor's size depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications.

$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$

In standby mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold ($V_{CS,SKIP}$ = 15mV (typ)).

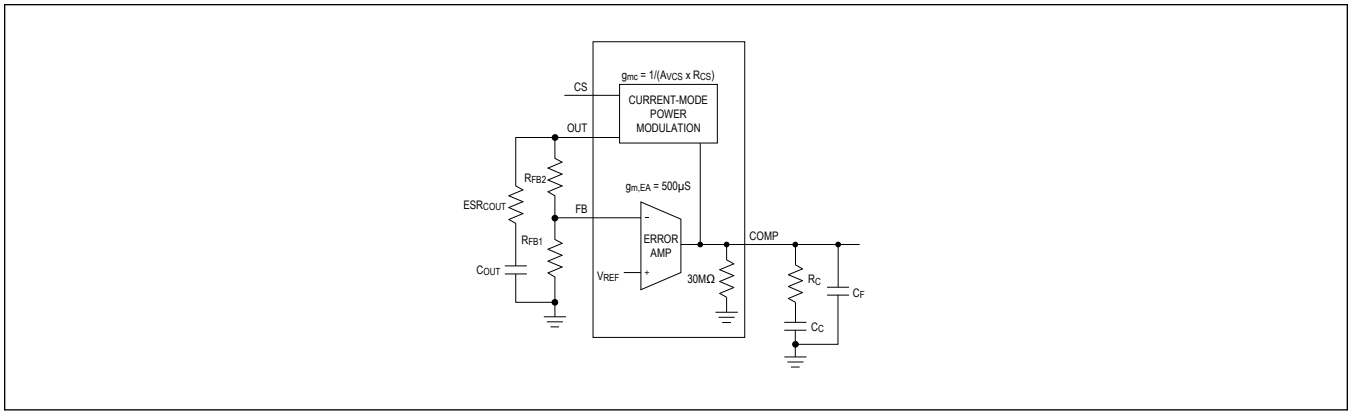


Figure 2. Compensation Network

Compensation-Components Calculation

The IC uses a current-mode-control scheme for boost controller. A single series resistor (R_C) and capacitor (C_C) is all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 2). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor (C_F) from COMP to AGND to cancel this ESR zero. The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 2. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by

$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in ohms and g_{mc} =1/(A_{VCS} x R_{DC}) in Siemens. A_{VCS} is the voltage gain of the current-sense amplifier and is typically 13V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in ohms. In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the frequency, as shown below:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The output capacitor and its ESR also introduce a zero:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of “n” identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor. The feedback voltage-divider has a gain of $GAIN_{FB}$ = V_{FB}/VOUT, where V_{FB} is 1V (typ). The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 500µS (typ), and ROUT,EA is the output resistance of the error amplifier, which is 30MΩ (typ) (see the *Electrical Characteristics* table.) A dominant pole (fdpEA) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by CF and RC to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB).

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (ROUT, EA + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_C in the range shown:

$$f_{pMOD} < f_C \le \frac{f_{SW}}{5}$$

At the crossover frequency, the total loop gain must be equal to 1.

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_c)} = 1$$

$$GAIN_{EA(fC)} = g_{m,\,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,\,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,\,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as shown:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (CF) from COMP to AGND. The value of C_F is shown:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

Applications Information

PCB Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (see Figure 3). If possible, mount all power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- BST diode footprint can be added if future use of a Schottky is expected.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. 2oz is recommended for higher currents such as 20A.
- Minimize current-sensing errors by connecting CS and OUT. Use kelvin sensing directly across the current-sense resistor (R_{CS}).
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (FB, CS, and OUT).

Layout Procedure

1. Place the power components first, with ground terminals adjacent (low-side FET, C_{IN}, C_{OUT}). If possible, make all these connections on the top layer with wide, copper-filled areas. Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite DL and DH to keep LX, PGND, DH, and the DL gate-drive lines short and wide. To keep the driver impedance low and for proper adaptive dead-time sensing, the DL and DH gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
2. Group the gate-drive components (BST diode and capacitor and LDO bypass capacitor, BIAS) together as close as possible to the controller IC. Be aware that gate currents of up to 1A flow from the bootstrap capacitor to BST, from DH to the gate of the external HS switch, and from the LX pin to the inductor. Up to 100mA of current flows from the BIAS capacitor through the bootstrap diode to the bootstrap capacitor. Dimension those traces accordingly.
3. Make the DC-DC controller ground connections as shown in Figure 3. This diagram can be viewed as having two separate ground planes: power ground (where all the high-power components go), and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly under the IC.
4. Connect the output power planes directly to the output filter capacitor's positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close as possible to the load.

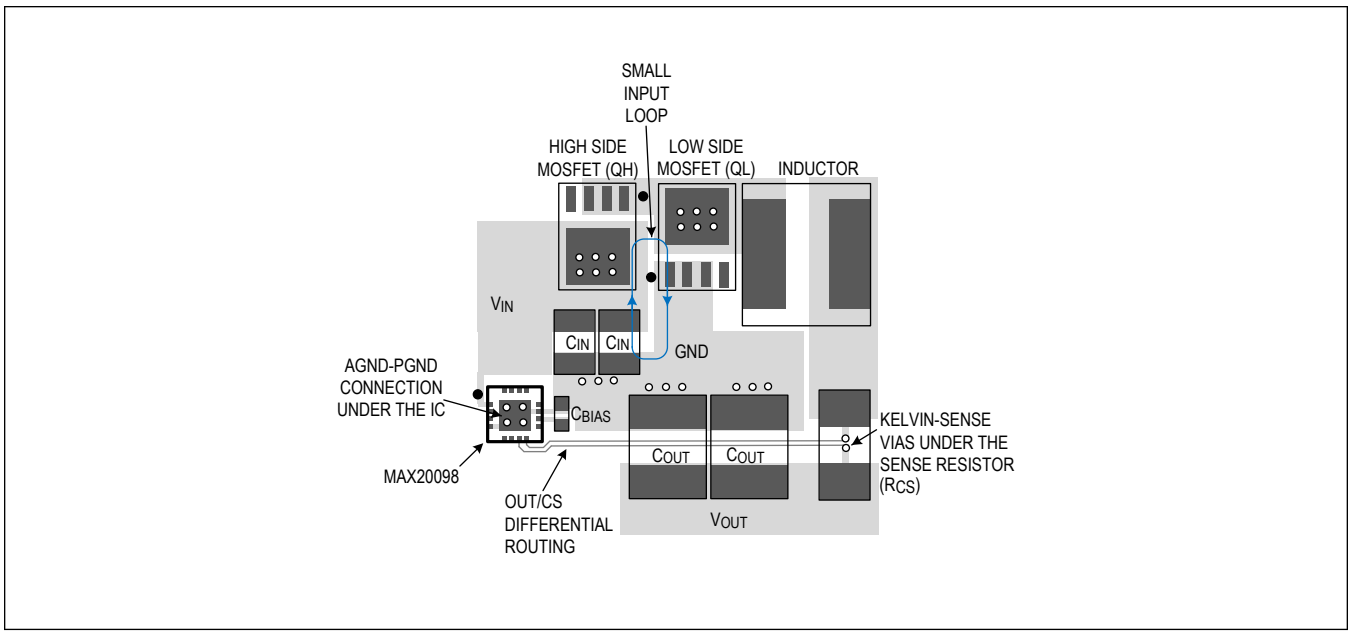
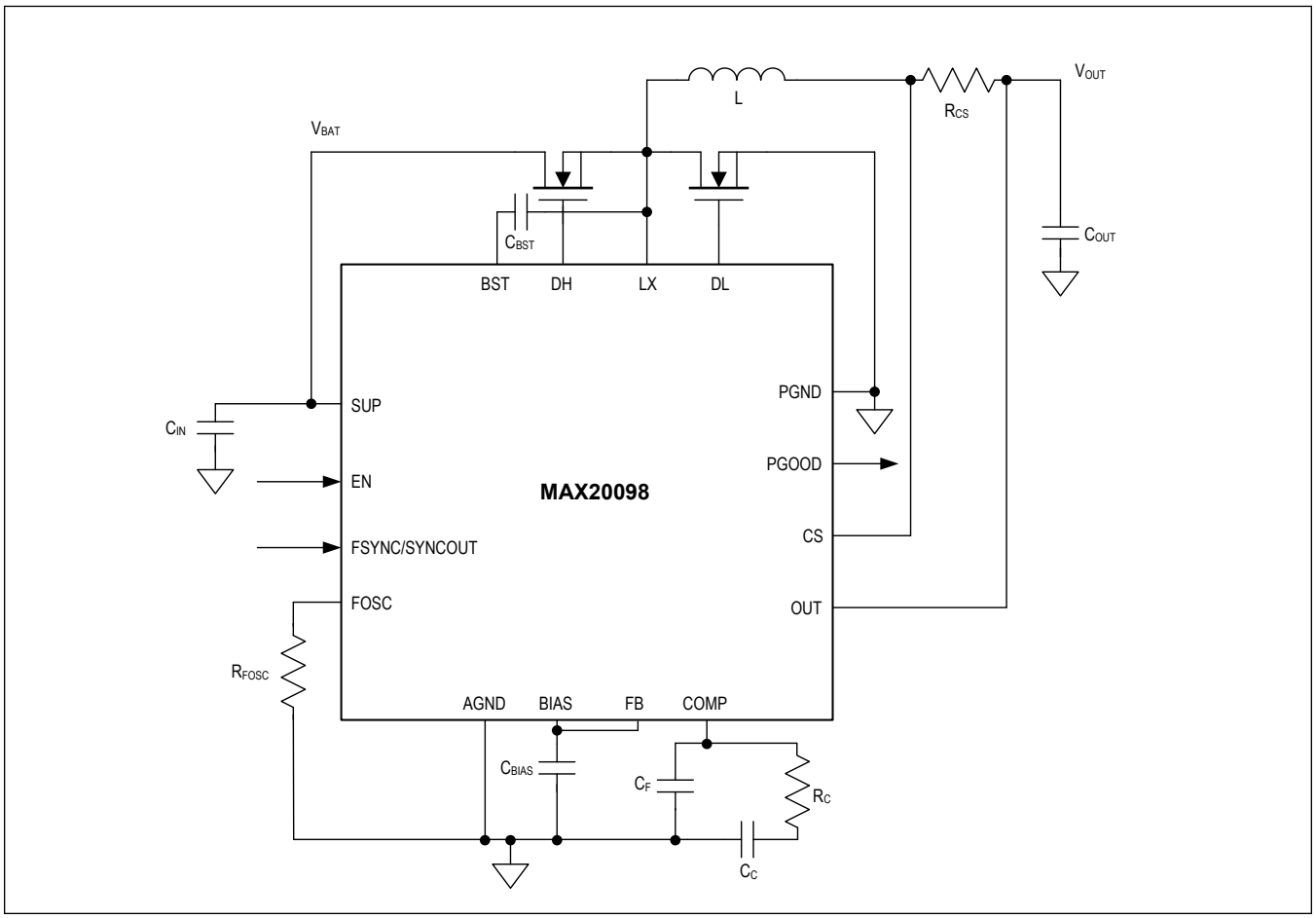


Figure 3. Layout Example

Typical Application Circuits



Ordering Information

PART	PIN-PACKAGE	VOUT		SPREAD SPECTRUM	SWITCH-OVER IN FPWM	SWITCH-OVER IN SKIP	SYNC/ SYNCOUT
		ADJUSTABLE	FIXED				
MAX20098ATEA/VY+	16 SW TQFN-EP*	1V to 10V	5V	Off	On	On	SYNC
MAX20098ATEB/VY+	16 SW TQFN-EP*	1V to 10V	3.3V	Off	On	On	SYNC
MAX20098ATEC/VY+	16 SW TQFN-EP*	1V to 10V	5V	On	On	On	SYNC
MAX20098ATED/VY+	16 SW TQFN-EP*	1V to 10V	3.3V	On	On	On	SYNC
MAX20098ATEE/VY+	16 SW TQFN-EP*	1V to 10V	3.3V	Off	Off	On	SYNC
MAX20098ATEF/VY+	16 SW TQFN-EP*	1V to 10V	3.3V	On	Off	On	SYNC
MAX20098ATEG/VY+	16 SW TQFN-EP*	1V to 10V	3.3V	On	Off	Off	SYNC

Note: All parts operate over the -40°C to +125°C automotive temperature range.

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package. SW = Side-wettable TQFN package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	9/17	Updated *Block Diagram*, pin 15 in *Pin Description* table, *PCB Layout Recommendations* section, and *Typical Application Circuit*	8, 9, 18, 19
2	10/17	Updated *Electrical Characteristics* table (adding a new Note 4 and renumbering the remaining notes); added new TOC18 in *Typical Operating Characteristics* section; added new Equation 2 in *Switching Frequency/External Synchronization* section, and renumbered the remaining equations	2–4, 8, 10–17
3	10/17	Changed derating for 16 SW TQFN in *Absolute Maximum Ratings* section from 28.8mW/°C to 20.8mW/°C; updated pin 3 in *Pin Description* table; updated *Block Diagram*; updated the last bullet in Switchover and added *Switchover* 2nd sentence in *MOSFET Gate Drivers (DH and DL)* sections; removed future product status from MAX20098ATEE/VY+ in *Ordering Information* table	2, 7, 9–11, 20
3.1		Corrected revision date on first page	1
4	1/18	Changed Minimum On-Time in *Benefits and Features* from 40ns to 50ns	1
5	1/18	Removed future product status from MAX20098ATEB/VY+, MAX20098ATED/VY+, and MAX20098ATEF/VY+ in *Ordering Information* table	20
6	3/18	Updated title, *General Description*, *Benefits and Features*, Notes in *Electrical Characteristics* table, TOC 4, *Fixed 5V Linear Regulator (BIAS)*, Switchover, *MOSFET Gate Drivers (DH and DL)*, *Current Limiting and Current-Sense Inputs* (OUT and CS), *Effective Input Voltage Range in the Buck Converter*, *Setting the Output Voltage*, *Input Capacitor*, Figure 2 caption, and *PCB Layout Recommendations* sections	1–21
7	5/18	Removed future part designation for MAX20098ATEC/VY+	20
8	9/18	Updated *Pin Description* and *High-Side Gate-Driver Supply (BST)* sections	8, 11
9	11/18	Updated *Electrical Characteristics* table (FSYNC Frequency Range), TOC18 in *Typical Operating Characteristics* section, and *Switching Frequency/External Synchronization* section; updated *Ordering Information* table and added MAX20098ATEG/VY+	3, 6, 10, 11, 20
10	4/19	Updated the data sheet title (added “Automotive”), *Benefits and Features*, *Absolute Maximum Ratings*, Package Thermal Characteristics, *Electrical Characteristics* (globals, table, and added Note 5), *Pin Description* table. Updated Switchover and Current Limiting *Switchover* and *Current-Sense Inputs (OUT and CS)* in the *Detailed Description* section	1-4, 6, 10, 12
11	6/19	Updated *Electrical Characteristics* and *Detailed Description*	3, 10
12	10/19	Updated TOC3 and TOC16 in *Typical Operating Characteristics* section 5	5, 6
13	7/20	Formula labels/formatting, update *Benefits and Features* to 1.1%, remove *Electrical Characteristics* Note 4, switchover range in *Block Diagram*, *Inductance* guidance, *Layout Example*	1, 6, 7, 12–24
14	8/20	Corrected units in *Electrical Characteristics*	6, 7
15	11/20	Updated Continuous Power dissipation and derating value in *Absolute Maximum Ratings*, Corrected symbol and units in *Electrical Characteristics*, Corrected units and edited text formatting in Switching Frequency, Edited Voltage monitoring description, Setting the output voltage, Current sense measurements, Corrected formula in Input capacitor, edited the figure on compensation network and edited formatting in Compensation-Component Calculation in *Detailed Descriptions*, Edited formatting in PCB Layout Recommendations in *Applications Information*	5, 6, 14–16, 18–22
16	10/21	Updated auto qualification in *Benefits and Features*	1

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