20V, 4-Channel Buck DC/DC with 8x Configurable 1.5A Power Stages

FEATURES

- **Wide V_{IN} Range: 3V to 20V**
- **Wide V_{OUT} Range: 0.4V to 0.83 • V_{IN}**
- **8× 1.5A Buck Power Stages Configurable as 1 to 4 Output Channels**
- **15 Unique Pin Selectable Output Configurations (1.5A to 12A per Channel)**
- **Internal Boost Capacitors for Reduced PCB Space**
- **No Load I_Q 27µA 1 Buck Enabled; 42µA All Bucks Enabled**
- **1% V_{OUT} Accuracy on All Channels**
- **Peak Current Mode Control (Burst Mode® Operation/Forced Continuous)**
- Precision RUN Inputs, Individual PGOOD Outputs for Power Sequencing
- 1MHz to 3MHz Frequency (RT Programmable, PLL SYNC, or Internal 2MHz Oscillator)
- TEMP Pin Output Indicates Die Temperature
- Output Current Monitors
- Differential Output Sense

APPLICATIONS

- Telecom/Industrial
- 12V Distributed Power Systems

DESCRIPTION

The LTC®3376 is a highly flexible multioutput power supply IC. The device includes four synchronous buck converters, configured to share eight 1.5A power stages, powered from independent 3V to 20V inputs. The DC/DCs are assigned to one of fifteen power configurations via pin strappable CFG0 to CFG3 pins. The LTC3376 includes the integration of ceramic capacitors into the package for the BST pins thereby saving PCB space. The common buck switching frequency may be programmed with an external resistor, synchronized to an external oscillator, or set to a default internal 2MHz clock.

The operating mode for all DC/DCs may be programmed via the SYNC/MODE pin for Burst Mode or forced continuous mode operation. The PGOOD1 to PGOOD4 outputs indicate when each enabled DC/DC is within a specified percentage of its final output.

Current monitors allow for external monitoring of each buck's load. The $EXTV_{CC}$ pin allows for the internal circuitry to run from a 3V to 5.5V rail for improved efficiency.

Precision RUN pin thresholds facilitate power-up sequencing. The LTC3376 is available in a 64 lead 7mm × 7mm BGA (0.8mm ball pitch).

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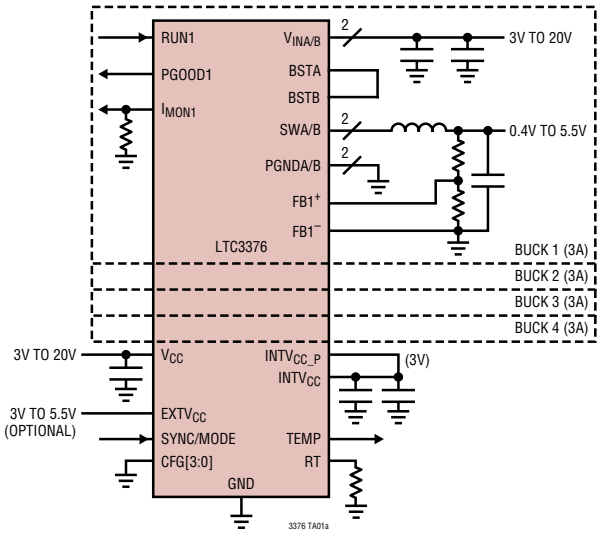
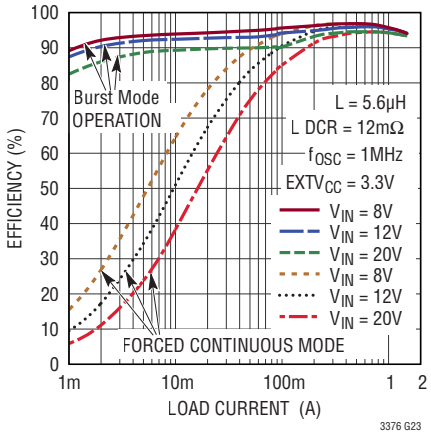
TYPICAL APPLICATION



1.5A Buck Efficiency vs I_{LOAD}, V_{OUT}=5V



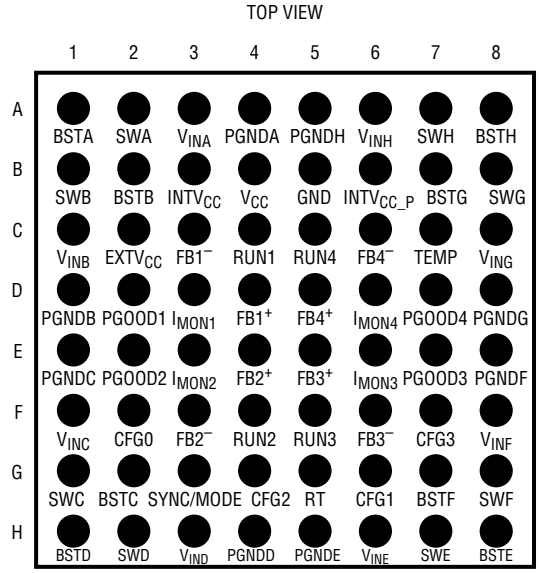
Rev 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC}, V_{INA-H} ..... –0.3V to 22V
FB1-4$^+$, RUN1-4, CFG1-3, EXTV_{CC}, PGOOD1-4, INTV_{CC}, INTV_{CC_P}, SYNC/MODE ..... –0.3V to 6V
CFG0, RT, TEMP, I_{MON1-4} ..... –0.3V to (INTV_{CC} + 0.3V)
INTV_{CC} – INTV_{CC_P} ..... –0.3V to 0.3V
FB1-4$^-$ ..... –0.3V to 0.3V
$I_{PGOOD1-4}$ 5mA
Operating Junction Temperature (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION



BGA PACKAGE
64-Lead (7.00mm × 7.00mm × 1.34mm)
T_{JMAX} = 125°C, θ_{JA} = 35°C/W, 0.8mm Ball Pitch

θ_{JCTOP} = 23°C/W, $\theta_{JCBOTTOM}$ = 16°C/W
θ Values Determined per JESD51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTC3376EY#PBF	SAC305 (RoHS)	LTC3376	e1	BGA	3	–40°C to 125°C
LTC3376IY#PBF		LTC3376				–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{INA-H} = 12V, RT tied to INTV_{CC}, V_{FB1-4^-} = 0V, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Voltage Range		●	3		20	V
I_{VCC}	V_{CC} Input Supply Current, EXTV_{CC} = 0V	All Bucks in Shutdown 1 Buck on, Sleeping, $V_{FB}$$^+$ = 0.41V Each Additional Buck, Sleeping 1 Buck on (Configured to 1 Power Stage), SYNC/MODE = INTV_{CC} (Note 3)			9 61 17 4.5	15 90 30	µA µA µA mA
	V_{CC} Input Supply Current, EXTV_{CC} = 3.3V	At Least One Buck On			7	12	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{INA-H} = 12V, RT tied to $INTV_{CC}$, V_{FB1-4^-} = 0V, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Total System Current Bootstrapped	1 Buck on, Sleeping, V_{FB}^+ = 0.41V (Note 4) 2 Bucks on, Sleeping, V_{FB}^+ = 0.41V (Note 4) All Bucks on (Note 4)			27 32 42		µA µA µA
	$EXTV_{CC}$ Input Supply Current, $EXTV_{CC}$ = 3.3V	1 Buck on, Sleep, V_{FB}^+ = 0.41V Each Additional Buck, Sleep 1 Buck on (Configured to 1 Power Stage), SYNC/MODE = $INTV_{CC}$ (Note 3)			56 17 4.5	85 30	µA µA mA
	Undervoltage Threshold on $INTV_{CC}$	$INTV_{CC}$ Voltage Falling	●	2.55	2.6	2.65	V
	Undervoltage Hysteresis on $INTV_{CC}$				250		mV
f_{OSC}	Internal Oscillator Frequency	RT = $INTV_{CC}$, SYNC/MODE = 0V RT = 402k, SYNC/MODE = 0V	● ●	1.84 1.84	2 2	2.16 2.16	MHz MHz
	Synchronization Frequency		●	1		3	MHz
External Low Voltage Supply (If Used)							
$EXTV_{CC}$	Optional External Supply Range		●	3		5.5	V
	Undervoltage Threshold on $EXTV_{CC}$	$EXTV_{CC}$ Voltage Falling	●	2.8	2.85	2.95	V
	Undervoltage Hysteresis on $EXTV_{CC}$				75		mV
1.5A Buck Regulators							
V_{IN}	Buck Input Voltage Range		●	3		20	V
	Undervoltage Threshold on V_{IN}	V_{IN} Voltage Falling Hysteresis	●	2.5	2.6 0.2	2.7	V V
	V_{INA-H} Input Supply Current, V_{INA-H} = 12V	All Bucks Off V_{INB}, V_{INC}, V_{INF}, V_{ING} V_{INA}, V_{IND}, V_{INE}, V_{INH}			 0.7 0	 1.4	 µA µA
		Buck On, Sleeping, V_{FB}^+ = 0.41V V_{INB}, V_{INC}, V_{INF}, V_{ING} V_{INA}, V_{IND}, V_{INE}, V_{INH}			 0.7 0	 1.4	 µA µA
		Buck On, SYNC/MODE=$INTV_{CC}$			5.2		mA
	Top Switch Current Limit, Duty < 18%	(Note 5)		2.3	2.62	3.0	A
V_{FB}^+	Feedback Regulation Voltage		●	396	400	404	mV
I_{FB}^+	Feedback Leakage Current	V_{FB}^+ = 0.41V		–30		30	nA
	Minimum Off-Time				90	140	ns
	Minimum On-Time		●		53	85	ns
	Top Switch Power FET On-Resistance				170		mΩ
	Bottom Switch Power FET On-Resistance				90		mΩ
	Top Switch Power FET Leakage	V_{INA-H} = 20V, SWA-H = 0V				0.1	µA
	Bottom Switch Power FET Leakage	V_{INA-H} = SWA-H = 20V			0.003	1	µA
	SW Pull-Down Resistance in Shutdown	RUN1-4 = 0V per Output Channel			1		kΩ
t_{SS}	Soft-Start Time	(Note 6)	●	0.3	1	2.5	ms
	Start-Up Delay Time	Starting Up from All EN's Low When at Least One EN Is Already High		100 40	250 100	500 250	µs µs
	PGOOD Lower Threshold	V_{FB}^+ Falling, Percentage of Regulated V_{FB}^+	●	95	96.75	98.5	%
	PGOOD Lower Threshold Hysteresis				1		%
	PGOOD Upper Threshold	V_{FB}^+ Rising, Percentage of Regulated V_{FB}^+	●	104.5	107.5	110.5	%
	PGOOD Upper Threshold Hysteresis				2.5		%
	PGOOD Filtering Time				100		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{INA-H} = 12V, RT tied to $INTV_{CC}$, V_{FB1-4^-} = 0V, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Regulators Combined							
	Top Switch Current Limit, Duty < 18%	1 Buck with 2 Power Stages Combined (Note 5)			5.25		A
		1 Buck with 3 Power Stages Combined (Note 5)			7.88		A
		1 Buck with 4 Power Stages Combined (Note 5)			10.5		A
		1 Buck with 5 Power Stages Combined (Note 5)			13.1		A
		1 Buck with 6 Power Stages Combined (Note 5)			15.8		A
		1 Buck with 7 Power Stages Combined (Note 5)			18.4		A
		1 Buck with 8 Power Stages Combined (Note 5)			21		A
Temperature Monitor							
$V_{TEMP(ROOM)}$	TEMP Voltage at 25°C			220	250	280	mV
$\Delta V_{TEMP/°C}$	V_{TEMP} Slope				10		mV/°C
OT	Overtemperature Shutdown (Note 7)	Temperature Rising			165		°C
	Overtemperature Hysteresis				10		°C
Current Monitors							
	I_{MON1-4} Voltage at 1.5A Load	R_{IMON} = 10k, Duty Cycle = 25%		0.9	1	1.1	V
	I_{MON1-4} Voltage at No Load	SYNC/MODE = $INTV_{CC}$			0		V
	I_{MON1-4} Slope	R_{IMON} = 10k			0.667		V/A
Interface Logic Pins (CFG0-3, SYNC/MODE, PGOOD1-4)							
I_{OH}	Output High Leakage Current	PGOOD1-4 at 5.5V				1	µA
V_{OL}	Output Low Voltage	PGOOD1-4, 3mA into Pin			0.03	0.4	V
V_{IH}	Input High Threshold	CFG0-3, SYNC/MODE	●	1.2			V
V_{IL}	Input Low Threshold	CFG0-3, SYNC/MODE	●			0.4	V
I_{IH}, I_{IL}	Input High, Low Leakage Current	CFG0-3 Pins at $INTV_{CC}$ & 0V SYNC/MODE Pin at 5.5V & 0V				1 1	µA µA
Interface Logic Pins (RUN1-4)							
	RUN Rising Threshold	First Regulator Turning On One Regulator or More Already in Use	● ●	350 280	730 300	1200 320	mV mV
	RUN Falling Threshold RUN Falling Threshold	Last Regulator Turning Off One Regulator or More Kept On	 ●	 180	690 200	 220	mV mV
	RUN Pin Leakage Current	RUN1-4 = 5.5V				1	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3376 is tested under pulsed load conditions such that $T_J \sim T_A$. The LTC3376E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3376I is guaranteed over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: There will be additional switching current on V_{INA-H} pins.

Note 4: Total System current is defined as total current from $V_{CC} + V_{INA-H}$ when all bucks are on (in Sleep), $V_{CC} = V_{INA-H} = 12V$, and $EXTV_{CC}$ is boot-strapped to run off of a 3.3V buck.

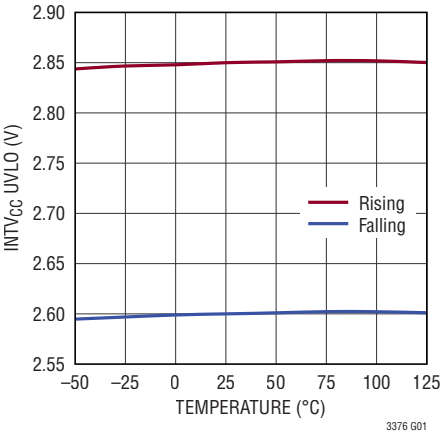
Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the specified maximum pin current rating may result in device degradation over time.

Note 6: The Soft-Start Time is the time from the start of switching until $V_{FB}^+ – V_{FB}^–$ reaches 360mV.

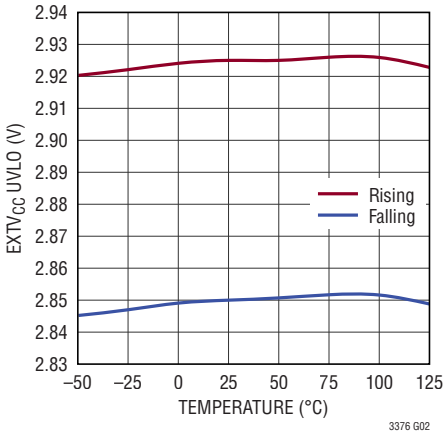
Note 7: The LTC3376 includes overtemperature protection which protects the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

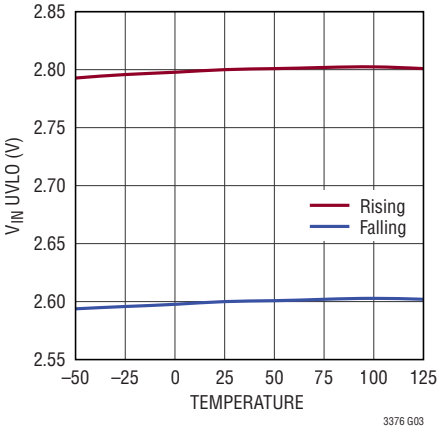
$INTV_{CC}$ Undervoltage Threshold vs Temperature



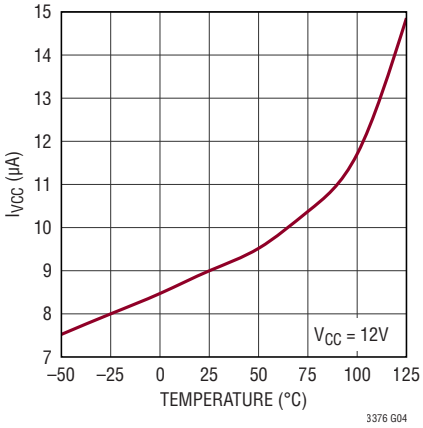
$EXTV_{CC}$ Undervoltage Threshold vs Temperature



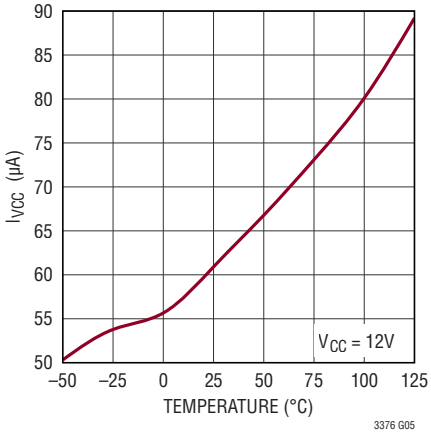
V_{IN} Undervoltage Threshold vs Temperature



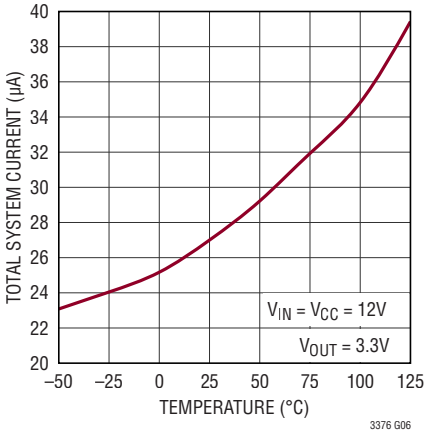
V_{CC} Current vs Temperature with All Bucks in Shutdown



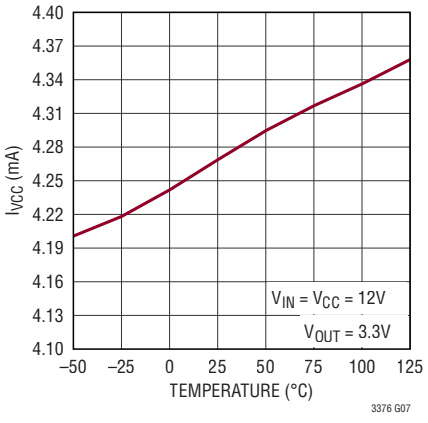
V_{CC} Current vs Temperature with One Buck On (Sleeping, Not Bootstrapped)



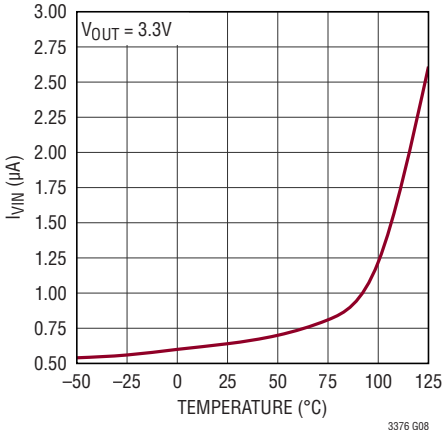
Total System Current vs Temperature with One Buck On (Sleeping, Bootstrapped)



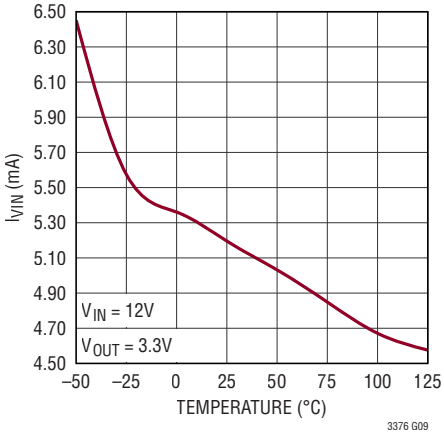
V_{CC} Current vs Temperature with One Buck On (Forced Continuous Mode, One Power Stage)



V_{IN} Current vs Temperature (Sleeping)

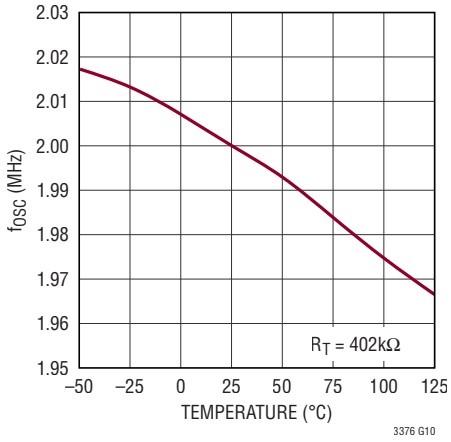


V_{IN} Current vs Temperature (Forced Continuous Mode, One Power Stage)

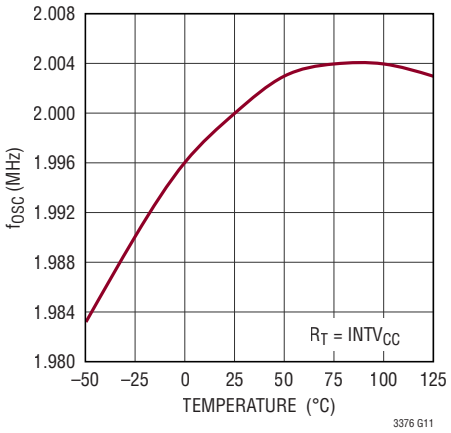


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

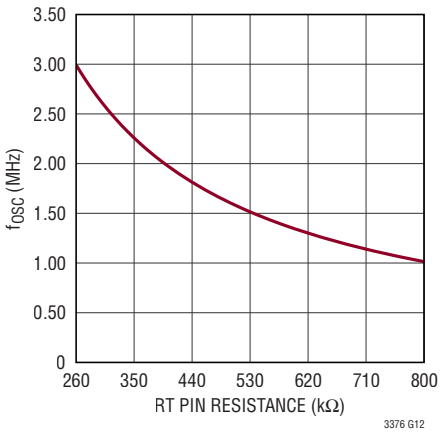
RT-Programmed Oscillator Frequency vs Temperature



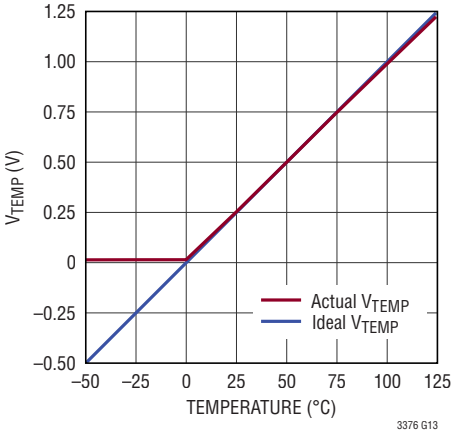
Default Oscillator Frequency vs Temperature



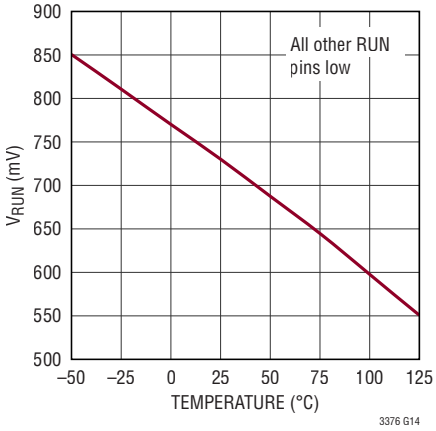
Oscillator Frequency vs R_T



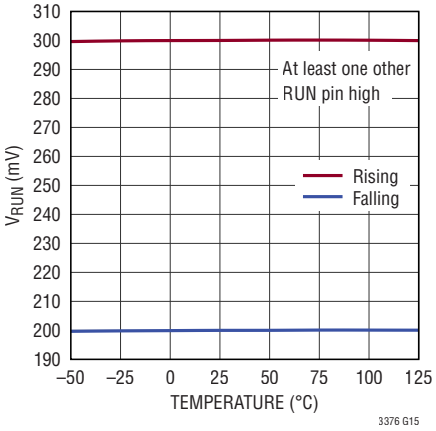
V_{TEMP} vs Temperature



RUN Pin Rising Threshold vs Temperature

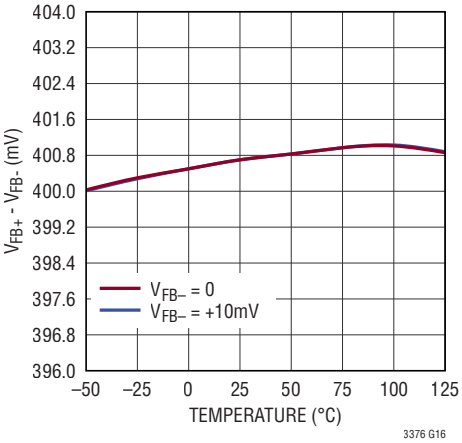


RUN Pin Threshold vs Temperature

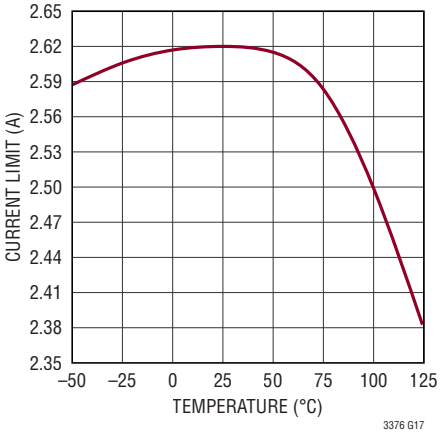


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

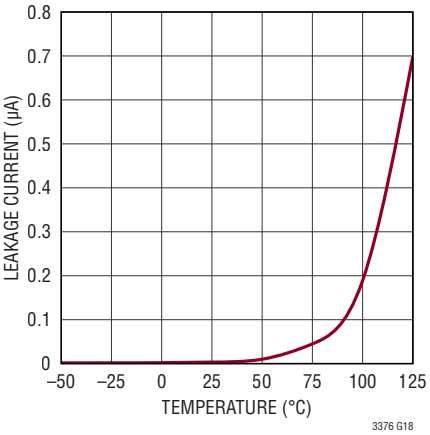
$V_{FB}^+ – V_{FB}^-$ vs Temperature



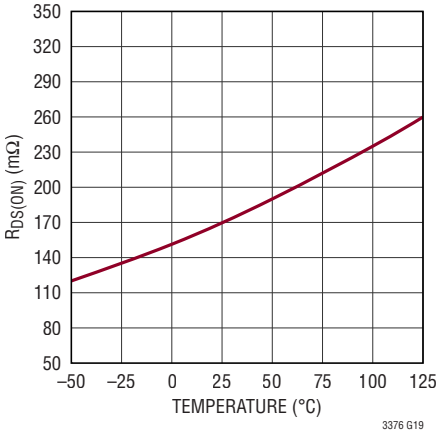
Top Switch Current Limit vs Temperature



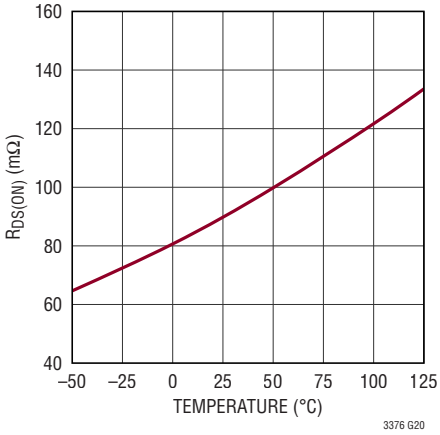
Top Switch Leakage vs Temperature



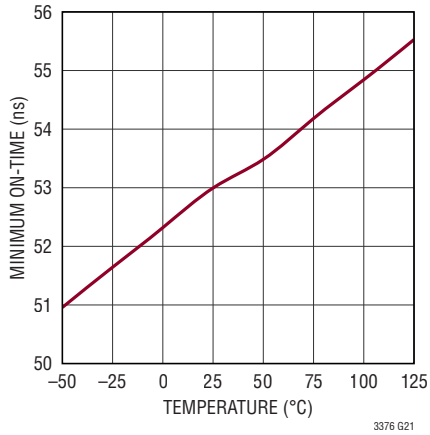
Top Switch $R_{DS(ON)}$ vs Temperature



Bottom Switch $R_{DS(ON)}$ vs Temperature

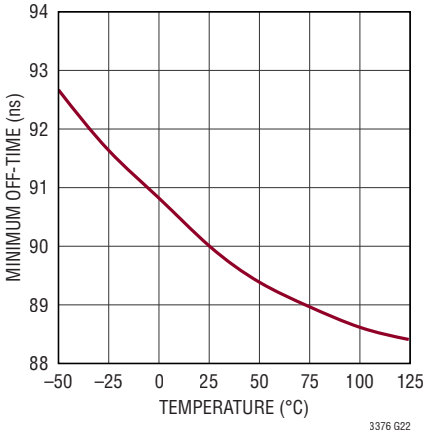


Minimum On-Time vs Temperature

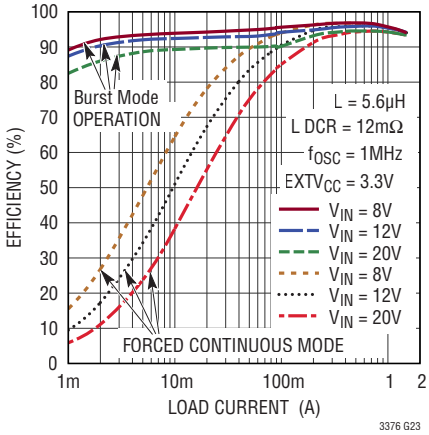


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

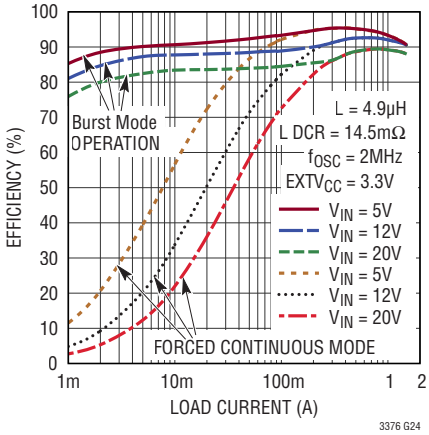
Minimum Off-Time vs Temperature



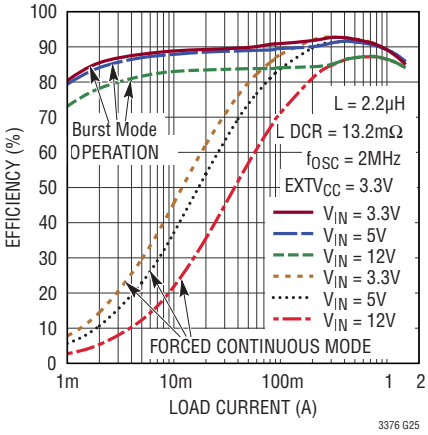
1.5A Buck Efficiency vs I_{LOAD}, V_{OUT}=5V



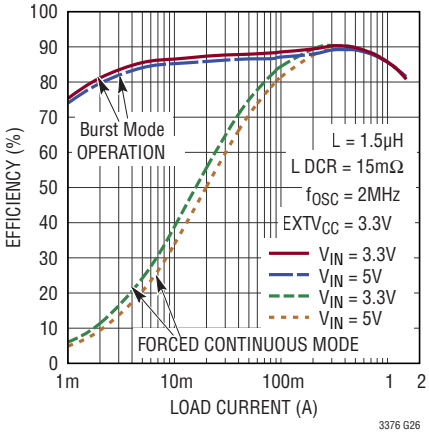
1.5A Buck Efficiency vs I_{LOAD}, V_{OUT}=3.3V



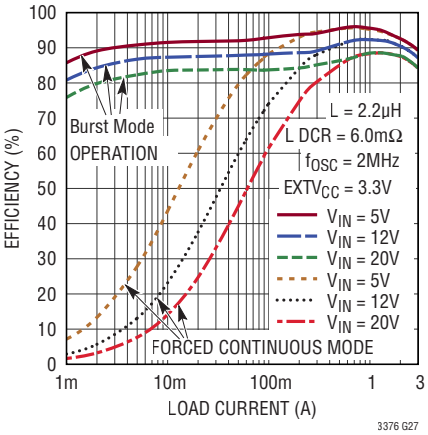
1.5A Buck Efficiency vs I_{LOAD}, V_{OUT}=1.8V



1.5A Buck Efficiency vs I_{LOAD}, V_{OUT}=1.2V

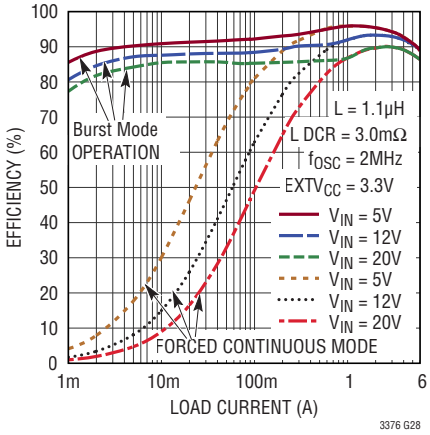


3A Buck Efficiency vs I_{LOAD}, V_{OUT}=3.3V

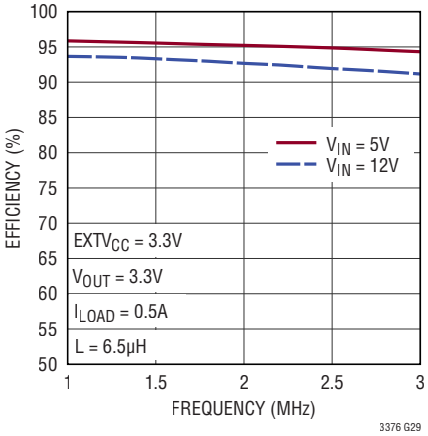


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

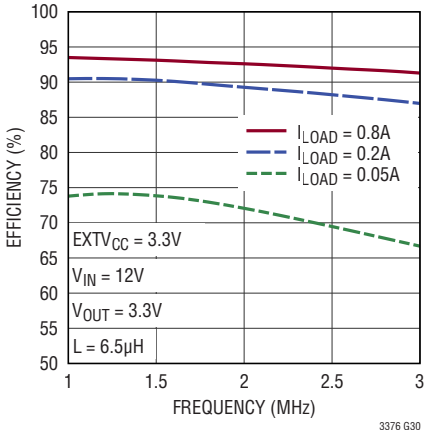
6A Buck Efficiency vs I_{LOAD}, V_{OUT}=3.3V



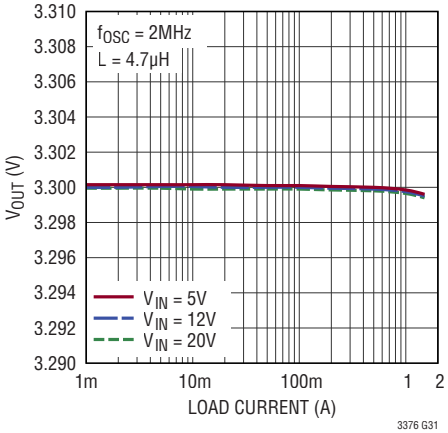
1.5A Buck Efficiency vs Frequency (Forced Continuous Mode)



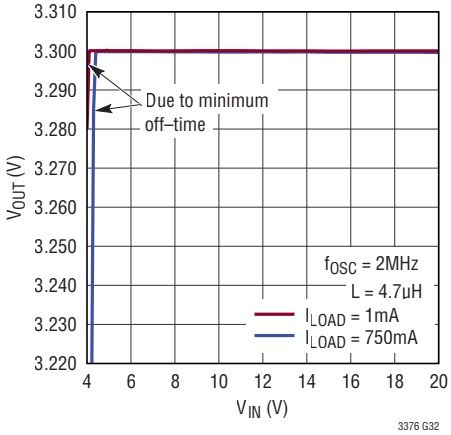
1.5A Buck Efficiency vs Frequency (Forced Continuous Mode)



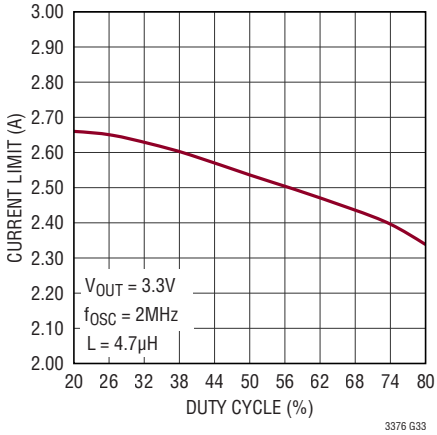
1.5A Buck Regulator Load Regulation (Forced Continuous Mode)



1.5A Buck Regulator Line Regulation (Forced Continuous Mode)

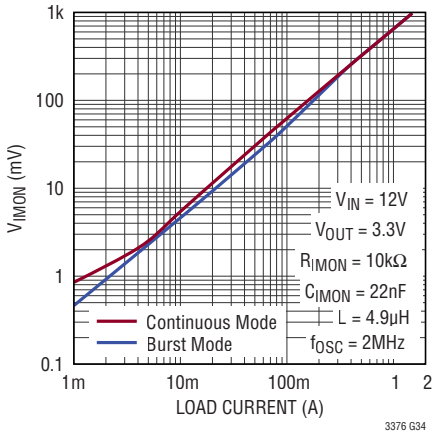


1.5 Buck Current Limit vs Duty Cycle

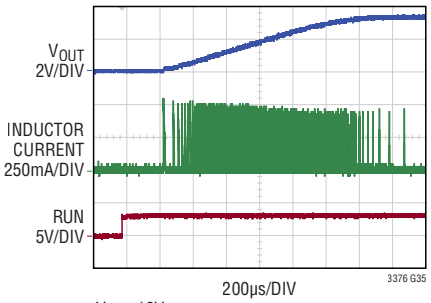


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

I_{MON} Voltage vs I_{LOAD}

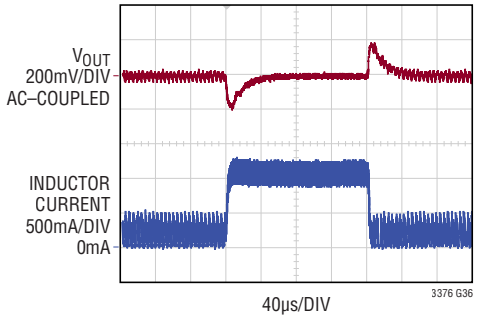


1.5A Buck Regulator No Load Start-Up Transient



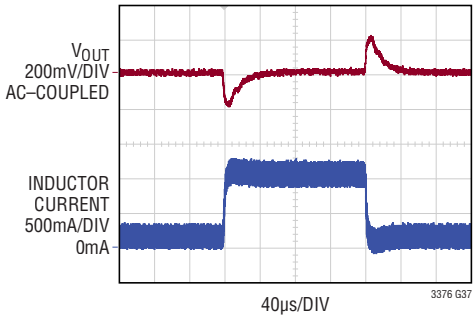
V_{IN} = 12V
V_{OUT} = 3.3V
L = 4.7µH

1.5A Buck Regulator, Transient Response (Burst Mode Operation)



LOAD STEP: 150mA to 1.05A
V_{IN} = 12V L = 4.7µH
V_{OUT} = 5V f_{OSC} = 2MHz
C_{OUT} = 22µF

1.5A Buck Regulator, Transient Response (Forced Continuous Mode)



LOAD STEP: 150mA to 1.05A
V_{IN} = 12V L = 4.7µH
V_{OUT} = 5V f_{OSC} = 2MHz
C_{OUT} = 22µF

PIN FUNCTIONS

BSTA (Pin A1): Boost Node for Power Stage A.

BSTB (Pin B2): Boost Node for Power Stage B.

BSTC (Pin G2): Boost Node for Power Stage C.

BSTD (Pin H1): Boost Node for Power Stage D.

BSTE (Pin H8): Boost Node for Power Stage E.

BSTF (Pin G7): Boost Node for Power Stage F.

BSTG (Pin B7): Boost Node for Power Stage G.

BSTH (Pin A8): Boost Node for Power Stage H.

CFG0 (Pin F2): Configuration Input Bit. With CFG1, CFG2 and CFG3, CFG0 configures the Buck output current power stage combinations. CFG0 should be tied to either $INTV_{CC}$ or GND. Do not float.

CFG1 (Pin G6): Configuration Input Bit. With CFG0, CFG2, and CFG3, CFG1 configures the Buck output current power stage combinations. CFG1 should be tied to either $INTV_{CC}$ or GND. Do not float.

CFG2 (Pin G4): Configuration Input Bit. With CFG0, CFG1, and CFG3, CFG2 configures the Buck output current power stage combinations. CFG2 should be tied to either $INTV_{CC}$ or GND. Do not float.

CFG3 (Pin F7): Configuration Input Bit. With CFG0, CFG1 and CFG2, CFG3 configures the Buck output current power stage combinations. CFG3 should be tied to either $INTV_{CC}$ or GND. Do not float.

$EXTV_{CC}$ (Pin C2): External V_{CC} Low Voltage Supply. The internal LDO regulator draws current from $EXTV_{CC}$ instead of from V_{CC} when $EXTV_{CC}$ is tied to a voltage higher than 3V. For output voltages of 3.3V and above this pin can be tied to that V_{OUT}. If this pin is tied to a supply other than a buck output, use a 4.7µF local bypass capacitor on this pin. $EXTV_{CC}$ should be tied to ground if not used. Do not float.

$FB1^+$ (Pin D4): Positive Feedback Pin for Buck Regulator 1. Receives feedback by a resistor divider connected across the output.

$FB2^+$ (Pin E4): Positive Feedback Pin for Buck Regulator 2. Receives feedback by a resistor divider connected across the output.

$FB3^+$ (Pin E5): Positive Feedback Pin for Buck Regulator 3. Receives feedback by a resistor divider connected across the output.

$FB4^+$ (Pin D5): Positive Feedback Pin for Buck Regulator 4. Receives feedback by a resistor divider connected across the output.

$FB1^-$ (Pin C3): Negative Feedback Pin for Buck Regulator 1. Connect directly to the GND side of the feedback resistor divider that connects across the output.

$FB2^-$ (Pin F3): Negative Feedback Pin for Buck Regulator 2. Connect directly to the GND side of the feedback resistor divider that connects across the output.

$FB3^-$ (Pin F6): Negative Feedback Pin for Buck Regulator 3. Connect directly to the GND side of the feedback resistor divider that connects across the output.

$FB4^-$ (Pin C6): Negative Feedback Pin for Buck Regulator 4. Connect directly to the GND side of the feedback resistor divider that connects across the output.

GND (Pin B5): LTC3376 Ground Pin. Connect this pin to system ground and to the ground plane. Do not float.

I_{MON1} (Pin D3): Current Monitor Pin for Buck Regulator 1. I_{MON1} outputs a current of 100µA (typical) at 1.5A load current for each power stage configured. Connect a resistor from I_{MON1} to GND. The value of this resistor should be chosen so that I_{MON1} is 1V at full load (1.5A per power stage). The I_{MON1} voltage will decrease by 0.67V/A at lower load currents. The I_{MON1} output current will be 0 when the regulator is sleeping in Burst Mode or is disabled.

I_{MON2} (Pin E3): Current Monitor Pin for Buck Regulator 2. I_{MON2} outputs a current of 100µA (typical) at 1.5A load current for each power stage configured. Connect a resistor from I_{MON2} to GND. The value of this resistor should be chosen so that I_{MON2} is 1V at full load (1.5A per power stage). The I_{MON2} voltage will decrease by 0.67V/A at lower load currents. The I_{MON2} output current will be 0 when the regulator is sleeping in Burst Mode or is disabled.

PIN FUNCTIONS

I_{MON3} (Pin E6): Current Monitor Pin for Buck Regulator 3. I_{MON3} outputs a current of 100µA (typical) at 1.5A load current for each power stage configured. Connect a resistor from I_{MON3} to GND. The value of this resistor should be chosen so that I_{MON3} is 1V at full load (1.5A per power stage). The I_{MON3} voltage will decrease by 0.67V/A at lower load currents. The I_{MON3} output current will be 0 when the regulator is sleeping in Burst Mode or is disabled.

I_{MON4} (Pin D6): Current Monitor Pin for Buck Regulator 4. I_{MON4} outputs a current of 100µA (typical) at 1.5A load current for each power stage configured. Connect a resistor from I_{MON4} to GND. The value of this resistor should be chosen so that I_{MON4} is 1V at full load (1.5A per power stage). The I_{MON4} voltage will decrease by 0.67V/A at lower load currents. The I_{MON4} output current will be 0 when the regulator is sleeping in Burst Mode or is disabled.

$INTV_{CC}$ (Pin B3): Internal 3V V_{CC} Regulator Bypass Pin. The control circuits are powered from this voltage. Do not load the $INTV_{CC}$ pin with external circuitry exceeding 2mA. If overloaded the LTC3376 will shut down. $INTV_{CC}$ current is supplied from $EXTV_{CC}$ if V_{EXTVCC} > 3V, otherwise current is drawn from V_{CC}. Bypass to GND with a single 4.7µF or larger low ESR ceramic capacitor.

$INTV_{CC_P}$ (Pin B6): Internal V_{CC} Power Stage Supply. The internal power drivers are powered from this voltage. The $INTV_{CC_P}$ pin is for internal use only. Bypass to GND with a single 10µF or larger low ESR ceramic capacitor. In all applications, $INTV_{CC_P}$ must connect to $INTV_{CC}$.

PGNDA (Pin A4): Ground Supply for Power Stage A. Connect the GND side of the V_{INA} bypass capacitors directly to this pin and then to the ground plane.

PGNDB (Pin D1): Ground Supply for Power Stage B. Connect the GND side of the V_{INB} bypass capacitors directly to this pin and then to the ground plane.

PGNDC (Pin E1): Ground Supply for Power Stage C. Connect the GND side of the V_{INC} bypass capacitors directly to this pin and then to the ground plane.

PGNDD (Pin H4): Ground Supply for Power Stage D. Connect the GND side of the V_{IND} bypass capacitors directly to this pin and then to the ground plane.

PGNDE (Pin H5): Ground Supply for Power Stage E. Connect the GND side of the V_{INE} bypass capacitors directly to this pin and then to the ground plane.

PGNDF (Pin E8): Ground Supply for Power Stage F. Connect the GND side of the V_{INF} bypass capacitors directly to this pin and then to the ground plane.

PGNDG (Pin D8): Ground Supply for Power Stage G. Connect the GND side of the V_{ING} bypass capacitors directly to this pin and then to the ground plane.

PGNDH (Pin A5): Ground Supply for Power Stage H. Connect the GND side of the V_{INH} bypass capacitors directly to this pin and then to the ground plane.

PGOOD1 (Pin D2): Power Good Pin for Buck Regulator 1 (Active High). Open-drain output. This pin is driven low when Buck 1's regulated output voltage falls below its PGOOD threshold or rises above its overvoltage threshold. PGOOD1 is also pulled low in the following scenarios: if the buck is disabled, if the buck is going through soft-start, if $INTV_{CC}$ is below the UVLO threshold, or if the LTC3376 is in OT.

PGOOD2 (Pin E2): Power Good Pin for Buck Regulator 2 (Active High). Open-drain output. This pin is driven low when Buck 2's regulated output voltage falls below its PGOOD threshold or rises above its overvoltage threshold. PGOOD2 is also pulled low in the following scenarios: if the buck is disabled, if the buck is going through soft-start, if $INTV_{CC}$ is below the UVLO threshold, or if the LTC3376 is in OT.

PGOOD3 (Pin E7): Power Good Pin for Buck Regulator 3 (Active High). Open-drain output. This pin is driven low when Buck 3's regulated output voltage falls below its PGOOD threshold or rises above its overvoltage threshold. PGOOD3 is also pulled low in the following scenarios: if the buck is disabled, if the buck is going through soft-start, if $INTV_{CC}$ is below the UVLO threshold, or if the LTC3376 is in OT.

PIN FUNCTIONS

PGOOD4 (Pin D7): Power Good Pin for Buck Regulator 4 (Active High). Open-drain output. This pin is driven low when Buck 4's regulated output voltage falls below its PGOOD threshold or rises above its overvoltage threshold. PGOOD4 is also pulled low in the following scenarios: if the buck is disabled, if the buck is going through soft-start, if $INTV_{CC}$ is below the UVLO threshold, or if the LTC3376 is in OT.

RT (Pin G5): Timing Resistor Pin for Setting Oscillator Frequency. This pin provides two modes of setting the switching frequency when not synchronizing to an external clock. Connecting a resistor from RT to GND sets the switching frequency based on the resistor value. If RT is tied to $INTV_{CC}$ the default internal 2MHz oscillator is used. Do not float.

RUN1 (Pin C4): Enable Input for Buck Regulator 1. Active high. Do not float.

RUN2 (Pin F4): Enable Input for Buck Regulator 2. Active high. In configurations where the Enable Input for Buck 2 is not used, tie RUN2 to GND. Do not float.

RUN3 (Pin F5): Enable Input for Buck Regulator 3. Active high. In configurations where the Enable Input for Buck 3 is not used, tie RUN3 to GND. Do not float.

RUN4 (Pin C5): Enable Input for Buck Regulator 4. Active high. In configurations where the Enable Input for Buck 4 is not used, tie RUN4 to GND. Do not float.

SWA (Pin A2): Switch Node for Power Stage A. External inductor connects to this pin.

SWB (Pin B1): Switch Node for Power Stage B. External inductor connects to this pin.

SWC (Pin G1): Switch Node for Power Stage C. External inductor connects to this pin.

SWD (Pin H2): Switch Node for Power Stage D. External inductor connects to this pin.

SWE (Pin H7): Switch Node for Power Stage E. External inductor connects to this pin.

SWF (Pin G8): Switch Node for Power Stage F. External inductor connects to this pin.

SWG (Pin B8): Switch Node for Power Stage G. External inductor connects to this pin.

SWH (Pin A7): Switch Node for Power Stage H. External inductor connects to this pin.

SYNC/MODE (Pin G3): Oscillator Synchronization and Mode Select Pin. Driving SYNC/MODE with an external clock signal synchronizes all switches to the applied frequency, and configures the buck converters to operate in forced continuous mode. Slope compensation automatically adapts to the external clock frequency. The absence of an external clock signal enables the frequency to be programmed by the RT pin. When not synchronizing to an external clock this input determines how the LTC3376 operates at light loads. Connecting this pin to ground selects Burst Mode operation. Connecting this pin to $INTV_{CC}$ selects forced continuous mode operation. Do not float.

TEMP (Pin C7): Temperature Indication Pin. TEMP outputs a voltage of 250mV (typical) at 25°C. The TEMP voltage changes by 10mV/°C (typical) giving an external indication of the LTC3376 internal die temperature.

V_{CC} (Pin B4): Internal Bias Supply. Bypass to GND with a 4.7µF or larger ceramic capacitor. V_{CC} has to be present even when the $EXTV_{CC}$ pin is used and must come up before $EXTV_{CC}$.

V_{INA} (Pin A3): Input Supply for Power Stage A. Bypass to PGNDA with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

V_{INB} (Pin C1): Input Supply for Power Stage B. Bypass to PGNDB with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

V_{INC} (Pin F1): Input Supply for Power Stage C. Bypass to PGNDC with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

PIN FUNCTIONS

V_{IND} (Pin H3): Input Supply for Power Stage D. Bypass to PGNDD with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

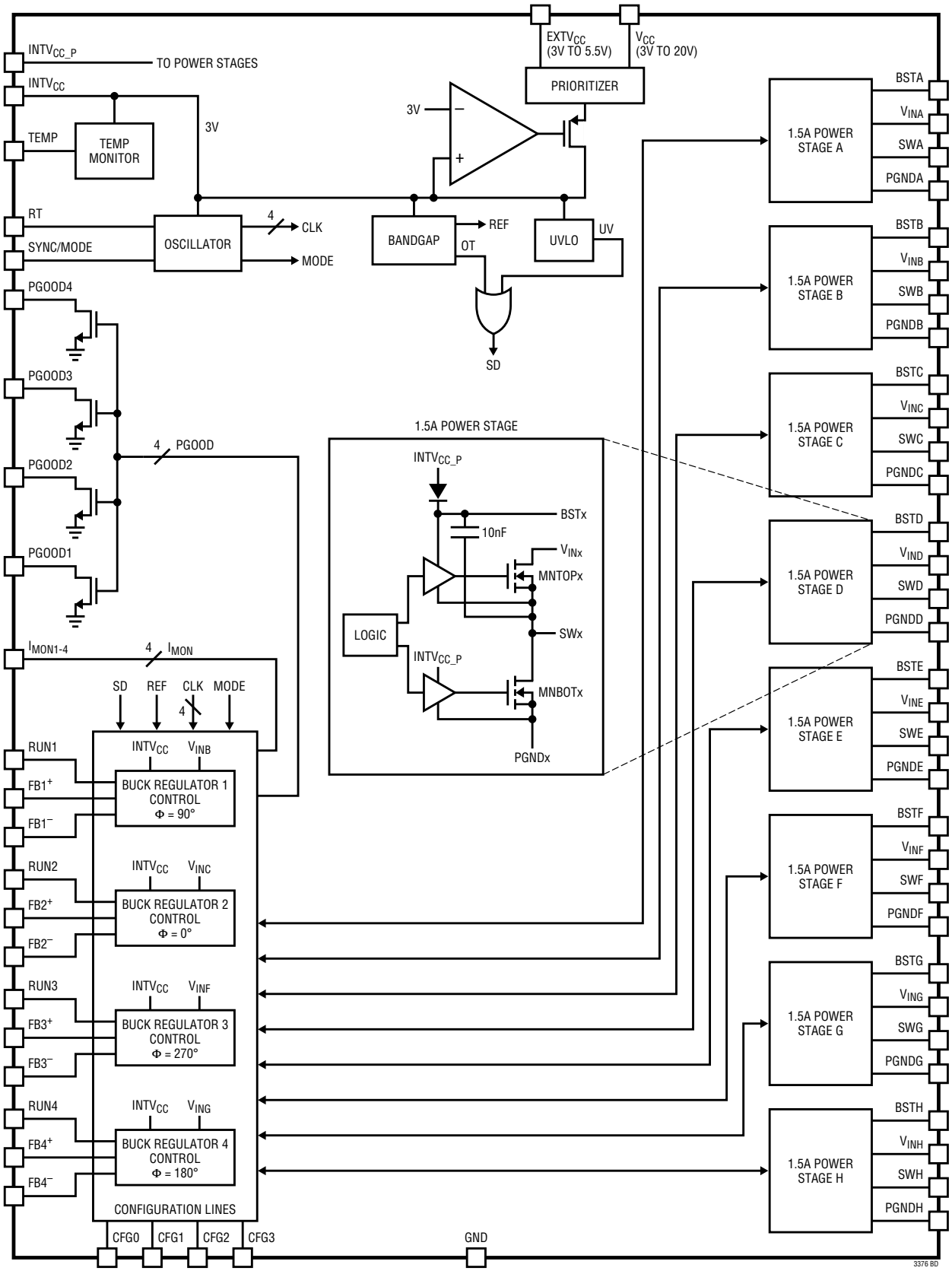
V_{INE} (Pin H6): Input Supply for Power Stage E. Bypass to PGNDE with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

V_{INF} (Pin F8): Input Supply for Power Stage F. Bypass to PGNDF with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

V_{ING} (Pin C8): Input Supply for Power Stage G. Bypass to PGNDG with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

V_{INH} (Pin A6): Input Supply for Power Stage H. Bypass to PGNDH with a 1µF ceramic capacitor and 10µF or larger ceramic capacitor.

BLOCK DIAGRAM



OPERATION

Buck Switching Regulators

The LTC3376 is a 20V monolithic, constant frequency, four channel, 12A configurable, peak current mode step-down DC/DC converter. The device includes four synchronous buck converters, configured to share eight 1.5A power stages. The LTC3376 includes the integration of ceramic capacitors into the package for all BST pins. These capacitors reduce PC board space by eliminating the need for external BST capacitors.

The buck switching regulators are internally compensated and require external feedback resistors to set the output voltage. An internal oscillator, which can be synchronized to an external oscillator, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor ramps up until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by an internal V_C voltage which the error amplifier regulates by comparing the voltage on the feedback pin with an internal 400mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference causing the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the bottom power switch turns on until the next clock cycle begins or, if in Burst Mode, until the inductor current falls to zero.

Each buck converter can operate at an independent V_{IN} voltage and has its own FB^+, FB^-, RUN, I_{MON}, and PGOOD pins to maximize flexibility. The RUN pins have two different enable threshold voltages that depend on the operating state of the LTC3376. The first buck regulator to turn on will have a RUN pin rising threshold of 730mV(typ). The last buck regulator to turn off will have a RUN pin falling threshold of 690mV(typ). If any one buck regulator is on, all other RUN pins will use the bandgap-based precision thresholds off 300mV(typ) rising and 200mV(typ) falling. The precision RUN thresholds may be used to provide event-based power-up sequencing by connecting the RUN pin to the output of another buck through a resistor divider. All buck regulators have forward and reverse-current limiting, short-circuit protection, and soft-start to limit inrush current during start-up. If the RUN pin of a buck is low, that buck is shut down to a low quiescent current state and the SW pin is pulled to PGND through a 1k resistor. If all buck regulators are off, most top level circuits are shut down, and the quiescent current of the LTC3376 is 9µA(typ). When a buck is enabled there is a 100µs(typ) delay before switching commences and the soft start ramp begins. If a buck is the first one to be enabled, then this delay is 250µs(typ).

The buck switching regulators are phased in 90° steps to reduce noise and input ripple. The phase step determines the fixed edge of the switching sequence, which is when the top switch turns on. The top switch off (bottom switch on) phase is subject to the duty cycle demanded by the regulator. Buck 2 is set to 0°. Buck 1 is set to 90°. Buck 4 is set to 180°. Buck 3 is set to 270°.

Buck Regulators with Combined Power Stages

Up to four buck regulators may be combined in a master-slave configuration in various combinations by setting the CFG0, CFG1, CFG2, and CFG3 pins. These configuration pins should either be tied to ground or tied to $INTV_{CC}$ in accordance with the desired configuration (Table 1). Any combined SW pins must be tied together, as must any of the combined V_{IN} and BST pins. The bucks have a common V_{IN} but each V_{IN} pin should have its own input bypass capacitors (see Applications Information). RUN1, $FB1^+$, $FB1^-$, I_{MON1}, and PGOOD1 are utilized by Buck 1. RUN2, $FB2^+$, $FB2^-$, I_{MON2}, and PGOOD2 are utilized by Buck 2. RUN3, $FB3^+$, $FB3^-$, I_{MON3}, and PGOOD3 are utilized by Buck 3. RUN4, $FB4^+$, $FB4^-$, I_{MON4}, and PGOOD4 are utilized by Buck 4. If a buck is not utilized in a particular configuration, then the RUN, FB^+, and FB^-, I_{MON}, PGOOD pins should be tied to GND. Its V_{IN}, SW, and BST pins will be used as a slave to another master and must be connected to that master's respective power pins.

Buck regulators can be combined to provide 3A, 4.5A, 6A, 7.5A, 9A, 10.5A, or 12A of output load current. For example, code 0110 (CFG[3:0]) configures Buck 1 to operate as a 4.5A regulator through V_{IN}/SW/BST pairs A, B, and H, while Buck 2 is disabled, Buck 3 operates as a 6A regulator through V_{IN}/SW/BST pairs C, D, E, and F, and Buck 4 operates as a 1.5A regulator through V_{IN}/SW/BST pair G.

OPERATION

Table 1. Master-Slave Program Combinations (Each Letter Corresponds to a V_{IN}/SW/BST/PGND Pair)

				OUTPUT CONFIGURATION			
CFG3	CFG2	CFG1	CFG0	BUCK 1	BUCK 2	BUCK 3	BUCK 4
0	0	0	0	AB	CD	EF	GH
0	0	0	1	ABH	CD	EF	G
0	0	1	0	ABH	CDE	F	G
0	0	1	1	ABDH	C	EF	G
0	1	0	0	AB	CDE	-	FGH
0	1	0	1	ABCD	-	EF	GH
0	1	1	0	ABH	-	CDEF	G
0	1	1	1	ABCD	-	-	EFGH
1	0	0	0	ABDEH	C	F	G
1	0	0	1	ABCDH	-	EF	G
1	0	1	0	ABCDE	-	-	FGH
1	0	1	1	ABCDEH	-	F	G
1	1	0	0	ABCDEF	-	-	GH
1	1	0	1	ABCDEFH	-	-	G
1	1	1	0	ABCDEFGH	-	-	-
1	1	1	1	AB	CD	EF	GH

Mode Selection

The buck switching regulators can operate in two different modes set by the SYNC/MODE pin: Burst Mode (when the SYNC/MODE pin is set low) and forced continuous PWM mode (when the SYNC/MODE pin is set high). The SYNC/MODE pin sets the same operating mode for all buck switching regulators.

In forced continuous mode, the oscillator runs continuously and the buck switch currents are allowed to reverse under light load conditions to maintain regulation. This mode allows the buck to run at a fixed frequency with minimal output ripple, even with zero output load.

In Burst Mode operation, at light loads the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping conserve input power. When the output capacitor drops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst only at light loads. At higher loads it will operate in constant frequency PWM mode.

Synchronizing the Oscillator to an External Clock

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values and improves transient response. Operation at lower frequencies improves efficiency by reducing internal gate charge losses and allows more extreme V_{IN} to V_{OUT} ratios. However, this also requires larger inductance values and/or capacitance to maintain low output voltage ripple. The LTC3376 has a default operating frequency of 2MHz.

The LTC3376's internal oscillator can alternatively be synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the top power device turn-on of buck 2 is locked to 110ns after the rising edge of the external frequency source. Buck 1 will be 90° out of phase with Buck 2. Buck 4 will be 180° out of phase with Buck 2. Buck 3 will be 270° out of phase with Buck 2. When synchronizing to an external clock, the buck regulators operate in forced continuous mode. The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the first rising edge of the SYNC pin, the internal PLL starts at the default frequency. The internal PLL then requires up to 1ms to gradually adjust its operating frequency to match the frequency and phase of the SYNC signal.

When the external clock is removed the LTC3376 will detect the absence of the external clock, and the oscillator gradually adjusts its operating frequency back to the default.

Power Failure Reporting Via PGOOD Pins

Power failure conditions are reported back by each buck's associated PGOOD pin. Each buck switching regulator has an internal power good (PGOOD_INT) signal. When the regulated output voltage of an enabled switcher rises above 97.75% of its regulation output voltage the PGOOD_INT signal transitions high. If the regulated output voltage subsequently falls below 96.75%(typ) of the regulation

OPERATION

output voltage the PGOOD_INT signal is pulled low. If a buck is enabled, its PGOOD_INT signal must be high for its external PGOOD pin to be high. An enabled buck's internal PGOOD_INT signal must stay low for greater than 100µs(typ) before its external PGOOD pin is pulled low, indicating to a microprocessor that a power failure fault has occurred. This 100µs filter time prevents the pin from being pulled low during a load transient. In addition, whenever the internal PGOOD_INT signal transitions high there will also be a 100µs assertion delay.

The LTC3376 also reports overvoltage conditions at the PGOOD pins. If an enabled buck regulator's output voltage rises above 107.5% (typ) of the regulation value, its PGOOD pin is pulled low after 100µs. Similarly, if an enabled output that is overvoltage subsequently falls below 105% (typ) of its regulated output voltage, its PGOOD pin transitions high again after 100µs.

An error condition that pulls the PGOOD pin low is not latched. When the error condition goes away, the PGOOD pin is released and is pulled high if no other error condition exists. PGOOD is also pulled low in the following scenarios: if the buck is disabled, if the buck is going through soft-start, if $INTV_{CC}$ is below the UVLO threshold, or if the LTC3376 is in OT (see below).

Current Monitors

Each buck regulator has a current monitor that supplies a current to the I_{MON} pin that is proportional to the average buck load current. The external resistor required from the I_{MON} pin to ground is a function of how many power stages are configured for a particular buck. If a buck regulator is configured to have only one power stage then a 10k resistor should be connected from I_{MON} to ground. At full load (1.5A) the voltage on the I_{MON} pin will be 1V (typical). At half load (0.75A) the voltage on the I_{MON} pin will be 0.5V. For combined output stages, the resistor required at the I_{MON} pin is given by:

$$R_{IMON} = \frac{10k\Omega}{[\#\ of\ channels]} \quad (1)$$

The I_{MON} pin voltage represents the average buck load and will take a few 100µs to settle. The current monitor is designed to be most accurate in continuous conduction mode but can function in Burst Mode at moderate loads with reduced accuracy if an external capacitor is applied to the I_{MON} pin. This capacitor should be selected such that the RC time constant is about 250µs or larger. The capacitor value to use on the I_{MON} pin (if desired) is given by:

$$C_{IMON} \geq \frac{250\mu s}{R_{IMON}} \quad (2)$$

Temperature Monitoring and Overtemperature Protection

To prevent thermal damage to the LTC3376 and its surrounding components, the LTC3376 incorporates an overtemperature (OT) function. When the LTC3376 die temperature reaches 165°C (typical) all enabled buck switching regulators are shut down and remain in shutdown until the die temperature falls to 155°C (typical).

The die temperature may be read by sampling the analog TEMP pin voltage. The temperature, T, indicated by the TEMP pin voltage is given by:

$$T = \frac{V_{TEMP}}{10mV} \bullet 1°C \quad (3)$$

where V_{TEMP} is the voltage on the TEMP pin.

The typical voltage at the TEMP pin is 250mV at 25°C. V_{TEMP} readings are valid for die temperatures higher than approximately 10°C. A bypass cap is not needed on the TEMP pin. If stray capacitance is present on the TEMP pin that is greater than 30pF, then a 15k resistor must be added in series at the pin to ensure the stability of the temperature monitor. If temperature monitoring functionality is not needed, the user may shut down the temperature monitor by tying TEMP to $INTV_{CC}$. This will reduce quiescent current by 5µA (typical). If none of the buck switching regulators are enabled, the temperature monitor is also shutdown to reduce quiescent current.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces a 3V supply from V_{CC} that powers the $INTV_{CC}$ pin and internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LTC3376's circuitry and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. The $INTV_{CC_P}$

OPERATION

pin powers all of the MOSFET gate drivers, must have its own 10µF bypass cap, and must be connected on the board to $INTV_{CC}$. Good bypassing is necessary to supply the high transient currents required by the power MOSFET drivers.

To improve efficiency the internal LDO can also draw current from the $EXTV_{CC}$ pin if the $EXTV_{CC}$ pin is 3V or higher. V_{CC} has to be present even if $EXTV_{CC}$ is used. Typically the $EXTV_{CC}$ pin can be tied to an output of one of the LTC3376 bucks, or it can be tied to an external supply of 3V or above. If $EXTV_{CC}$ is connected to a supply other than a buck output, be sure to bypass it with a local ceramic capacitor. If the $EXTV_{CC}$ pin is below 2.8V, the internal LDO will consume current from V_{CC}. Applications with high input voltage and high switching frequency in which the LDO pulls current from V_{CC} will increase die temperature because of the higher power dissipation in the LDO. Do not load the $INTV_{CC}$ pin with external circuitry exceeding 2mA.

APPLICATIONS INFORMATION

Buck Switching Regulator Output Voltage and Feedback Network

The output voltage of each buck switching regulator is programmed by a resistor divider across the switching regulator's output connecting to its feedback pin and is given by $V_{OUT} = V_{FB}^{+}(1 + R2/R1)$ as shown in Figure 1 where V_{FB}^{+} = 400mV. Typical values for R1 range from 20k to 200k. 1% or better resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB^{+} pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response if the resistor divider has a large V_{OUT}/V_{FB}^{+} ratio.

The LTC3376 includes low offset, high input impedance differential sense for applications that require remote sensing. Connect FB^{+} to the center tap of the feedback divider across the output load, and FB^{-} to the load ground.

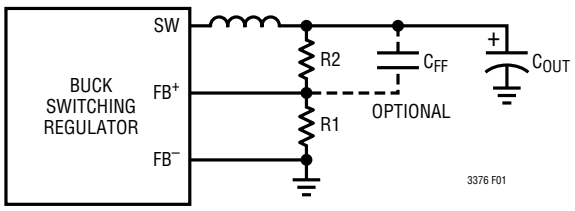


Figure 1. Feedback Components

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

The operating frequency for all of the LTC3376 buck regulators can be determined by an external resistor that is connected from the RT pin to ground. The operating frequency is calculated using the following equation:

$$f_{OSC} = 2MHz\left(\frac{402k\Omega}{R_T}\right) \quad (4)$$

While the LTC3376 is designed to function with operating frequencies between 1MHz and 3MHz, it has internal safety clamps that prevent the oscillator from running faster than 4MHz (typical) or slower than 500kHz (typical). Tying the RT pin to $INTV_{CC}$ sets the oscillator to the default internal operating frequency of 2MHz (typical).

Although the maximum programmable switching frequency is 3MHz for the LTC3376, the minimum on-time of the LTC3376 imposes a minimum operating duty cycle. The typical minimum on-time is 53ns. The highest

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switching frequency ($f_{SW(MAX)}$) for low duty cycle applications can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{BOTSW}}{t_{ON(MIN)}\left(V_{IN(MAX)} - V_{TOPSW} + V_{BOTSW}\right)} \quad (5)$$

where $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage, V_{TOPSW} and V_{BOTSW} are the internal switch drops, and $t_{ON(MIN)}$ is the minimum top switch on-time. This equation shows that a slower switching frequency is necessary to accommodate a very high V_{IN}/V_{OUT} ratio.

For higher duty cycle applications, the minimum off-time also imposes a max switching frequency which can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{IN} - V_{OUT} - V_{TOPSW}}{t_{OFF(MIN)}\left(V_{IN} + V_{BOTSW} - V_{TOPSW}\right)} \quad (6)$$

where $t_{OFF(MIN)}$ is the minimum top switch off-time. This equation shows that a slower switching frequency is also necessary to accommodate a very low V_{IN}/V_{OUT} ratio.

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance value, RMS current rating, saturation current rating, DCR, and core loss.

If the duty cycle of operation is 50% or less, choose the inductor based on the following equation:

$$L = V_{OUT} \bullet \frac{1 - \frac{V_{OUT}}{V_{IN(MAX)}}}{0.2 \bullet I_{MAX} \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN}} \le 0.5 \quad (7)$$

where f_{SW} is the switching frequency, $V_{IN(MAX)}$ is the maximum input voltage that the buck will run at, and I_{MAX} is 1.5A times the number of power stages (the maximum rated load current for the LTC3376). For operation at duty cycles higher than 50%, use instead the following equation to select the inductor:

$$L = 1.25 \bullet \frac{V_{IN(MAX)}}{f_{SW} \bullet I_{MAX}} \text{ for } \frac{V_{OUT}}{V_{IN}} > 0.5 \quad (8)$$

To avoid overheating of the inductor, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short-circuit conditions should also be taken into consideration.

In addition, ensure that the saturation current rating (typically labeled I_{SAT}) is higher than the maximum expected load plus half the inductor ripple:

$$I_{SAT} > I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (9)$$

where $I_{LOAD(MAX)}$ is the maximum output load current and ΔI_L is the inductor ripple current as calculated by:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (10)$$

A more conservative choice would be to choose an inductor with an I_{SAT} rating higher than the maximum current limit of the LTC3376 which is 3.0A per power stage.

For highest efficiency, choose an inductor with the lowest series resistance (DCR). The core material should be intended for high frequency applications. Table 2 shows recommended inductors from several manufacturers.

Input Capacitors

The LTC3376 has individual input supply pins for each buck power stage. All of these pins must be decoupled with low ESR capacitors to their own PGND. These capacitors should be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage that it will operate at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance. See Table 3 for recommended ceramic capacitor manufacturers.

Regardless of how the power stages are configured, each input supply voltage pin, V_{INA-H}, needs to be decoupled

APPLICATIONS INFORMATION

Table 2. Recommended Inductors

PART NUMBER	L (µH)	MAX DCR (mΩ)	CURRENT RATING (A)	DIMENSIONS (L × W × H)	VENDOR
XEL4030-102MEB	1	9.78	10.7	4mm × 4mm × 3.1mm	Coilcraft
XFL4020-152MEB	1.5	15.8	9.1	4.3mm × 4.3mm × 2.1mm	www.coilcraft.com
XEL4030-222MEB	2.2	22.1	7.8	4mm × 4mm × 3.1mm	
XFL4020-472MEB	4.7	57.4	5	4.3mm × 4.3mm × 2.1mm	
744383360068	0.68	27	4.5	3mm × 3mm × 2mm	Wurth Electronics Inc.
74438357010	1	13.5	7.4	4.1mm × 4.1mm × 3.1mm	www.we-online.com
74404042015	1.5	31	2.95	4mm × 4mm × 1.8mm	
74439344022	2.2	10.5	8	6.65mm × 6.65mm × 3.3mm	
PCMB042T-1R0MS	1	27	4.5	4.15mm × 4mm × 1.8mm	Susumu
PCMB053T-1R5MS	1.5	20	6	4.7mm × 4.85mm × 2.8mm	www.susumu-usa.com
FDSD0420-H-R68M=P3	0.68	22	6.5	4.2mm × 4.2mm × 2mm	Murata
FDSD0420D-1R0M=P3	1	29	5.1	4.2mm × 4.2mm × 2mm	www.murata.com
FDSD0420D-2R2M=P3	2.2	47	3.6	4.2mm × 4.2mm × 2mm	

independently to PGNDA-H with a 1µF capacitor as close to the pins as possible and at least a 10µF capacitor. Connect each ground of each capacitor to a wide PCB trace on the top layer of the PCB that connects directly to the PGND pin and then to the GND plane.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or if there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LTC3376 circuit is plugged in to a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTC3376's voltage rating. This situation is easily avoided (see Linear Technology Application Note 88).

Table 3. Ceramic Capacitor Manufacturers

VENDOR	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com

Output Capacitor, Output Ripple, and Loop Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated at the LTC3376 SW pins to produce the DC output. In this role it determines the output ripple. Thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and to stabilize the LTC3376's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications. Use X5R or X7R ceramic capacitors. This choice will provide low output ripple and good transient response.

The LTC3376 is internally compensated and has been designed to operate at a high bandwidth for fast transient response capability. The selection of C_{OUT} will affect the bandwidth of the system and the optimal value is given by the following equation:

$$C_{OUT} = 100 \bullet \frac{(\#\ \text{of power stages})}{f_{SW} \bullet V_{OUT}} \quad (11)$$

where f_{SW} is the switching frequency.

This calculated C_{OUT} value is the capacitance required after voltage and temperature derating. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage

APPLICATIONS INFORMATION

bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

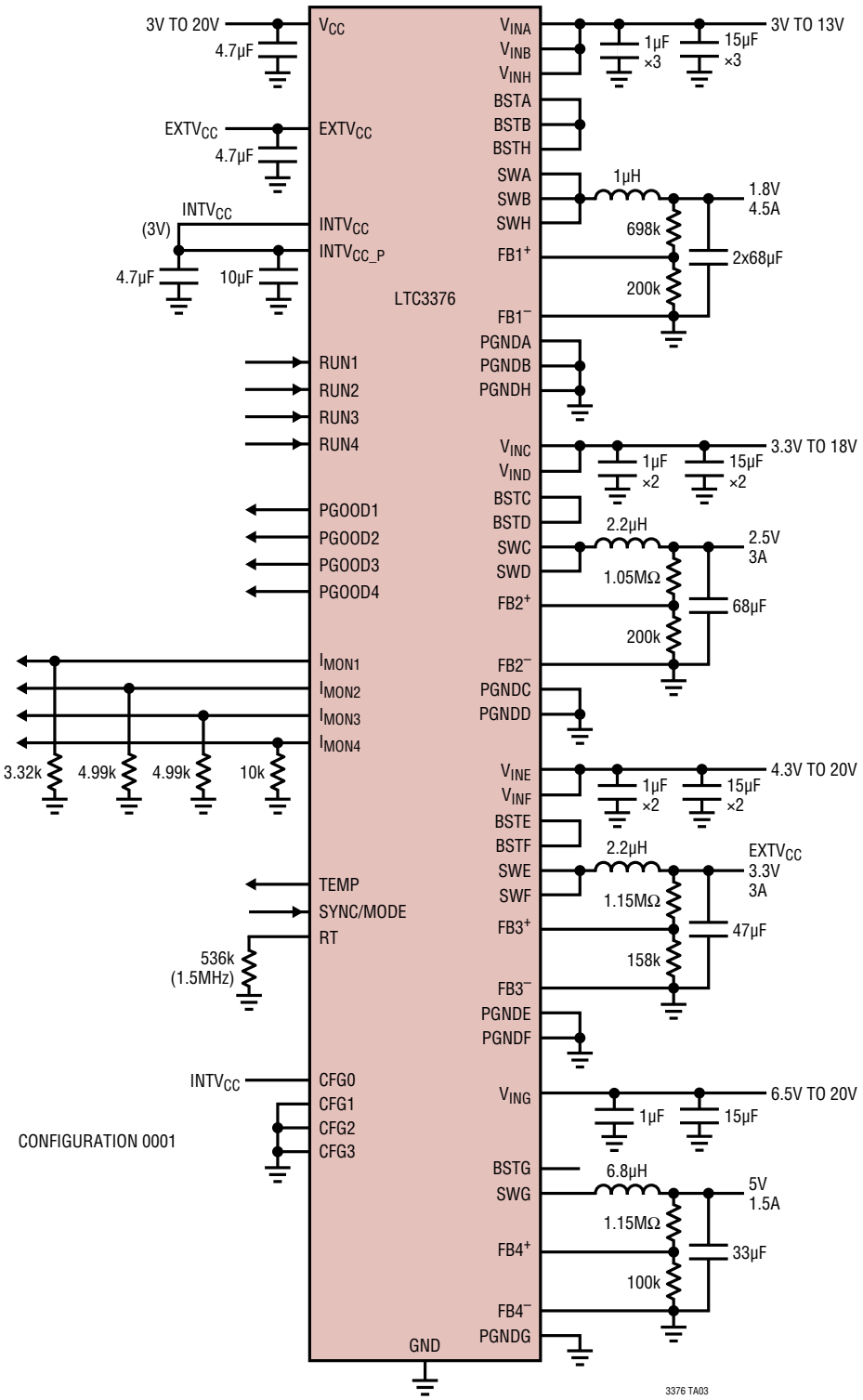
PCB Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3376:

1. The input supply pins (V_{INA-H}) should each have local decoupling capacitors with their ground pins connecting back to the PGND pin (PGNDA-H) of the IC with as short and wide a trace as possible before connecting to the GND plane. The V_{IN} and PGND pins are placed next to each other on the outer edge of the IC for this purpose. Note that large switched currents flow in the LTC3376's V_{IN} and PGND pins, and in the V_{IN} input capacitor. The loop formed by the input capacitor should be made as tight as possible by placing the capacitor adjacent to the V_{IN} and PGND pins and choosing a small case size such as 0402 for the 1µF capacitor and 0603 for the 10µF capacitor. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.
2. When connecting BST pins together for ganging, the BST trace should be as short as possible.
3. The switching power traces connecting SWA-H to their respective inductors should be short and wide to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from the switching nodes or poor performance could result.
4. Keep the FB^+, FB^-, RT, TEMP, and RUN nodes small so that ground traces will shield them from the SW and BST nodes.
5. The GND pin should connect directly to the ground side of the $INTV_{CC}$ bypass cap and then connect to the ground connection of other analog components (RT resistor, I_{MON} resistor, V_{CC} and $EXTV_{CC}$ bypass caps) before connecting down to the GND plane.
6. The bypass capacitor from $INTV_{CC}$ to GND should be as close to the $INTV_{CC}$ pin as possible and connected with a wide trace.
7. The bypass capacitor from $INTV_{CC_P}$ to GND should be as close to the $INTV_{CC_P}$ pin as possible and connected with a wide trace. The ground side of this capacitor should connect directly to the GND plane.
8. The GND side of the switching regulator output capacitors should connect to the GND plane.
9. The FB^- pin should connect directly to the GND side of the feedback resistor.
10. The power stages should have a symmetric layout with respect to V_{IN}, PGND, BST, and SW traces.
11. See Evaluation Kit Design Files for recommended layouts.

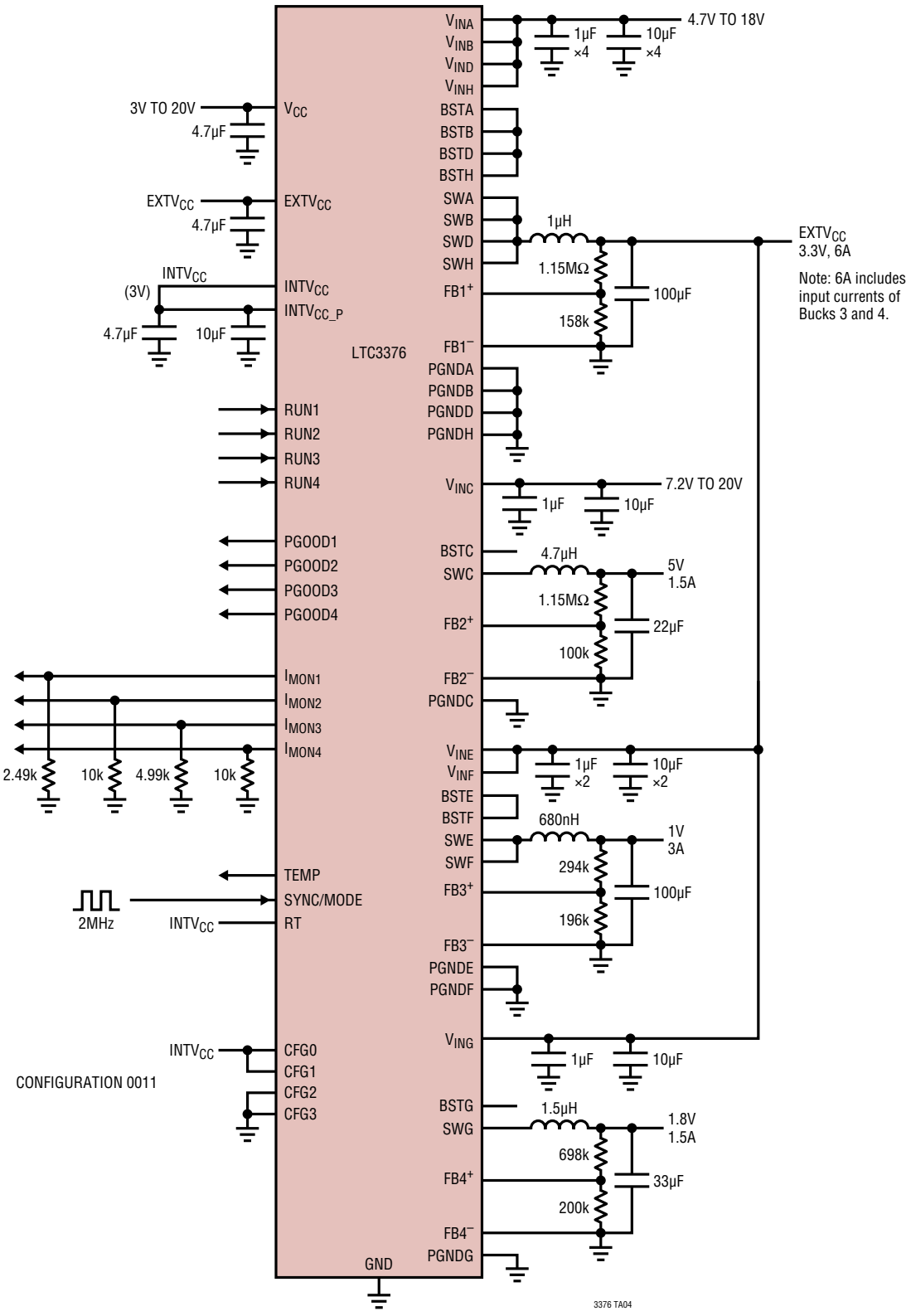
TYPICAL APPLICATIONS

Four Rail (1.8V/4.5A, 2.5V/3A, 3.3V/3A, 5V/1.5A) System with Bootstrapped $EXTV_{CC}$ Drive



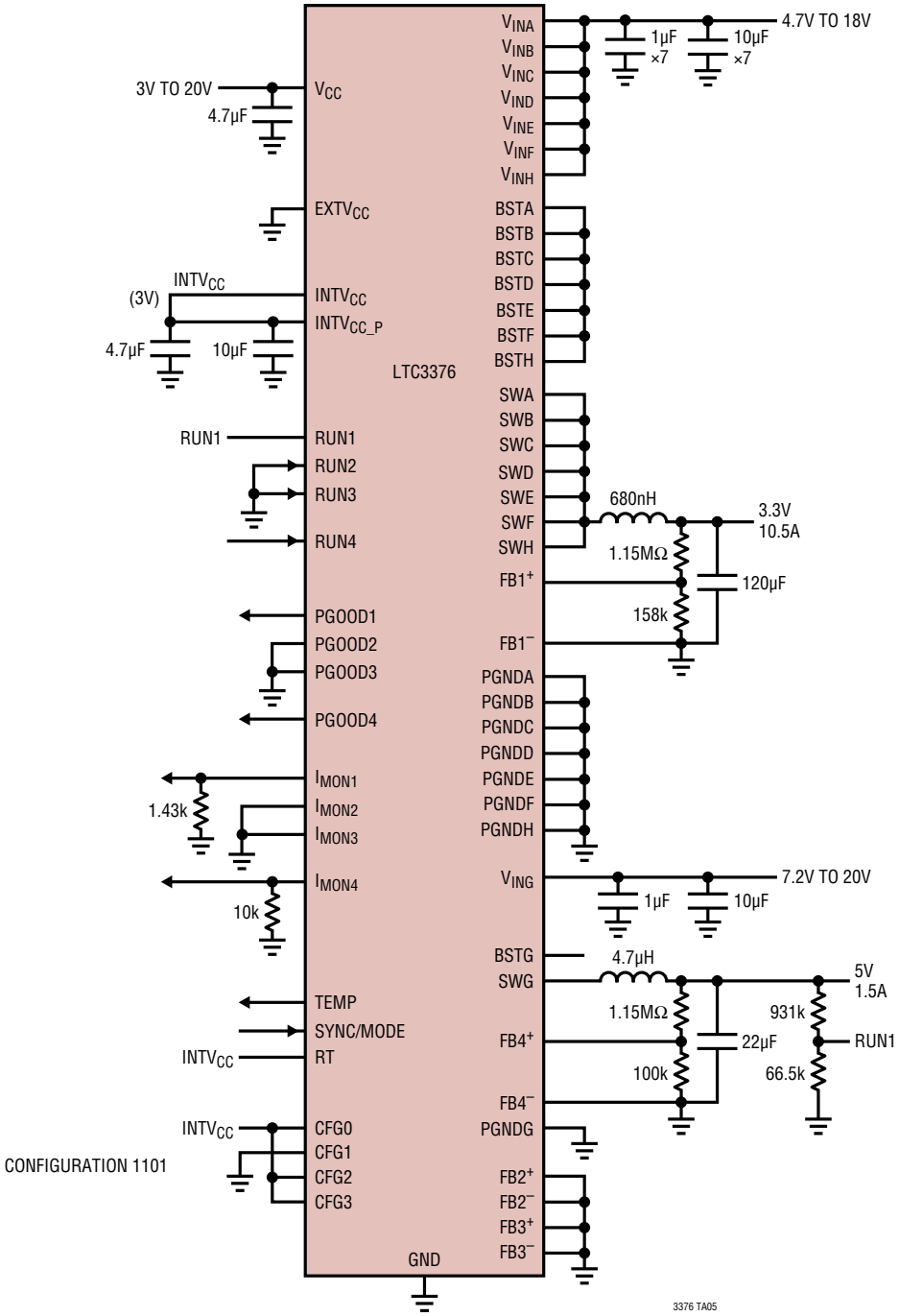
TYPICAL APPLICATIONS

Four Rail (3.3V/6A, 5V/1.5A, 1V/3A, 1.8V/1.5A) System with Bootstrapped $EXTV_{CC}$ Drive



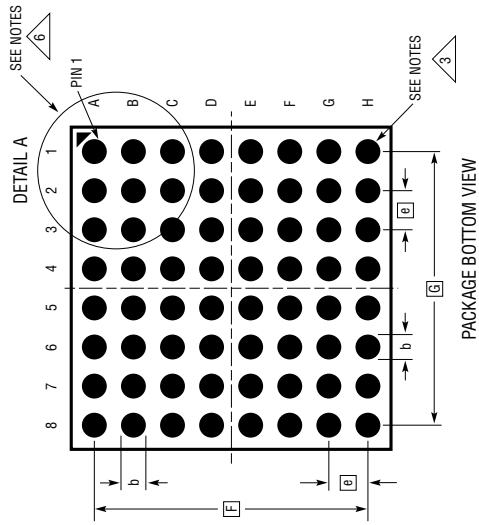
TYPICAL APPLICATIONS

Two Rail (3.3V/10.5A, 5V/1.5A) System

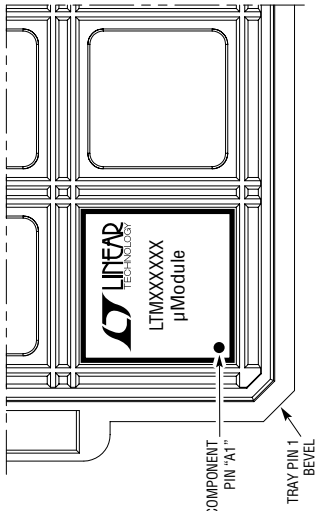


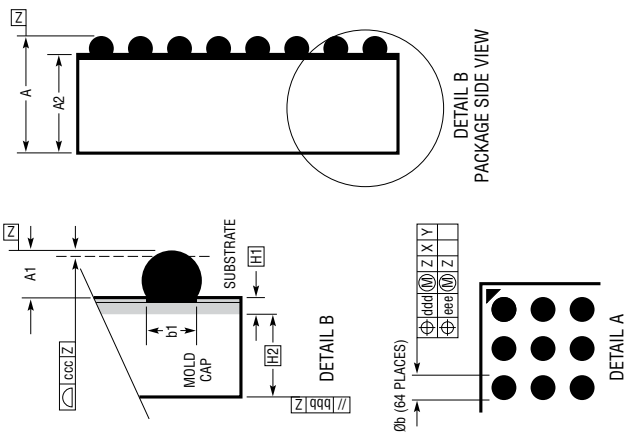
PACKAGE DESCRIPTION

BGA Package
64-Lead (7.00mm × 7.00mm × 1.34mm)
(Reference LTC DWG # 05-08-1587 Rev Ø)

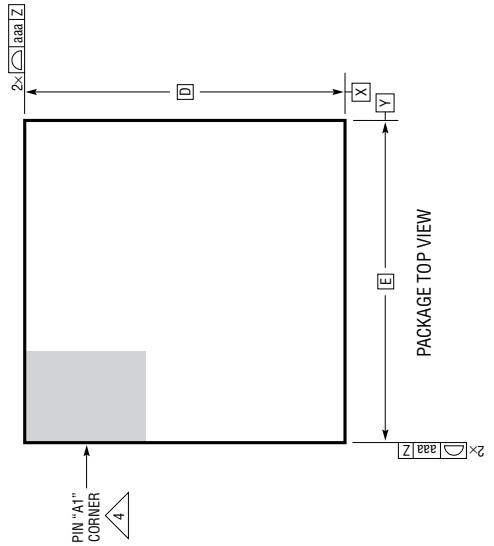


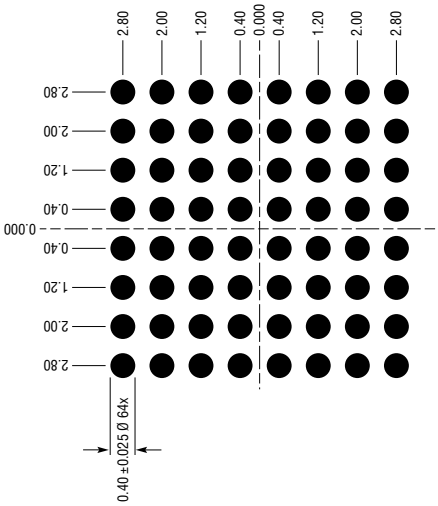
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.15	1.34	1.53	
A1	0.30	0.40	0.50	BALL HT
A2	0.85	0.94	1.03	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.00		
E		7.00		
e		0.80		
F		5.60		
G		5.60		
H1		0.24		SUBSTRATE THK
H2		0.70		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 64				





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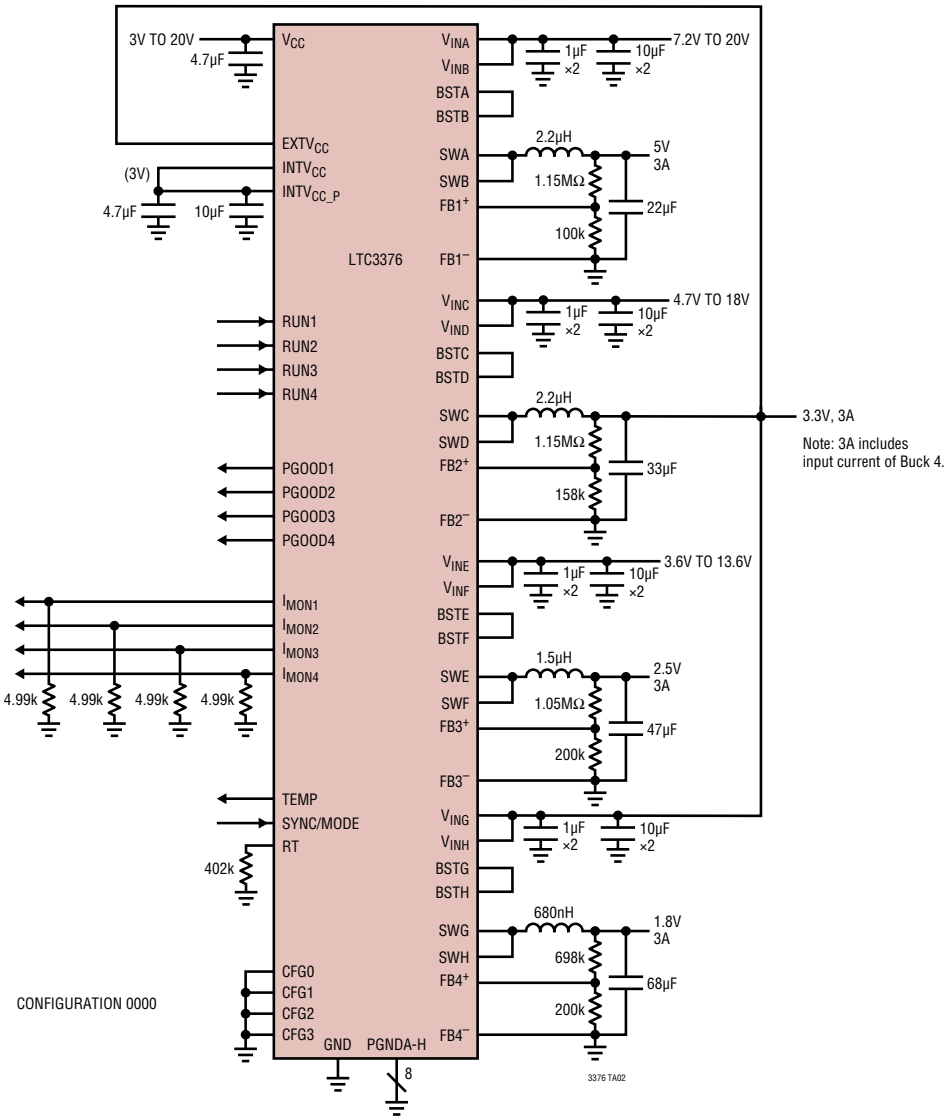
TYPICAL APPLICATION

Four Rail (5V/3.3V/2.5V/1.8V, 3A) System with Bootstrapped $EXTV_{CC}$ Drive



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3370/ LTC3371	4-Channel 8A Configurable 1A Buck DC/DCs	Four Synchronous Buck Regulators with 8× 1A Power Stages. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor. 8 Configurations Possible, Precision PGOOD Indication. 800mV FB Regulation. LTC3371 Has a Watchdog Timer; Buck 1 Accuracy ±1%, others ±2.5%; LTC3370: 32-Lead 5mm × 5mm QFN. LTC3371: 38-Lead 5mm × 7mm QFN and TSSOP.
LTC3374/ LTC3375	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor. 15 Configurations Possible. 800mV FB Regulation. All Bucks ±2.5% Accuracy. LTC3375 Has I^2C Programming with a Watchdog Timer and Pushbutton; LTC3374: 38-Lead 5mm × 7mm QFN and TSSOP, LTC3375: 48-Lead 7mm × 7mm QFN.
LTC3374A	High Accuracy 8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor; 15 Configurations Possible. 800mV FB Regulation. Buck 1 Accuracy ±1%, Others ±2%; Overvoltage Monitor Included in PGOOD.

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