20V, 200mA, Ultralow Noise, Ultrahigh PSRR Precision DAC/Reference Buffer

FEATURES

- **Ultralow Wideband Noise: 1.2μV_{RMS} (10Hz to 100kHz)**
- **Ultralow 1/f Noise: 0.6μV_{P-P} (0.1Hz to 10Hz)**
- **Ultralow Spot Noise: 4nV/√Hz at 1kHz and Above**
- **Ultrahigh PSRR: 73dB at 1MHz**
- **Ultralow Input Offset: 125μV**
- **Output Source Current: 200mA**
- **Wide Input Voltage Range: 1.8V to 20V**
- **Rail to Rail Output Voltage Range: 0V to 15V**
- **Single Capacitor Improves Noise and PSRR**
- **Fast Start-Up for V_{IN} Pin**
- $\overline{\text{FAULT}}$ Flag
- High Bandwidth: 1MHz
- Low Dropout Voltage: 350mV
- Programmable Current Limit
- Precision Enable/UVLO
- Parallelable for Lower Noise and Higher Current
- Internal Current Limit with Foldback
- Minimum Output Capacitor: 4.7μF Ceramic
- Reverse Supply and Reverse Current Protection
- Thermal Limit with Hysteresis
- 10-Lead 3mm × 3mm DFN and 12-Lead MSOP

APPLICATIONS

- High Speed/High Precision Data Converters
- High Precision Voltage References
- Very Low Noise Instrumentation

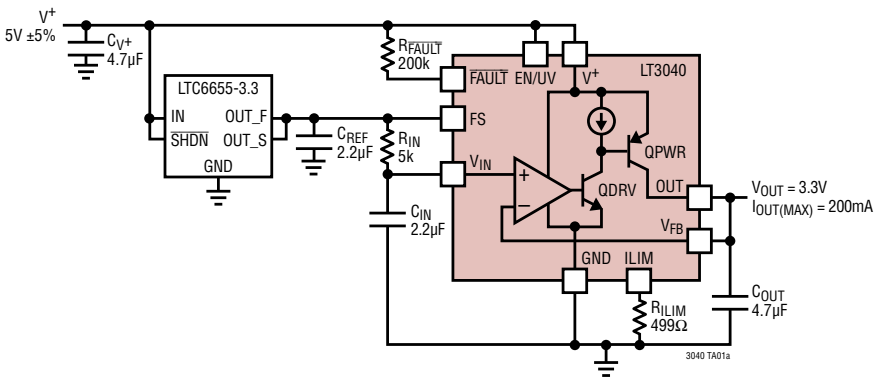
DESCRIPTION

The LT®3040 is a high performance, robust Voltage Output Reference/DAC buffer that employs a unique architecture that seeks to maintain the precision and accuracy of the Reference or DAC while sourcing up to 200mA. It features ADI's ultralow noise and ultrahigh PSRR architecture for powering noise sensitive, high accuracy systems. Designed as an advanced voltage buffer for Voltage Output References/DACs, the LT3040 features extremely low 1/f noise, very low wideband noise, excellent PSRR over a wide frequency range and low dropout performance – a typical 350mV dropout at 200mA of source current.

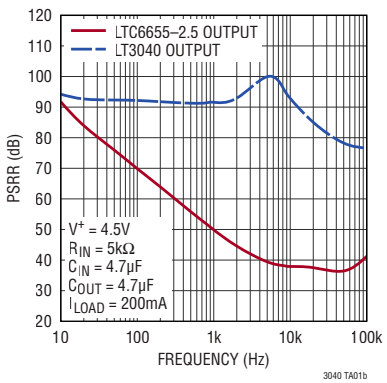
Operating quiescent current is nominally 2.5mA and drops to <1μA in shutdown. The LT3040's wide output voltage range (0V to 15V) while maintaining unity-gain operation provides virtually constant output noise, PSRR, bandwidth and load regulation independent of the V_{IN} voltage. Additionally, the buffer features programmable current limit, fast start capability and a $\overline{\text{FAULT}}$ flag to indicate faults on the output.

The LT3040 is stable with a minimum 4.7μF ceramic output capacitor. Built-in protection includes reverse supply voltage protection, reverse current protection, internal current limit with fold-back and thermal limit with hysteresis. The LT3040 is available in thermally enhanced 12-Lead MSOP and 10-Lead 3mm × 3mm DFN packages.

TYPICAL APPLICATION



Power Supply Ripple Rejection



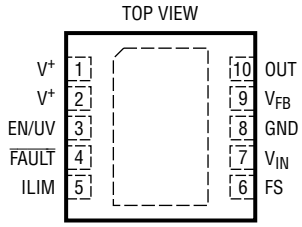
Rev. 0

ABSOLUTE MAXIMUM RATINGS

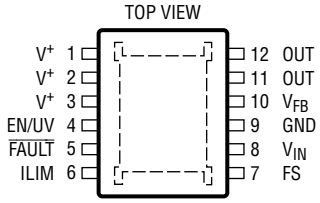
(Note 1)

V^+ Pin Voltage ..... ±22V
EN/UV Pin Voltage ..... ±22V
V^+-to-EN/UV Differential Voltage ..... ±22V
$\overline{FAULT}$ Pin Voltage (Note 10) .....–0.3V, 22V
ILIM Pin Voltage (Note 10) ..... –0.3V, 1V
V_{IN} Pin Voltage (Note 10) ..... –0.3V, 16V
V_{IN} Pin Current (Note 7) ..... ±20mA
V_{FB} Pin Voltage (Note 10) ..... –0.3V, 16V
V_{FB} Pin Current (Note 7) ..... ±20mA
OUT Pin Voltage (Note 10) ..... –0.3V, 16V
OUT-to-V_{FB} Differential (Note 14) ..... ±1.2V
V^+-to-OUT Differential ..... ±22V
V^+-to-V_{FB} Differential ..... ±22V
FS Pin Voltage (Note 10) ..... –0.3V, 16V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 9)
E-Grade, I-Grade ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 28°C/W, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3040EMSE#PBF	LT3040EMSE#TRPBF	3040	12-Lead Plastic MSOP	–40°C to 125°C
LT3040IMSE#PBF	LT3040IMSE#TRPBF	3040	12-Lead Plastic MSOP	–40°C to 125°C
LT3040EDD#PBF	LT3040EDD#TRPBF	LHGM	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3040IDD#PBF	LT3040IDD#TRPBF	LHGM	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V^+ Voltage (Note 2)	I_{LOAD} = 200mA, V^+ UVLO Rising	●		1.78	2	V
	V^+ UVLO Hysteresis			55		mV
Output Offset Voltage V_{OS} ($V_{OUT} – V_{IN}$) (Notes 4, 16)	V^+ = 2V, I_{LOAD} = 1mA, V_{OUT} = 0.3V		–125		125	µV
	V^+ = 2V, I_{LOAD} = 1mA, V_{OUT} = 0.3V	●	–300		300	µV
	V^+ = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.25V		–125		125	µV
	V^+ = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.25V	●	–300		300	µV
Input Bias Current (I_{VIN}) (Notes 4, 15)	V^+ = 2V, I_{LOAD} = 1mA, V_{IN} = 0.3V	●	–70		50	nA
	V^+ = 2V, I_{LOAD} = 1mA, V_{IN} = 1.25V		–30		30	nA
	V^+ = 2V, I_{LOAD} = 1mA, V_{IN} = 1.25V	●	–75		50	nA
Line Regulation (ΔV_{OS})	V^+ = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 0.3V	●		0.5	±3	µV/V
	V^+ = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.25V	●		0.5	±3	µV/V
Load Regulation (ΔV_{OS})	I_{LOAD} = 1mA to 200mA, V^+ = 2V, V_{OUT} = 0.3V (Note 4)	●		0.1	0.5	mV
	I_{LOAD} = 1mA to 200mA, V^+ = 2V, V_{OUT} = 1.25V (Note 4)	●		0.1	0.5	mV
Change in V_{OS} with V_{IN} (Notes 4, 15, 19)	V_{IN} = 0.1V to 0.85V, V^+ = 20V, I_{LOAD} = 1mA	●		10	100	µV
	V_{IN} = 0.95V to 15V, V^+ = 20V, I_{LOAD} = 1mA	●		35	200	µV
Dropout Voltage $V^+ = V_{OUT(NOMINAL)}$ (Note 21)	I_{LOAD} = 1mA			45	65	mV
		●			100	mV
	I_{LOAD} = 50mA			155	220	mV
		●			310	mV
	I_{LOAD} = 100mA (Note 5)			225	315	mV
		●			410	mV
	I_{LOAD} = 200mA (Note 5)			350	520	mV
		●			600	mV
GND Pin Current $V^+ = V_{OUT(NOMINAL)}$ (Note 6)	I_{LOAD} = 10µA			2.6		mA
	I_{LOAD} = 1mA	●		2.7	5	mA
	I_{LOAD} = 50mA	●		3.7	5.8	mA
	I_{LOAD} = 100mA	●		4.8	8	mA
	I_{LOAD} = 200mA	●		8	14	mA
Output Noise Spectral Density (Notes 4, 8, 19)	I_{LOAD} = 200mA, Frequency = 10Hz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, V_{OUT} = 3.3V			45		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 10Hz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, NPN Region			25		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 10kHz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, NPN Region			4		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 10kHz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, PNP Region			6		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 0.1Hz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, V_{OUT} = 3.3V			300		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 0.1Hz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, NPN Region			300		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 0.1Hz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, NPN Region			300		$nV/\sqrt{Hz}$
	I_{LOAD} = 200mA, Frequency = 0.1Hz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, PNP Region			200		$nV/\sqrt{Hz}$
Output RMS Noise (Notes 4, 8, 19)	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, V_{OUT} = 3.3V			1.25		μV_{RMS}
	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, NPN Region			1.2		μV_{RMS}
	I_{LOAD} = 200mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, PNP Region			1.8		μV_{RMS}
	I_{LOAD} = 200mA, BW = 0.1Hz to 10Hz, C_{OUT} = 4.7µF, C_{IN} = 0.47µF, V_{OUT} = 3.3V			2.4		μV_{P-P}
	I_{LOAD} = 200mA, BW = 0.1Hz to 10Hz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, NPN Region			1.5		μV_{P-P}
	I_{LOAD} = 200mA, BW = 0.1Hz to 10Hz, C_{OUT} = 4.7µF, C_{IN} = 4.7µF, PNP Region			1		μV_{P-P}
EA Switchover Point (Note 19) (PNP to NPN Input-Pair Switchover)	V^+ = 2V, I_{LOAD} = 1mA, V_{IN} Rising			917		mV
	V^+ = 2V, I_{LOAD} = 1mA, V_{IN} Falling			882		mV
EA Switchover Hysteresis (Note 19) (PNP to NPN Input-Pair Switchover)	V^+ = 2V, I_{LOAD} = 1mA			35		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ripple Rejection NPN Region $V^+ – V_{OUT}$ = 2V (Avg.) (Notes 4, 8, 19)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 4.7µF V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN}= 0.47µF V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 0.47µF V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN}= 0.47µF V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 0.47µF			117 88 76 73 56		dB dB dB dB dB
Ripple Rejection PNP Region $V^+ – V_{OUT}$ = 2V (Avg.) (Notes 4, 8, 19)	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 4.7µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN}= 0.47µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 0.47µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN}= 0.47µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 200mA, C_{OUT} = 4.7µF, C_{IN} = 0.47µF			104 88 76 67 57		dB dB dB dB dB
Fast Start Current Limit	$V_{FS} = V_{IN}$ + 0.2V, 0.1V ≤ V_{IN} ≤ 15V			10		mA
Fast Start Threshold	Turn ON ($V_{FS} – V_{IN}$) Turn OFF ($V_{FS} – V_{IN}$)			100 7		mV mV
$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 100µA	●		100	200	mV
$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 20V	●			1	µA
EN/UV Pin Threshold	EN/UV Trip Point Rising (Turn-On), V^+ = 2V	●	1.18	1.24	1.32	V
EN/UV Pin Hysteresis	EN/UV Trip Point Hysteresis, V^+ = 2V			170		mV
EN/UV Pin Current	$V_{EN/UV}$ = 0V, V^+ = 20V $V_{EN/UV}$ = 1.24V, V^+ = 20V $V_{EN/UV}$ = 20V, V^+ = 0V	● ●		 0.2 10	±1 20	µA µA µA
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)	V^+ = 6V	 ●		0.3	2 10	µA µA
Internal Current Limit (Note 12)	V^+ = 2V, V_{OUT} = 0V V^+ = 12V, V_{OUT} = 0V V^+ = 20V, V_{OUT} = 0V	● ●	220 130	270 300 180	320 250	mA mA mA
Programmable Current Limit	Programming Scale Factor: 2V < V^+ < 20V (Note 11) V^+ = 2V, V_{OUT} = 0V, R_{ILIM} = 625Ω V^+ = 2V, V_{OUT} = 0V, R_{ILIM} = 2.5kΩ	 ● ●	 180 45	125 200 50	 220 55	mA•kΩ mA mA
Reverse Input Current	V^+ = –20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{IN} = 0V	●			50	µA
Reverse Output Current	V^+ = 0V, V_{OUT} = 5V, V_{IN} = Open			2	5	µA
Minimum Load Required (Note 13)	V_{OUT} < 1V	●	10			µA
Long Term Drift (R_{IN} = 0Ω) (Note 20)	LT3040 DD Package (Measured at V_{IN} = 1.25V) 250 Hours 1000 Hours 4500 Hours LT3040 MSE Package (Measured at V_{IN} = 1.25V) 250 Hours 1000 Hours 4500 Hours			 3.2 5.2 6.7 2.3 3.5 5.1		 µV µV µV µV µV µV
Thermal Hysteresis (Note 18)	ΔT = –40°C to 125°C			<±20		µV
Thermal Shutdown	T_J Rising Hysteresis			162 8		°C °C
Thermal Regulation	10mS Pulse			–0.01		%W

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The EN/UV pin threshold must be met to ensure device operation.

Note 3: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of supply voltage and output current, especially due to the internal current limit foldback that starts to decrease current limit at $V^+ – V_{OUT} > 12V$. If operating at maximum output current, limit the supply voltage range. If operating at the maximum supply voltage, limit the output current range.

Note 4: V_{FB} tied directly to OUT.

Note 5: Dropout voltage is the minimum supply-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in higher dropout voltage compared to hard dropout—which is measured when $V^+ = V_{OUT(NOMINAL)}$. For lower output voltages, below 1.5V, dropout voltage is limited by the minimum supply voltage specification. Analog Devices is unable to guarantee maximum dropout voltage specifications for DFN package at high currents due to production test limitations with Kelvin sensing the package pins. Please consult the Typical Performance Characteristics for curves of dropout voltage as a function of output load current and temperature measured in a typical application circuit.

Note 6: GND pin current is tested with $V^+ = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher supply voltages. Note that GND pin current does not include ILIM pin current but quiescent current does include it.

Note 7: V_{IN} and V_{FB} pins are clamped using diodes and two 25Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current. See Typical Performance Characteristics and refer to Applications Information for more information.

Note 8: Adding a capacitor at the V_{IN} pin decreases output voltage noise. Adding this capacitor bypasses the reference voltage source's or the DAC's noise. The output noise then equals the error amplifier noise. Use of a V_{IN} pin bypass capacitor also increases start-up time.

Note 9: The LT3040 is tested and specified under pulsed load conditions such that $T_J \approx T_A$. The LT3040E is 100% tested at 25°C and performance is guaranteed from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3040I is guaranteed over the full –40°C to 125°C operating temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 10: Parasitic diodes exist internally between the ILIM, V_{IN}, FS, $\overline{FAULT}$, V_{FB} and OUT pins and the GND pin. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

Note 11: The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V^+ – V_{OUT}$ differentials greater than 12V

Note 12: The internal back-up current limit circuitry incorporates fold-back protection that decreases current limit for $V^+ – V_{OUT} > 12V$. Some level of output current is provided at all $V^+ – V_{OUT}$ differential voltages. Consult the Typical Performance Characteristics graph for current limit vs $V^+ – V_{OUT}$.

Note 13: For an output voltage less then 1V, the LT3040 requires a 10µA minimum load current for stability.

Note 14: Maximum OUT-to-V_{FB} differential is guaranteed by design.

Note 15: The bias current cancellation circuit used to cancel any IR drop across external resistors does not operate for V_{IN} pin voltages below 100mV due to circuit limitations. As a result, the bias current increases exponentially below this voltage. See Typical Performance Characteristics

Note 16: The Offset Voltage specification does not include the effects of line and load regulation.

Note 17: Deviations in output voltage from the reference setpoint are cumulative; errors in output regulation due to offset, line and load regulation add up.

Note 18: Hysteresis in the offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis measures the maximum output change for the averages of three hot or cold temperature cycles. For instruments that are stored at well controlled temperatures (within 20 to 30 degrees of operational temperature), it's usually not a dominant error source. Typical hysteresis is the worst-case of 25°C to cold to 25°C to hot to 25°C, preconditioned by one thermal cycle.

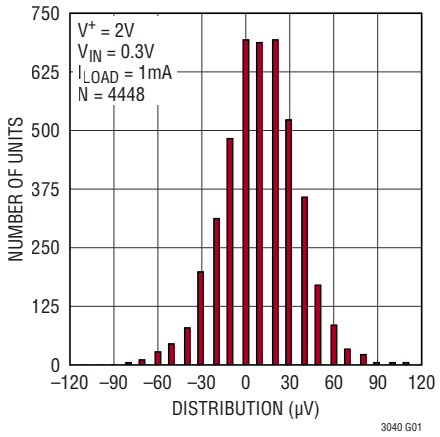
Note 19: To achieve rail-to-rail output operation, LT3040 uses either a PNP or a NPN input differential pair. There is a transition from the PNP to NPN differential pair at around the 0.9V with a typical hysteresis of about 35mV. See Applications Section for more information.

Note 20: Long-term stability typically has a logarithmic characteristic. Changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one-third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability is also affected by differential stresses between the IC and the board material created during board assembly.

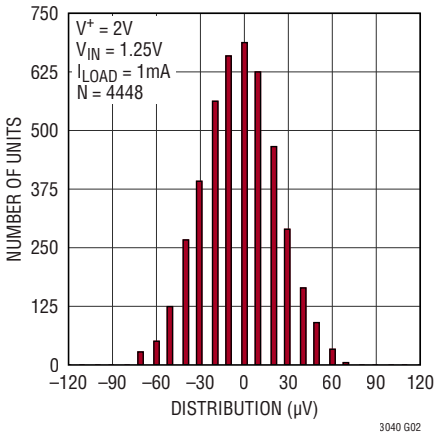
Note 21: Dropout voltage measurements are done by forcing a voltage at the V_{IN} pin.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

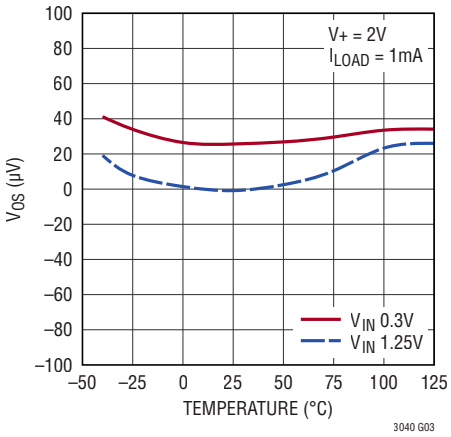
Input Offset Voltage



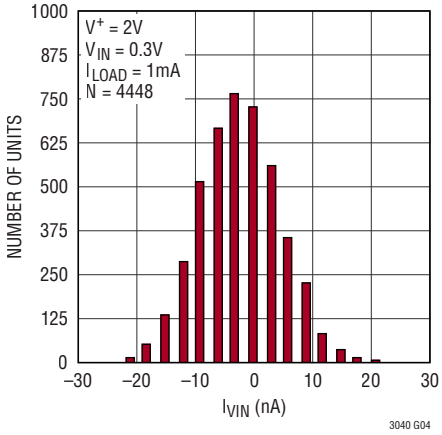
Input Offset Voltage



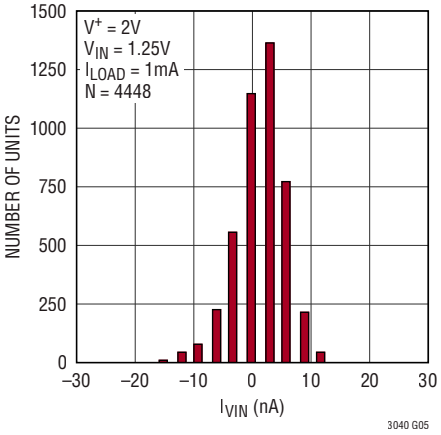
Input Offset Voltage



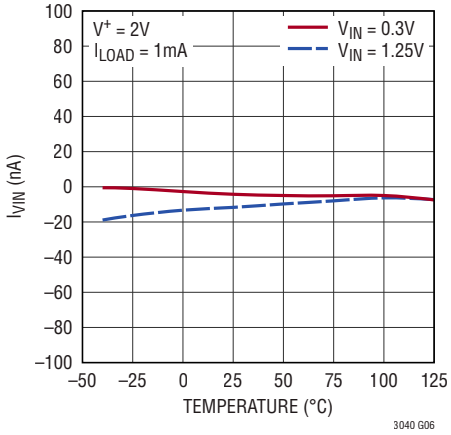
Input Bias Current



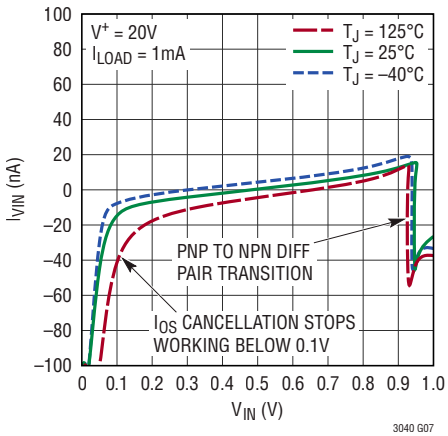
Input Bias Current



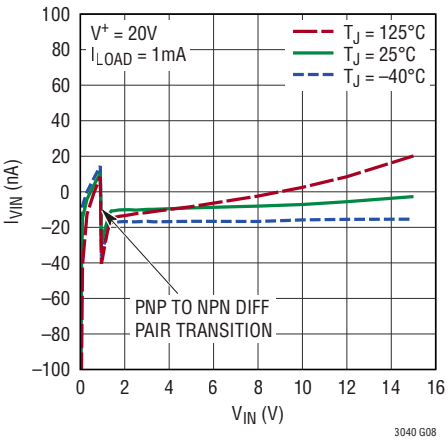
Input Bias Current



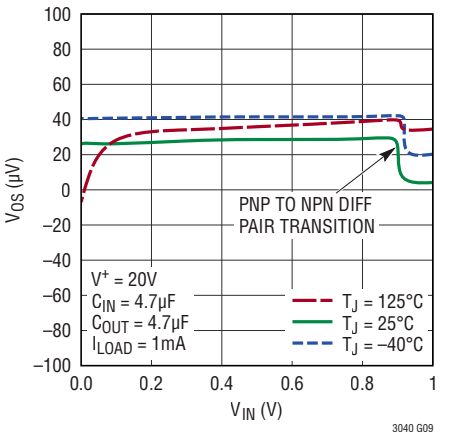
Input Bias Current



Input Bias Current

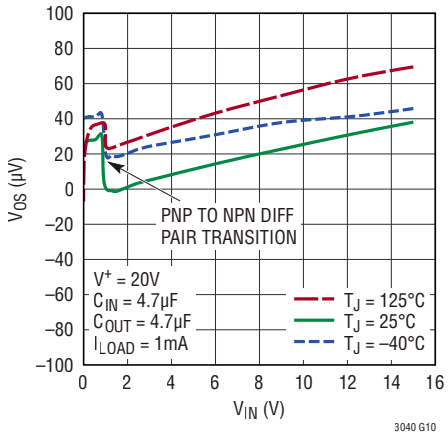


Input Offset Voltage

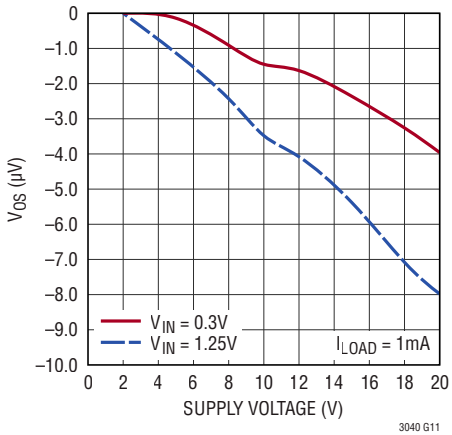


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

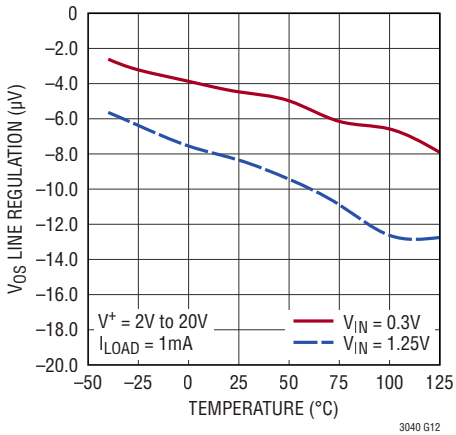
Input Offset Voltage



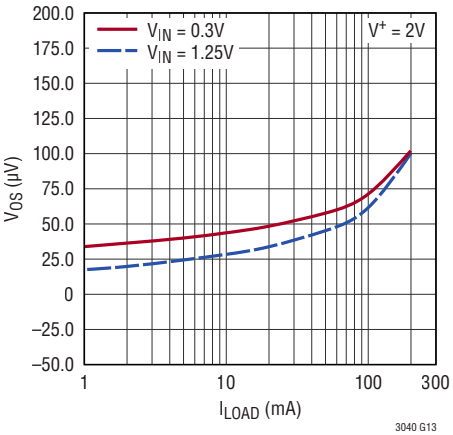
Line Regulation



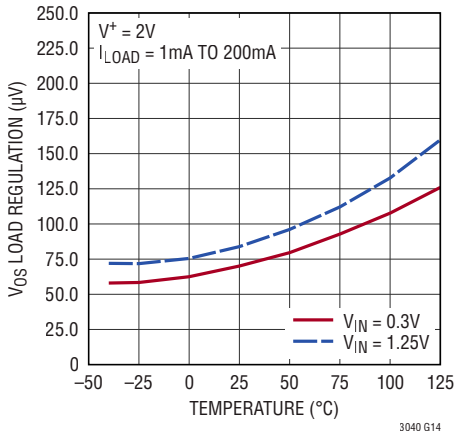
Line Regulation



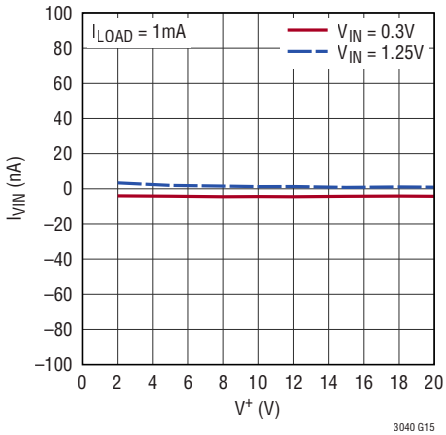
Load Regulation



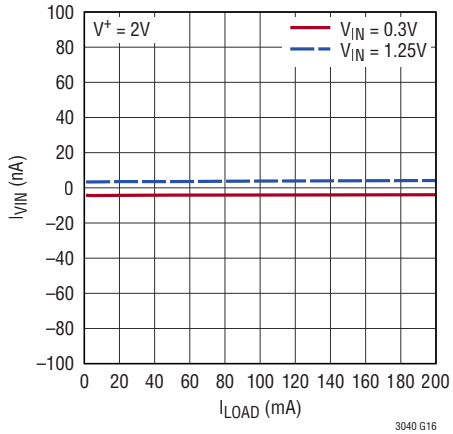
Load Regulation



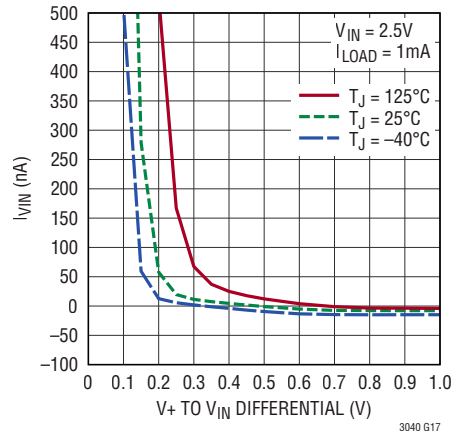
Input Bias Current



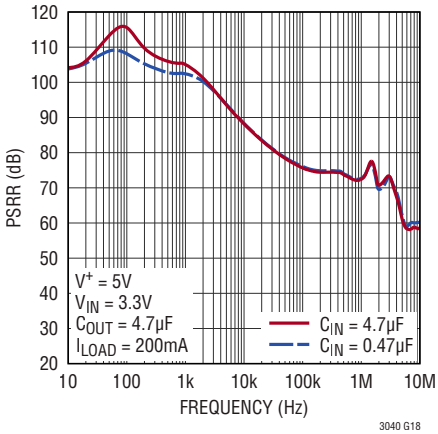
Input Bias Current



Input Bias Current

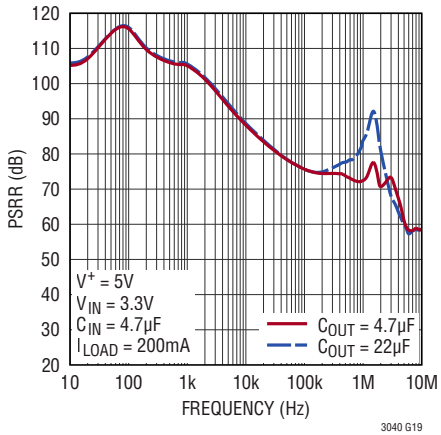


Power Supply Ripple Rejection

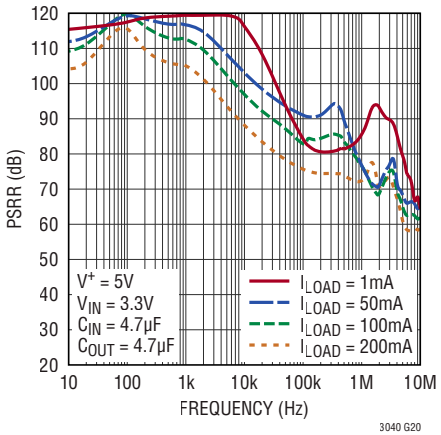


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

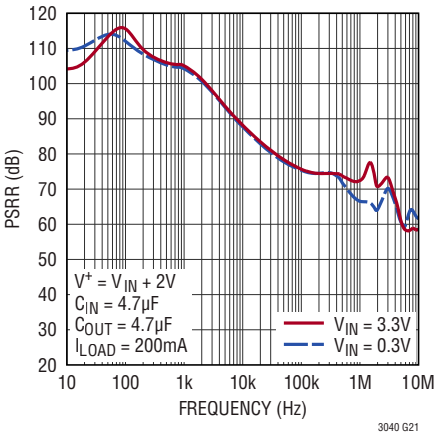
Power Supply Ripple Rejection



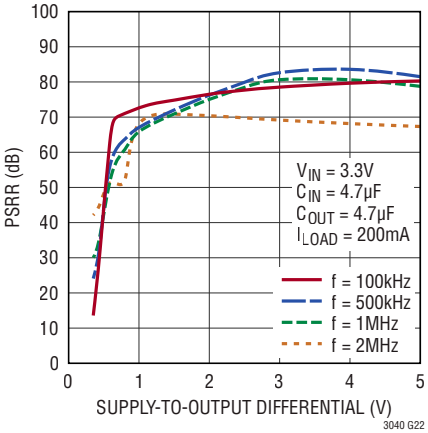
Power Supply Ripple Rejection



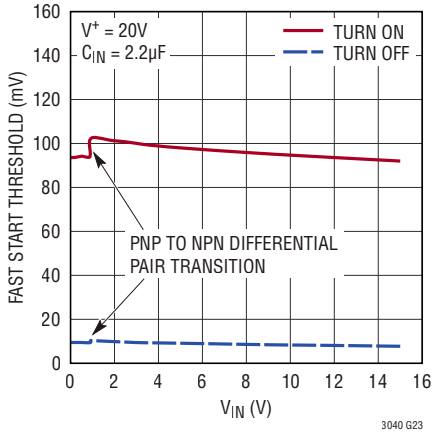
Power Supply Ripple Rejection



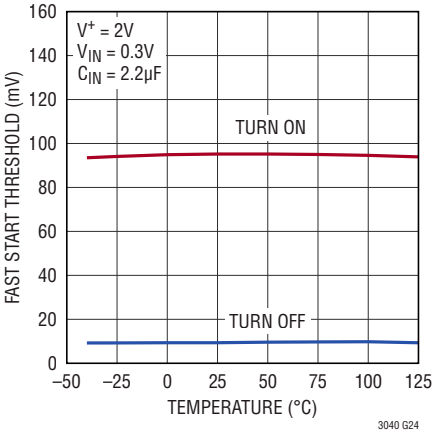
Power Supply Rejection Ratio



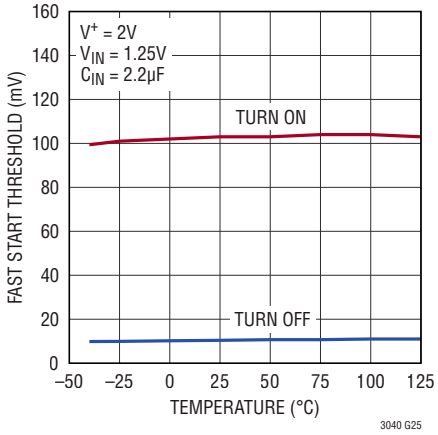
Fast Start Threshold Voltage



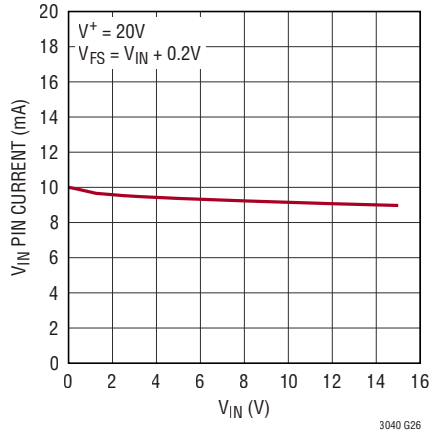
Fast Start Threshold Voltage



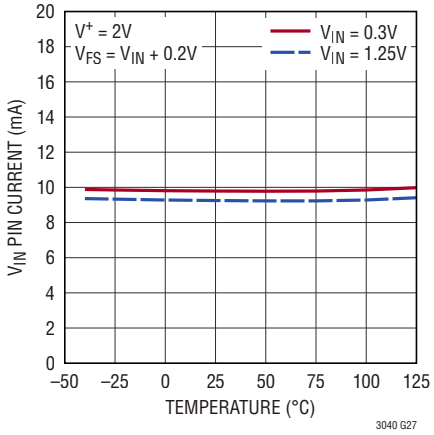
Fast Start Threshold Voltage



Fast Start Current Limit

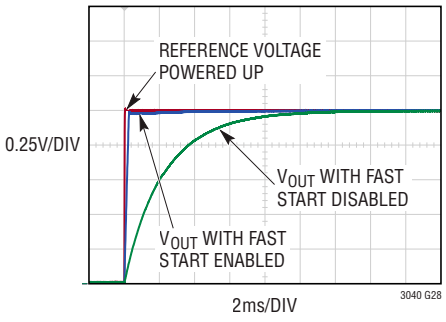


Fast Start Current Limit



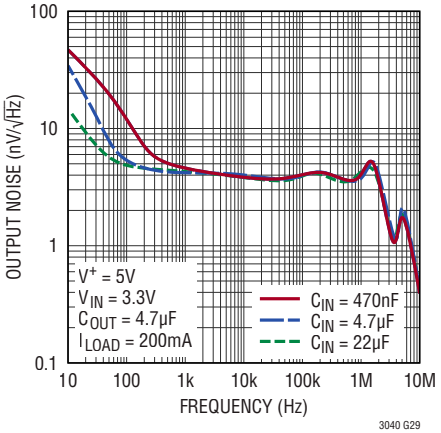
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

Start-Up Time with and without Fast Start Enabled

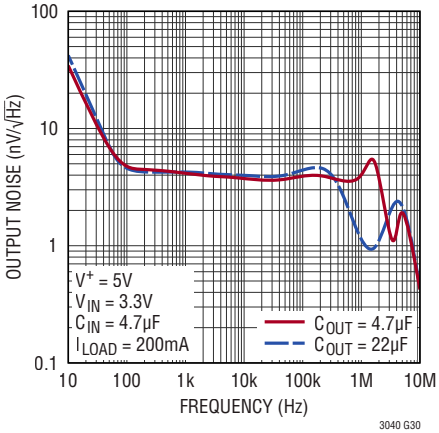


V^+ = 2V
R_{IN} = 1kΩ
C_{IN} = 2.2µF
I_{LOAD} = 1mA

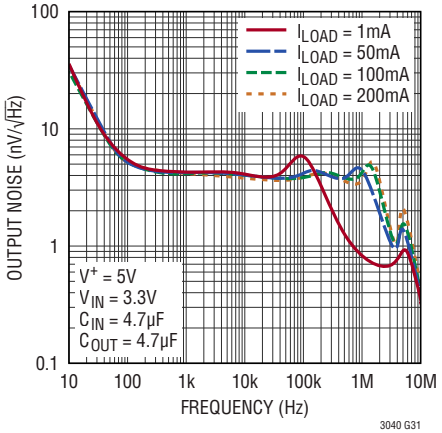
Noise Spectral Density



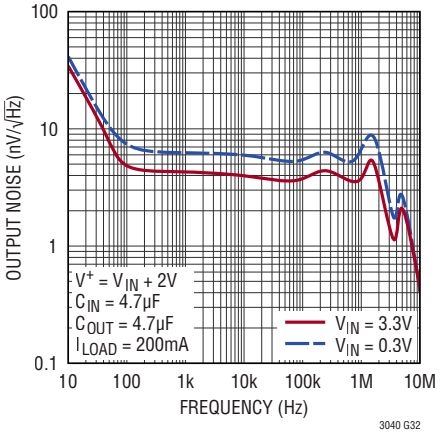
Noise Spectral Density



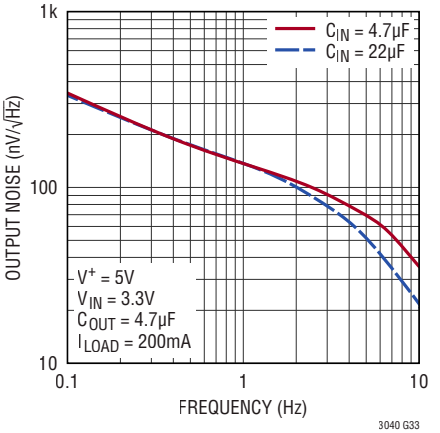
Noise Spectral Density



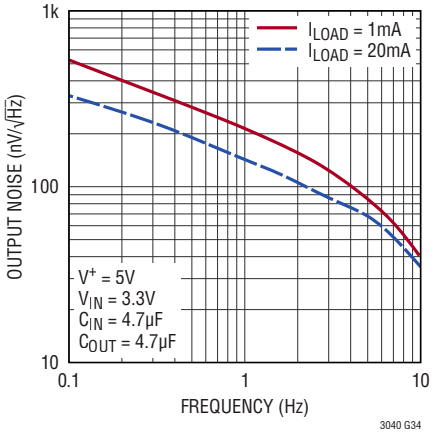
Noise Spectral Density



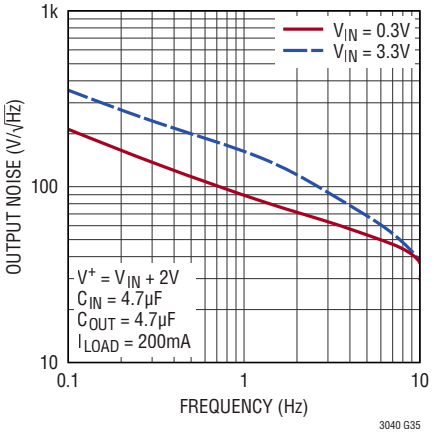
Noise Spectral Density



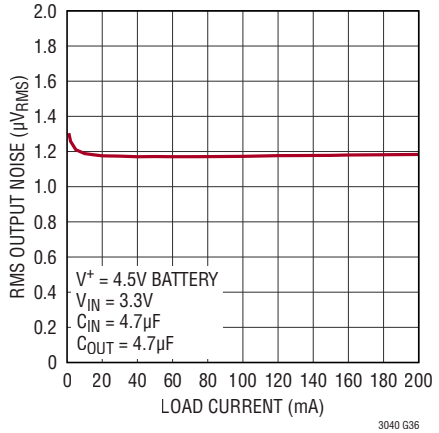
Noise Spectral Density



Noise Spectral Density

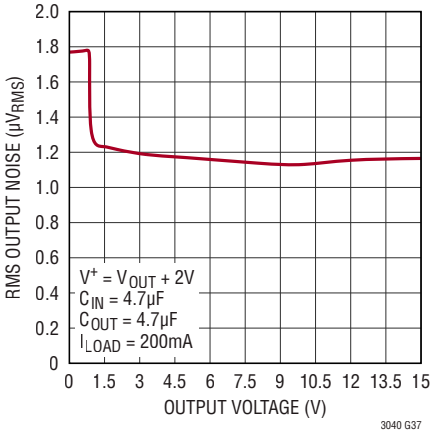


Integrated RMS Output Noise (10Hz to 100kHz)

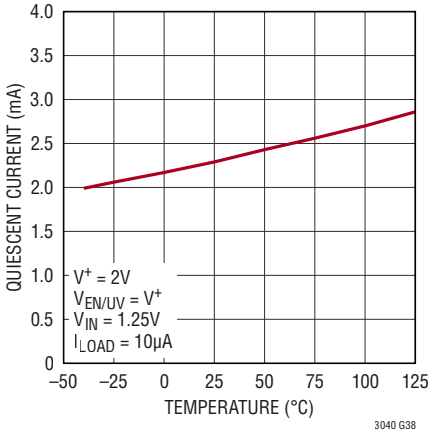


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

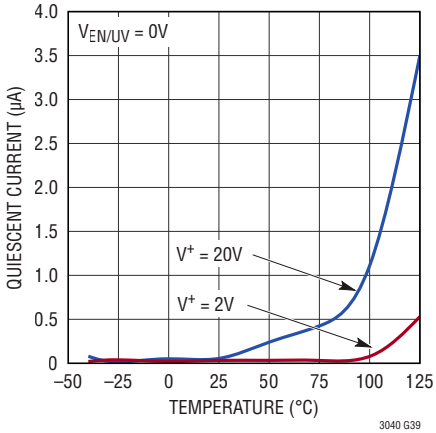
Integrated RMS Output Noise (10Hz to 100kHz)



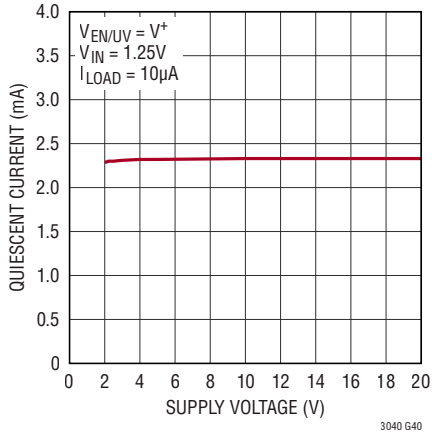
Quiescent Current



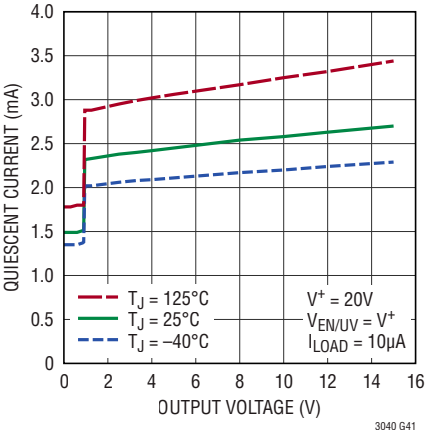
Quiescent Current in Shutdown



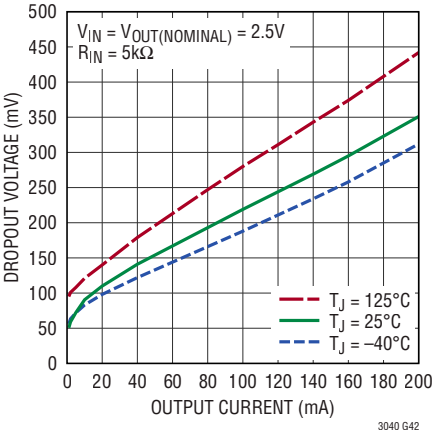
Quiescent Current



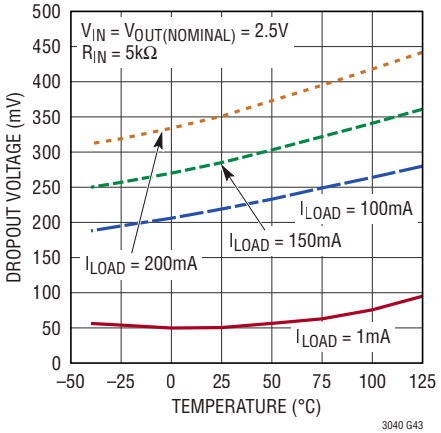
Quiescent Current



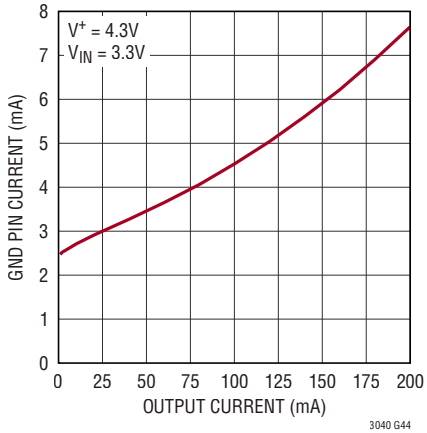
Typical Dropout Voltage



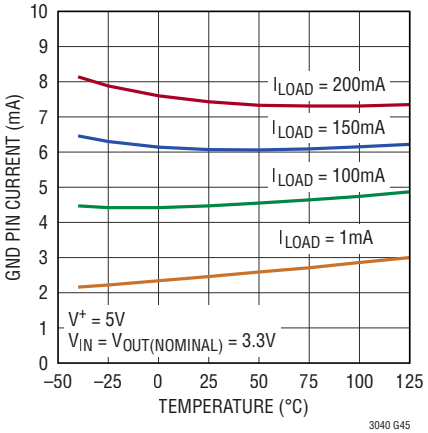
Dropout Voltage



GND Pin Current

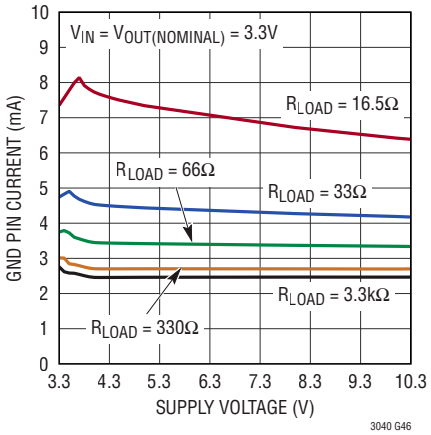


GND Pin Current

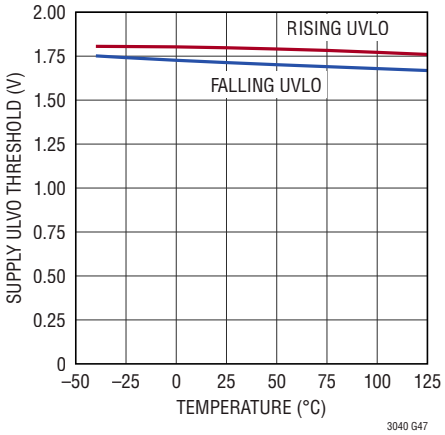


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

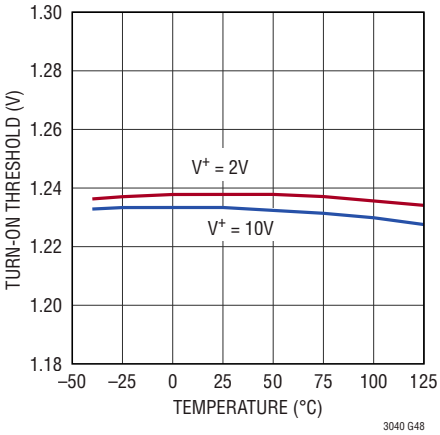
GND Pin Current



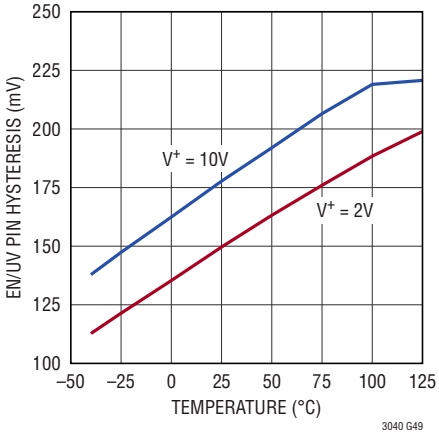
Minimum Supply Voltage



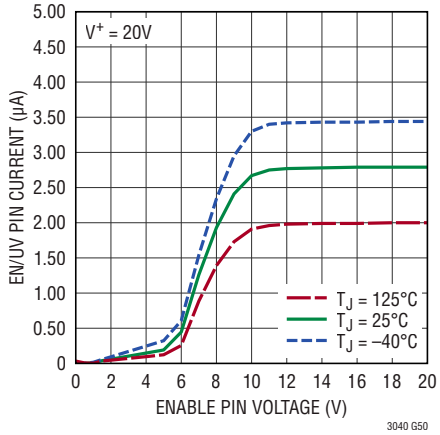
EN/UV Turn-On Threshold



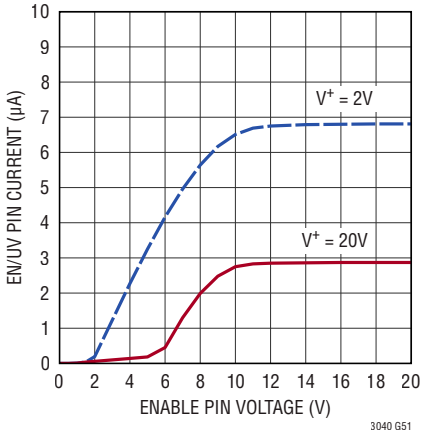
EN/UV Pin Hysteresis



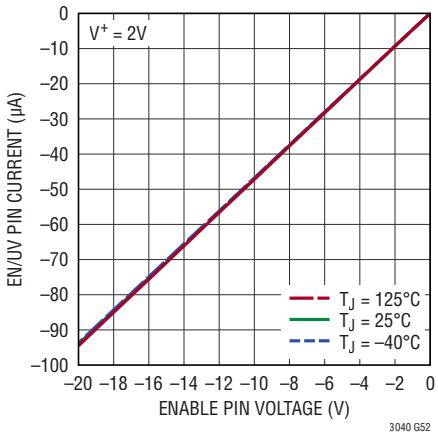
Enable Pin Current



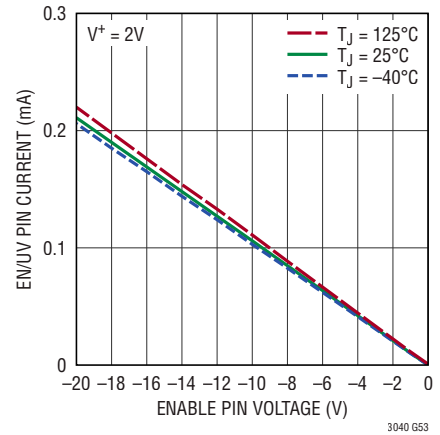
Enable Pin Current



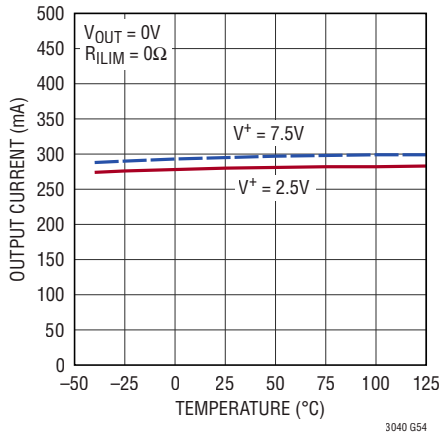
Reverse Enable Pin Current



Supply Pin Current

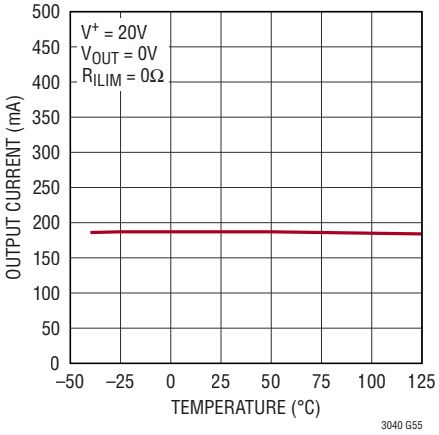


Internal Current Limit

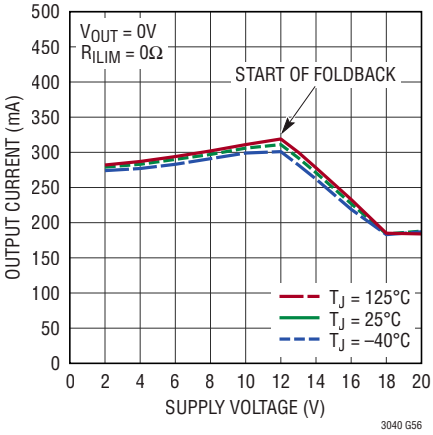


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

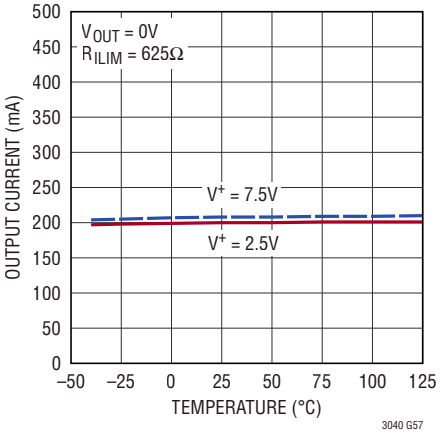
Internal Current Limit



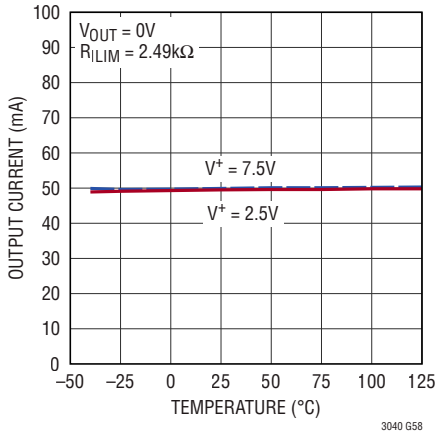
Internal Current Limit



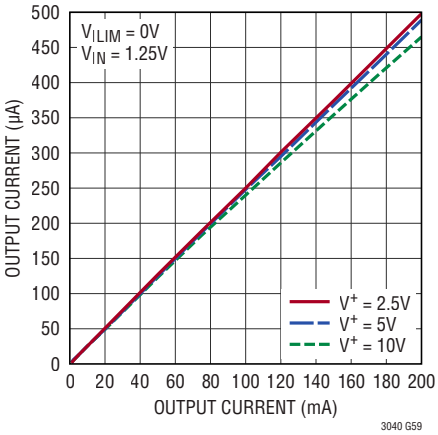
Programmable Current Limit



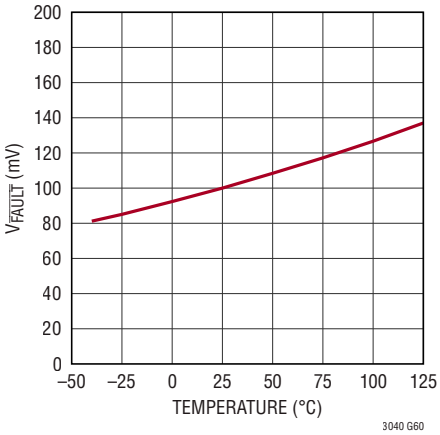
Programmable Current Limit



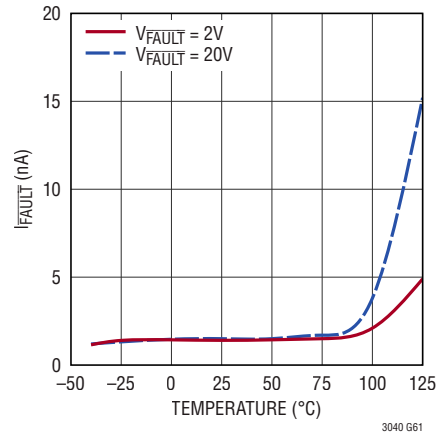
ILIM Pin Current



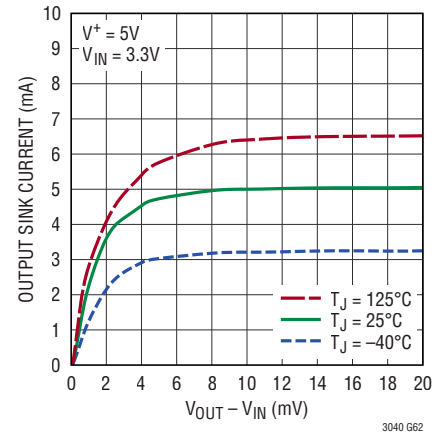
$\overline{\text{FAULT}}$ Output Low Voltage



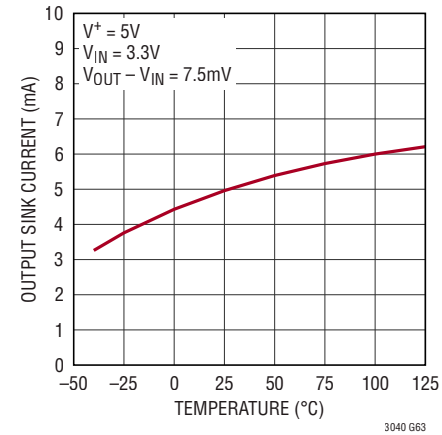
$\overline{\text{FAULT}}$ Pin Leakage Current



Output Overshoot Recovery Current Sink

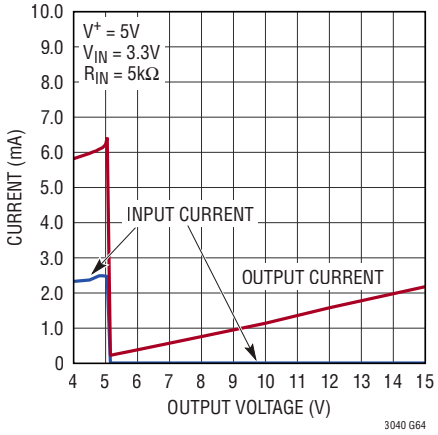


Output Overshoot Recovery Current Sink

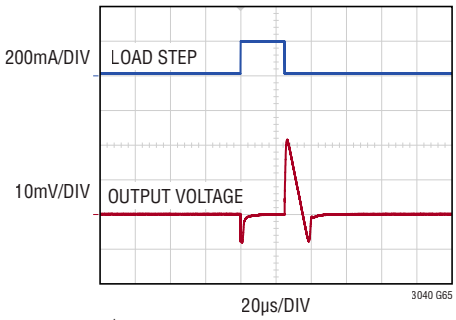


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

V_{OUT} Forced Above $V_{OUT(NOMINAL)}$

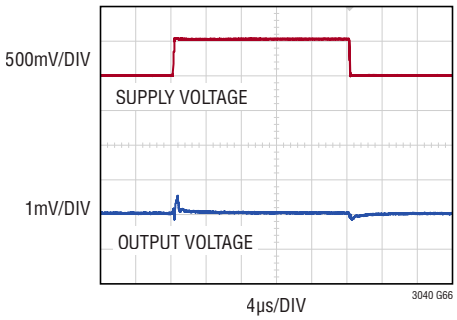


Load Transient Response



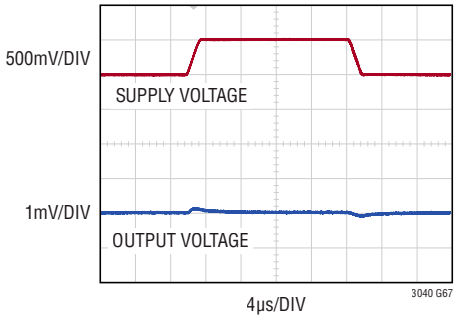
V^+ = 5V
V_{IN} = 3.3V
C_{OUT} = 4.7µF
C_{IN} = 0.47µF
LOAD STEP = 10mA TO 200mA

Line Transient Response



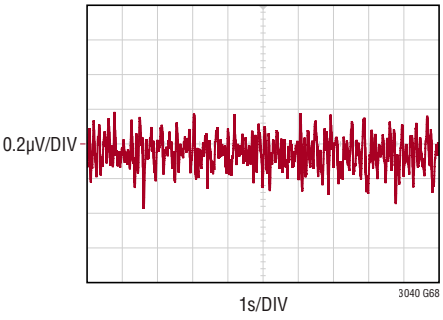
V^+ = 4V to 4.5V
V_{IN} = 3.3V
C_{OUT} = 4.7µF
C_{IN} = 0.47µF
I_{LOAD} = 200mA
t_{RISE} = t_{FALL} = 100ns

Line Transient Response



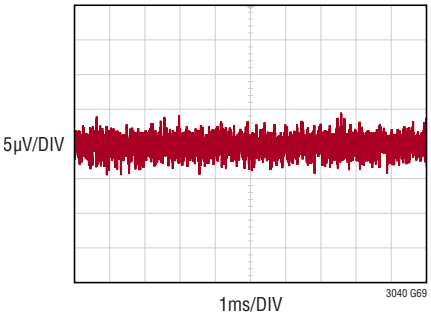
V^+ = 4V to 4.5V
V_{IN} = 3.3V
C_{OUT} = 4.7µF
C_{IN} = 0.47µF
I_{LOAD} = 200mA
t_{RISE} = t_{FALL} = 1µs

Output Noise: 0.1Hz to 10kHz



V^+ = 4V
V_{IN} = 2.5V (LTC6655 SUPPLYING V_{IN})
C_{OUT} = 4.7µF
C_{IN} = 4.7µF
R_{IN} = 5kΩ
I_{LOAD} = 200mA

Output Noise: 10Hz to 100kHz



V^+ = 5V
V_{IN} = 3.3V (LT3042 SUPPLYING V_{IN})
C_{OUT} = 4.7µF
C_{IN} = 4.7µF
R_{IN} = 5kΩ
I_{LOAD} = 200mA

PIN FUNCTIONS (DFN/MSOP)

V^+ (Pins 1, 2/Pins 1, 2, 3): Supply. These pins supply power to the buffer. The LT3040 requires a bypass capacitor at the V^+ pin. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 4.7µF supply bypass capacitor generally suffices, applications with large load transients may require higher supply capacitance to prevent supply droop. The LT3040 withstands reverse voltages on V^+ with respect to GND, V_{FB} and OUT. In the case of a reversed supply, which occurs if a battery is plugged-in backwards, the LT3040 acts as if a diode is in series with its input. Hence, no reverse current flows into the LT3040 and no negative voltage appears at the load. The device protects itself and the load.

EN/UV (Pin 3/Pin 4): Enable/UVLO. Pulling the LT3040's EN/UV pin low places the part in shutdown. Quiescent current in shutdown drops to less than 1µA and the output voltage turns off. Alternatively, the EN/UV pin can set a V^+ supply under-voltage lockout (UVLO) threshold using a resistor divider between V^+, EN/UV and GND. The LT3040 typically turns on if the EN/UV voltage exceeds 1.24V on its rising edge, with a 170mV hysteresis on its falling edge. The EN/UV pin can be driven above the supply voltage and maintain proper functionality. If unused, tie EN/UV to V^+. Do not float the EN/UV pin.

$\overline{\text{FAULT}}$ (Pin 4/Pin 5): Fault Flag. $\overline{\text{FAULT}}$ is an open drain pin that indicates an OUT pin fault. $\overline{\text{FAULT}}$ pulls low if the fast start circuitry is active (See FS pin description for more details). $\overline{\text{FAULT}}$ pin also pulls low if the output is not in regulation due to current limit, thermal shutdown, the part in dropout and UVLO. If this functionality is not used, float the $\overline{\text{FAULT}}$ pin. A parasitic substrate diode exists between the $\overline{\text{FAULT}}$ pin and GND pin of the LT3040; do not drive $\overline{\text{FAULT}}$ more than 0.3V below GND. $\overline{\text{FAULT}}$ functionality is valid only when the part is powered on and enabled.

ILIM (Pin 5/Pin 6): Current Limit Programming. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the LT3040's GND pin. The programming scale factor is nominally 125mA • kΩ. The ILIM pin sources current proportional (1:400) to output current; therefore, it also serves as a current monitoring pin with a 0V to 300mV range. If the programmable current limit functionality is not needed, tie ILIM to GND. A parasitic substrate diode exists between ILIM and GND pins of the LT3040; do not drive ILIM more than 0.3V below GND during normal operation or during a fault condition.

FS (Pin 6/Pin 7): Fast Start. Connecting this pin across an input low pass filter resistor (see Typical Application) fast starts the LT3040. Fast Start Circuitry is typically triggered active if $V_{FS} - V_{IN} \geq 100mV$ and stays active until $V_{FS} - V_{IN} \leq 7mV$. If the fast start circuit is active, it typically sources 10mA of current into the V_{IN} pin (See Fast Start under Applications Information section). If fast start functionality is not needed, connect this pin to V_{IN}.

V_{IN} (Pin 7/Pin 8): Input. This pin is the noninverting input of the error amplifier and the regulation set-point for the LT3040. The LT3040's output voltage is determined by V_{IN}. Output voltage range is from 0V to 15V. Adding a capacitor from V_{IN} to GND improves noise, PSRR and transient response at the expense of increased start- up time. A parasitic substrate diode exists between V_{IN} and GND pins of the LT3040; do not drive V_{IN} more than 0.3V below GND during normal operation or during a fault condition. V_{IN} is internally clamped to V_{FB} by a 1.5V clamp. Refer to the Power Supply Sequencing section in Applications Information for additional details.

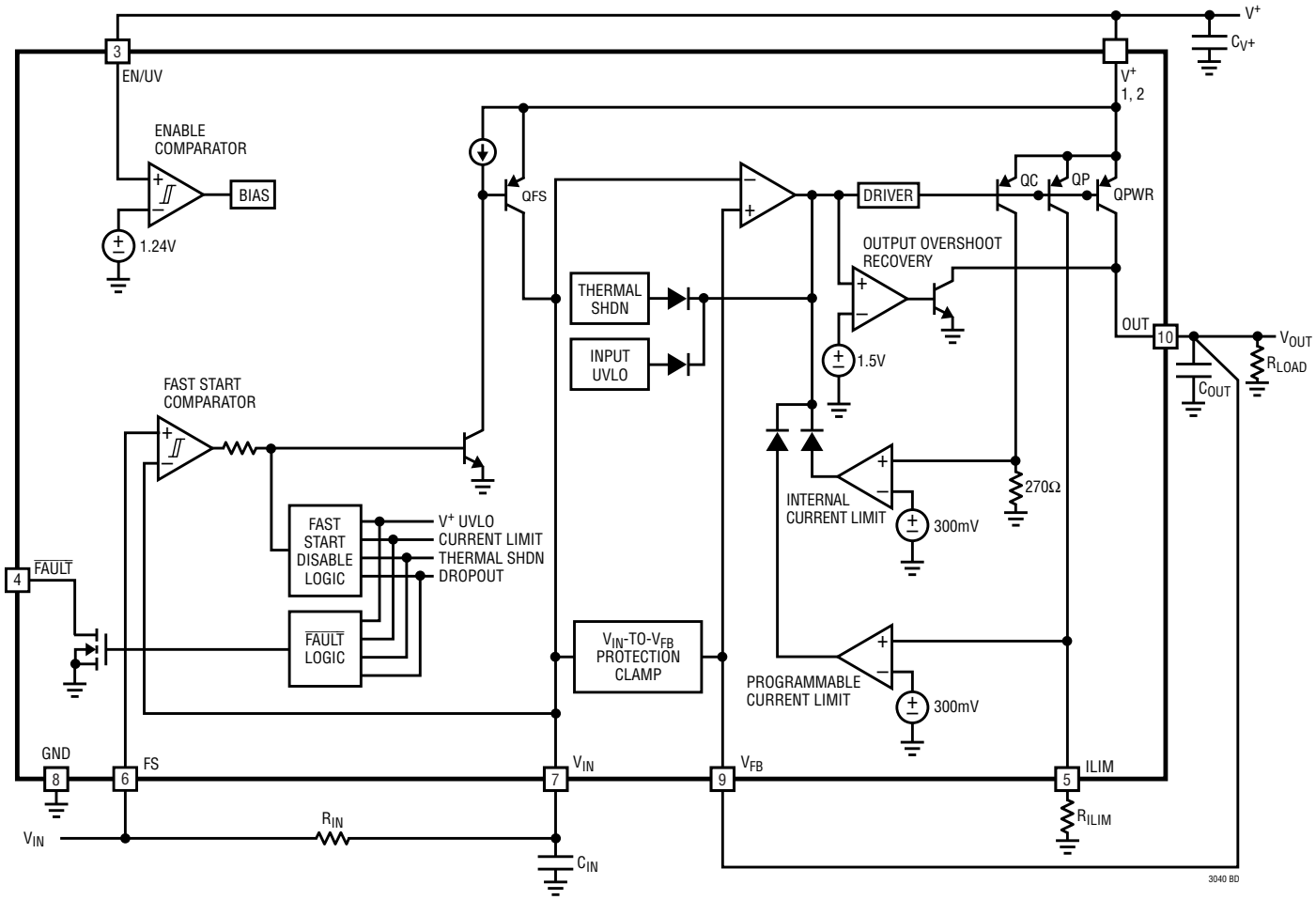
GND (Pin 8, Exposed Pad Pin 11/Pin 9, Exposed Pin Pad 13): Ground. The exposed backside is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and tie it directly to the GND pin.

V_{FB} (Pin 9/Pin 10): Output Feedback. This pin is the inverting input to the error amplifier. This pin should always be tied to OUT pin in unity gain feedback. For optimal transient performance and load regulation, Kelvin connect V_{FB} directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the V_{IN} pin capacitor directly together. Moreover, place the supply and output capacitors (and their GND connections) very close together. A parasitic substrate diode exists between V_{FB} and GND pins of the LT3040; do not drive V_{FB} more than 0.3V below GND during normal operation or during a fault condition.

PIN FUNCTIONS (DFN/MSOP)

OUT (Pin 10/Pins 11, 12): Output. This pin supplies power to the load. For stability, use a minimum 4.7µF output capacitor with an ESR below 50mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients. Refer to the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and GND pins of the LT3040; do not drive OUT more than 0.3V below GND during normal operation or during a fault condition.

BLOCK DIAGRAM



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The LT3040 is a high performance low dropout voltage buffer featuring ADI's ultralow noise (4nV/√Hz at 10kHz) and ultrahigh PSRR (73dB at 1MHz) architecture for powering noise sensitive applications. Designed as a high-performance rail-to-rail voltage buffer, the LT3040 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability and fault indicator flag.

The LT3040 is easy to use and incorporates all of the protection features expected in a high-performance voltage buffer. Included are short-circuit protection, safe operating area protection, reverse supply voltage protection, reverse current protection and thermal shutdown with hysteresis.

Output Voltage

The LT3040's rail-to-rail error amplifier allows for a wide output voltage range from 0V to V^+ minus dropout—up to 15V. A PNP-based input pair is active for 0V to ~0.9V output and an NPN-based input pair is active for output voltages greater than ~0.9V, with an abrupt transition between the two input pairs at ~0.9V output with approximately 35mV of hysteresis. The NPN-based input pair is designed to offer the best overall performance. Refer to the Electrical Characteristics table for details on offset voltage, V_{IN} offset pin current, output noise and PSRR variation with the error amp input pair.

The PNP and the NPN input pairs are trimmed separately for offset voltage. As a result, the PNP and the NPN offsets could end up significantly different from each other within the offset limits specified in the EC table. The offset voltage behavior in the transition region for a typical part is as shown in Figure 1. The range of variation in the offset voltage is shown in Figure 2.

The LT3040 always operates in unity gain configuration. This allows the LT3040 to have loop gain, frequency response and bandwidth independent of the output voltage. As a result, noise, PSRR and transient performance do not change with output voltage. Moreover, since none of the error amp gain is needed to amplify the V_{IN} pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

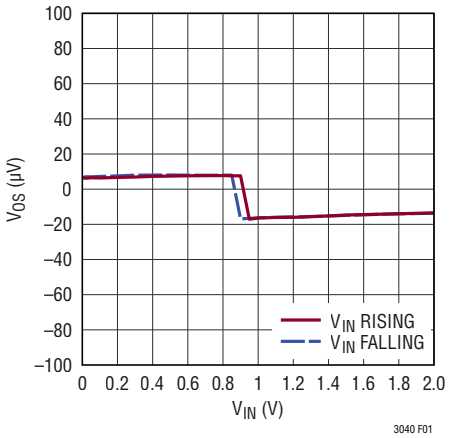

Figure 1. PNP to NPN Diff Pair Transition

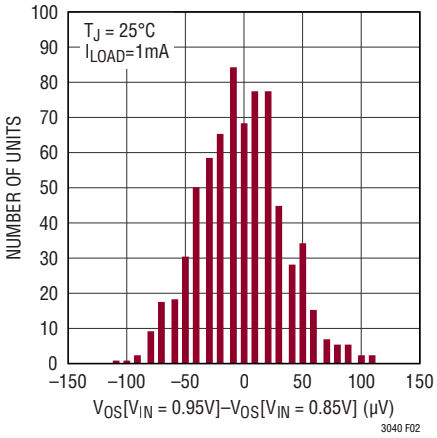

Figure 2. PNP to NPN V_{OS} Distribution

If an application uses the LT3040 with a filter resistor from FS to V_{IN} or a current limit resistor into V_{IN}, any leakage paths to or from the V_{IN} pin create errors in the output voltage. If necessary, use high quality insulation (e.g., Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High humidity environments may require a surface coating at the V_{IN} pin to provide a moisture barrier.

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Minimize board leakage by encircling the V_{IN} pin with a guard ring operated at a potential close to itself—ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. Leakages of 100nA into or out of the V_{IN} pin creates a 100µV error (with a 1kΩ resistor connecting to V_{IN}) in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over wide operating temperature range. Figure 3 illustrates a typical guard ring layout technique.

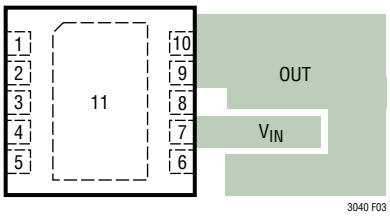

Figure 3. DD Package Guard Ring Layout

Since the V_{IN} pin is a high impedance node, unwanted signals may couple into the V_{IN} pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the V_{IN} pin with a small capacitance to ground if allowed by the application resolves this issue—10nF is normally sufficient.

Output Sensing

The LT3040's V_{FB} pin provides a Kelvin sense connection to the output.

Additionally, as shown in Figure 4, it is very important for stability to tie the V_{FB} pin directly to the output capacitor (C_{OUT}) and the GND side of the V_{IN} pin capacitor (C_{IN}) directly to the GND side of C_{OUT} as well as keeping the GND sides of supply capacitor (C_V+) and C_{OUT} close together. Refer to the PCB Layout Considerations section for an example layout that meets these requirements.

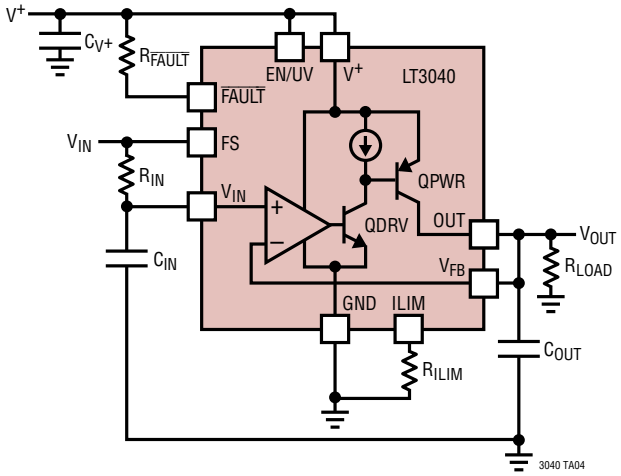

Figure 4. C_{IN} and C_{OUT} Connections for Stability

The LT3040 requires an output capacitor for stability. Given its high bandwidth (about 1MHz), ADI recommends low ESR and ESL ceramic capacitors. A minimum 4.7µF output capacitor with an ESR below 50mΩ and an ESL below 2nH is required for stability. To minimize effects of board inductances on the LT3040's dynamic performance, Kelvin connect the V_{FB} pin directly to the output capacitor as well as Kelvin connect the GND side of the V_{IN} pin capacitor (C_{IN}) directly to the GND side of the output capacitor. Also, tie the supply capacitor's GND connection as close as possible to the output capacitor's GND connection.

Given the high PSRR and low noise performance attained using a single 4.7µF ceramic output capacitor, larger values of output capacitor only marginally improves the performance because the regulator bandwidth decreases with increasing output capacitance — hence, there is little to be gained by using larger than the minimum 4.7µF output capacitor. Nonetheless, larger values of output capacitance do decrease peak output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3040 increase the effective output capacitance.

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Give extra consideration to the type of ceramic capacitors used. They are manufactured with variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIS temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in the small packages, but they tend to have stronger voltage and temperature coefficients as shown in Figure 5 and Figure 6. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

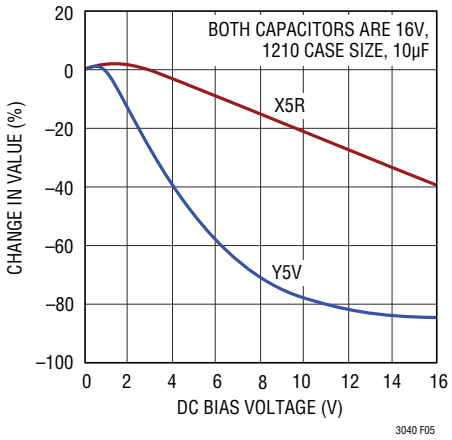

Figure 5. Ceramic Capacitor DC Bias Characteristics

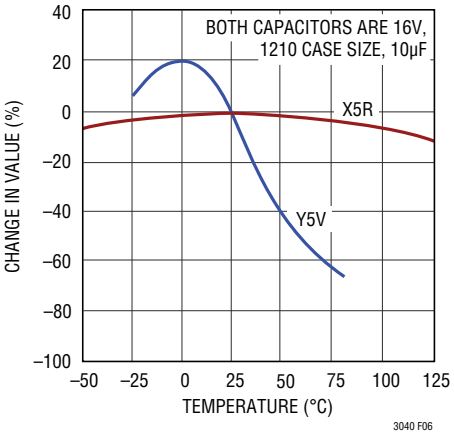

Figure 6. Ceramic Capacitor Temperature Characteristics

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for LT3040. The X7R dielectric has better stability across temperature, while X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance change due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in Figure 7, capacitor DC bias characteristics tend to improve as component case size increases, but verification of expected capacitance at the operating voltage is highly recommended.

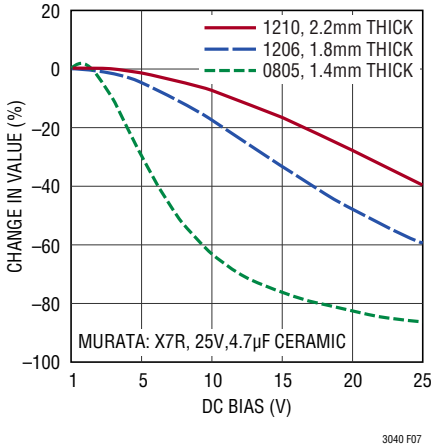

Figure 7. Capacitor Voltage Coefficient for Different Case Sizes

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress upon it, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

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One measure of stability is the closed loop response of the buffer. Figure 8 shows the closed loop response for LT3040 with a 4.7µF output capacitor.

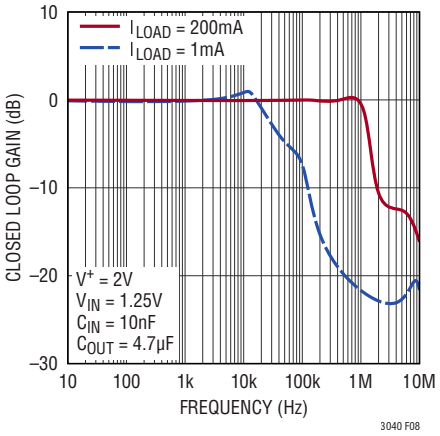

Figure 8. LT3040 Closed Loop Response

Stability and Supply Capacitance

The LT3040 is stable with a minimum 4.7µF V^+ pin capacitor. ADI recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the LT3040's supply and ground terminals, the use of low value supply capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the supply capacitor is the cause and not because of LT3040's instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the LT3040 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connect two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self-inductance of the wires — therefore a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the supply and ground wires) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted in close proximity powers the LT3040, a 4.7µF supply capacitor suffices for stability. However, if a distantly located supply powers the LT3040, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 4.7µF minimum) per 8" of wire length. The minimum supply capacitance needed to stabilize the application also varies with the output capacitance as well as the load current. Placing additional capacitance on the LT3040's output helps. However, this requires significantly more capacitance compared to additional supply bypassing. Series resistance between the power supply and the LT3040 V^+ input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the LT3040 supply in parallel with a 4.7µF ceramic capacitor.

Output Noise

The LT3040 offers many advantages with respect to noise performance. Traditional buffers or linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting output voltage and the noise gain created by this resistor divider. Many low noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3040 does not use an internal voltage reference. The external voltage source (Voltage Reference/Voltage Output DAC) will dominate the output voltage noise. The resultant voltage noise equals the external reference noise which in turn is RMS summed with the error amplifier's noise. The typical noise contribution from LT3040's error amplifier is $4nV/\sqrt{Hz}$. In order to achieve this noise specification, the external voltage source can use a filter resistor connected between

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the LT3040's FS and V_{IN} pins. The low pass filter (LPF) created by this bypass resistor along with the V_{IN} pin capacitor bypasses the noise contribution from the voltage source. To ensure fast start-up of LT3040 with this LPF in place, the LT3040's fast start-up circuit charges the V_{IN} pin capacitor with a 10mA (typical) current source.

One problem that conventional linear regulators face is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the LT3040's unity-gain follower architecture presents no gain from the V_{IN} pin to the output. Therefore, if a capacitor bypasses the voltage source noise, then the output noise is independent of the programmed output voltage. The resultant output noise is then set just by the error amplifier's noise — typically $4nV/\sqrt{Hz}$ from 10kHz to 1MHz and $1.2\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth using a 4.7µF V_{IN} pin capacitor. Paralleling multiple LT3040s further reduces noise by $\sqrt{N}$, for N parallel regulators.

Refer to the Typical Performance Characteristics section for noise spectral density and RMS integrated noise over various load currents and V_{IN} pin capacitances.

V_{IN} Pin (BYPASS) Capacitance: Noise, PSRR, Transient Response and Soft-Start

In addition to reducing output noise, using a V_{IN} pin bypass capacitor also improves PSRR and transient performance. Note that any bypass capacitor leakage may deteriorate the LT3040's DC regulation. Capacitor leakage of 100nA results in a 100µV DC error for a 1k impedance at the V_{IN} pin. The use of a good quality low leakage ceramic capacitor is recommended.

Using a V_{IN} bypass capacitor may soft-start the output and limit inrush current. If fast start functionality is not used and a filter resistor (R_{IN}) is used (refer to Figure 9) then the RC time constant, formed by the V_{IN} pin resistor and capacitor, controls the soft start time. Ramp up rate from 0% to 90% of nominal V_{OUT} is:

$$t_{SS} = 2.3 \bullet R_{IN} \bullet C_{IN}$$

If the fast start functionality is used (see next section) then the soft-start time is dependent on the amount of the capacitor used and the voltage input at the FS pin. In this case the ramp up rate to within 10mV of nominal V_{OUT} is:

$$t_{SS(FS)} = C_{IN} \bullet V_{FS}/10mA$$

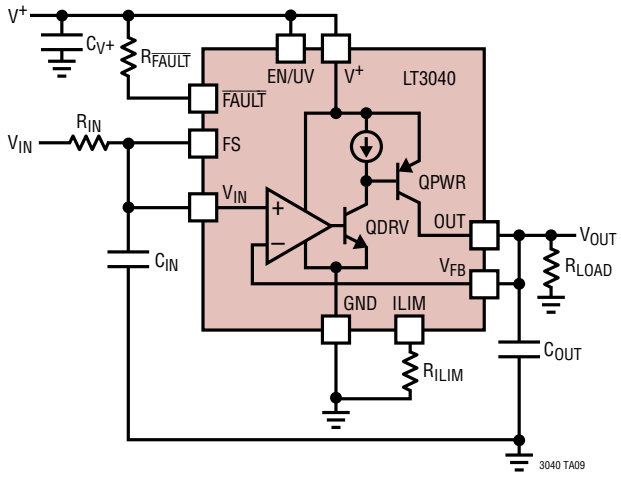

Figure 9. Low Pass Filter with Fast-Startup Disabled

Fast Start

For ultralow noise applications that require low 1/f noise, a V_{IN} filter with a very low frequency pole may be necessary. This significantly increases the start-up time in accordance with the RC time constant of the V_{IN} filter. The LT3040 incorporates fast start-up circuitry that sources the V_{IN} pin with a typical current of 10mA during start-up to rapidly charge the filter capacitor, decreasing start-up time.

The 10mA current source turns on if the FS to V_{IN} differential is greater than 100mV and remains engaged if the FS pin is greater than the V_{IN} pin by 7mV. This current decreases to 0mA as V_{IN} pin charges to the FS pin voltage. If the regulator is in current limit, dropout, thermal shutdown or if supply voltage is below minimum V^+, the fast start function is disabled.

While using the fast start functionality, if the V_{IN} slew rate approaches the FS slew rate during startup, the V_{IN} pin voltage may catch up to the FS pin while FS is rising. This will shut off the fast start current until FS rises ~100mV above V_{IN}. This is intended operation. This turn on and turn off will cause stair stepping at the V_{IN} pin

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voltage. Increasing the V_{IN} cap value will smooth the V_{IN} pin start-up.

If fast start-up capability is not used, tie FS to V_{IN}.

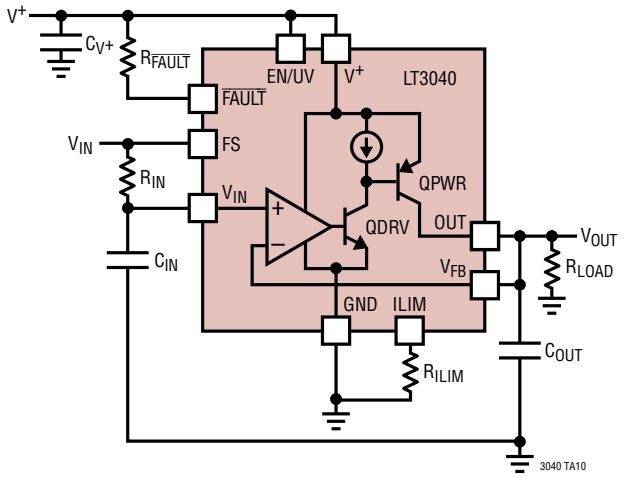

Figure 10. Low Pass Filter with Fast-Startup Enabled

V_{IN} Slew Rate

The LT3040's error amplifier is bandwidth limited. If the V_{IN} pin slews too fast in the positive direction, the error amplifier reacts and enters current limit. If the V_{IN} pin voltage stops slewing, the LT3040's bandwidth limitation causes the output to overshoot significantly before settling into regulation. In order to avoid undesirable overshoots at the output, ADI recommends limiting the V_{IN} pin slew rate to less than or equal to 1V/µs.

A similar behavior is expected for negative slew rates on the V_{IN} pin where the output undershoots significantly. If V_{IN} slews fast in the negative direction, the error amplifier shuts off and the output discharge is a function of the LT3040's load current. Thus, larger undershoots are expected at heavier load conditions.

To limit slew rates when using the fast start functionality of the LT3040, the minimum C_{IN} requirement is governed by:

$$100mA \bullet C_{OUT}/ILIM \leq C_{IN}$$

where ILIM is the output current limit. The internal current limit for LT3040 is around 280mA (180mA in foldback).

When using a minimum output capacitor without any external current limit, use at least 2.2µF capacitor at the V_{IN} pin if using the fast start circuitry. This capacitor limits the slew rate on the V_{IN} pin while also ensuring that the V_{IN} pin doesn't overshoot during fast start up. For applications with lower current limit or higher output capacitance, a larger V_{IN} capacitor is required.

Power Supply Sequencing

The LT3040 is able to withstand voltages as high as the Absolute Maximum rating on the FS and V_{IN} pins even when the part is turned off. However, for optimum application performance and to protect the peripheral circuitry used with the LT3040, ADI recommends that the LT3040 is powered up (or enabled) before or in sync with the voltage application at V_{IN}. During turn-off, ADI recommends powering down V_{IN} before or in sync with the LT3040.

The LT3040's V_{IN} pin is internally clamped to the V_{FB} pin (typical clamp voltage of 1.5V), if V_{IN} is powered while the LT3040 is shutdown, there is a possibility that the Absolute Maximum rating for the voltage differential from V_{IN} to V_{FB} or the current rating (max 20mA) on the V_{IN} and V_{FB} pins or both may be exceeded; damaging the part.

In applications where the V_{IN} supply is not current limited to less than or equal to 20mA, connect a protection resistor from the Voltage Source (Voltage Reference/Voltage Output DAC) to the FS/V_{IN} pin. Use a minimum resistor of 50Ω/V to limit the current below the Abs Max Rating of 20mA for the V_{IN} to V_{FB} clamp. For example, if connecting a 5V reference use at least a 250Ω (5V • 50Ω/V) resistor. If the V_{IN} pin is powered high while LT3040 is in shutdown, the DC current flowing through the internal V_{IN} to V_{FB} clamp may pull output above ground.

Filtering High Frequency Spikes

For applications where the LT3040 is used to post-regulate a switching converter, its high PSRR effectively suppresses any "noise" present at the switcher's switching frequency — typically 100kHz to 4MHz. However, the very high frequency (100s of MHz) "spikes" — beyond the LT3040's bandwidth — associated with the switcher's power switch transition times will almost directly pass

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through the LT3040. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (e.g. 0.5˝) PCB trace between the switcher's output and the LT3040's input can serve as an LC-filter to suppress these very high frequency spikes.

Enable/UVLO

The EN/UV pin is used to put the buffer into a micro-power shutdown state. The LT3040 has an accurate 1.24V turn-on threshold on the EN/UV pin with 170mV of hysteresis. This threshold can be used in conjunction with a resistor divider from the V^+ supply to define an accurate under-voltage lockout (UVLO) threshold for the buffer. The EN/UV pin current (I_{EN}) at the threshold from the Electrical Characteristics table needs to be considered when calculating the resistor divider network:

$$V^+_{(UVLO)} = 1.24V \bullet (1+(R_{EN2}/R_{EN1})) + I_{EN} \bullet R_{EN2}$$

The EN/UV pin current (I_{EN}) can be ignored if R_{EN1} is less than 75kΩ. If unused, tie EN/UV pin to V^+.

Externally Programmable Current Limit

The ILIM pin's current limit threshold is 300mV. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which in turn programs the LT3040's current limit. The programming scale factor is 125mA • kΩ. For example, a 1kΩ resistor programs the current limit to 125mA and a 2kΩ resistor programs the current limit to 62.5mA. For good accuracy, Kelvin connect this resistor to the LT3040's GND pin.

In cases where V^+-to-OUT differential is greater than 12V, the LT3040's foldback circuitry decreases the internal current limit. As a result, internal current limit may over-ride the externally programmed current limit level to keep the LT3040 within its safe-operating-area (SOA). See the Internal Current Limit vs Supply-to-Output Differential graph in the Typical Performance Characteristics section.

As shown in the Block Diagram, the ILIM pin sources current proportional (1:400) to output current; therefore, it also serves as a current monitoring pin with a 0V to 300mV range. If external current limit or current monitoring is not used, tie ILIM to GND.

Output Overshoot Recovery

During a load step from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn the power transistor OFF. Given that there is no load (or very light load) present at the output, it takes a long time to discharge the output capacitor.

As illustrated in the Block Diagram, the LT3040 incorporates an overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event V_{FB} is higher than V_{IN}. This current is typically about 4mA. No load recovery is disabled for supply voltages less than 2.5V or output voltages less than 1.5V.

If V_{FB} is externally held above V_{IN}, the current sink turns ON in an attempt to restore V_{FB} to its programmed voltage. The current sink remains ON until the external circuitry releases V_{FB}.

Output Source and Sink

The LT3040 is capable of sourcing 200mA of current. However, the LT3040 does not support a current sink capability. Although the output overshoot recovery circuit can typically sink 4mA of current, this capability is triggered only for AC loop perturbations. For a DC current sink capability tie a resistor from OUT to GND.

Direct Paralleling for Higher Current

Higher output current is obtained by paralleling multiple LT3040s. Tie all V_{IN} pins together and all V^+ pins together.

Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3040s. PCB trace resistance in mΩ/inch is shown in Table 1.

Table 1. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in

APPLICATIONS INFORMATION

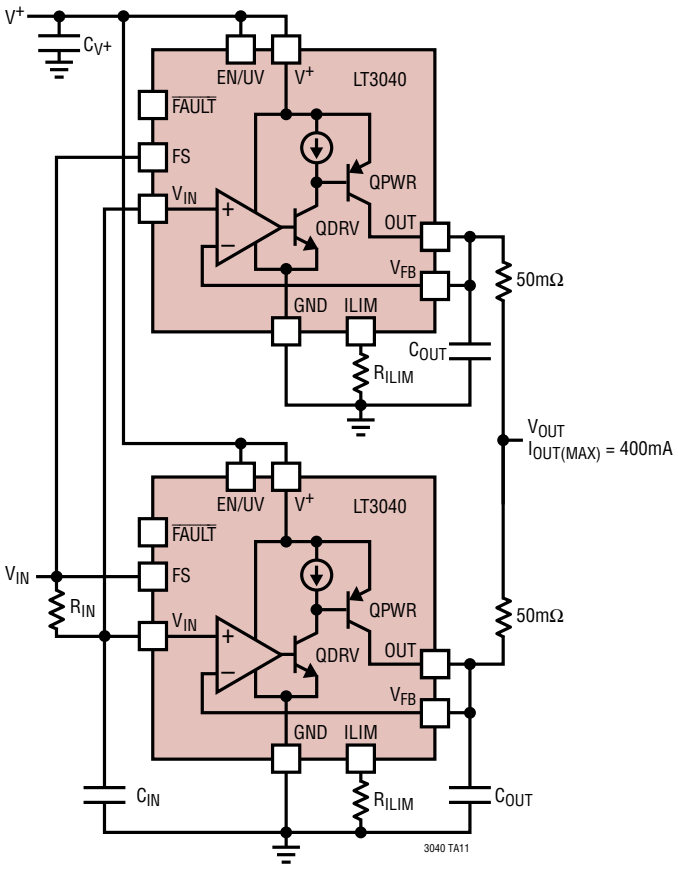

Figure 11. Parallel Devices

The small worst-case offset of 0.3mV for each paralleled LT3040 minimizes the required ballast resistor value. Figure 11 illustrates that two LT3040s, each using a 50mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 50mΩ external resistors only add 10mV of output regulation drop with a 400mA maximum current. With a 3.3V output, this only adds 0.3% to the regulation accuracy. As has been discussed previously, tie the V_{FB} pin directly to the output capacitor.

More than two LT3040s can also be paralleled for even higher output current and lower output noise. Paralleling multiple LT3040s is also useful for distributing heat on the PCB. For applications with high supply-to-output voltage differential, an input series resistor or resistor in parallel with the LT3040 can also be used to spread heat.

PCB Layout Considerations

Given the LT3040's high bandwidth and ultrahigh PSRR, careful PCB layout must be employed to achieve full device performance. Figure 12 shows an example layout that delivers full performance of the regulator. Refer to the LT3040's DC2783A demo board manual for further details.

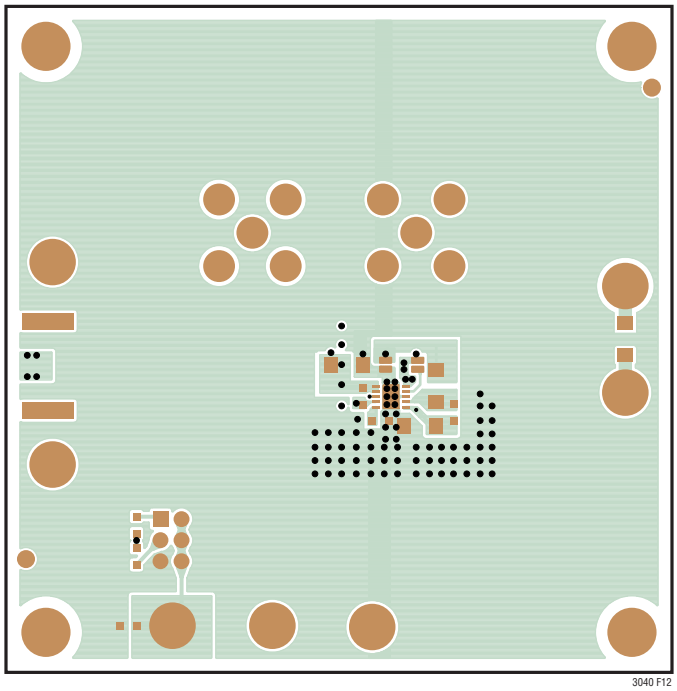

Figure 12. Example DFN Layout

Thermal Considerations

The LT3040 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 162°C with about 8°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature, (125°C for E-, I-grades). It is important to consider all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources in close proximity to the LT3040.

The undersides of the DFN and MSOP packages have exposed metal from the lead frame to the die attachment. Both packages allow heat to directly transfer from the die

APPLICATIONS INFORMATION

junction to the PCB metal to limit maximum operating junction temperature.The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by the regulator.

Table 2 and Table 3 list thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4 layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 2. Measured Thermal Resistance for DFN Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm^2	2500mm^2	2500mm^2	34°C/W
1000mm^2	2500mm^2	2500mm^2	34°C/W
225mm^2	2500mm^2	2500mm^2	35°C/W
100mm^2	2500mm^2	2500mm^2	36°C/W

*Device is mounted on top side

Table 3. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm^2	2500mm^2	2500mm^2	33°C/W
1000mm^2	2500mm^2	2500mm^2	33°C/W
225mm^2	2500mm^2	2500mm^2	34°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on top side

Calculating Junction Temperature

Example: Given an output voltage of 2.5V and supply voltage of 5V ± 5%, output current range from 1mA to 200mA and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The LT3040's power dissipation is:

$$I_{OUT(MAX)} \bullet (V^+_{(MAX)} - V_{OUT}) + I_{GND} \bullet V^+_{(MAX)}$$

where:

$I_{OUT(MAX)}$ = 200mA $V^+_{(MAX)}$ = 5.25V

I_{GND} (at I_{OUT} = 200mA and V^+ = 5.25V) = 7.2mA

thus:

$$P_{DISS} = 0.2A \bullet (5.25V - 2.5V) + 7.2mA \bullet 5.25V = 0.59W$$

Using a DFN package, the thermal resistance is in the range of 34°C/W to 36°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

$$0.59W \bullet 35°C/W = 20.7°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{JMAX} = 85°C + 20.7°C = 105.7°C$$

Overload Recovery

Like many IC power regulators, the LT3040 incorporates safe-operating-area (SOA) protection. The SOA protection activates at supply-to-output differential voltages greater than 12V. The SOA protection decreases the current limit as the supply-to-output differential increases and keeps the power transistor inside a safe operating region for all values of supply-to-output voltages up to the LT3040's absolute maximum ratings. The LT3040 provides some level of output current for all values of supply-to-output differentials. Refer to the Current Limit curves in the Typical Performance Characteristics section. When power is first applied and supply voltage rises, the output follows the supply and keeps the supply-to-output differential low to allow the regulator to supply large output current and start-up into high current loads.

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Due to current limit foldback, however, at high supply voltages a problem can occur if the output voltage is low and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the supply voltage has already turned ON. The load line in such cases intersects the output current profile at two points. The regulator now has two stable operating points. With this double intersection, the power supply may need to be cycled down to zero and brought back up again to make the output recover. Other linear regulators with foldback current limit protection (such as the LT1965 and LT1963A, etc.) also exhibit this phenomenon, so it is not unique to the LT3040.

Protection Features

The LT3040 incorporates several protection features for battery-powered applications. Precision current limit and thermal overload protection protect the LT3040 against overload and fault conditions at the device's output. For normal operation, do not allow the junction temperature to exceed 125°C (E-, I-grade).

To protect the LT3040's low noise error amplifier, the V_{IN}-to-V_{FB} protection clamp limits the maximum voltage between V_{IN} and V_{FB} to ±1.5V with a maximum DC current of 20mA through the clamp. So, for applications where V_{IN} is actively driven by a voltage source, the voltage source must be current limited to 20mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the V_{IN} pin capacitor (C_{IN}) to 22µF.

The LT3040 also incorporates reverse supply protection whereby the V^+ pin withstands reverse voltages of up to –20V without causing any supply current flow and without developing negative voltages at the OUT pin. The regulator protects both itself and the load against batteries that are plugged-in backwards.

In circuits where a backup battery is required, several different output to supply conditions can occur. The output voltage may be held up while the supply is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all of these cases, the reverse current protection circuitry prevents current flow from output to the supply.

Nonetheless, due to the V_{FB}-to-V_{IN} clamp, unless the V_{IN} pin is floating, current can flow to GND through the bypass resistor as well as up to 15mA to GND through the output overshoot recovery circuitry. This current flow through the output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between V_{FB} and V_{IN} pins, with its anode at the V_{FB} pin.

Long Term Drift

Long term drift is a settling of the offset voltage while the part is powered up. The offset slowly drifts at levels of µV. The first 1000 hours of being powered up sees the most shift. By the end of 3000 hours, most parts have settled and will not shift appreciably. The plot in Figure 13 is representative of the LT3040 long term drift.

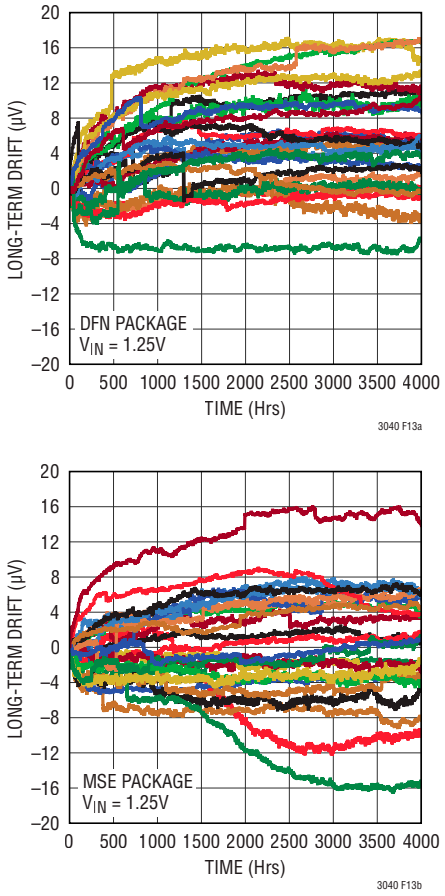

Figure 13. LT3040 Long Term Drift

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IR Reflow Shift

As with many precision devices, the LT3040 will experience an offset voltage shift when soldered to a PCB. This shift is caused by uneven contraction and expansion of the plastic mold compound against the die and the copper pad underneath the die. Critical devices in the circuit will experience a change of physical force or pressure, which in turn changes its electrical characteristics, resulting in subtle changes in circuit behavior. Lead free solder reflow profiles reach over 250°C, which is considerably higher than lead based solder. A typical lead-free IR reflow profile is shown in Figure 14. The experimental results simulating this shift are shown in Figure 15. In this experiment, LT3040 is run through IR reflow oven once.

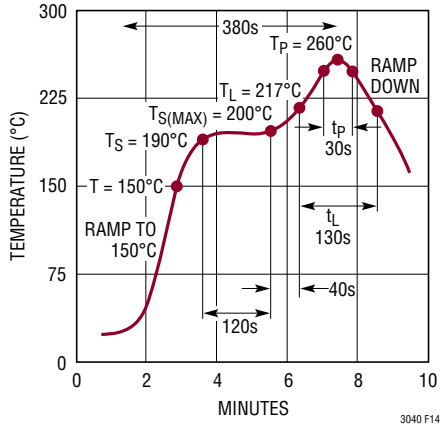


Figure 14. IR Reflow Profile

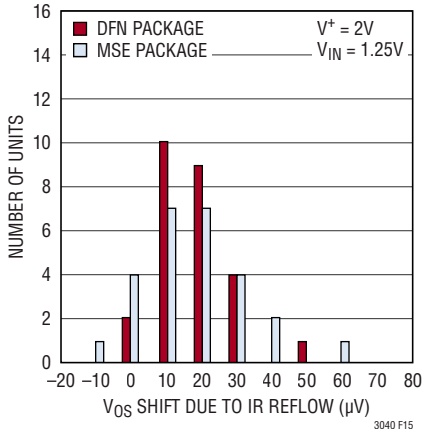


Figure 15. ΔV_{OS} due to IR Reflow

Thermal Hysteresis

Thermal hysteresis is caused by the same effect as IR reflow shift. However, in the case of thermal hysteresis, the temperature is cycled between its specified operating extremes to simulate how the part will behave as it experiences extreme temperature excursions and then returns to room temperature. For example, the LT3040 rated for –40°C to 125°C was repeatedly cycled between 125°C and –40°C. Figure 16 illustrates the thermal hysteresis of the LT3040, where each time the part's temperature passed through 25°C after cold and hot excursions, the offset voltage was recorded.

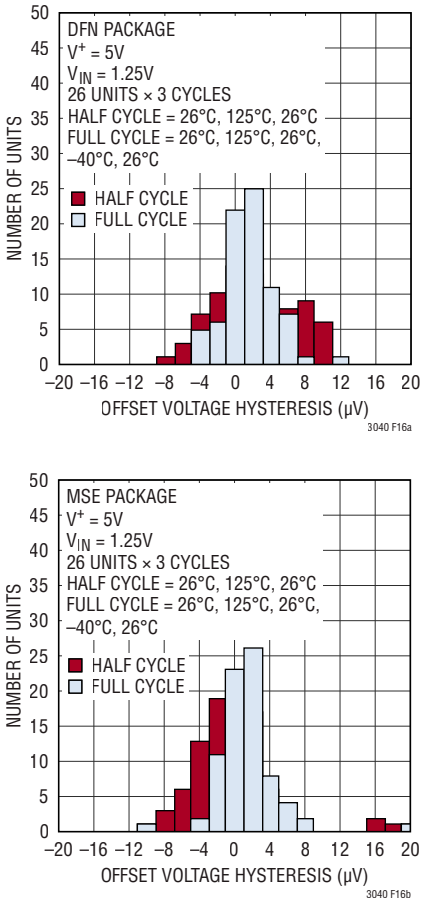
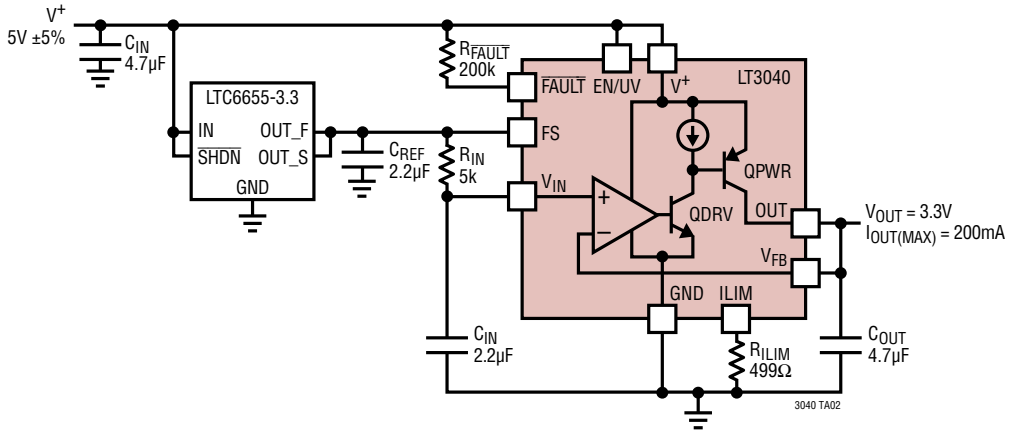


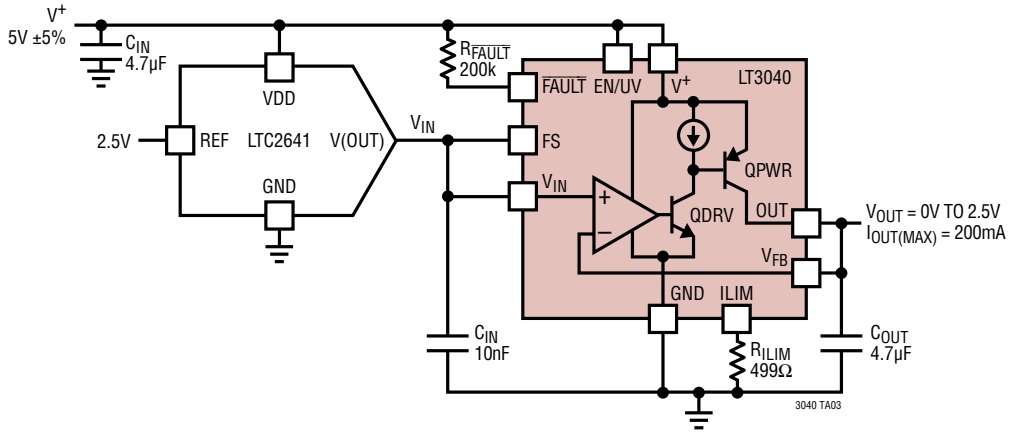
Figure 16. Input Offset Thermal Hysteresis

TYPICAL APPLICATIONS

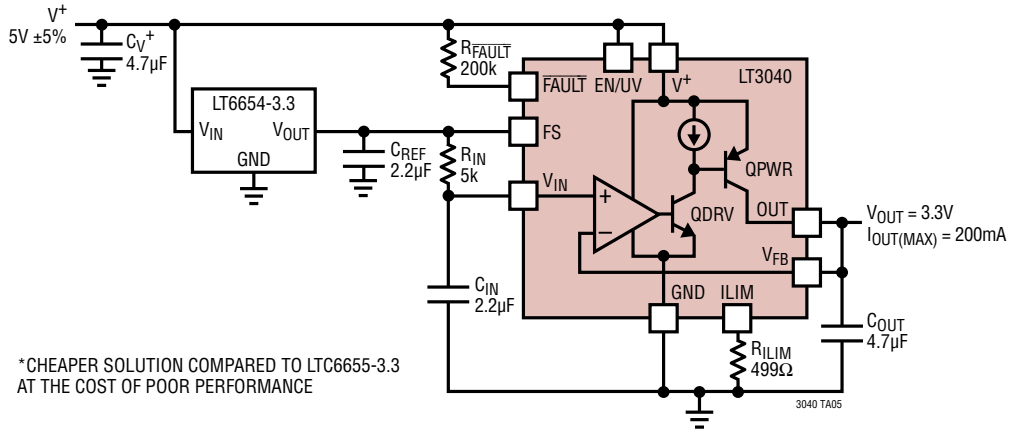
200mA 3.3V Precision Reference



200mA 0V to 2.5V Precision DAC



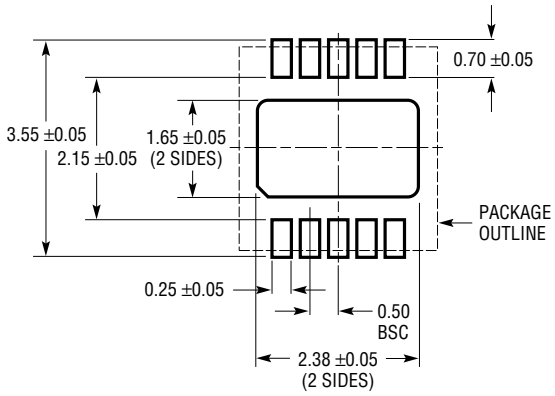
200mA 3.3V Precision Reference*



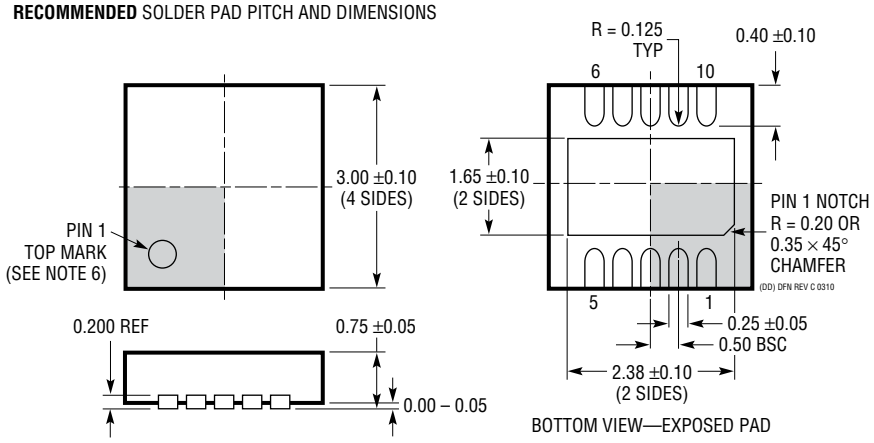
*CHEAPER SOLUTION COMPARED TO LTC6655-3.3
AT THE COST OF POOR PERFORMANCE

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



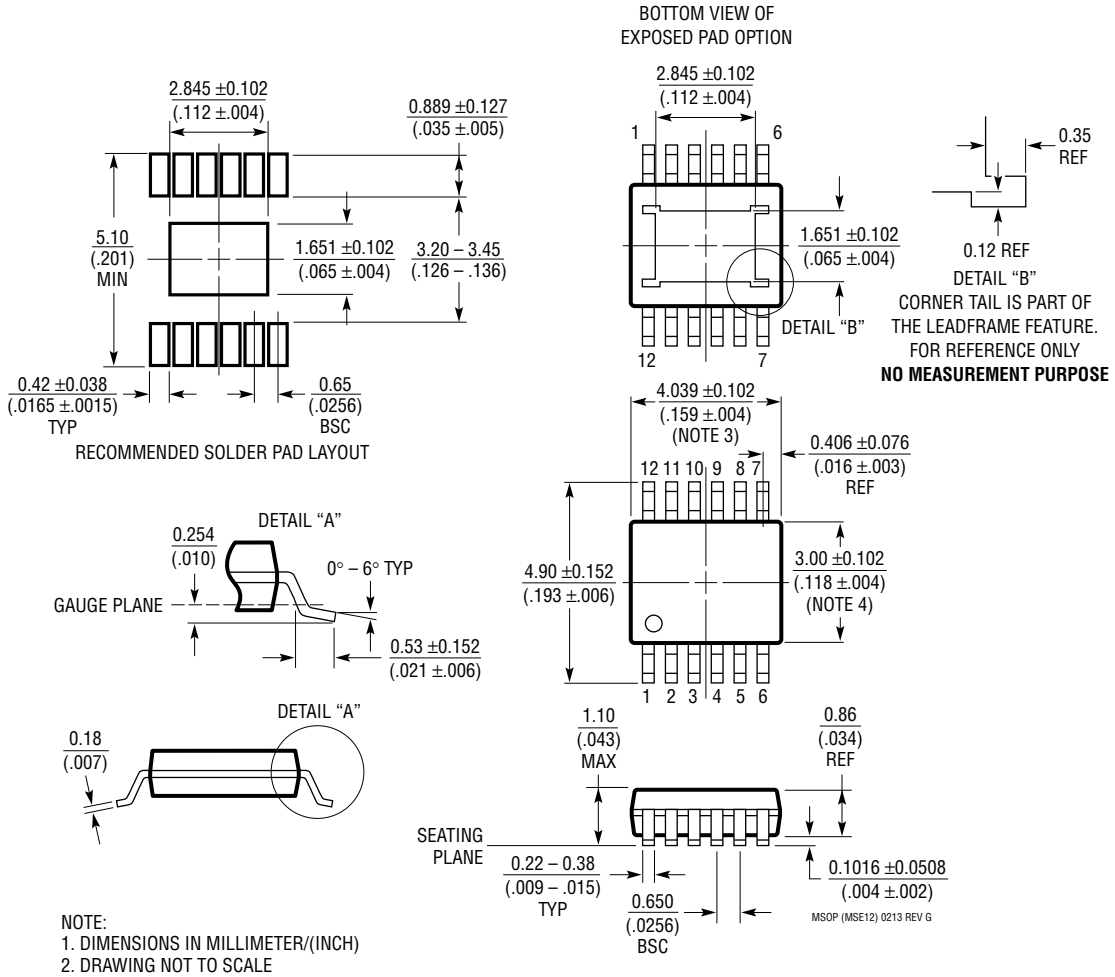
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

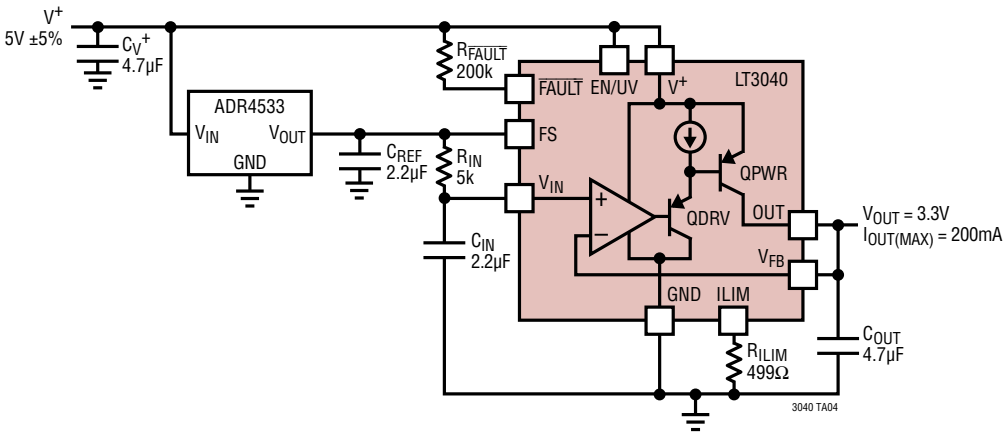
PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3050	100mA LDO with Diagnostics and Precision Current Limit	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.8V to 45V, 3mm × 2mm DFN and MSOP Packages
LT3060	100mA Low Noise LDO with Soft-Start	300mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.8V to 45V, 2mm × 2mm DFN and ThinSOT Packages
LT3082	200mA, Parallelable, Low Noise LDO	Outputs May Be Paralleled for Higher Output Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 2.2µF, Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; MS8E and 2mm × 3mm DFN-6 Packages
LT3042	200mA, Ultralow Noise and Ultrahigh PSRR LDO	0.8µV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm × 3mm DFN and MSOP Packages
LT6658	36V, Dual Output (150mA/50mA) Low Noise Buffered Voltage Reference	0.05% Max, 10ppm/°C Max Drift, 1.5ppm$_{P-P}$ Noise (0.1Hz to 10Hz), 1.2V/1.8V/2.5V/3.3V/5V Versions, MSOP-16E Package
LTC6655	Precision Low Noise Reference	2ppm/°C Max, 650nV_{P-P} Noise (0.1Hz to 10Hz) 100% Tested at 25°C, –40°C and 125°C
LTC2641	Single 16-/14-/12-Bit V_{OUT} DACs with ±1LSB INL, DNL	±1LSB (Max) INL, DNL, 3mm x 3mm DFN and MSOP Packages, 120µA Supply Current, SPI Interface

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Analog Devices Inc.:

LT3040IDD#TRPBF LT3040EMSE#TRPBF LT3040IMSE#TRPBF LT3040EDD#PBF LT3040EDD#TRPBF LT3040EMSE#PBF LT3040IDD#PBF LT3040IMSE#PBF DC2783A