EV-ADF4371SD2Z User Guide

UG-1474

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Evaluating the ADF4371 Microwave Wideband Synthesizer with Integrated VCO

FEATURES

Selfcontained board, including ADF4371 frequency synthesizer with integrated VCO, loop filter (180 kHz), USB interface, and voltage regulators
Windows®-based software allows control of synthesizer functions from a PC
Externally powered by 6 V

EVALUATION KIT CONTENTS

EV-ADF4371SD2Z evaluation board

EQUIPMENT NEEDED

Windows-based PC with USB port for evaluation software
System demonstration platform, serial only (SDP-S)
EVAL-SDP-CS1Z controller board
Power supply (6 V)
Spectrum analyzer
50 Ω terminators
Low noise REF_{IN} source (optional)

DOCUMENTS NEEDED

ADF4371 data sheet
EV-ADF4371SD2Z user guide

REQUIRED SOFTWARE

ACE software, Version 1.10 or newer
ADF4371 plugin, Version 0.1.6 or newer

GENERAL DESCRIPTION

The EV-ADF4371SD2Z evaluates the performance of the ADF4371 frequency synthesizer with an integrated voltage controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the evaluation board is shown in Figure 1. The evaluation board contains the ADF4371 frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, and subminiature Version A (SMA) connectors.

This board requires an SDP-S board (not supplied with the kit). The SDP-S allows software programming of the EV-ADF4371SD2Z device.

Full specifications for the ADF4371 frequency synthesizer are available in the product data sheet, which must be consulted in conjunction with this user guide when working with the evaluation board.

EV-AD4371SD2Z EVALUATION BOARD PHOTOGRAPH

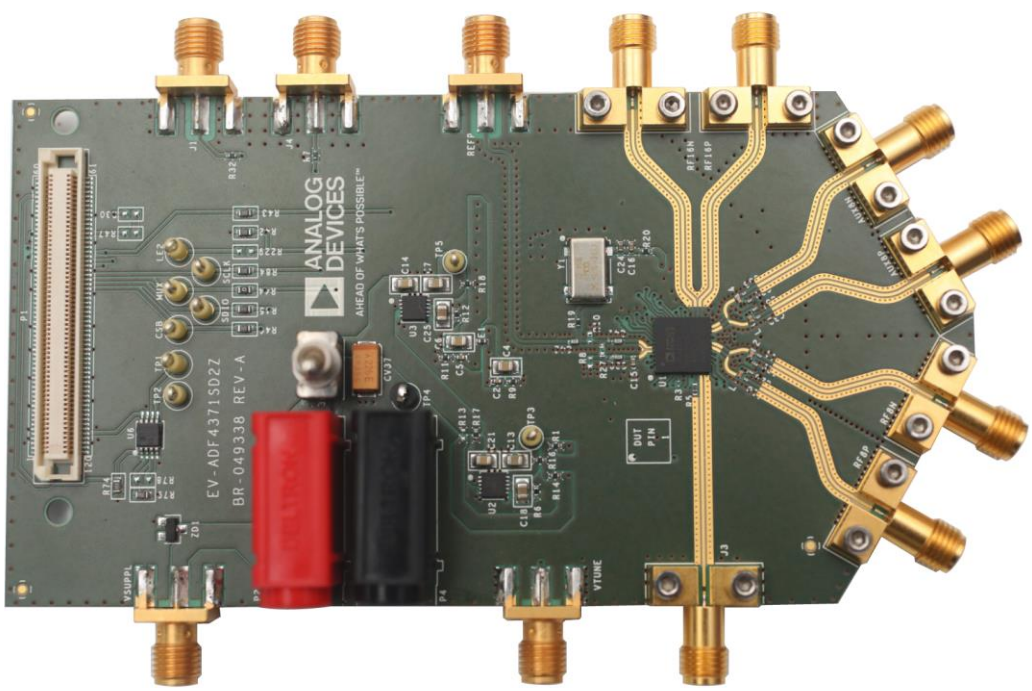

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Figure 1.

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REVISION HISTORY

1/2019—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

To install the ACE software and ADF4371 plugin, perform the following steps:

1. Install the latest version of the ACE software platform.
2. If the ADF4371 plugin appears automatically, proceed to Step 4.
3. Double click the ADF4371 plugin file, **Board.ADF371.0.1.6.acezip**.
4. Check that the ADF4371 plugin appears when the EV-ADF4371SD2Z board is attached through the system demonstration platform (SDP) connector to the PC.

EVALUATION BOARD SETUP PROCEDURES

To run the software, perform the following steps:

1. Select **Start** > **All Programs** > **Analog Devices** > **ACE**.
2. On the **Select Device and Connection** tab, choose **ADF4371** and the **ADF4371 board** appears under attached hardware.
3. When connecting the EV-ADF4371SD2Z board, allow 5 sec to 10 sec for the label on the status bar to change.

EVALUATION BOARD HARDWARE

The EV-ADF4371SD2Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z. The SDP-B is not recommended.

The EV-ADF4371SD2Z schematics are shown in Figure 10, Figure 11, Figure 12, and Figure 13. The silkscreens for the evaluation board are shown in Figure 14 and Figure 15.

POWER SUPPLIES

The EV-ADF4371SD2Z board is powered by a 6 V power supply connected to the VSUPPL SMA, or the red banana plug, P2. Connect GND to the black banana plug, P4.

The power supply circuitry has two LT3045, high performance, low noise, and low dropout (LDO) regulators.

One LT3045 is used to generate 5 V to drive the VCO supply pins. The remaining supplies are powered from the other LT3045, which is set to 3.3 V voltage.

Use Switch S1 to switch the 6 V to the board on and off.

RF OUTPUT

The EV-ADF4371SD2Z has three pairs of SMA, 3.5 mm output connectors: RF8P/RF8N, AUX8P/AUX8N, and RF16P/RF16N (differential outputs). The EV-ADF4371SD2Z board has one single 2.92 mm connector, J3, for the RF32P pin. RF32 is also differential, but the RF32N pin is terminated by a 50 Ω on-board resistor. Because they are sensitive to impedance mismatch, connect the radio frequency (RF) outputs to equal load impedances.

If only one port of a differential pair is used, terminate the complementary port with an equal load terminator (in general, a 50 Ω terminator).

LOOP FILTER

The loop filter schematic is included in the board schematic in Figure 10. Figure 2 shows the loop filter component placement. The loop filter on the evaluation board is optimized for fractional mode performance with a phase frequency detector (PFD) frequency of 100 MHz and 1.8 mA charge pump current. The values of the loop filter components are as follows:

- Resistors: RCPOUT = 91 Ω, R2 = 400 Ω, R4 = 200 Ω, R15 = 0 Ω
- Capacitors: C20 = 220 pF, C19 = 0.018 μF, C23 = 330 pF

The lowest rms jitter is achieved in integer mode by using a high PFD frequency. This jitter can be tested by using the same filter with a PFD frequency of 200 MHz (enabling the doubler) and 2.4 mA charge pump current. Additional optimization is still possible depending on target frequency and integration limits.

In general, narrower loop filter bandwidths have lower spurious signals. Wide loop filters in integer N mode can achieve <50 fs jitter with very clean reference frequency input (REF_{IN}) signals.

ADDITIONAL OPTIMIZATION ON LOOP FILTER

The PLL loop bandwidth can be optimized for different parameters like reference spurs or VCO noise, depending on the system requirements.

Reducing Σ-Δ Modulator (SDM) Noise

In fractional mode, SDM noise becomes apparent and starts to contribute to overall phase noise. This noise can be reduced to insignificant levels by using a series resistor between the CPOUT pin and the loop filter. Place this resistor close to the CPOUT pin. Select a reasonable resistor value that does not affect the loop bandwidth and phase margin of the designed loop filter. In most cases, a 91 Ω resistor value produces the best results. This resistor is not required in integer mode (SDM not enabled) or when a narrow-band loop filter (SDM noise attenuated) is used. This resistor is labeled as RCPOUT in schematics.

Optimizing Spurious Signals

On the evaluation board, the loop filter is placed at the secondary side of the board to create a more compact layout and so that the board is more tolerant to external signals. Using a capacitor on the same side with the ADF4371 (the primary side) results in higher isolation on internally generated spurious signals. For this purpose, a small valued capacitor (10 pF) can be placed close to the VTUNE pin to achieve lower spurious signal levels.

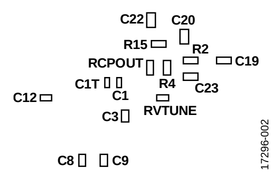

Figure 2. Loop Filter Component Placement

REFERENCE SOURCE

The EV-ADF4371SD2Z board is supplied with a low noise 100 MHz crystal oscillator (XO) from Crystek (CCHD-575-50-100.000).

To use an external single-ended REF_{IN}, connect a low noise reference source to the REFP SMA connector. Remove Resistor R19 (0 Ω) and Resistor R20 (0 Ω) to remove power from the crystal and break the connection to the REFP input.

DEFAULT CONFIGURATION

All components necessary for local oscillator (LO) generation are inserted on the EV-ADF4371SD2Z board. The EV-ADF4371SD2Z board is shipped with 100 MHz XO, the ADF4371 synthesizer with an integrated VCO, and a 180 kHz loop filter (charge pump current (I_{CP}) = 1.8 mA).

DOUBLER AND QUADRUPLER OUTPUT

The ADF4371 contains a frequency doubler and quadrupler to double the 4 GHz to 8 GHz VCO signal on RF16P and RF16N and quadruple the VCO signal on RF32P and RF32N. It is advised to not enable the doubler and quadrupler at the same time.

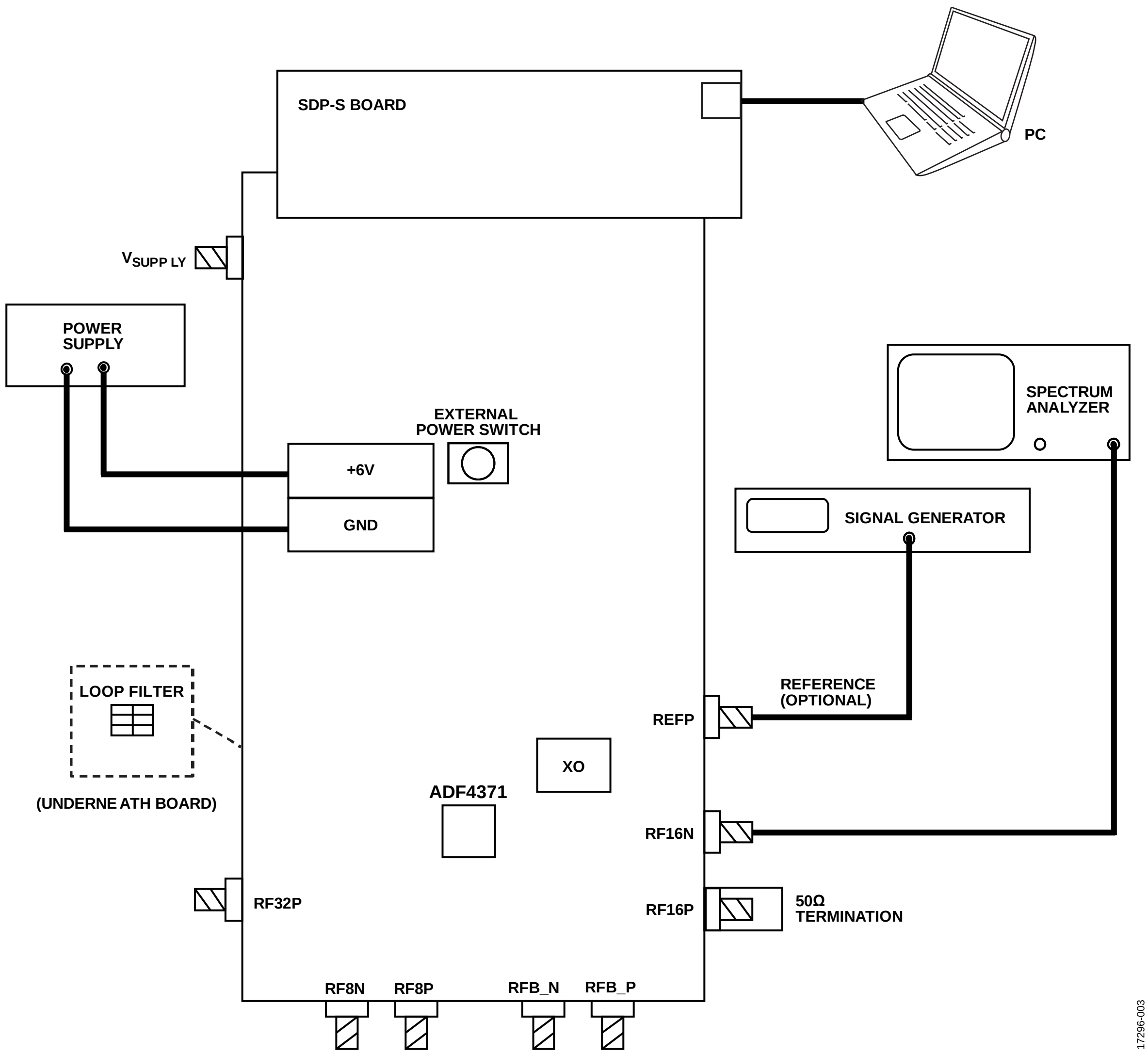

Figure 3. Evaluation Board Setup Diagram

EVALUATION BOARD SOFTWARE

The ACE software is the main platform that is used to control the EV-ADF4371SD2Z. The ADF4371 plugin includes user interfaces that relate to the ADF4371 and allow evaluation of the device. Use the following steps to open the main control window for ADF4371.

1. Launch the ACE application. With the SDP-S board connected to the EV-ADF4371SD2Z, the attached hardware appears in the graphical user interface (GUI) as shown in Figure 4.
2. Double click the **ADF4371 Board** icon, and the tab shown in Figure 5 appears.
3. Double click the **ADF4371** icon that appears on the board GUI to open the main control window shown in Figure 8.

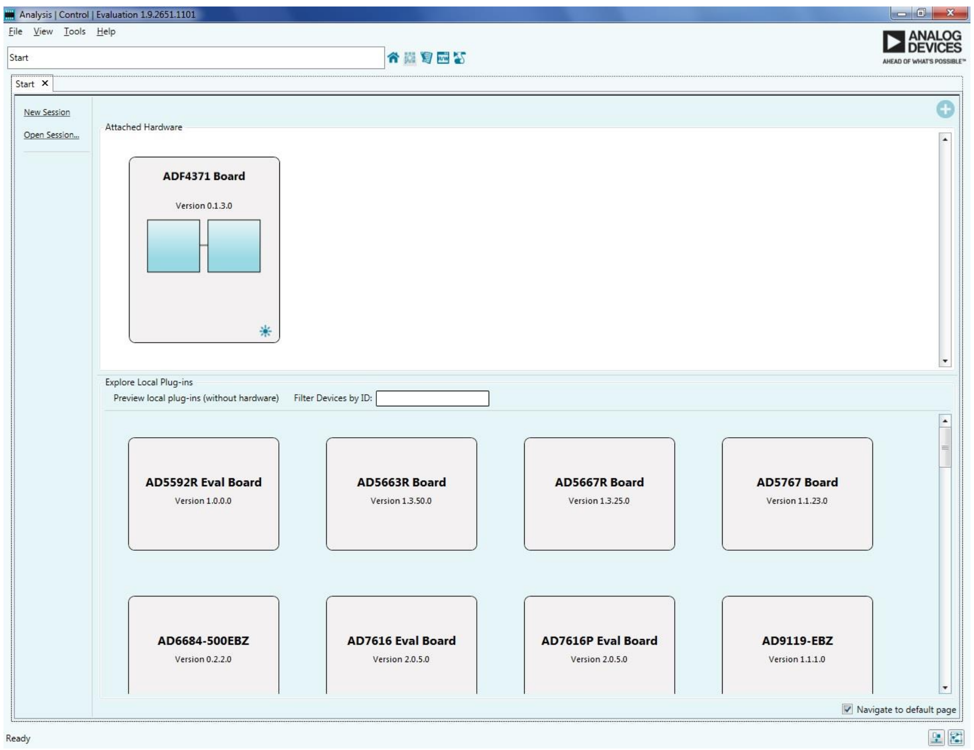

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Figure 4. ACE Start Page, Attached Hardware (ADF4371 Evaluation Board)

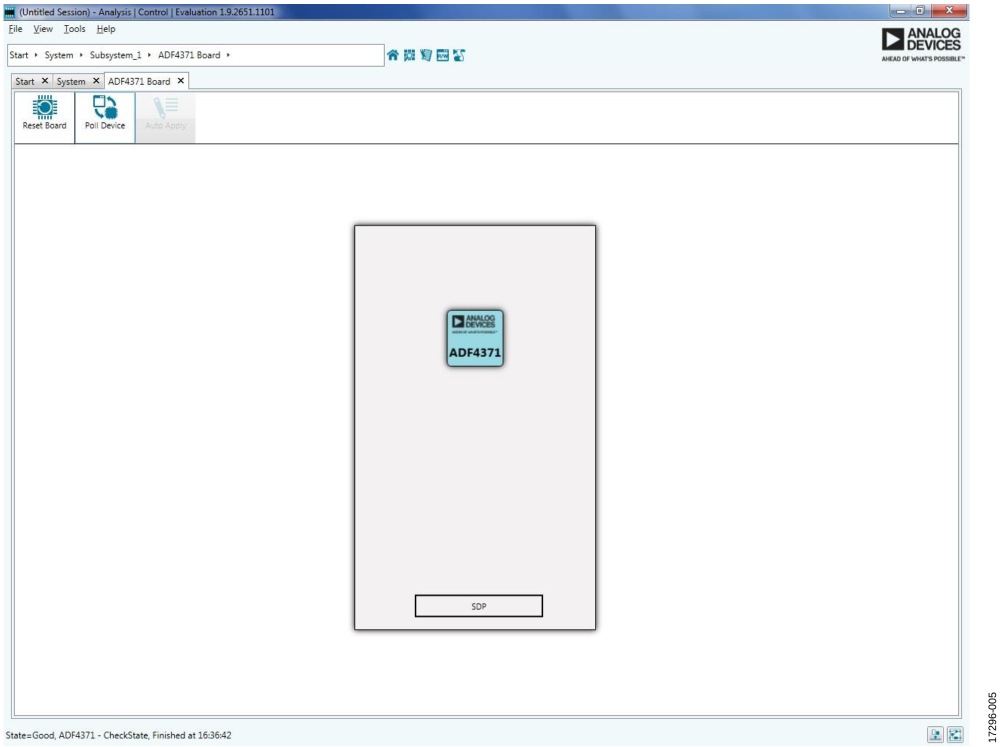


Figure 5. ACE Board Page, Device Selection

MAIN CONTROLS

The main controls are available in the high level register map shown in Figure 8. To modify registers, perform the following steps:

1. Click **Write All Registers / Initialize** to load all registers and initialize the device.
2. Modify the registers as desired.
3. Click **Apply Changes** to load modified settings to the device. This action loads the updated registers only. All registers can be reloaded using the **Write All Registers / Initialize** button.

QUADRUPLER OUTPUT CONTROLS

For the main, auxiliary, and doubler outputs, the optimal harmonic performance is achieved by using the automatic filter outputs. However, for the quadrupler output, some additional software settings may need to be adjusted to achieve optimal performance.

The settings are available in the **Outputs** section (shown in Figure 6). The output settings include the **Tracking Filter Mux** box that can be set to automatic or manual, the **Quad Bias** box that varies from the lowest setting 0 to the highest of 3, and the **Quad Band Filter** box that varies from 0 to 7.

The bias and filter settings in Table 1 are recommended for quadrupler output.

Table 1. Filter and Bias Setting for Quadrupled Output

Frequency (GHz)	Filter	Bias
<18	7	3
18 to 19	3	3
19 to 20.5	1	0
20.5 to 26	0	0
>26	0	1

The recommended settings for quadrupler frequencies from 16 GHz to 18 GHz are shown in Figure 6. The summarized filter performance is shown in Figure 7.

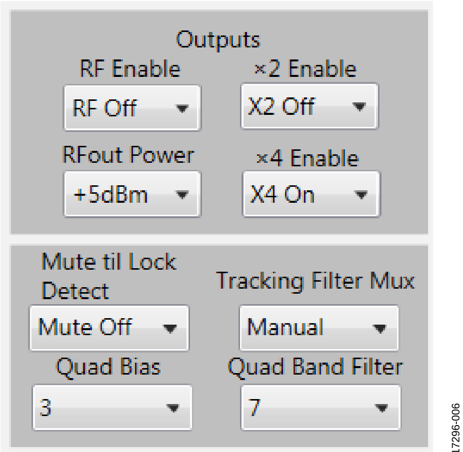


Figure 6. Recommended Quadrupler Filter Settings, 16 GHz to 18 GHz

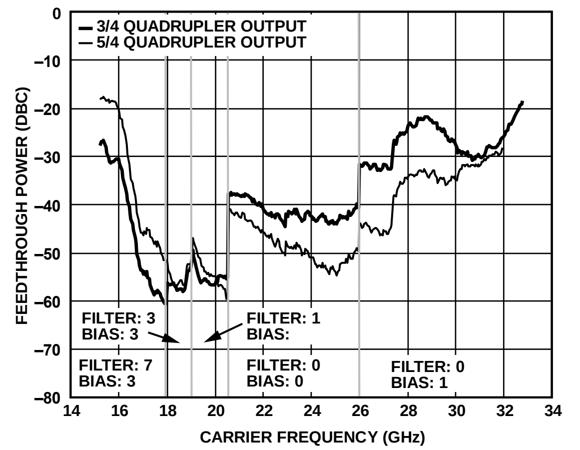


Figure 7. Aggregated Quadrupler Filter Performance, 3/4 Quadrupler Output and 5/4 Quadrupler Output

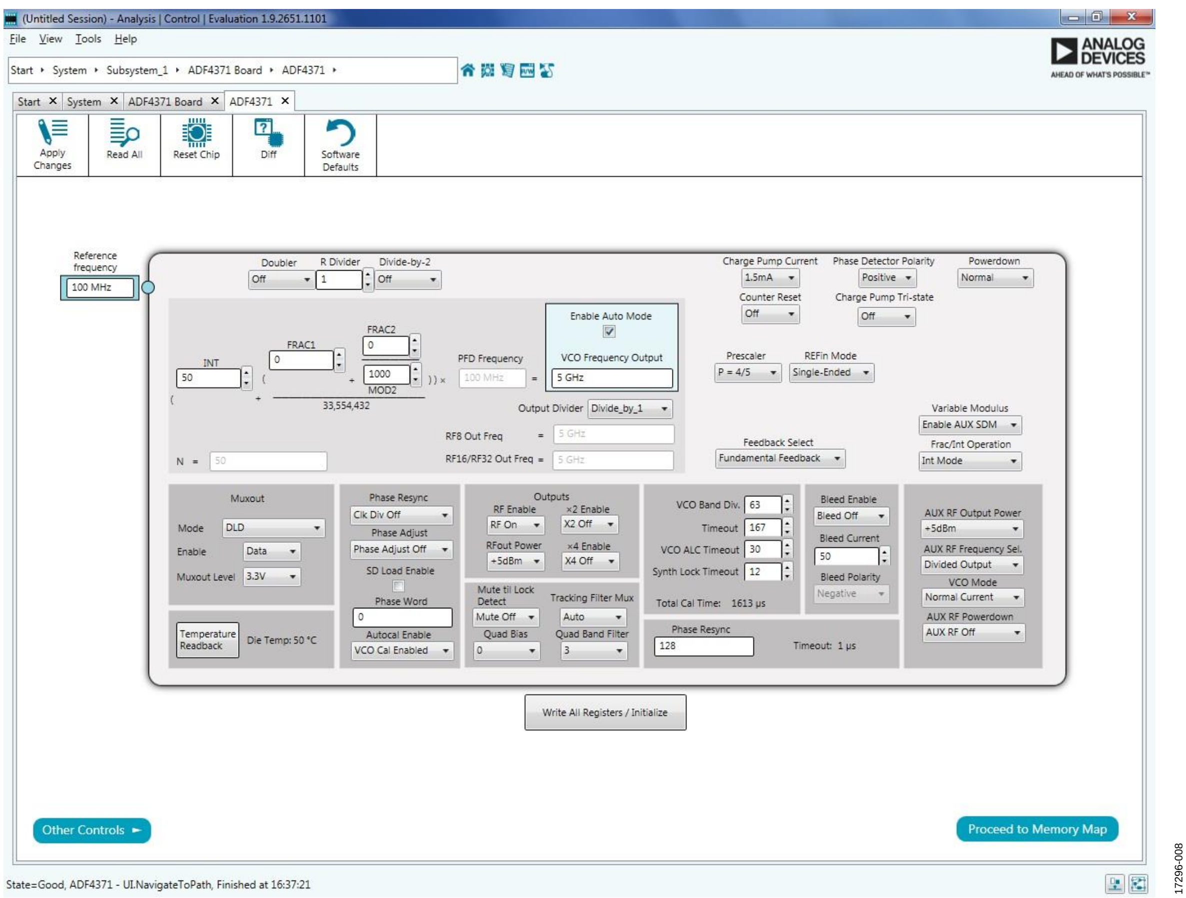
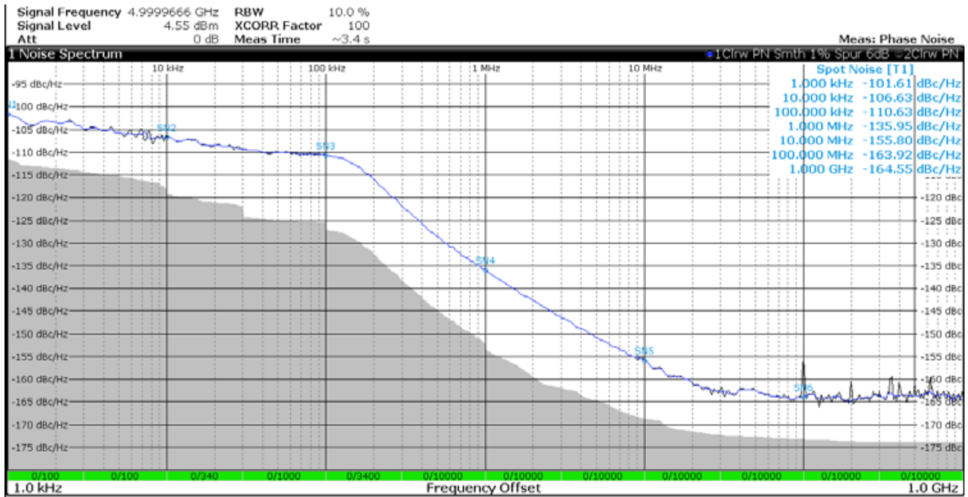


Figure 8. Software Front Panel Display, Main Controls

EVALUATION AND TEST

To evaluate and test the performance of the ADF4371, prepare the hardware and software setup as explained in the Evaluation Board Hardware section and the Evaluation Board Software section.

Run the software and set the **VCO Frequency Output** to 5 GHz. Measure the output spectrum and single sideband phase noise on a spectrum analyzer. Figure 9 shows a phase noise plot of the SMA RF8P pin equal to 5 GHz.



Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM	Jitter
1	1	1.000 kHz	1.000 GHz		-56.81 dBc	116.99 m°/2.04 mrad	172.547 kHz	64.997 fs

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Figure 9. Single Sideband Phase Noise

EVALUATION BOARD SCHEMATICS AND ARTWORK

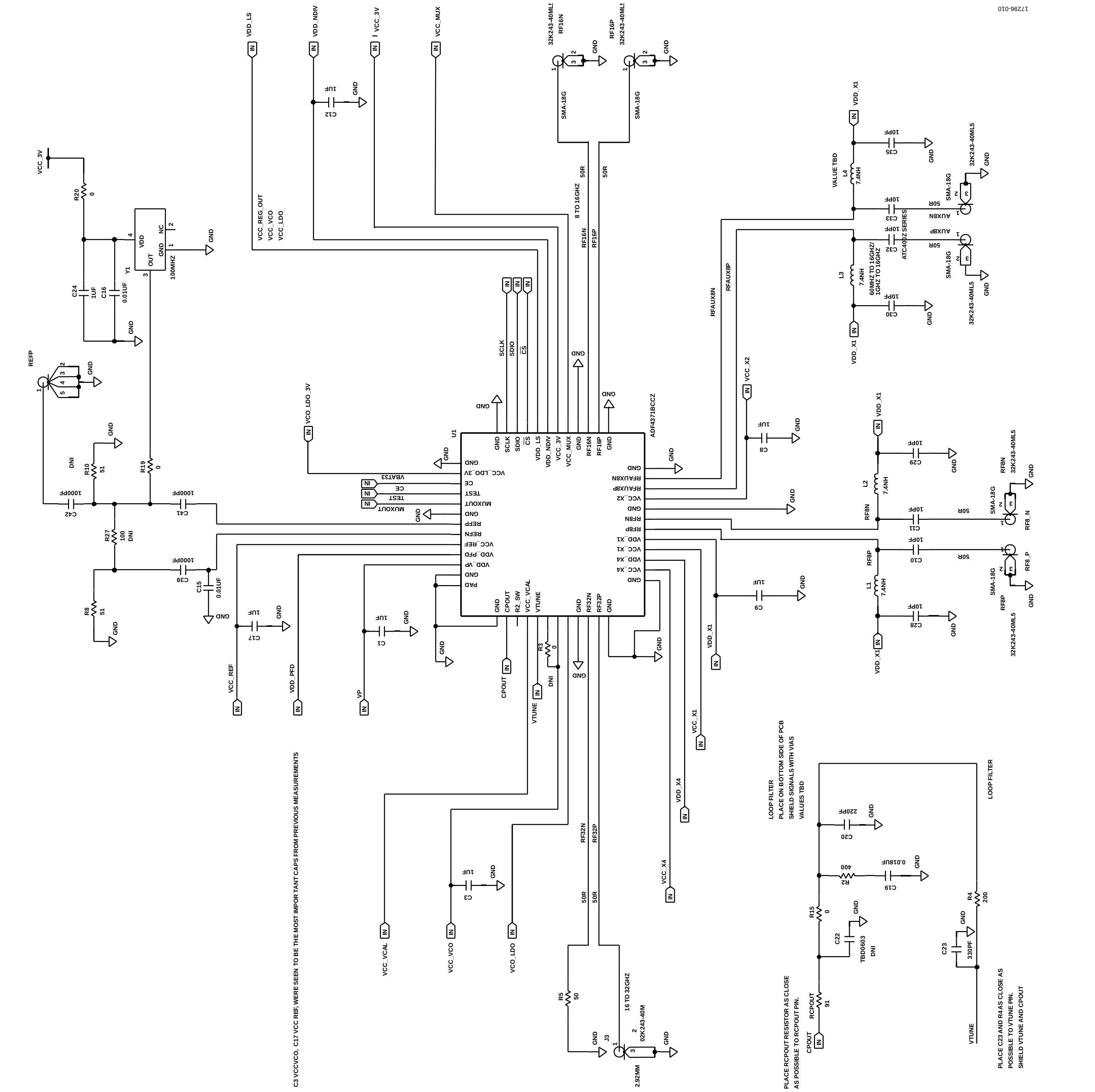

Figure 10. Evaluation Board Schematic, ADF4371 Connections and Loop Filter

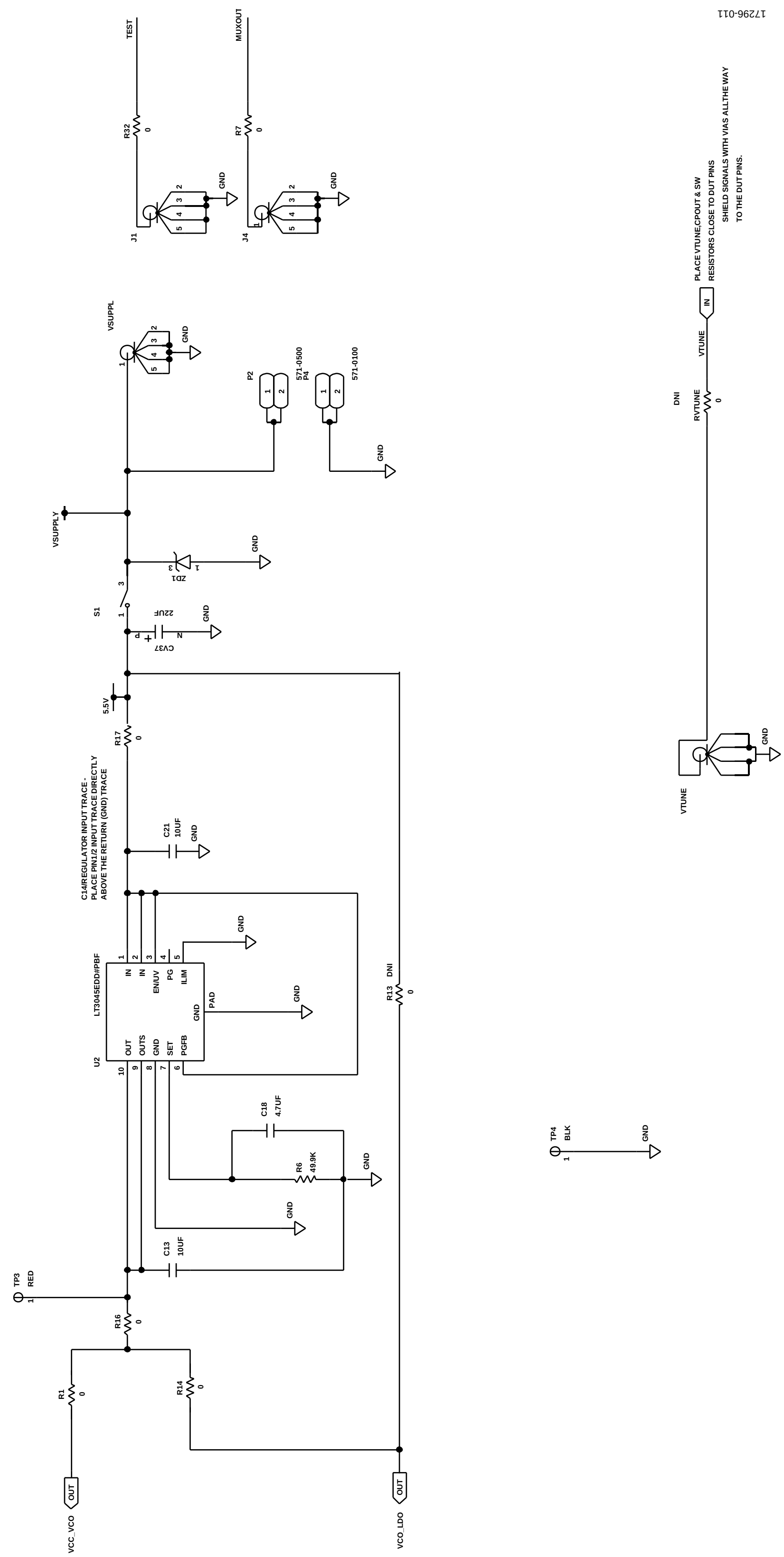

Figure 11. Evaluation Board Schematic, 5 V LDO Regulator

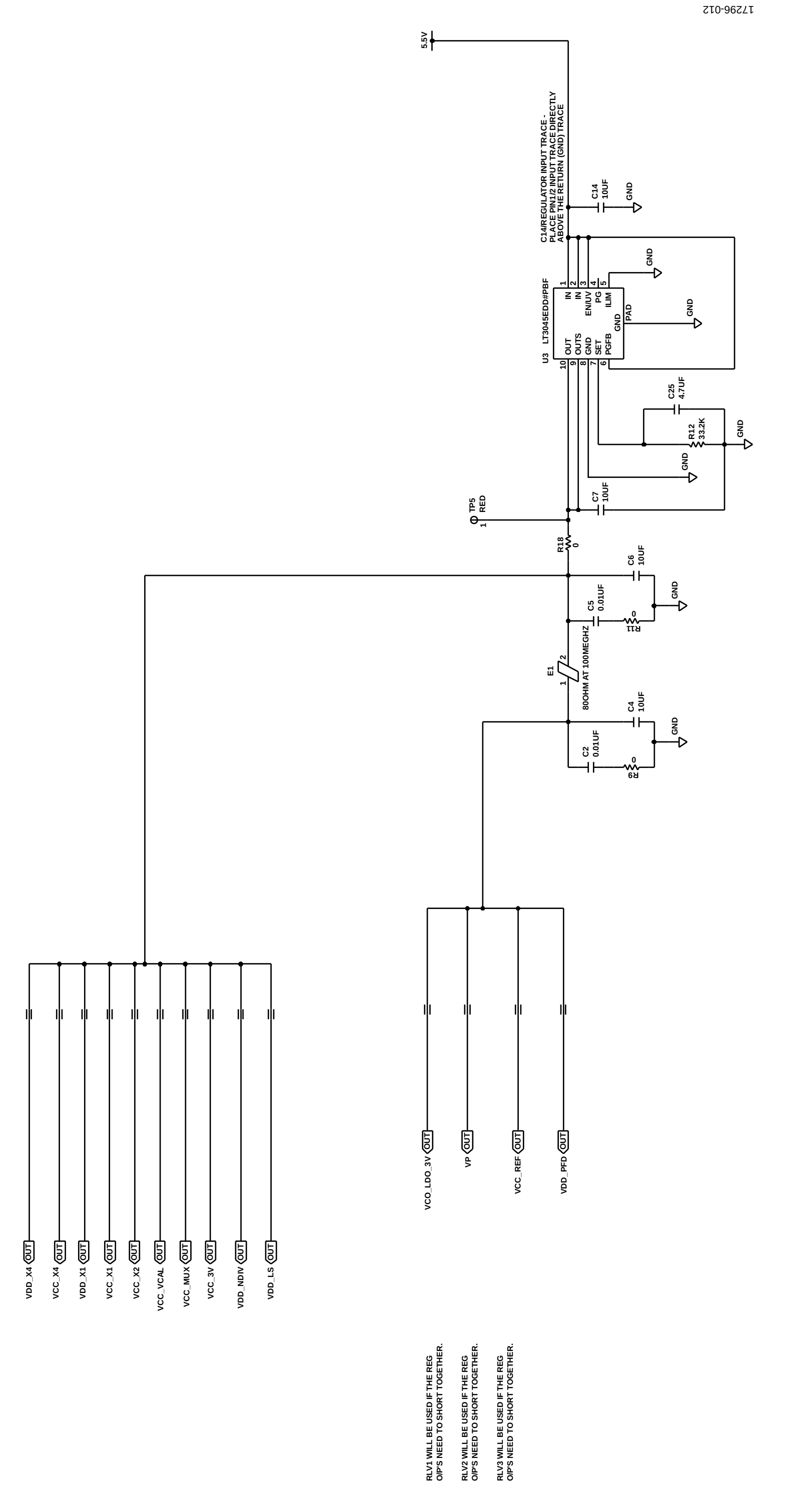

Figure 12. Evaluation Board Schematic, 3.3 V LDO Regulator

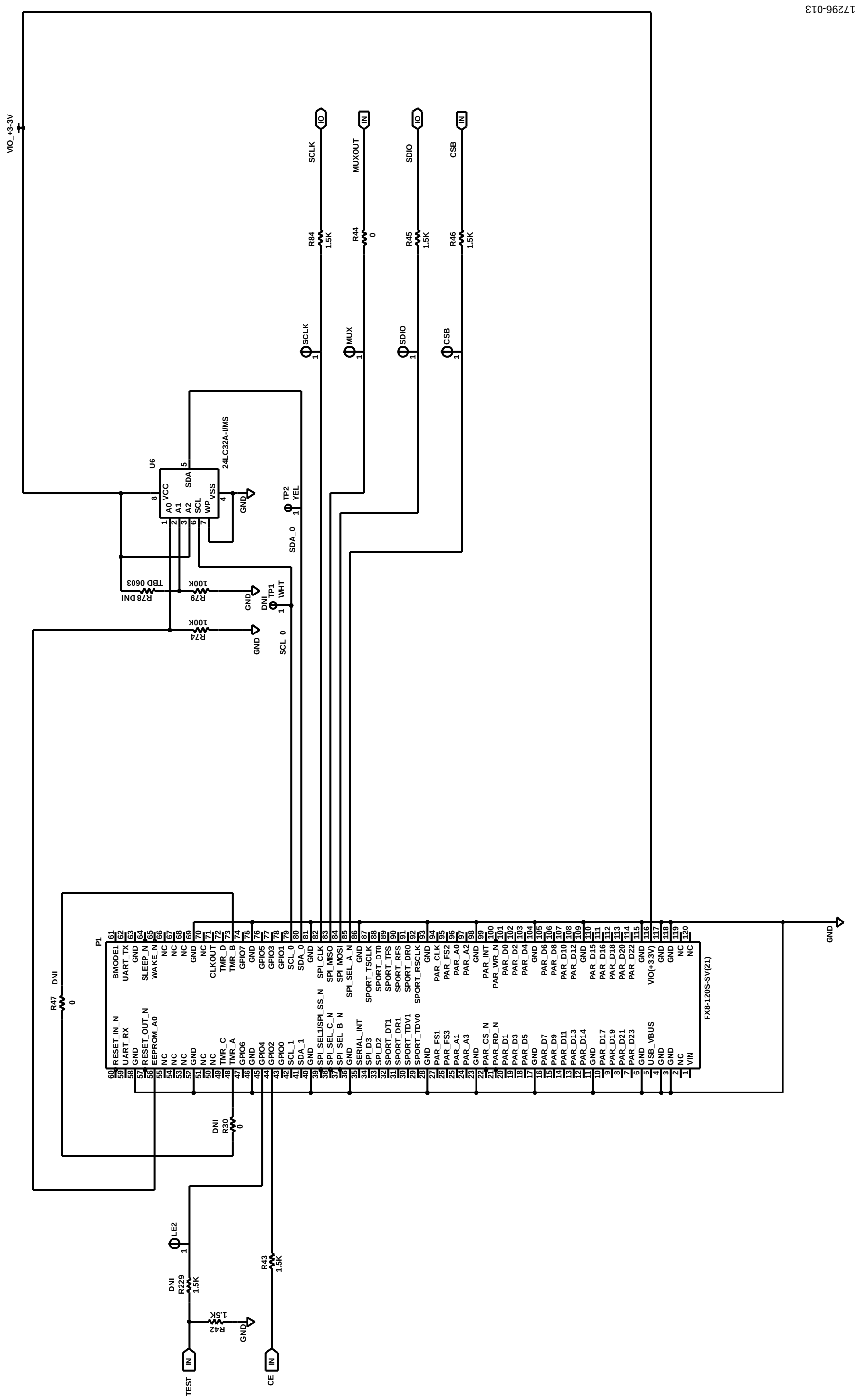

Figure 13. Evaluation Board Schematic, Board Connector

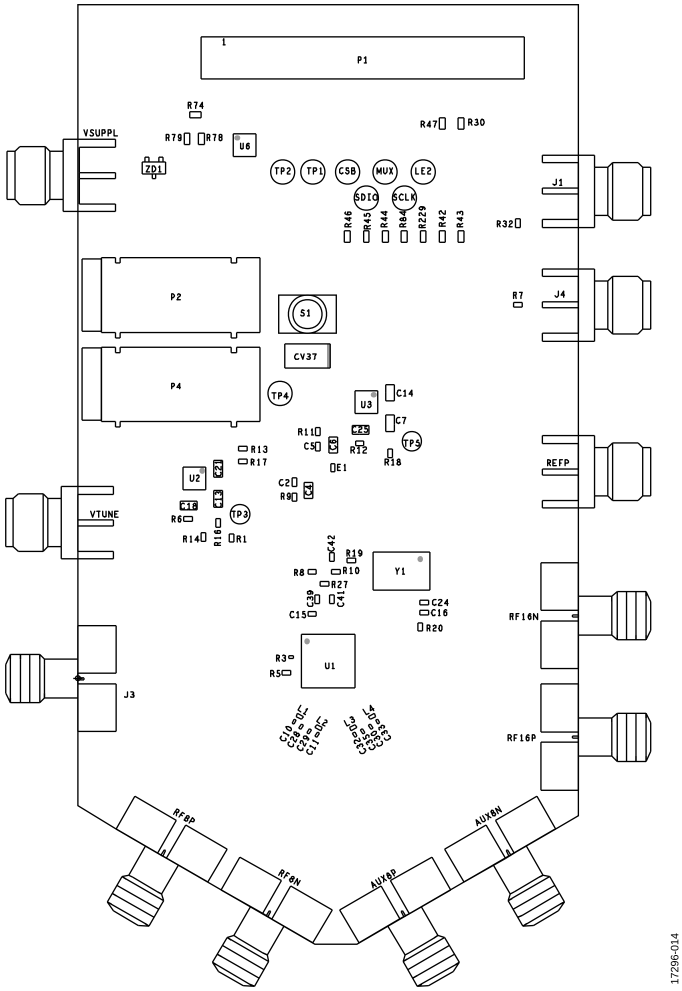

Figure 14. Evaluation Board Silk Screen, Top Side

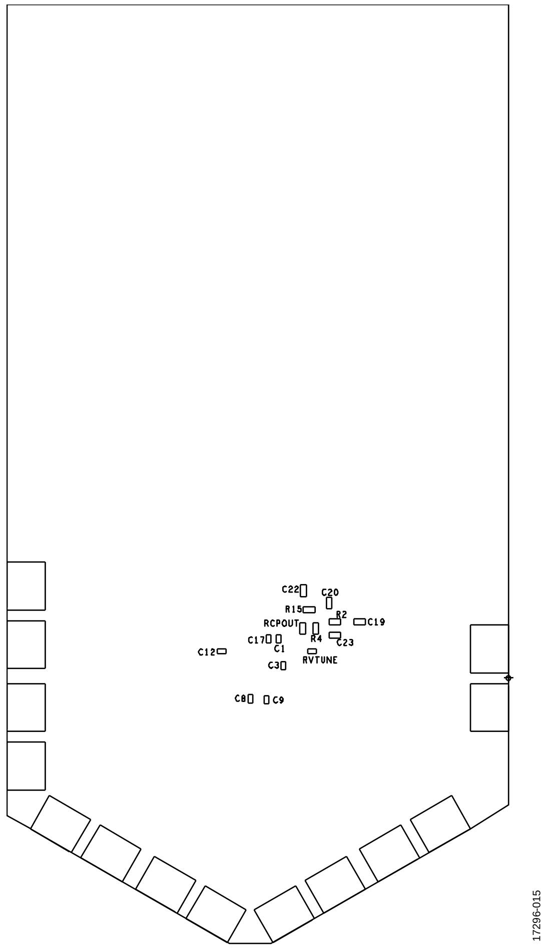

Figure 15. Evaluation Board Silk Screen, Bottom Side

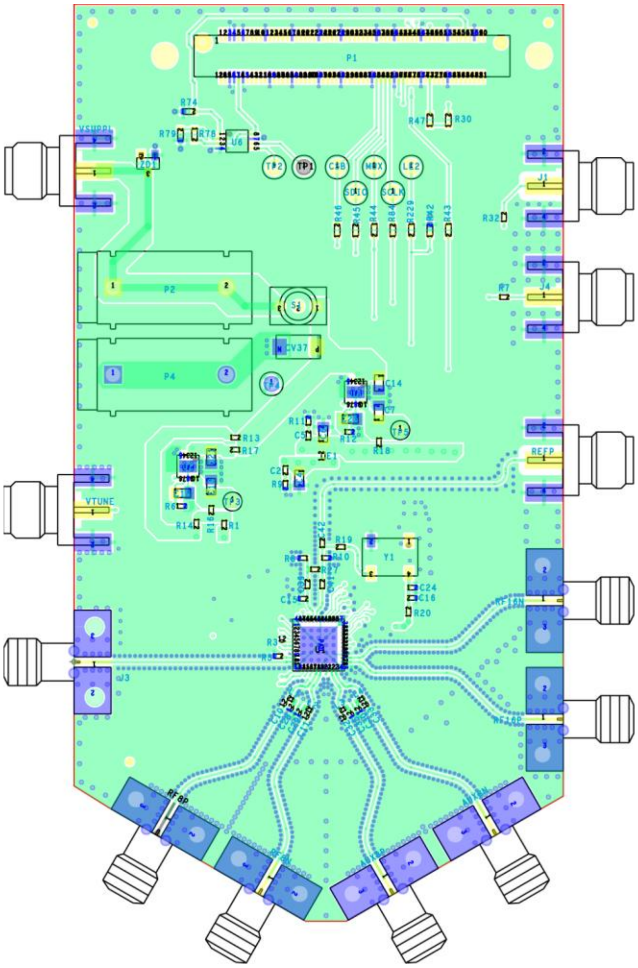

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Figure 16. Evaluation Board Layer 1, Primary

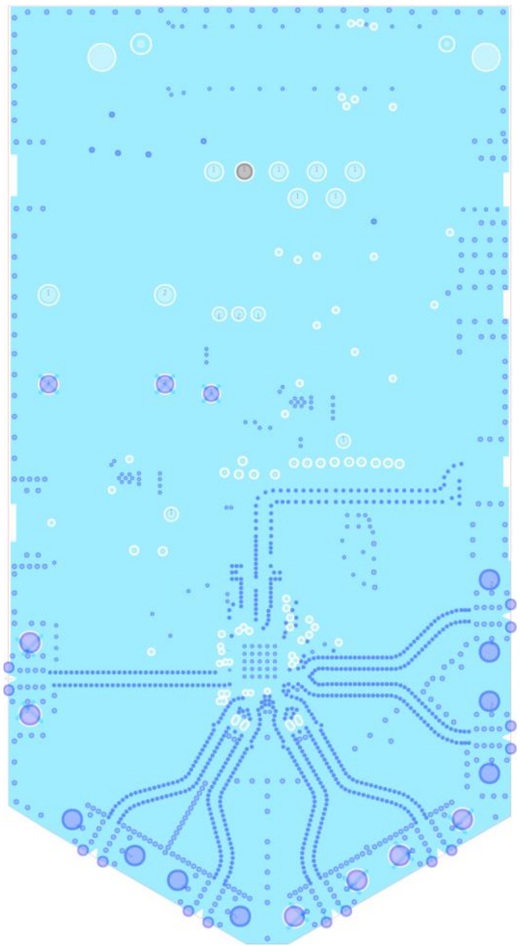

Figure 17. Evaluation Board Layer 2, Ground

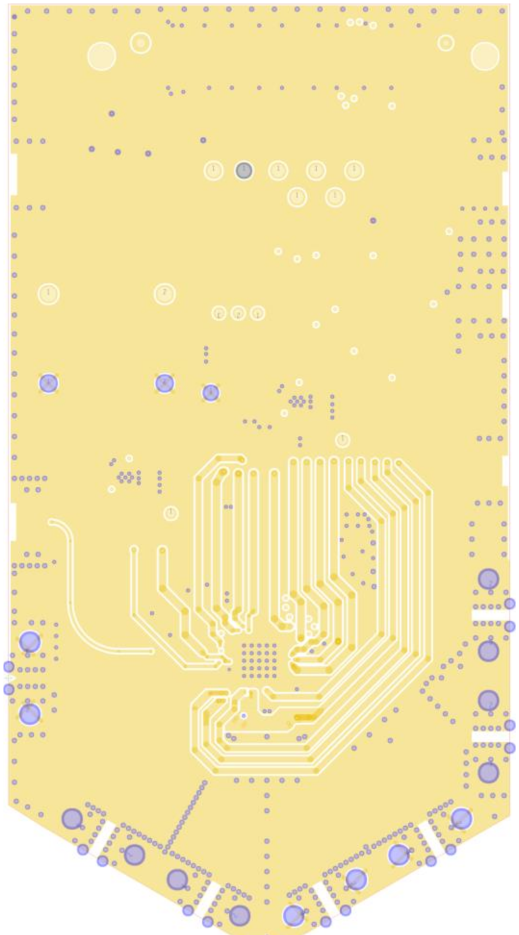

Figure 18. Evaluation Board Layer 3, Power

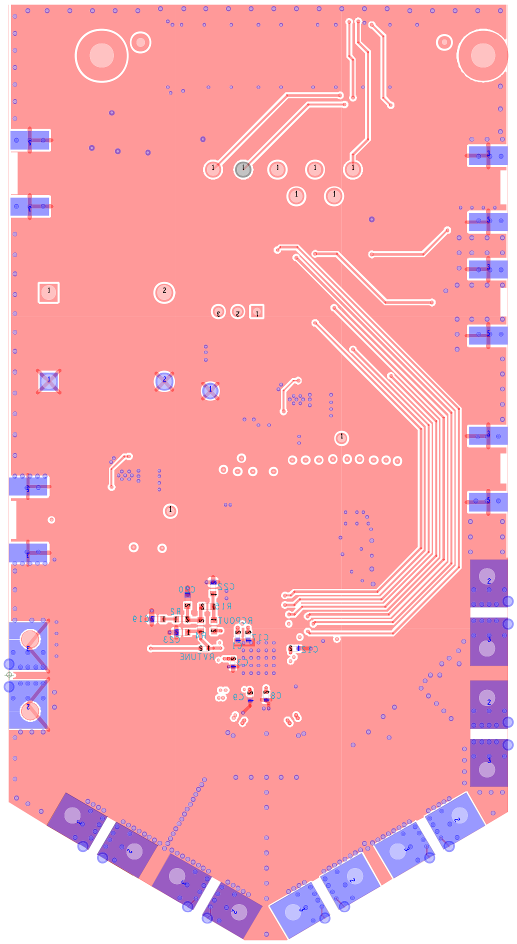

Figure 19. Evaluation Board Layer 4, Secondary

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Value	Manufacturer	Part Number
AUX8N, AUX8P, RF8N, RF8P, RF16N, RF16P	Printed circuit boards (PCBs), SMA, right angle jack connectors	32K243-40ML5	Rosenberger	32K243-40ML5
C1, C3, C8, C9, C12, C17, C24	Capacitors, ceramic, X6S	1 µF	TDK	C1005X6S1C105K050BC
C10, C11, C28, C29, C30, C35	Ceramic capacitors, C0G (NP0), general-purpose	10 pF	Murata	GRM0335C1E100JA01D
C4, C6, C7, C13, C14, C21	Ceramic capacitors, X5R, general-purpose	10 µF	Murata	GRM21BR61C106KE15L
C2, C5, C15, C16	Ceramic capacitors, X7R, general-purpose	0.01 µF	Murata	GRM155R71E103KA01D
C18, C25	Ceramic capacitors, X5R, general-purpose	4.7 µF	Murata	GRM21BR61E475KA12L
C19	Ceramic capacitor, X7R 0603	0.018 µF	AVX	06033C183JAT2A
C20	Chip capacitor, C0G, 0603	220 pF	TDK	C1608C0G1H221J
C23	Capacitor, ceramic, NP0	330 pF	TDK	CGJ3E3C0G2D331J080AA
C32, C33	Multilayer ceramic capacitors (MLCCs), NP0, RF and microwave	10 pF	American Technical Ceramics	400Z100FT16T
C39, C41, C42	Ceramic capacitors, C0G (NP0), general-purpose	1000 pF	Murata	GRM1555C1H102JA01
CSB, LE2, MUX, SCLK, SDIO, TP2	PCB test point connectors	Yellow	Components Corporation	TP-104-01-04
CV37	Tantalum solid electrolytic ceramic	22 µF	AVX	TCJC226M025R0100
E1	Chip ferrite bead	80 Ω at 100 MHz	Murata	BLM15PX800SN1D
J1, J4, REFP, VSUPPL, VTUNE	PCBs, coaxial, SMA, end launch connectors	142-0701-801	Cinch Connectivity Solutions	142-0701-801
J3	PCB, SMA, right angle jack connector	02K243-40M	Rosenberger	02K243-40M
L1, L2, L3, L4	Chip inductors	7.4 nH	Coilcraft	0302CS-7N4XJLU
P1	PCB, vertical type receptacle, surface-mount device (SMD) connector	FX8-120S-SV(21)	Hirose	FX8-120S-SV(21)
P2	PCB, single socket connector	Red	Deltron	571-0500
P4	PCB, single socket connector	Black	Deltron	571-0100
R1, R7, R9, R11, R14, R16, R17, R18, R19, R20, R32	Thick film, chip resistors	0 Ω	Multicomp	MC00625W040210R
R12	Thick film, chip resistor	33.2 kΩ	Vishay	CRCW040233K2FKED
R15, R44	Film, SMD resistors, 0603	0 Ω	Multicomp	MC0603WG00000T5E-TC
R2	Precision, thin film, chip resistor	400 Ω	Vishay	PAT0603E4000BST1
R27	High frequency, thin film, chip resistor	100 Ω	Vishay	FC0402E1000BST1
R4	Thick film, chip resistor	200 Ω	Multicomp	MC 0.063W 0603 1% 200R
R42, R43, R45, R46, R84	Thick film, chip resistors	1.5 kΩ	Multicomp	MC 0.063W 0603 1% 1K5
R5	High frequency, chip resistor	50 Ω	Vishay	FC0402E50R0BST1
R6	Antisurge, high power, thick film, chip resistor	49.9 kΩ	Vishay	RCS040249K9FKED
R74, R79	Thick film, chip resistors	100 kΩ	Multicomp	MC 0.063W 0603 1% 100K
RCPOUT	Thick film, chip resistor	91 Ω	Yageo	RC0603FR-0791RL
S1	Single-pole single-throw, momentary switch	TT11AGPC104	TE Connectivity	TT11AGPC104
TP3, TP5	PCB test point connectors	Red	Keystone Electronics	5000
TP4	PCB test point connector	Black	Keystone Electronics	5006

Reference Designator	Description	Value	Manufacturer	Part Number
U1	Microwave, wideband synthesizer with integrated VCO	ADF4371BCCZ	Analog Devices, Inc.	ADF4371BCCZ
U2, U3	20 V, 500 mA, ultralow noise, ultrahigh power supply rejection ratio (PSRR), linear regulators	LT3045EDD#PBF	Analog Devices, Inc.	LT3045EDD#PBF
U6	32 kB, serial electronically erasable programmable read-only memory (EEPROM)	24LC32A-I/MS	Microchip Technology	24LC32A-I/MS
Y1	Ultralow, phase noise XO, high density, complementary metal-oxide semiconductor (HCMOS)	100 MHz	Crystek	CCHD-575-50-100.000
ZD1	BZX84C 6.8 V, Zener, SOT-23 diode	BZX84-C6V8	Philips	BZX84-C6V8

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