18 GHz to 44 GHz, GaAs, pHEMT, MMIC, 1/2 W Power Amplifier

Data Sheet

ADPA7006CHIP

FEATURES

Output P1dB: 29 dBm
P_{SAT}: 29.5 dBm
Gain: 23.5 dB
Output IP3: 38 dBm
Supply voltage: 5 V at 800 mA
Integrated power detector
50 Ω matched input/output
Die size: 2.750 mm × 1.805 mm × 0.102 mm

APPLICATIONS

Military and space
Test instrumentation
Communications

FUNCTIONAL BLOCK DIAGRAM

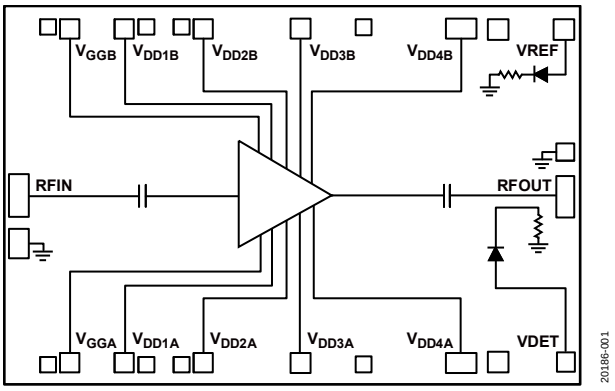

Figure 1.

GENERAL DESCRIPTION

The ADPA7006CHIP is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 18 GHz to 44 GHz. The amplifier provides 23.5 dB of small signal gain, 29 dBm output power for 1 dB compression, and a typical output third-order intercept of 38 dBm. The ADPA7006CHIP requires 800 mA from a 5 V supply on the supply voltage (V_{DD}), and features inputs and outputs that are internally matched to 50 Ω, facilitating integration in multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm wire bonds that are less than 0.31 mm long.

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REVISION HISTORY

7/2019—Revision 0: Initial Version

SPECIFICATIONS

18 GHz TO 20 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, quiescent supply current (I_{DQ}) = 800 mA for nominal operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		18		20	GHz	
GAIN			22.5		dB	
Gain Flatness			±0.75		dB	
Gain Variation Over Temperature			0.011		dB/°C	
NOISE FIGURE			9.5		dB	
RETURN LOSS						
Input			13		dB	
Output			17		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		26		dBm	
Saturated Output Power	P_{SAT}		27		dBm	
Output Third-Order Intercept	IP3		34		dBm	Measurement taken at output power (P_{OUT}) per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		800		mA	Adjust the gate bias voltage (V_{GGx}) from −1.5 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

20 GHz TO 28 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, quiescent supply current (I_{DQ}) = 800 mA for nominal operation, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		28	GHz	
GAIN		23	25		dB	
Gain Flatness			±1.0		dB	
Gain Variation Over Temperature			0.026		dB/°C	
NOISE FIGURE			7.5		dB	
RETURN LOSS						
Input			16		dB	
Output			24		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26.0	28.5		dBm	
Saturated Output Power	P_{SAT}		29		dBm	
Output Third-Order Intercept	IP3		36		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		800		mA	Adjust the gate bias voltage (V_{GGX}) from −1.5 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

28 GHz TO 36 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 800 mA for nominal operation, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		28		36	GHz	
GAIN		21.5	23.5		dB	
Gain Flatness			±0.5		dB	
Gain Variation Over Temperature			0.016		dB/°C	
NOISE FIGURE			5.5		dB	
RETURN LOSS						
Input			16		dB	
Output			23		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26.5	29		dBm	
Saturated Output Power	P_{SAT}		29.5		dBm	
Output Third-Order Intercept	IP3		38		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		800		mA	Adjust the gate bias voltage (V_{GGx}) from −1.5 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

36 GHz TO 44 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 800 mA for nominal operation, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		21	23		dB	
Gain Flatness			±0.3		dB	
Gain Variation Over Temperature			0.03		dB/°C	
NOISE FIGURE			5		dB	
RETURN LOSS						
Input			23		dB	
Output			23		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	24.2	27		dBm	
Saturated Output Power	P_{SAT}		28		dBm	
Output Third-Order Intercept	IP3		38		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Current	I_{DQ}		800		mA	Adjust the gate bias voltage (V_{GGX}) from −1.5 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DDxx})	6.0 V
Gate Bias Voltage (V_{GG1})	−1.5 V to 0 V
Radio Frequency (RF) Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 92.6 mW/°C Above 85°C)	8.3 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1B Passed, 750 V
Reliability Information	
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T = 85°C, V_{DD} = 5 V, I_{DQ} = 800 mA)	128.2°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the printed circuit board (PCB) thermal design is required. θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
C-14-7	10.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

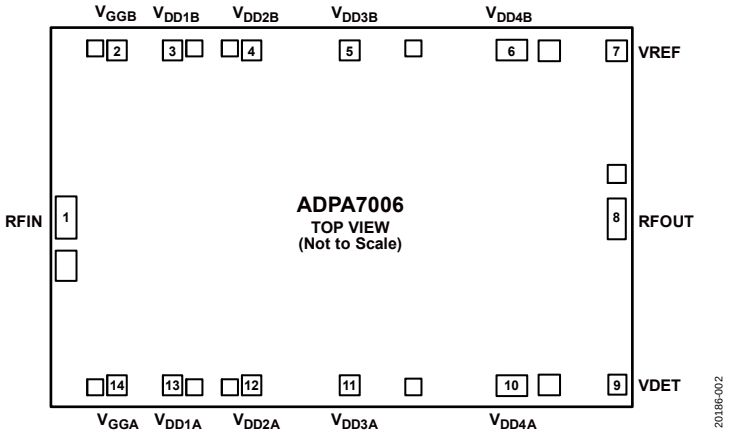

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
2, 14	V_{GGA}, V_{GGB}	Amplifier Gate Control.
3, 4, 5, 6, 10, 11, 12, 13	V_{DD1B}, V_{DD2B}, V_{DD3B}, V_{DD4B}, V_{DD4A}, V_{DD3A}, V_{DD2A}, V_{DD1A}	Drain Bias for the Amplifier.
7	VREF	Reference Diode. Use this pad for temperature compensation of the VDET RF output power measurements. When used in combination with VDET, this voltage provides temperature compensation to the VDET RF output power measurements.
8	RFOUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
9	VDET	Detector Diode for Measuring the RF Output Power. Detection via this pad requires the application of a dc bias voltage through an external series resistor. When used in combination with VREF, the difference voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power.
Die Bottom	GND	The pads and die bottom must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

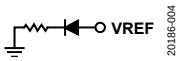

Figure 4. VREF Interface Schematic

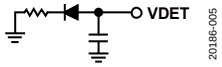

Figure 5. VDET Interface Schematic

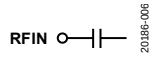

Figure 6. RFIN Interface Schematic

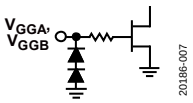

Figure 7. V_{GGA}, V_{GGB} Interface Schematic

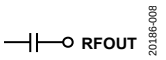

Figure 8. RFOUT Interface Schematic

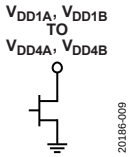

Figure 9. V_{DD1A}, V_{DD1B} to V_{DD4A}, V_{DD4B} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTIC

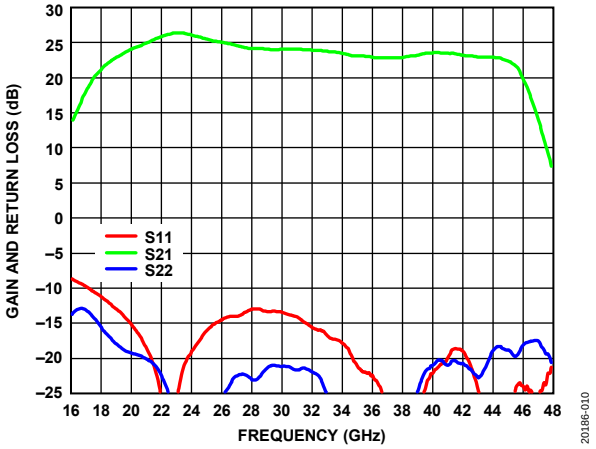

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 800 mA

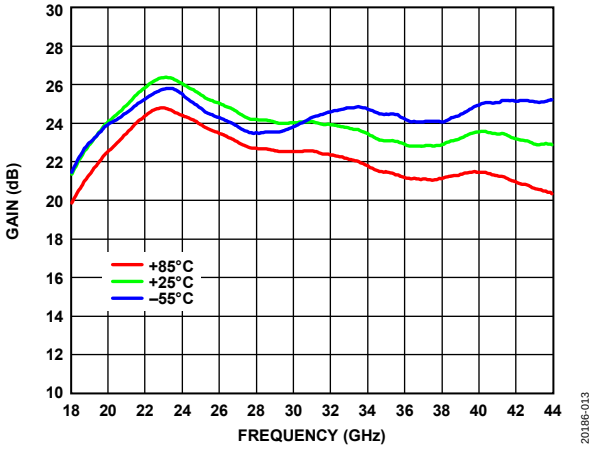

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

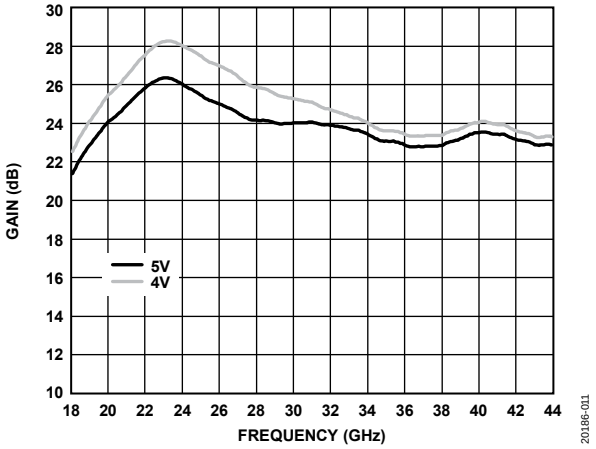

Figure 11. Gain vs. Frequency for Various Supply Voltages (V_{DD}), I_{DQ} = 800 mA

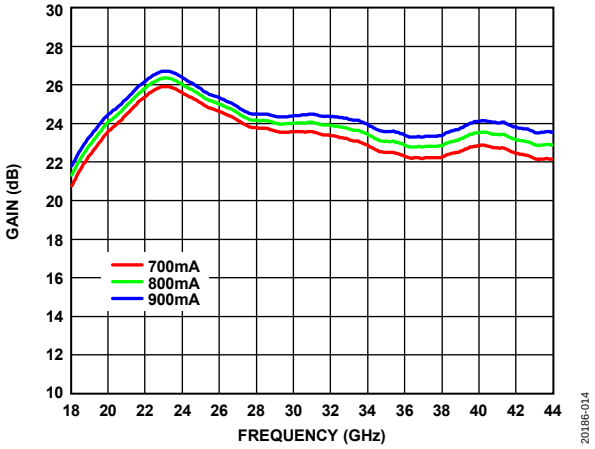

Figure 14. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

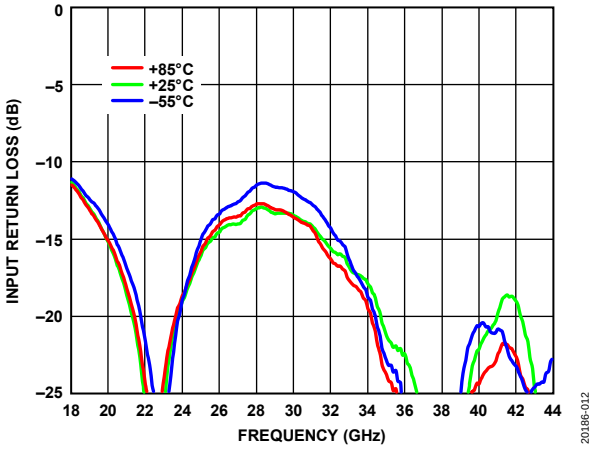

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

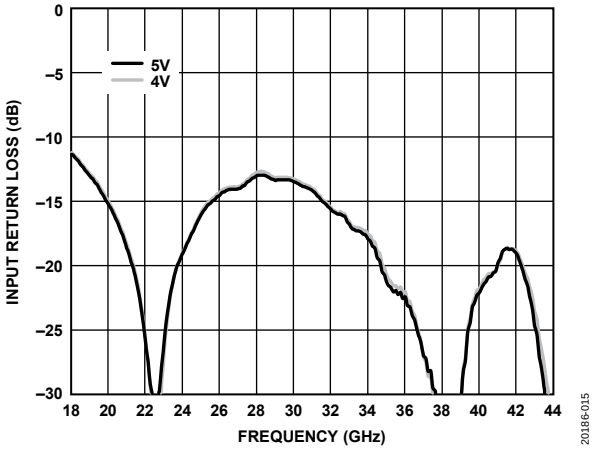

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 800 mA

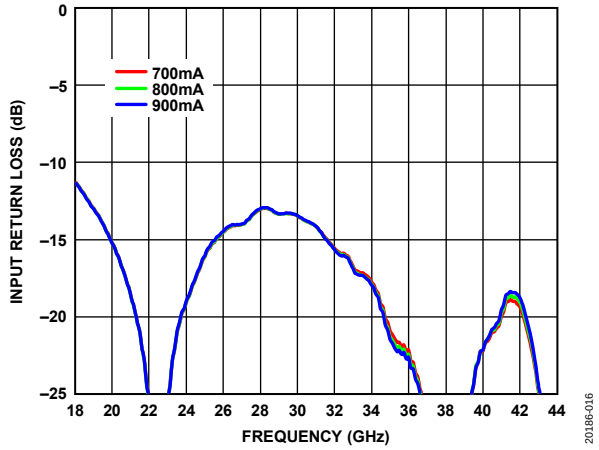

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

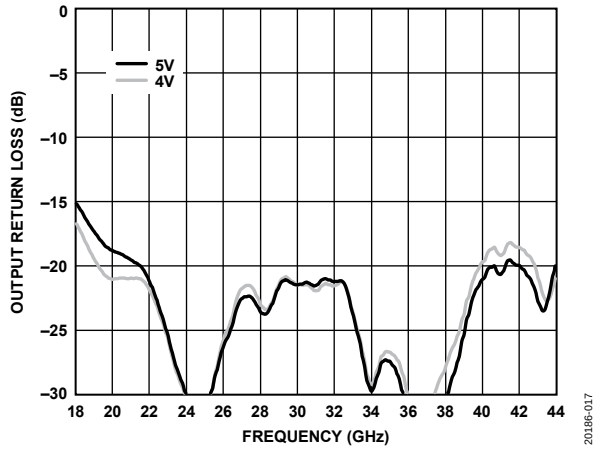

Figure 17. Output Return Loss vs Frequency for Various Supply Voltages (V_{DD}), I_{DQ} = 800 mA

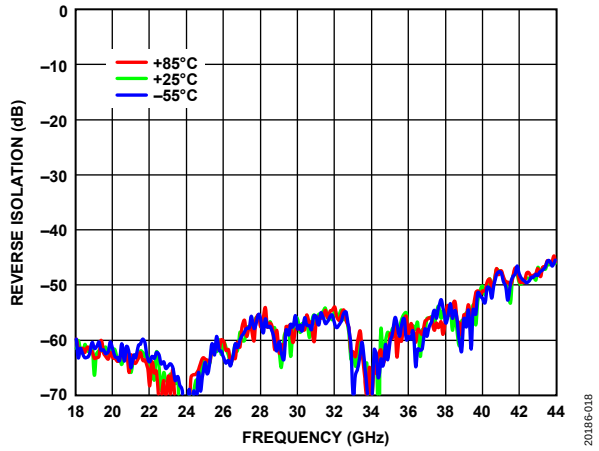

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

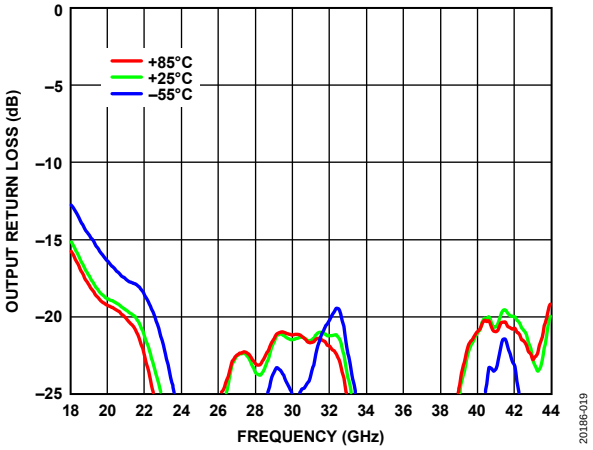

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

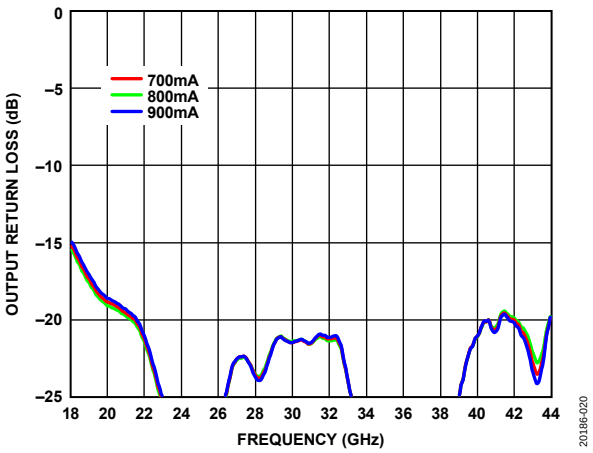

Figure 20. Output Return Loss vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

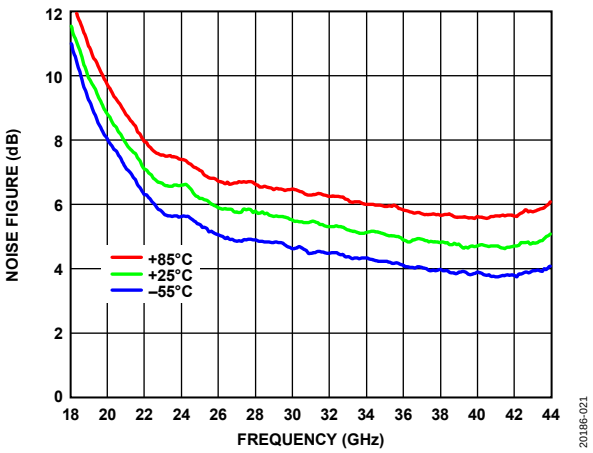

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

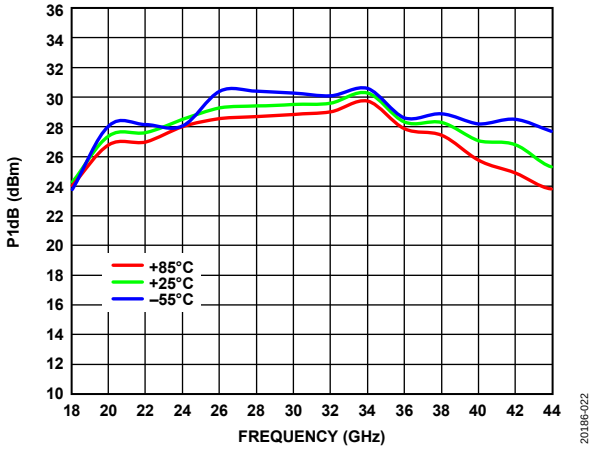

Figure 22. Output Power for 1 dB Compression (P1dB) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

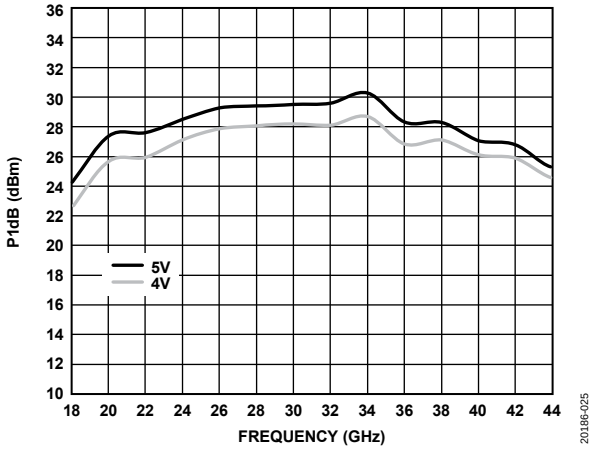

Figure 25. P1dB vs. Frequency for Various Supply Voltages (V_{DD}), I_{DQ} = 800 mA

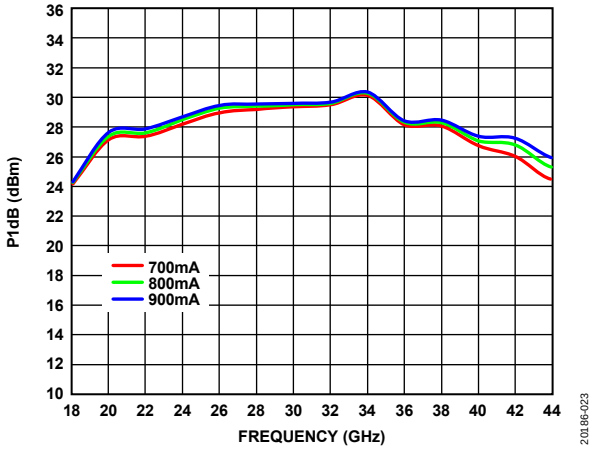

Figure 23. P1dB vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

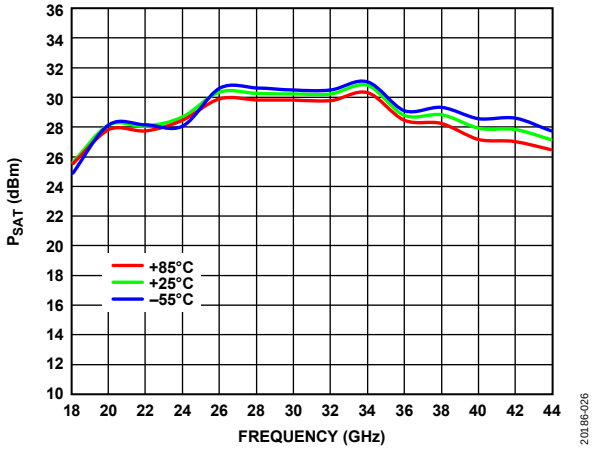

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA

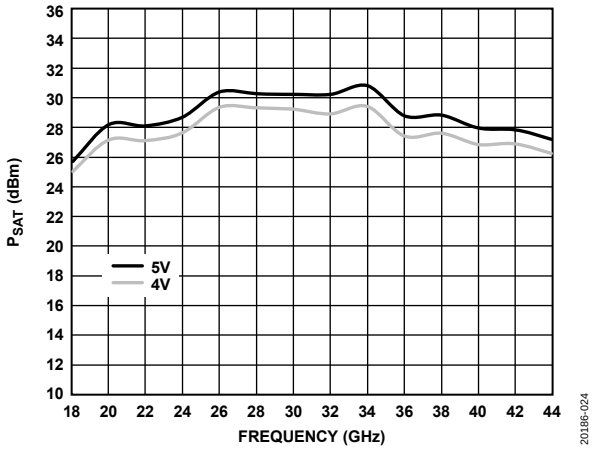

Figure 24. Saturated Output Power (P_{SAT}) vs. Frequency for Various Supply Voltages (V_{DD}), Drain Current (I_{DD}) = 800 mA

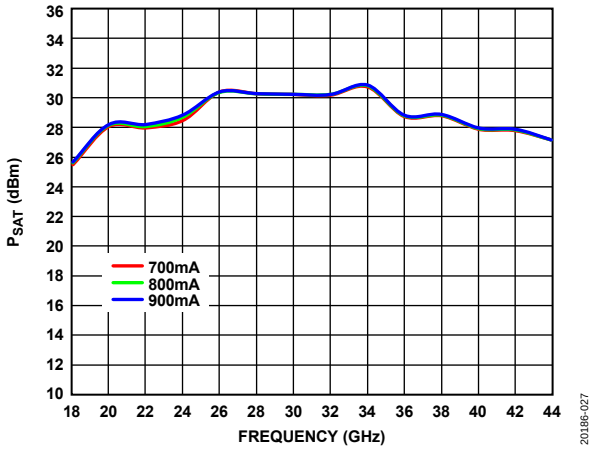

Figure 27. P_{SAT} vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

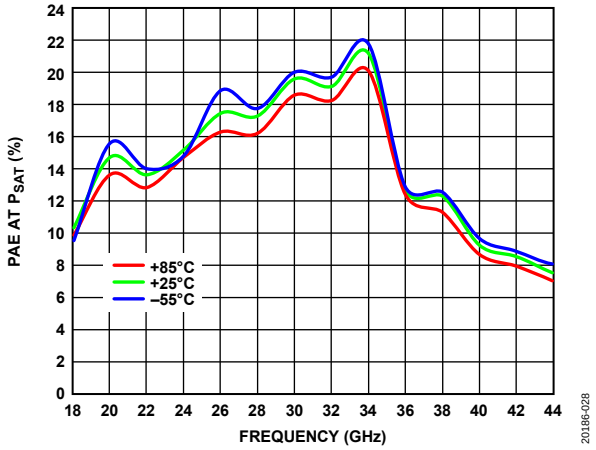

Figure 28. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 800 mA, PAE Measured at P_{SAT}

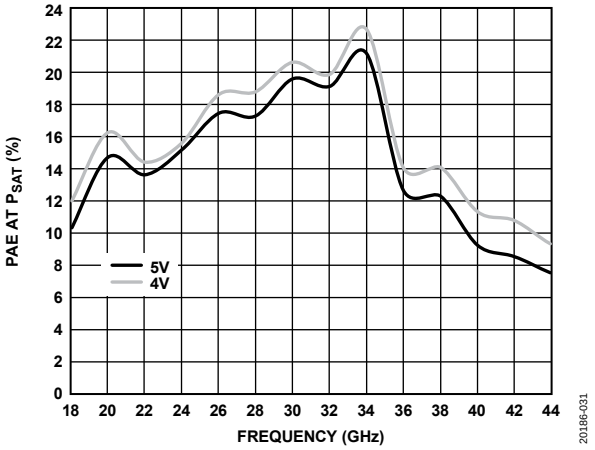

Figure 31. PAE vs. Frequency for Various Supply Voltages (V_{DD}), I_{DQ} =800 mA, PAE Measured at P_{SAT}

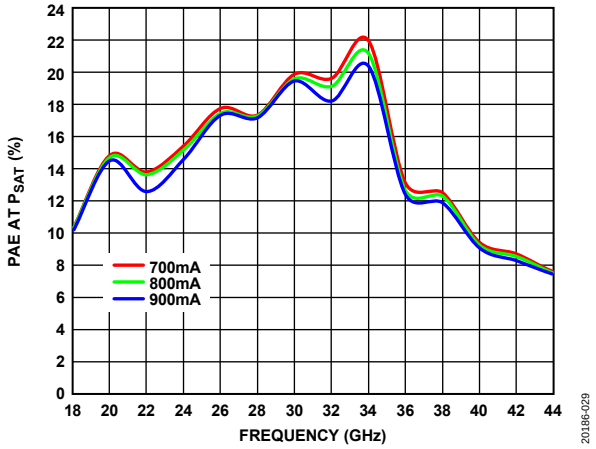

Figure 29. PAE vs. Frequency for Various Supply Current (I_{DQ}), V_{DD} = 5 V, PAE Measured at P_{SAT}

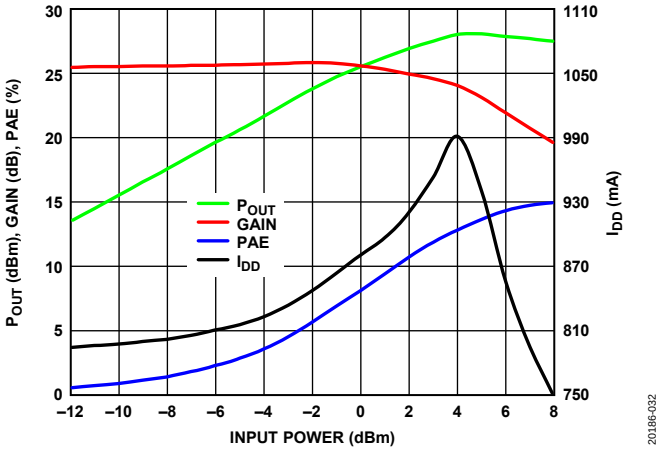

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 22 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

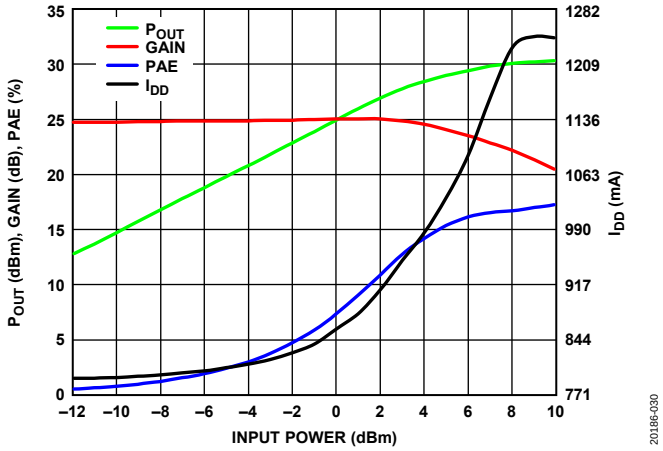

Figure 30. Output Power (P_{OUT}), Gain, PAE, and I_{DD} vs. Input Power, 26 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

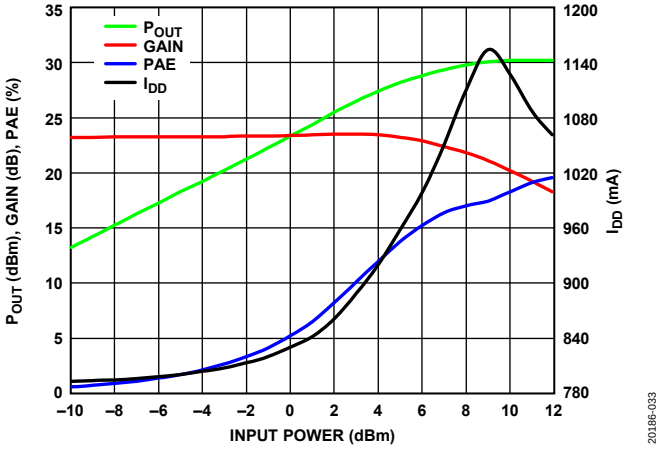

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

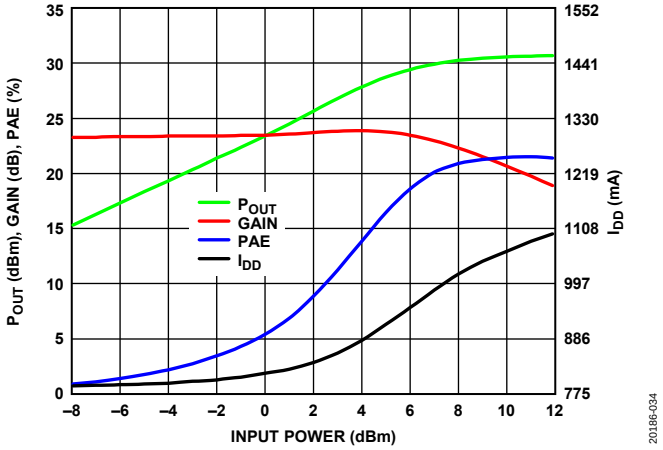

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 34 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

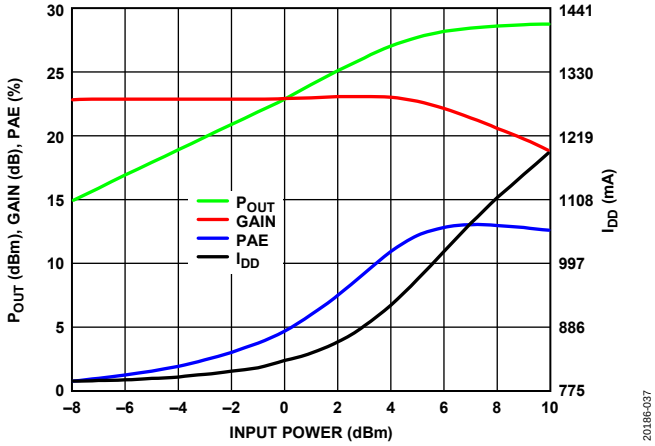

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 38 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

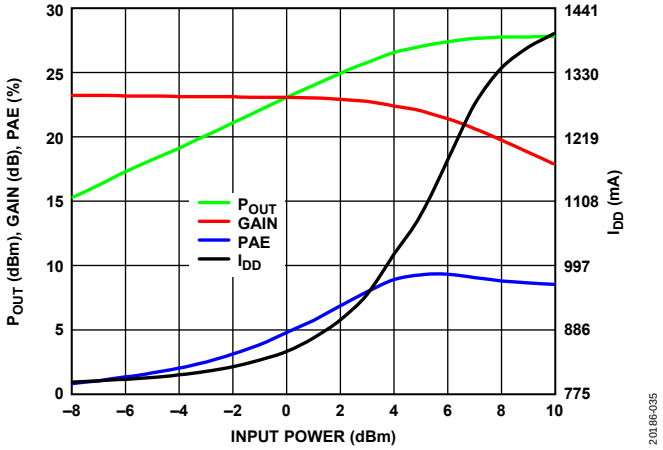

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 42 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

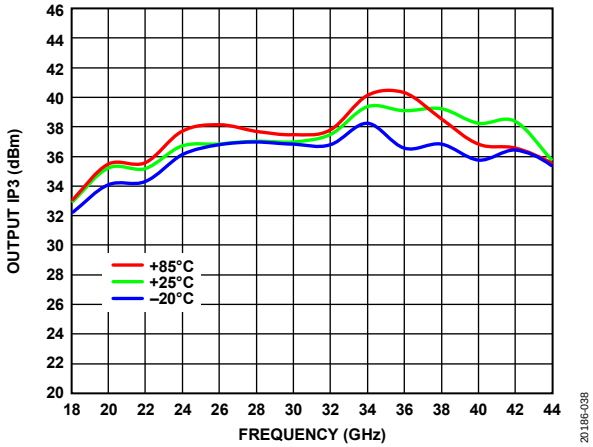

Figure 38. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DD} = 800 mA

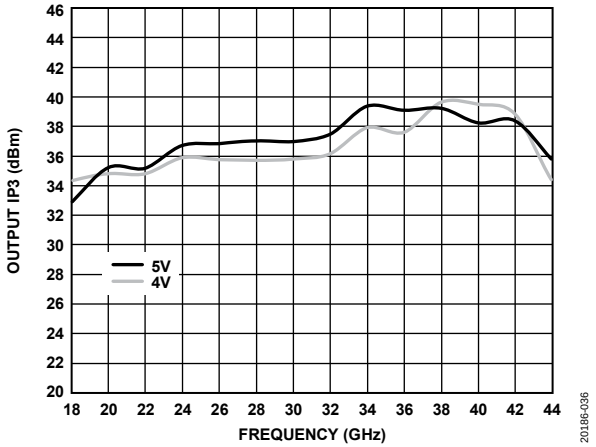

Figure 36. Output IP3 vs. Frequency for Various Supply Voltages (V_{DD}), P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 800 mA

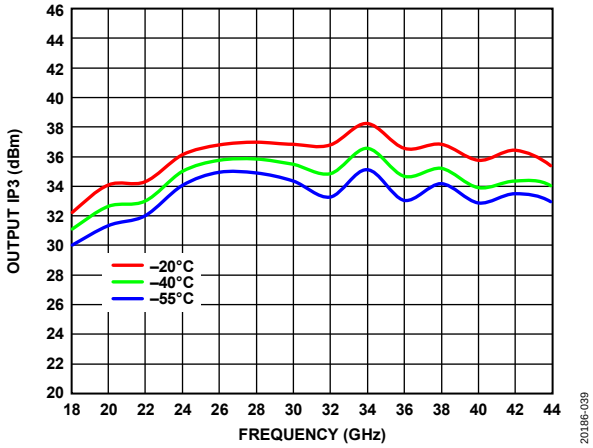

Figure 39. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 800 mA

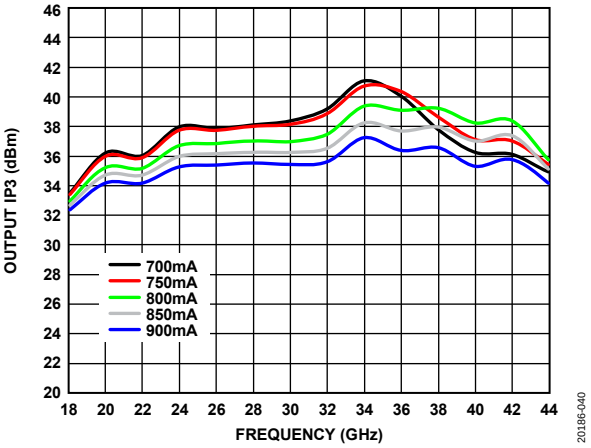

Figure 40. Output IP3 vs Frequency for Various Supply Currents (I_{DQ}), P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V

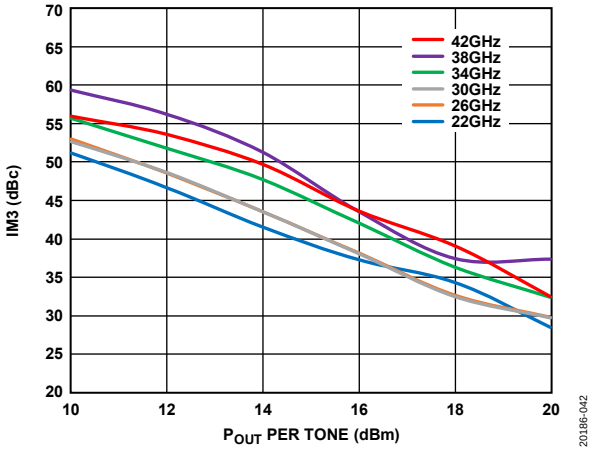

Figure 42. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 800 mA

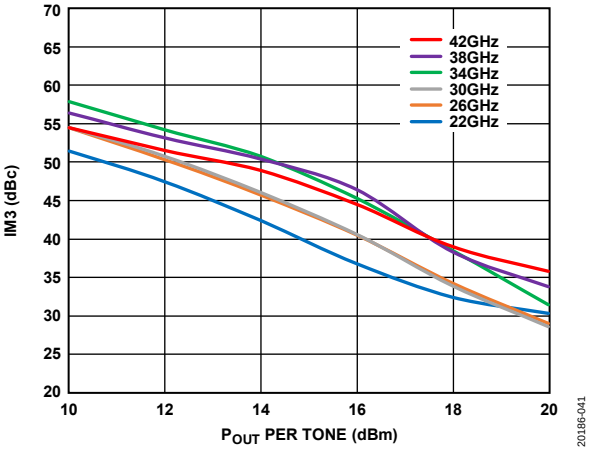

Figure 41. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 800 mA

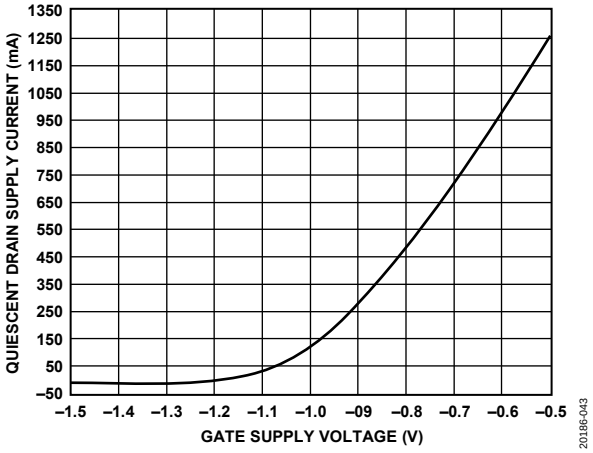

Figure 43. Quiescent Supply Current (I_{DQ}) vs. Gate Supply Voltage (V_{GGx})

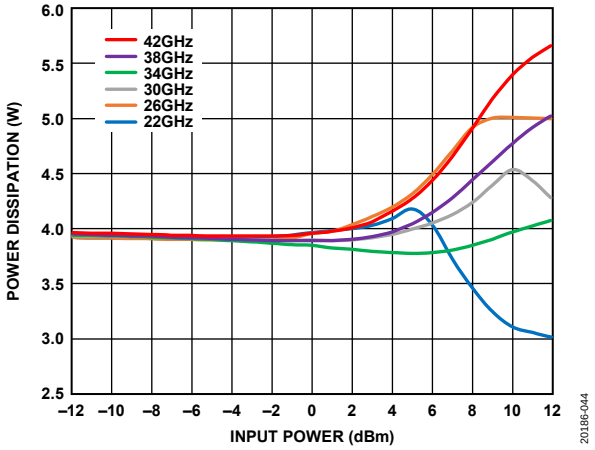

Figure 44. Power Dissipation vs. Input Power at T = 85°C, V_{DD} = 5 V, I_{DD} = 800 mA

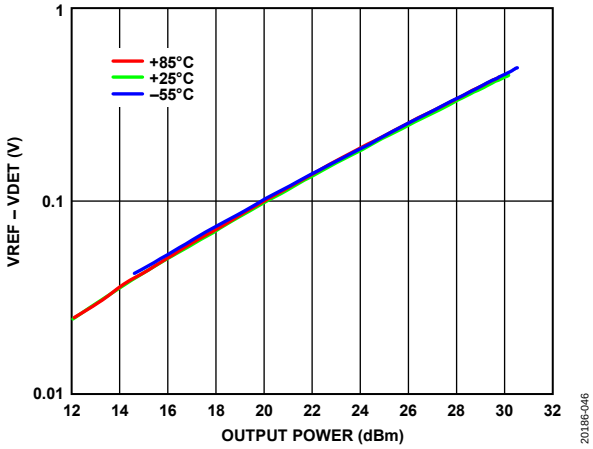

Figure 46. Detector Voltage (VREF – VDET) vs. Output Power for Various Temperatures at 32 GHz, V_{DD} = 5 V, I_{DD} = 800 mA

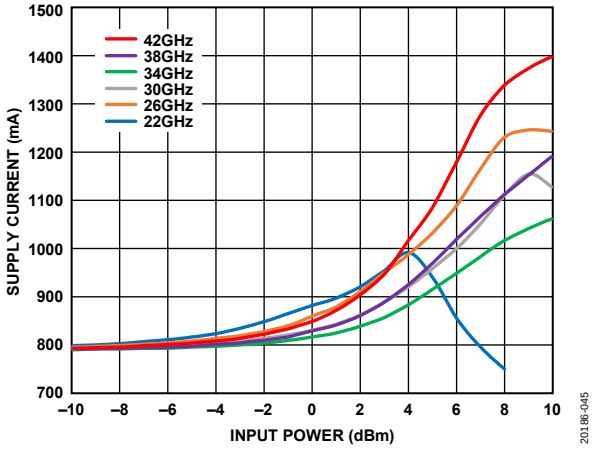

Figure 45. Supply Current (I_{DD}) vs. Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 800 mA

CONSTANT DRAIN CURRENT (I_{DD}) OPERATION

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 900 mA for nominal operation, unless otherwise noted. Figure 47 to Figure 50 biased using the HMC980LP4E active bias control.

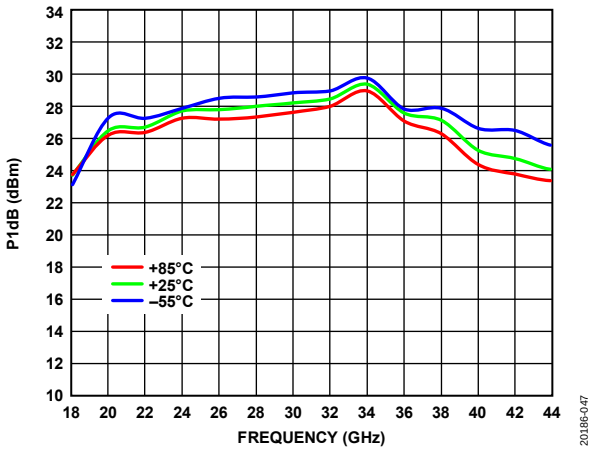

Figure 47. P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

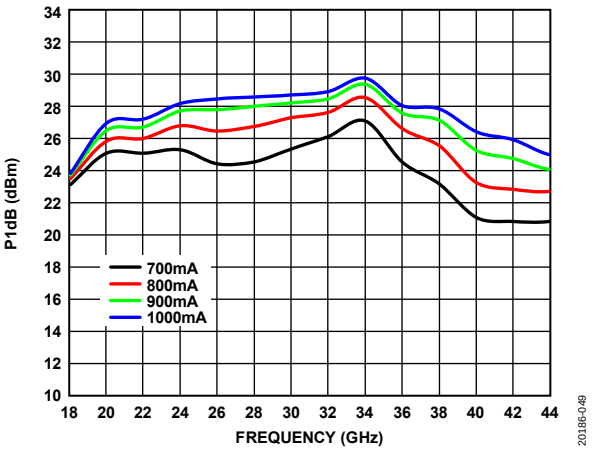

Figure 49. P1dB vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

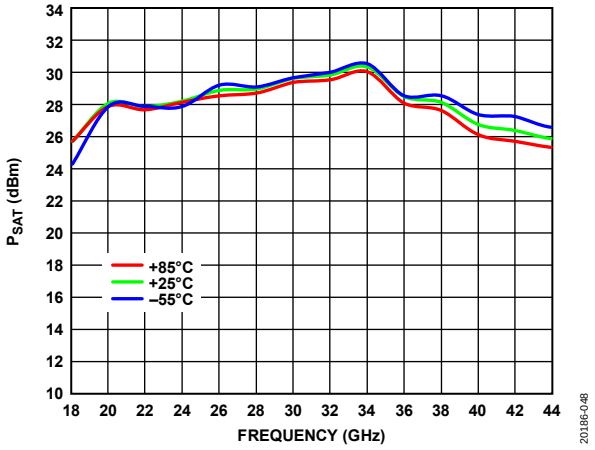

Figure 48. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

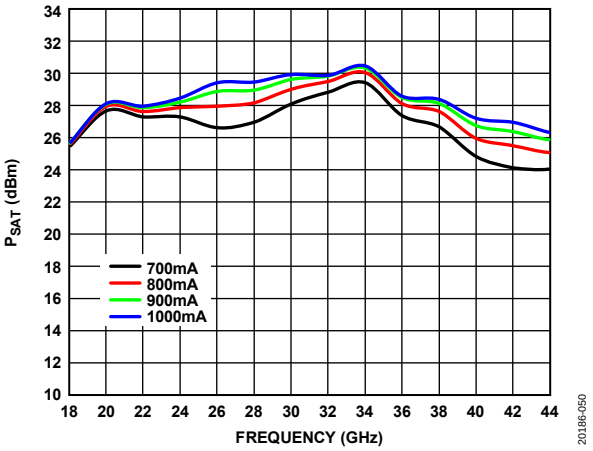

Figure 50. P_{SAT} vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

THEORY OF OPERATION

The architecture of the ADPA7006CHIP, a medium power amplifier, is shown in Figure 51. The ADPA7006CHIP uses two cascaded, four-stage amplifiers operating in quadrature between six 90° hybrids.

The input signal is divided evenly in two, and then each signal is divided in two again. Each path is amplified through three independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 23 dB and a P_{SAT} value of 28 dBm.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 51).

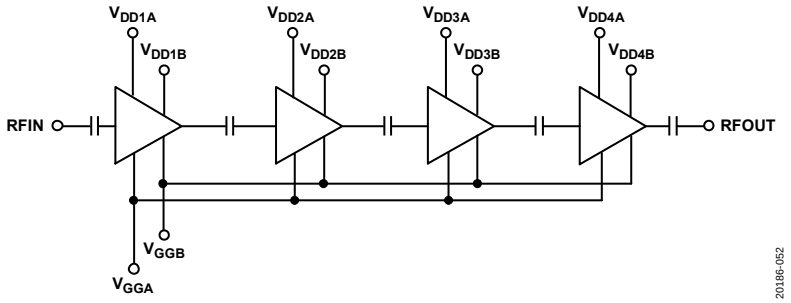

Figure 51. ADPA7006CHIP Architecture

APPLICATIONS INFORMATION

The ADPA7006CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all primary and alternate V_{GGx} and V_{DDxx} pads.

V_{GGA} and V_{GGB} are the gate bias pads for the cascaded amplifiers.

V_{DD1A}, V_{DD1B}, V_{DD2A}, V_{DD2B}, V_{DD3A}, V_{DD3B}, V_{DD4A}, and V_{DD4B} are the drain bias pads for the cascaded amplifiers.

All measurements for this device were taken using the typical application circuit (see Figure 62) and were configured as shown in the assembly diagram (see Figure 64 and Figure 65).

The recommended bias sequence during power-up is as follows:

1. Connect GND to RF and dc ground.
2. Set the primary gate bias voltages, V_{GGA} and V_{GGB}, to −1.5 V.
3. Set all the drain bias voltages, V_{DDx}x, to 5 V.
4. Increase the gate bias voltage to achieve a quiescent current, and set I_{DQ} = 800 mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the primary gate bias voltage, V_{GGA}, to −1.5 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

Simplified bias pad connections to dedicated gain stages and dependence and independence among pads are shown in Figure 51.

The V_{DD} = 5 V and I_{DQ} = 800 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7006CHIP at different bias conditions may provide performance that differs from what is shown in the nominal (V_{DD} = 5 V and I_{DQ} = 800 mA) typical performance characteristic figures. Biasing the ADPA7006CHIP for higher drain current typically results in higher P1dB, output IP3, and gain at the expense of increased power consumption.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω transmission lines on 0.127 mm thick alumina thin film substrates are recommended for bringing the RF to and from the chip. Raise the die 0.075 mm to ensure that the surface of the die is coplanar with the surface of the substrate.

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm. To ensure wideband matching, a 15 fF capacitive stub is recommended on the PCB before the ribbon bond.

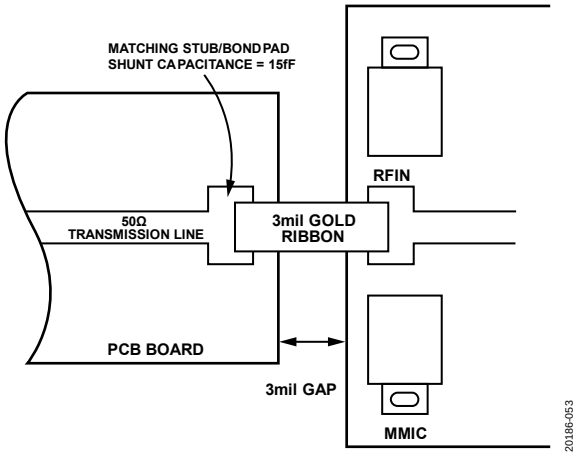

Figure 52. High Frequency Input Wideband Matching

Table 8. Power Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W)	V_{GGx} (V)
700	22.5	29.5	39.2	3.5	−0.7
800	22.9	29.6	37.5	4.0	−0.66
900	23.4	29.7	35.6	4.5	−0.62

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T = 25°C.
[2] Adjust V_{GGA} from −2 V to 0 V to achieve the desired drain current.

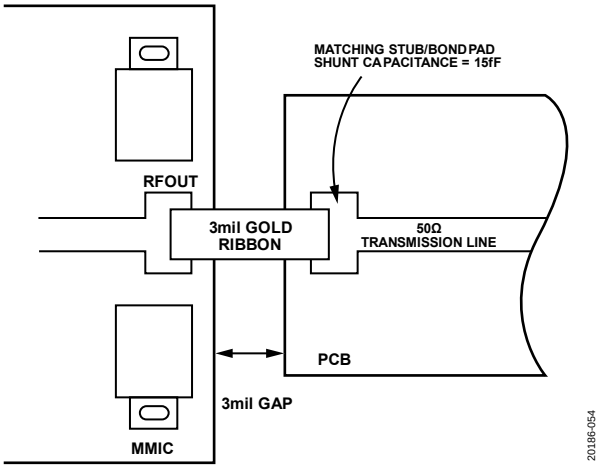

Figure 53. High Frequency Output Wideband Matching

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

Mounting

Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 3 mil × 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded dc bonds of 0.025 mm diameter, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm.

Alternatively, short RF bonds that are ≤3 mm and made with two 1 mm wires can be used.

BIASING THE ADPA7006CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller designed to meet the bias requirements for enhancement mode and depletion mode amplifiers, such as the ADPA7006CHIP. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self protection in the event of a short circuit, an internal charge pump that generates the negative voltage needed on the gate of the ADPA7006CHIP, and the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-DIE.

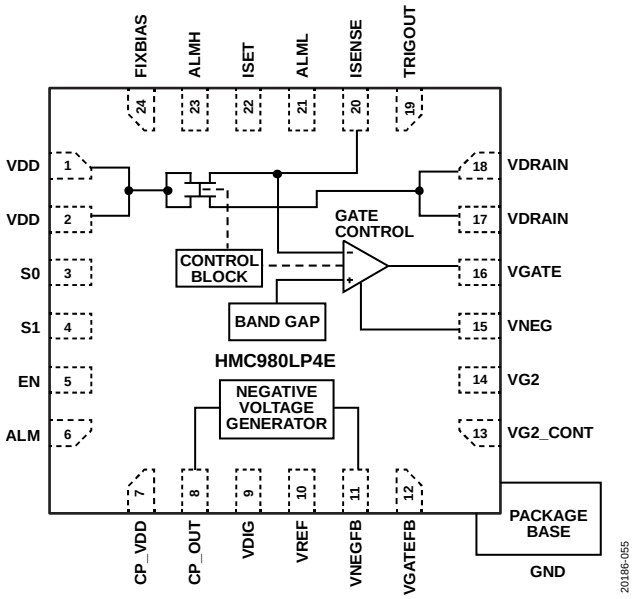

Figure 54. HMC980LP4E Active Bias Control

APPLICATION CIRCUIT SETUP

Figure 55 shows an application circuit using the HMC980LP4E to control the ADPA7006CHIP. When using an external negative supply for VNEG, refer to the application circuit shown in Figure 56.

In the application circuit shown in Figure 55, the ADPA7006CHIP drain voltage and drain current are set by the following equations:

$$V_{DRAIN}\ (5\ V) = V_{DD}\ (5.77\ V) - I_{DRAIN}\ (900\ mA) \times 0.85$$

$$I_{DRAIN}\ (900\ mA) = 150 \div R10\ (125\ \Omega)$$

LIMITING VGATE FOR THE ADPA7006CHIP V_{GGx} AMR (ABSOLUTE MAXIMUM RATING) REQUIREMENT

When using the HMC980LP4E to control the ADPA7006CHIP, the minimum voltages for VNEG and VGATE must be −1.5 V to keep them within the absolute maximum rating limit for the V_{GGx} pad of the ADPA7006CHIP. To set the minimum voltages, set R15 and R16 to the values shown in Figure 56 and Figure 57. Refer to the AN-1363 Application Note for more information and calculations for R15 and R16.

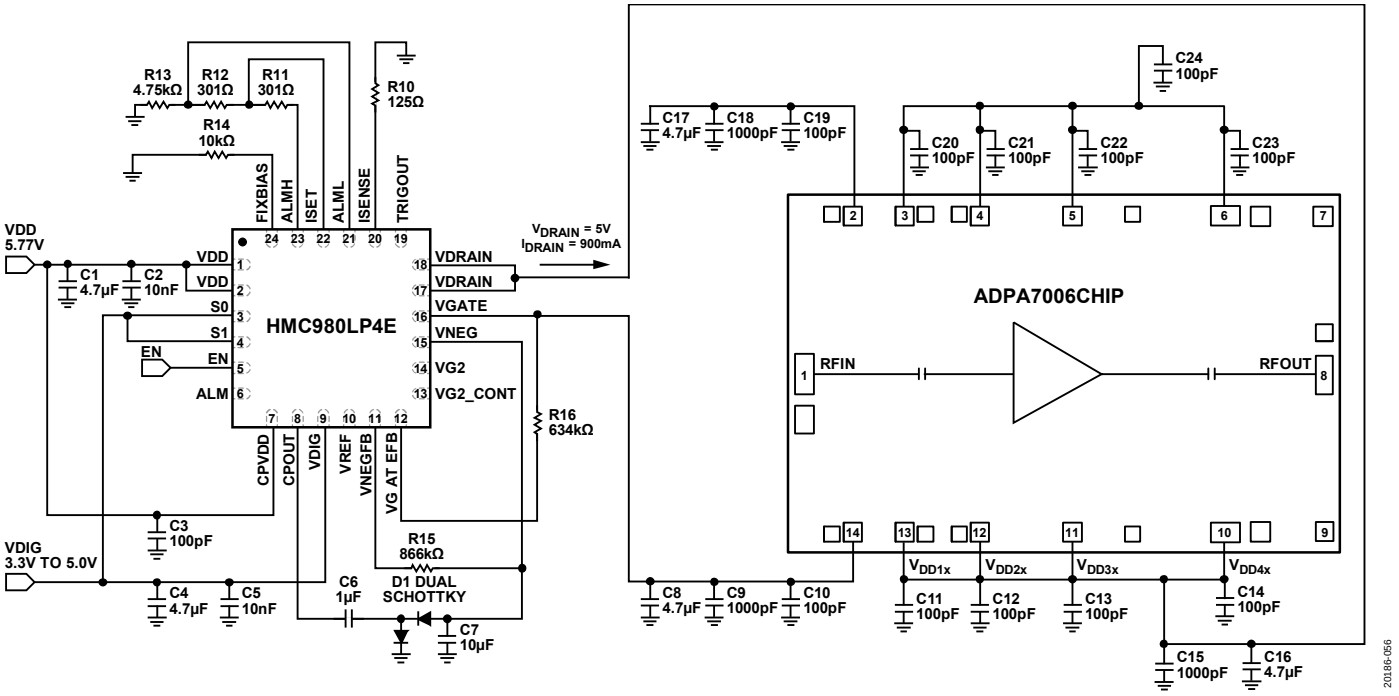

Figure 55. Application Circuit Using the HMC980LP4E with the ADPA7006CHIP

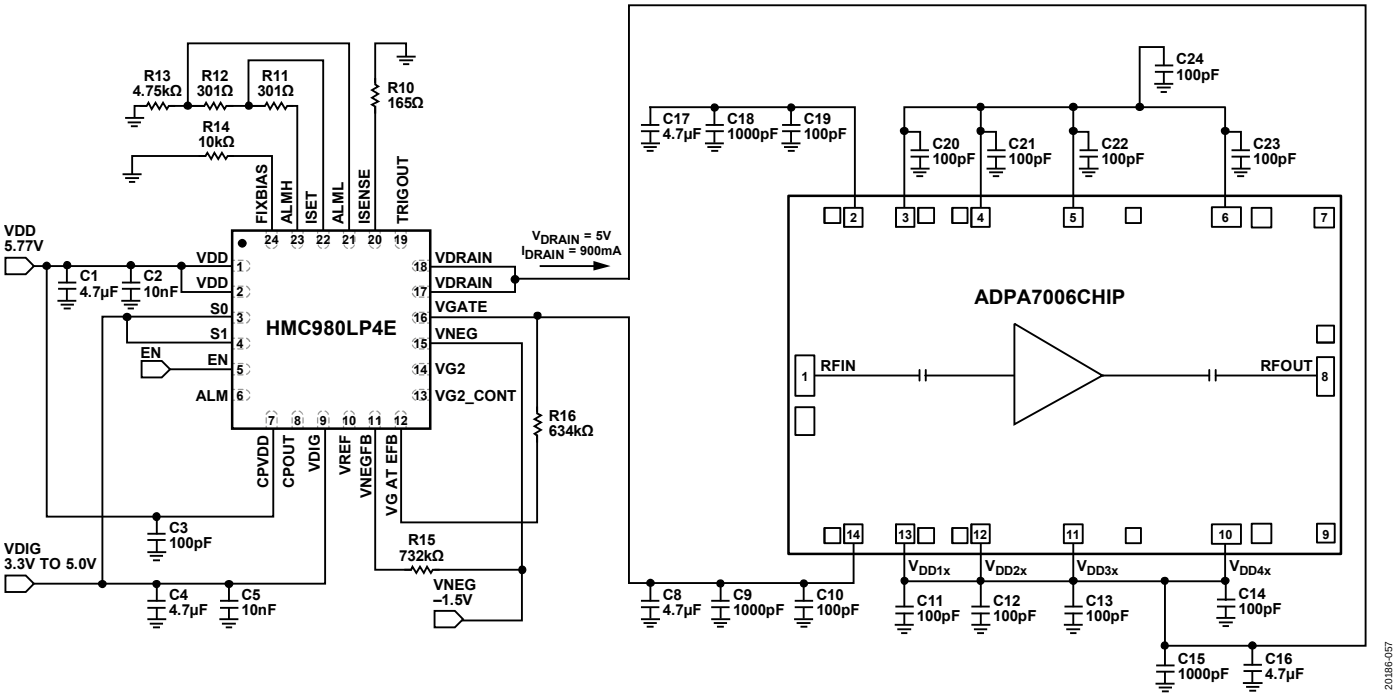

Figure 56. Application Circuit Using the HMC980LP4E with the ADPA7006CHIP (External Negative Voltage Source)

HMC980LP4E BIAS SEQUENCE

The dc supply sequence described in this section is required to prevent damage to the HMC980LP4E when using the device to control the ADPA7006CHIP.

Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. VDIG = 3.3 V.
2. S0 = 3.3 V.
3. VDD = 5.77 V.
4. VNEG = −1.5 V (this step is unnecessary if using an internally generated voltage).
5. EN = 3.3 V (transition from 0 V to 3.3 V turns on V_{GATE} and V_{DRAIN})

Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. EN = 0 V (transition from 3.3 V to 0 V turns off V_{DRAIN} and V_{GATE}).
2. VNEG = 0 V (unnecessary if using internally generated voltage).
3. VDD = 0 V.
4. S0 = 0 V.
5. VDIG = 0 V.

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7006CHIP on or off by applying 3.3 V or 0 V, respectively, to the EN pad. At EN = 3.3 V, V_{GATE} drops to −1.5 V and V_{DRAIN} turns on at 5 V. V_{GATE} then rises until I_{DRAIN} = 800 mA, and the closed control loop regulates I_{DRAIN} at 900 mA. When EN = 0 V, V_{DRAIN} is set to −1.5 V and V_{DRAIN} is set to 0 V.

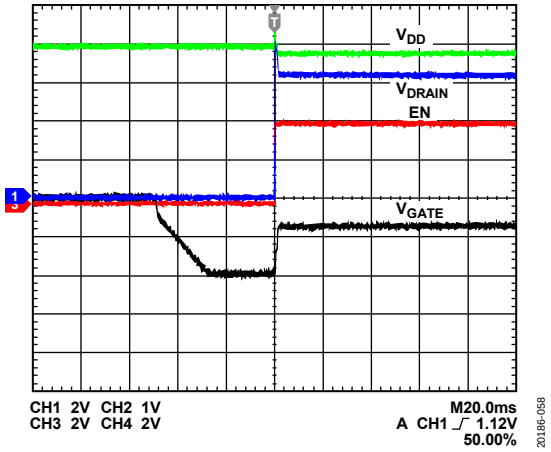

Figure 57. Turn On HMC980LP4E Outputs to ADPA7006CHIP

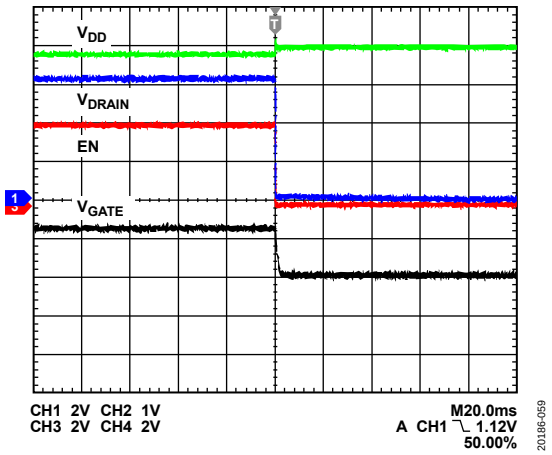

Figure 58. Turn Off HMC980LP4E Outputs to ADPA7006CHIP

CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses closed-loop feedback to continuously adjust VGATE to maintain a constant gate current bias over dc supply variation, temperature, and device to device variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1db is shown in Figure 62, where the RF performance is slightly lower than constant gate voltage bias operation due to a lower drain current at high input powers as the device reaches 1dB compression.

The output P1dB performance for constant drain current bias can be increased toward constant gate voltage bias performance by increasing the set current toward the I_{DD} it reaches under RF drive in the constant gate voltage bias condition, as shown in Figure 62. The limit of increasing I_{DQ} under the constant current operation is set by thermal limitations which can be found in the absolute maximum ratings table from the amplifier data sheet with the maximum power dissipation specification. As the I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely and the power dissipation increases. Therefore, take the exchange between power dissipation and output P1dB performance into consideration when using constant drain current biasing.

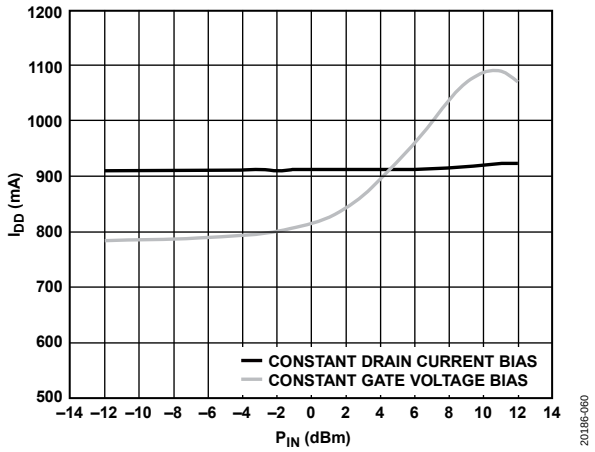

Figure 59. I_{DD} vs. Input Power (P_{IN}), V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias vs. Constant Gate Voltage Bias

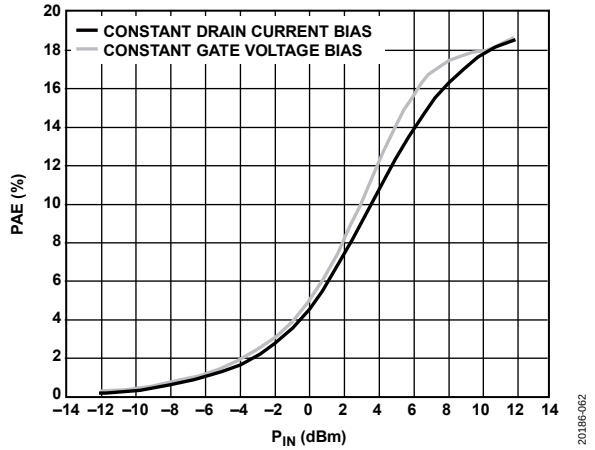

Figure 60. PAE vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz Constant Drain Current Bias vs. Constant Gate Voltage Bias

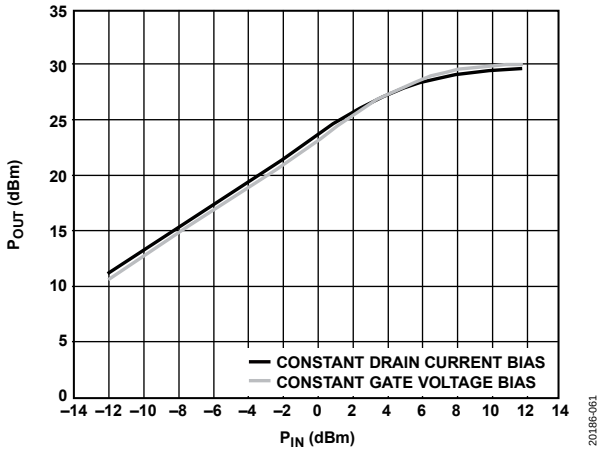

Figure 61. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz Constant Drain Current Bias vs. Constant Gate Voltage Bias

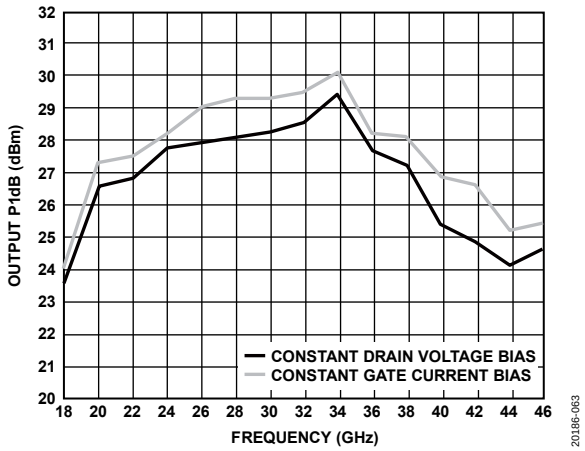

Figure 62. Output P1dB vs. Frequency, V_{DD} = 5 V, Constant Drain Current Bias vs. Constant Gate Voltage Bias

TYPICAL APPLICATION CIRCUIT

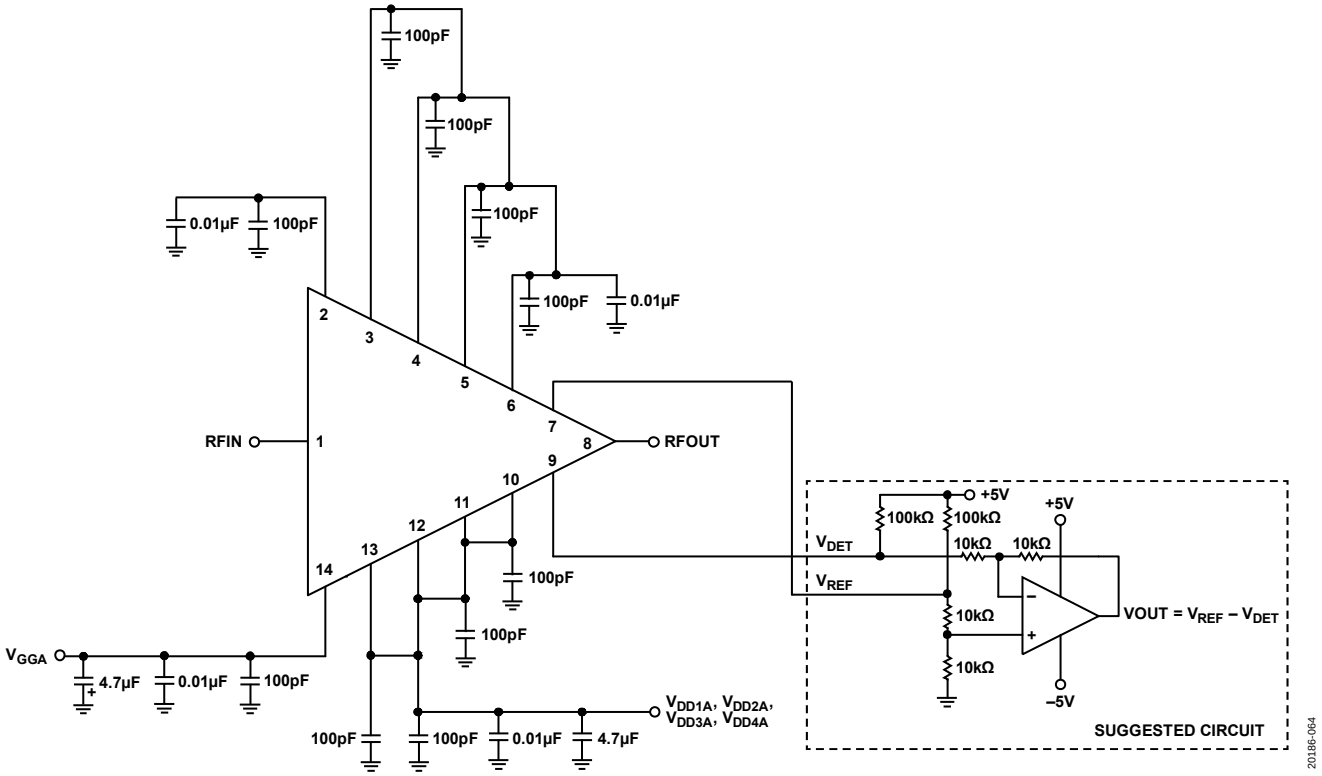

Figure 63. Typical Application Circuit

ASSEMBLY DIAGRAMS

PRIMARY ASSEMBLY DIAGRAM

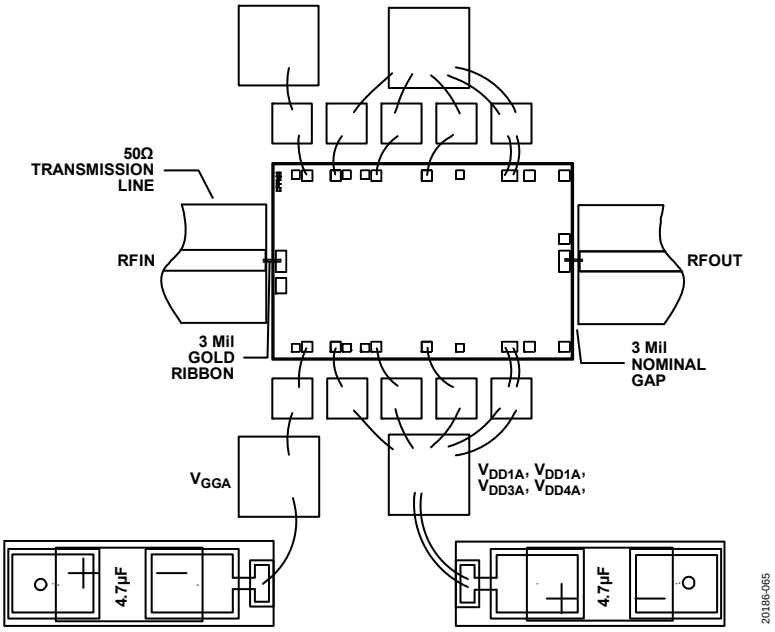

Figure 64. Primary Assembly Diagram

ALTERNATE ASSEMBLY DIAGRAM

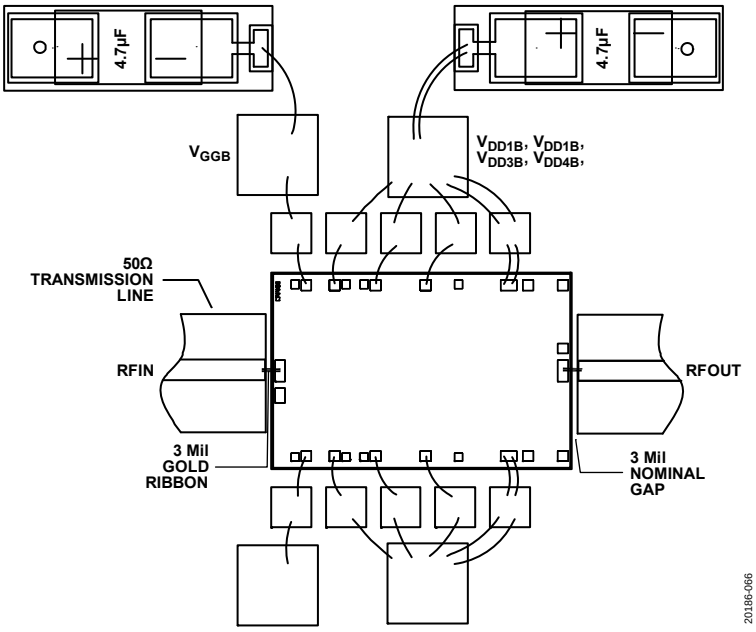

Figure 65. Alternate Assembly Diagram

OUTLINE DIMENSIONS

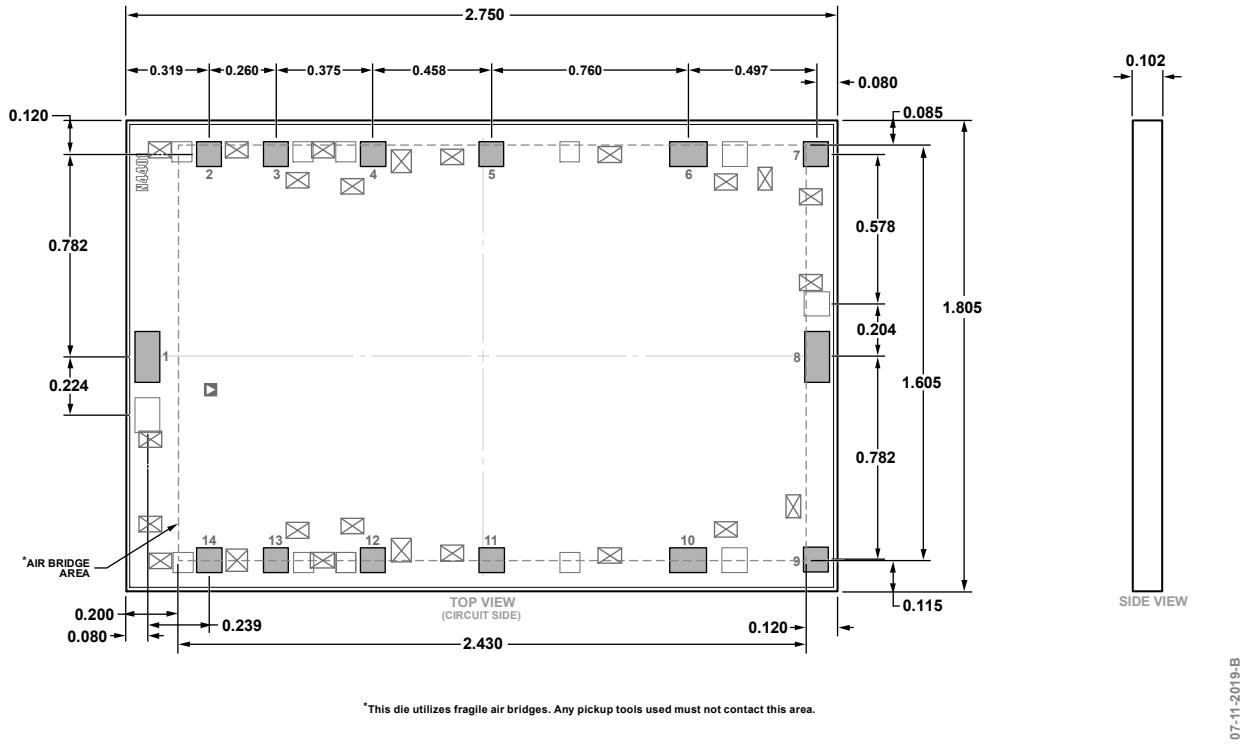

Figure 66. 14-Pad Bare Die [CHIP]
(C-14-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADPA7006CHIP	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-7
ADPA7006C-KIT	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-7

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