

FEATURES

225 ps propagation delay through the switch
4.5 Ω switch connection between ports
Data rate 1.244 Gbps
2.5 V/3.3 V supply operation
Level translation
 3.3 V to 2.5 V
 2.5 V to 1.8 V
Small signal bandwidth 610 MHz
6-lead SC70 package

APPLICATIONS

3.3 V to 2.5 V voltage translation
2.5 V to 1.8 V voltage translation
Bus switching
Docking stations
Memory switching
Analog switch applications

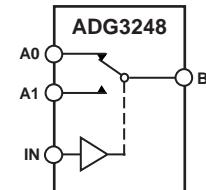
GENERAL DESCRIPTION

The ADG3248 is a 2.5 V or 3.3 V, high performance 2:1 multiplexer/demultiplexer. It is designed on a low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance. The low on resistance allows the input to be connected to the output without additional propagation delay or generating additional ground bounce noise.

Each switch of the ADG3248 conducts equally well in both directions when on. The ADG3248 exhibits break-before-make switching action, preventing momentary shorting when switching channels.

The ADG3248 is available in a tiny 6-lead SC70 package.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. SWITCHES SHOWN FOR A LOGIC 0 INPUT

04404-001

Figure 1.

Table 1. ADG3248 Truth Table

IN Pin Logic Level	Function
Low (L)	B = A0
High (H)	B = A1

PRODUCT HIGHLIGHTS

- 3.3 V or 2.5 V supply operation.
- Extremely low propagation delay through switch.
- 4.5 Ω switches connect inputs to outputs.
- Tiny SC70 package.

Rev. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
 Tel: 781.329.4700 www.analog.com
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TABLE OF CONTENTS

Features	1	Pin Configuration and Function Descriptions.....	5
Applications.....	1	Typical Performance Characteristics	6
General Description	1	Terminology	9
Functional Block Diagram	1	Bus Switch Applications	10
Product Highlights	1	Mixed Voltage Operation, Level Translation.....	10
Revision History	2	Analog Switching	10
Specifications.....	3	Multiplexing.....	11
Absolute Maximum Ratings.....	4	Outline Dimensions.....	12
ESD Caution.....	4	Ordering Guide	12

REVISION HISTORY

10/07—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Table 1	1
Changes to Table 3,.....	4
Changes to Ordering Guide	12

10/03—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.3 V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.¹

Table 2.

Parameter	Symbol	Conditions	Min	B Version Typ ²	Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	$V_{CC} = 2.7$ V to 3.6 V	2.0			V
	V_{INH}	$V_{CC} = 2.3$ V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	$V_{CC} = 2.7$ V to 3.6 V		0.8		V
	V_{INL}	$V_{CC} = 2.3$ V to 2.7 V		0.7		V
Input Leakage Current	I_I			± 0.01	± 1	μA
Off State Leakage Current	I_{OZ}	$0 \leq A, B \leq V_{CC}$		± 0.01	± 1	μA
On State Leakage Current	I_{OL}	$0 \leq A, B \leq V_{CC}$		± 0.01	± 1	μA
Maximum Pass Voltage	V_P	$V_A/V_B = V_{CC} = 3.3$ V, $I_O = -5 \mu A$	2.0	2.5	2.9	V
		$V_A/V_B = V_{CC} = 2.5$ V, $I_O = -5 \mu A$	1.5	1.8	2.1	V
CAPACITANCE ³						
A Port Off Capacitance	C_A Off	$f = 1$ MHz		3.5		pF
B Port Off Capacitance	C_B Off	$f = 1$ MHz		4.5		pF
A, B Port On Capacitance	C_A, C_B On	$f = 1$ MHz		8.5		pF
Control Input Capacitance	C_{IN}	$f = 1$ MHz		4		pF
SWITCHING CHARACTERISTICS ³						
Propagation Delay A to B or B to A, t_{PD}^4	t_{PHL}, t_{PLH}	$C_L = 50$ pF, $V_{CC} = 3$ V			0.225	ns
Propagation Delay Matching ⁵					5	ps
Transition Time	t_{TRANS}	$R_L = 510 \Omega, C_L = 50$ pF		16	29	ns
Break-Before-Make Time	t_{BBM}	$R_L = 510 \Omega, C_L = 50$ pF	5	10		ns
Maximum Data Rate		$V_{CC} = 3.3$ V; $V_A/V_B = 2$ V			1.244	Gbps
Channel Jitter		$V_{CC} = 3.3$ V; $V_A/V_B = 2$ V			45	ps p-p
DIGITAL SWITCH						
On Resistance	R_{ON}	$V_{CC} = 3$ V, $V_A = 0$ V, $I_{BA} = 8$ mA		4.5	8	Ω
		$V_{CC} = 3$ V, $V_A = 1.7$ V, $I_{BA} = 8$ mA		12	28	Ω
		$V_{CC} = 2.3$ V, $V_A = 0$ V, $I_{BA} = 8$ mA		5	9	Ω
		$V_{CC} = 2.3$ V, $V_A = 1$ V, $I_{BA} = 8$ mA		9	18	Ω
On-Resistance Matching	ΔR_{ON}	$V_{CC} = 3$ V, $V_A = 0$ V, $I_A = 8$ mA		0.1	0.5	Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital inputs = 0 V or V_{CC}		0.01	1	μA

¹ Temperature range is as follows for B Version: $-40^\circ C$ to $+85^\circ C$.

² Typical values are at $25^\circ C$, unless otherwise stated.

³ Guaranteed by design, not subject to production test.

⁴ The digital switch contributes no propagation delay other than the resistance-capacitance (RC) delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

⁵ Propagation delay matching between channels is calculated from the on-resistance matching and load capacitance of 50 pF.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V _{CC} to GND	-0.5 V to +4.6 V
Digital Inputs to GND	-0.5 V to +4.6 V
DC Input Voltage	-0.5 V to +4.6 V
DC Output Current	25 mA per channel
Operating Temperature Range Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
θ _{JA} Thermal Impedance	332°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C
Pb-Free Soldering	
Reflow, Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	20 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

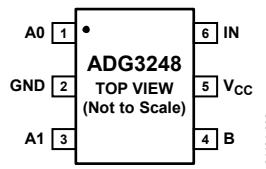


Figure 2. 6-Lead SC70

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Port A0, Input or Output.
2	GND	Ground Reference.
3	A1	Port A1, Input or Output.
4	B	Port B, Input or Output.
5	V _{CC}	Positive Power Supply Voltage.
6	IN	Channel Select.

TYPICAL PERFORMANCE CHARACTERISTICS

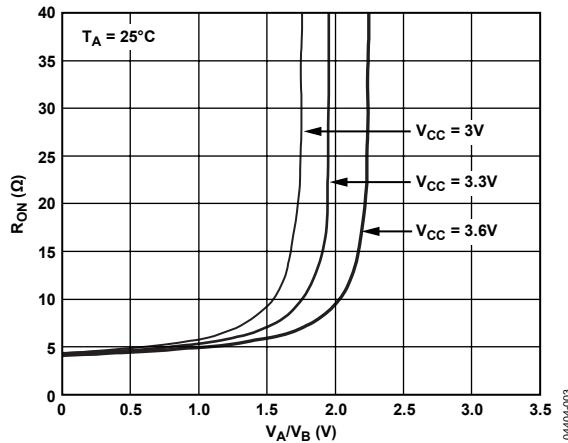


Figure 3. On Resistance vs. Input Voltage

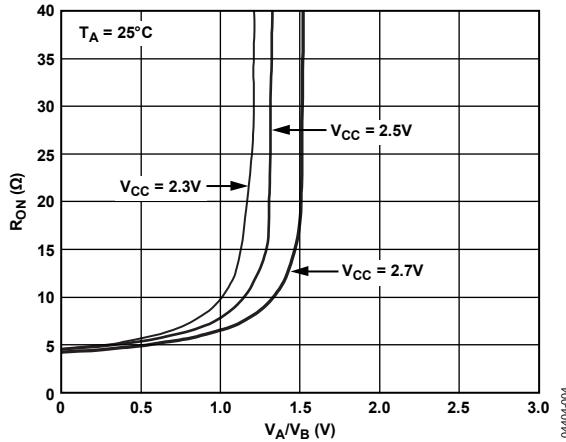


Figure 4. On Resistance vs. Input Voltage

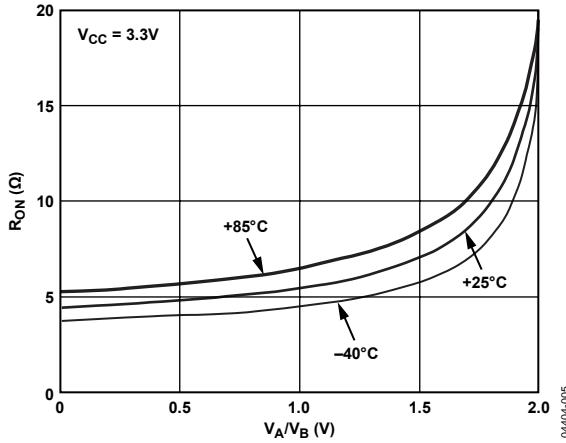


Figure 5. On Resistance vs. Input Voltage for Different Temperatures

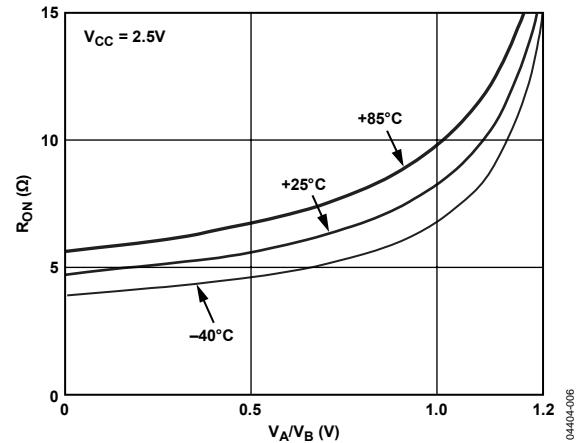
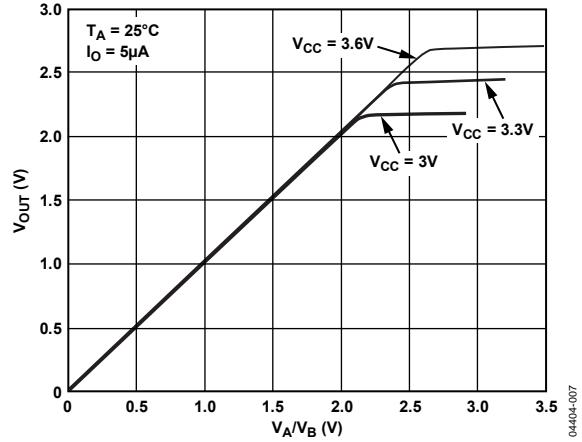
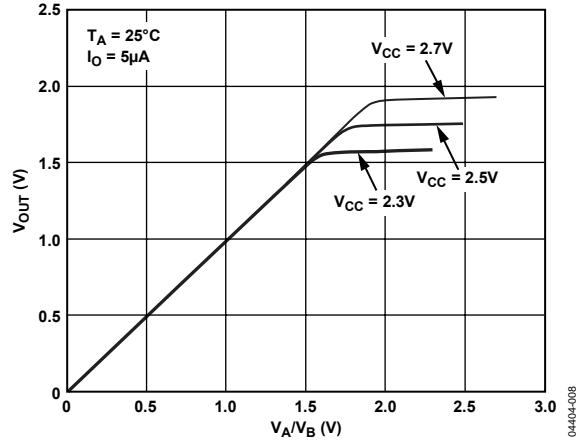
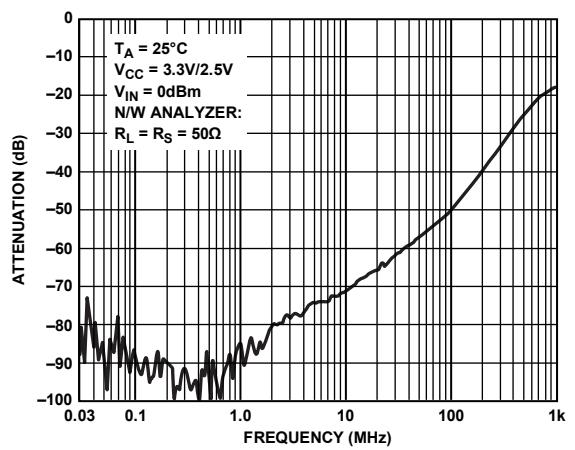
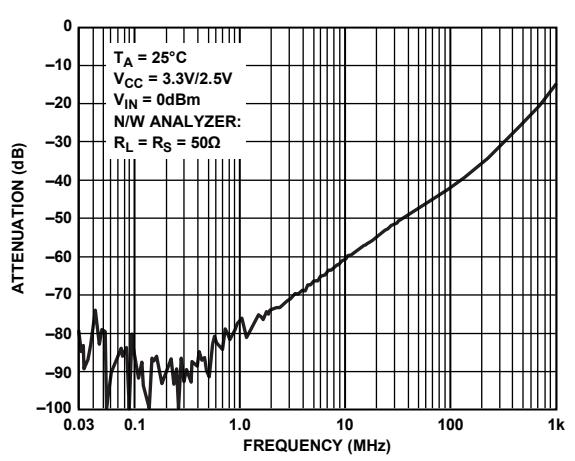
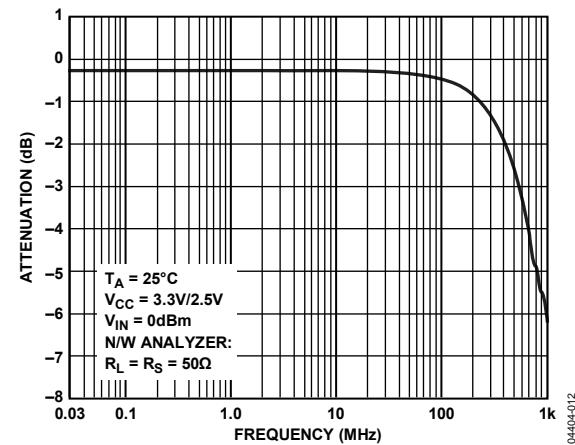
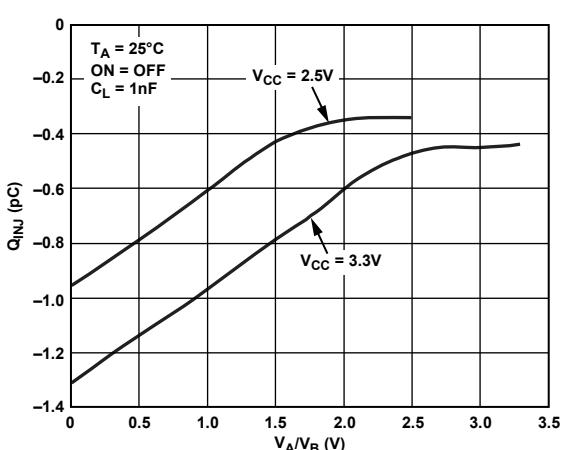
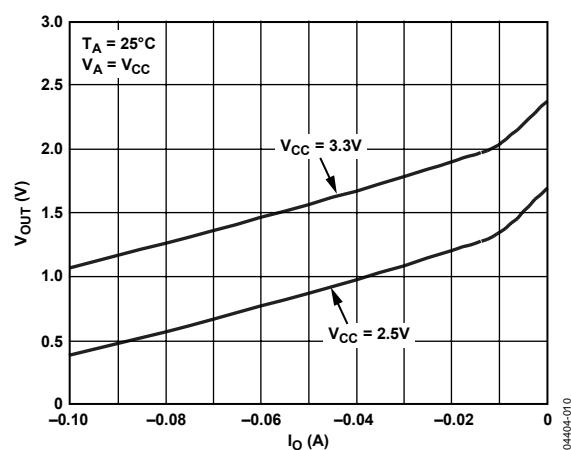
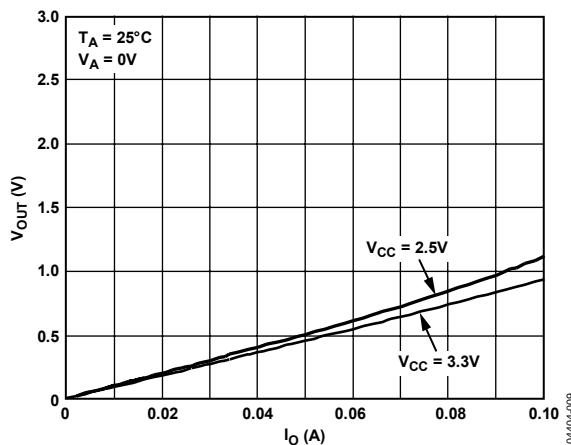
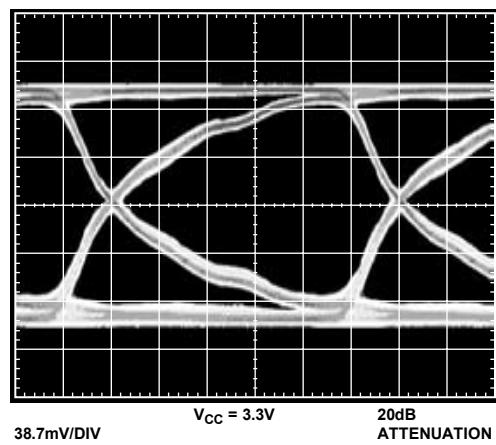
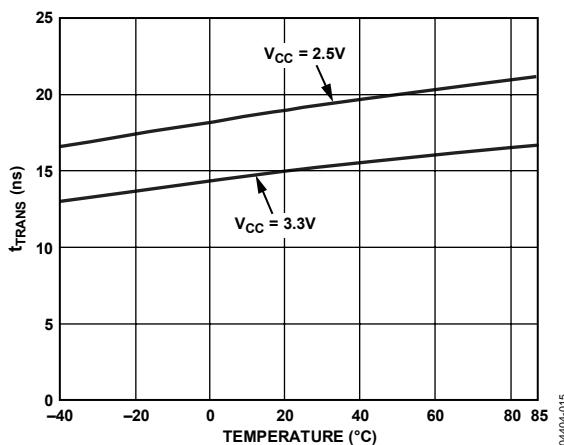


Figure 6. On Resistance vs. Input Voltage for Different Temperatures

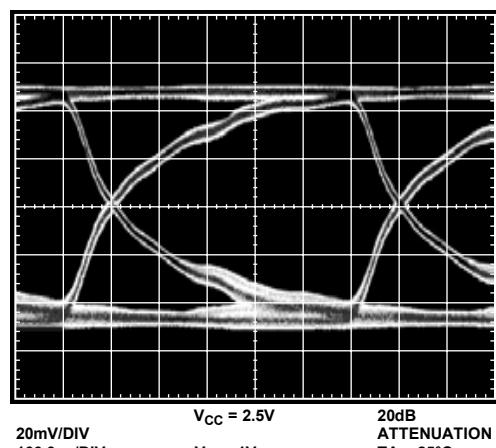
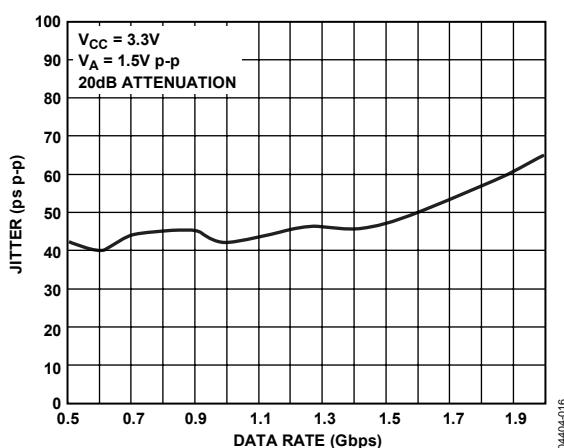
Figure 7. Pass Voltage vs. V_{CC} Figure 8. Pass Voltage vs. V_{CC}



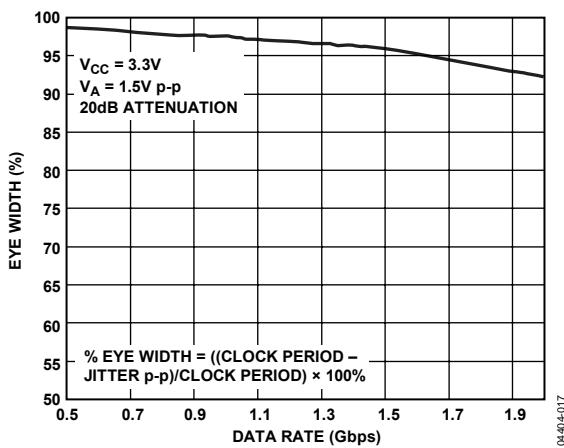
ADG3248



04404-018



04404-019



TERMINOLOGY

V_{CC}	C_{X Off} Off switch capacitance.
Positive power supply voltage.	
GND	C_{X On} On switch capacitance.
Ground (0 V) reference.	
V_{INH}	C_{IN} Control input capacitance. C _{IN} consists of IN.
Minimum input voltage for Logic 1.	
V_{INL}	I_{CC} Quiescent power supply current. I _{CC} represents the leakage current between the V _{CC} and ground pins and is measured when all control inputs are at a logic high or logic low level and the switches are off.
Maximum input voltage for Logic 0.	
I_I	t_{PLH}, t_{PHL} Data propagation delay through the switch in the on state. Propagation delay is related to the RC time constant R _{ON} × C _L , where C _L is the load capacitance.
Input leakage current at the control inputs.	
I_{OZ}	t_{BBM} On or off time measured between the 90% points of both switches when switching from one to another.
Off state leakage current. I _{OZ} is the maximum leakage current at the switch pin in the off state.	
I_{OL}	t_{TRANS} Time taken to switch from one channel to the other, measured from 50% of the in signal to 90% of the out signal.
On state leakage current. I _{OL} is the maximum leakage current at the switch pin in the on state.	
V_P	Maximum Data Rate Maximum rate at which data can be passed through the switch.
Maximum pass voltage. V _P relates to the clamped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.	
R_{ON}	Channel Jitter Peak-to-peak value of the sum of the deterministic and random jitter of the switch channel.
Ohmic resistance offered by a switch in the on state. R _{ON} is measured at a given voltage by forcing a specified amount of current through the switch.	
ΔR_{ON}	
On resistance match between any two channels, that is, R _{ON max} – R _{ON min} .	

BUS SWITCH APPLICATIONS

MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches can provide an ideal solution for interfacing between mixed voltage systems. The ADG3248 is suitable for applications in which voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 2.5 V to 1.8 V or bidirectionally from 3.3 V directly to 2.5 V.

Figure 20 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs; therefore, placing the ADG3248 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

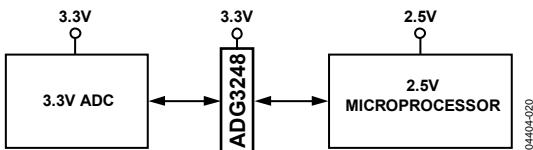


Figure 20. Level Translation Between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC} , the maximum output signal is clamped to within a voltage threshold below the V_{CC} supply. In this case, the output is limited to 2.5 V, as shown in Figure 22.

This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

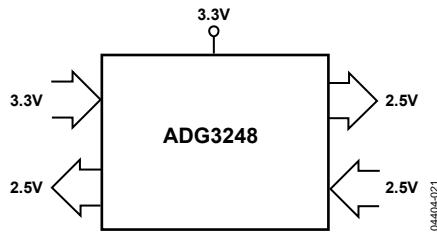


Figure 21. 3.3 V to 2.5 V Voltage Translation

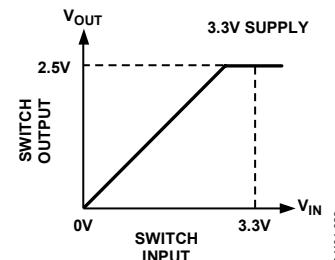


Figure 22. 3.3 V to 2.5 V Voltage Translation

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V and the input signal range is 0 V to V_{CC} , the maximum output signal is clamped to within a voltage threshold below the V_{CC} supply. In this case, the output is limited to approximately 1.8 V, as shown in Figure 24.

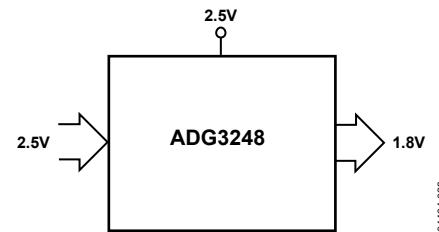


Figure 23. 2.5 V to 1.8 V Voltage Translation

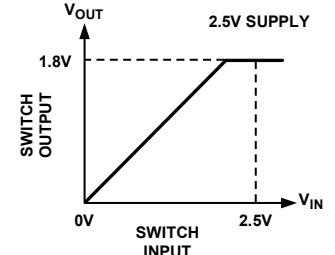


Figure 24. 2.5 V to 1.8 V Voltage Translation

ANALOG SWITCHING

Bus switches can be used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller on and off channel capacitance, and thus better frequency performance than their analog counterparts. The bus switch channel itself, consisting solely of an NMOS switch, limits the operating voltage (see Figure 3 for a typical plot) but, in many cases, this does not present an issue.

MULTIPLEXING

Many systems, such as docking stations and memory banks, have a large number of common bus signals. Common problems faced by designers of these systems include

- Large delays caused by capacitive loading of the bus
- Noise due to simultaneous switching of the address and data bus signals

Figure 25 shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. If a bus switch is used as shown in Figure 26, the output load on the memory address and data bits is halved. The speed at which data from the selected bank can flow is much improved because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also reduced.

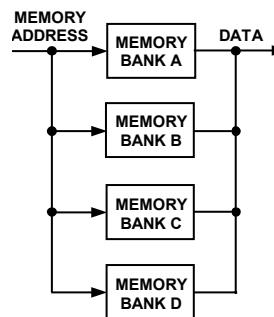


Figure 25. All Memory Banks Are Permanently Connected to the Bus

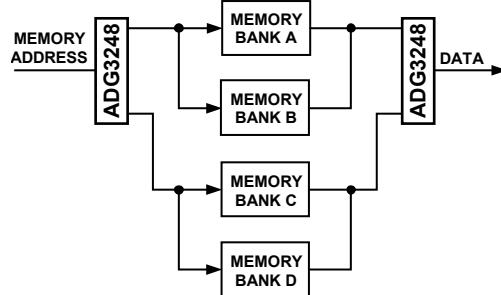
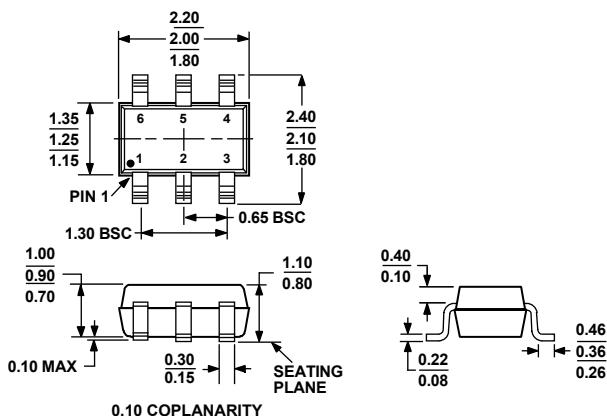


Figure 26. ADG3248 Used to Reduce Both Access Time and Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 27. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG3248BKS-R2	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKS-REEL	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKS-REEL7	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SMA
ADG3248BKSZ-REEL7 ¹	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	S1W

¹ Z = RoHS Compliant Part.

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