-20V, 1A, Ultralow Noise, Ultrahigh PSRR Negative Linear Regulator

FEATURES

- Ultralow RMS Noise: 1.4μV_{RMS} (10Hz to 100kHz)
- Ultralow Spot Noise: 4nV/√Hz at 10kHz
- Ultrahigh PSRR: 75dB at 1MHz
- Output Current: 1A
- Wide Input Voltage Range: -3.5V to -20V
- Single Capacitor Improves Noise and PSRR
- 100μA SET Pin Current: ±0.5% Initial Accuracy
- Single Resistor Programs Output Voltage
- Programmable Current Limit
- Low Dropout Voltage: 350mV
- Output Voltage Range: 0V to -19V
- Programmable Power Good and Fast Start-Up
- Bi-directional Precision Enable/UVLO
- VIOC pin to manage power dissipation
- Parallelable for Lower Noise and Higher Current
- Internal Current Limit with Foldback
- Minimum Output Capacitor: 10μF Ceramic
- Compact, 14-lead, 4mm x 3mm DFN package

APPLICATIONS

- RF Power Supplies and Precision Power Supplies
- Very Low Noise Instrumentation
- High-speed/High-precision Data Converters
- Medical Applications: Diagnostics and Imaging
- Post-regulator for Switching Supplies

DESCRIPTION

The **LT3099** is a high-performance, low-dropout negative linear regulator featuring Analog Devices, Inc.'s ultralow noise and ultrahigh power-supply rejection ratio (PSRR) architecture for powering noise-sensitive applications. Designed as a precision current reference followed by a high-performance voltage buffer, the LT3099 can be easily paralleled to reduce noise further, increase output current, and spread heat on the PCB.

The device supplies 1A at a typical 350mV dropout voltage. The operating quiescent current is nominally 2.9mA and drops to 5μA in shutdown. The LT3099's wide output voltage range (0V to -19V) error amplifier operates at unity gain and provides virtually constant output noise, PSRR, bandwidth, and load regulation independent of the programmed output voltage. Additionally, the regulator features a bi-directional enable pin, programmable current limit, fast start-up capability, and programmable power good for indicating output voltage regulation. The regulator incorporates a tracking function to control an upstream supply to maintain a constant voltage across the LT3099 and minimize power dissipation.

Built-in protection includes an internal current limit with foldback and a thermal limit with hysteresis. The LT3099 is available in a thermally enhanced 4mm × 3mm DFN package.

TYPICAL APPLICATION

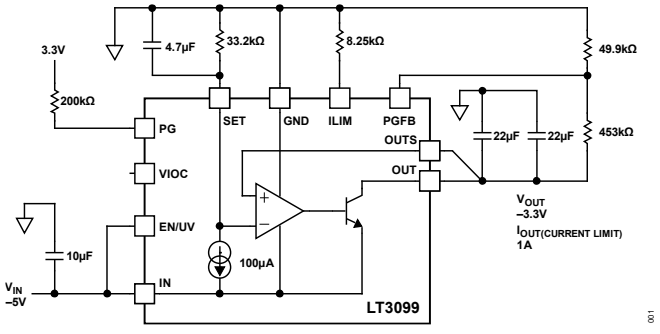


Figure 1. Typical Application Circuit

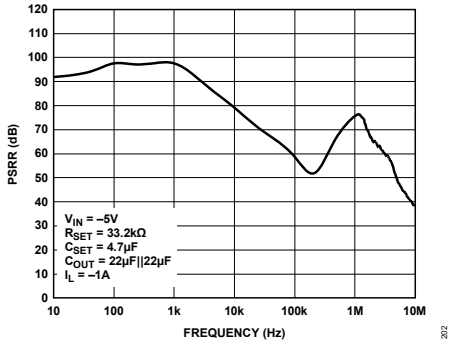


Figure 2. PSSR vs. Frequency

TABLE OF CONTENTS

REVISION HISTORY

04/2025 - Rev. 0, Initial Release.

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_J = −40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, output capacitance (C_{OUT}) = one 10µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range[1]	I_{LOAD} = 1A	-20		-3.5	V
SET Pin Current (I_{SET})	V_{IN} = -3.5V, I_{LOAD} = 1mA, V_{OUT} = -1.5V, T_A = 25°C	99.5	100	100.5	µA
	-20V < V_{IN} < -3.5V, -19V < V_{OUT} < 0V, 1mA < I_{LOAD} < 1A[2]	99	100	101	µA
Fast Start-Up SET Pin Current	V_{PGFB} = -289mV, V_{IN} = -3.5V, V_{SET} = -1.5V		10		mA
Output Offset Voltage, V_{OS} (V_{OUT} – V_{SET})[3]	V_{IN} = -3.5V, I_{LOAD} = 1mA, V_{OUT} = -1.5V	-1		1	mV
	-20V < V_{IN} < -3.5V, -19V < V_{OUT} < 0V, 1mA < I_{LOAD} < 1A[2]	-2		2	
Line Regulation (ΔI_{SET})	V_{IN} = -3.5V to -20V, I_{LOAD} = 1mA, V_{OUT} = -1.5V		1	±15	nA/V
Line Regulation (ΔV_{OS})	V_{IN} = -3.5V to -20V, I_{LOAD} = 1mA, V_{OUT} = -1.5V[3]		0.3	±20	µV/V
Load Regulation (ΔI_{SET})	I_{LOAD} = 1mA to 1A, V_{IN} = -3.5V, V_{OUT} = -1.5V		3		nA
Load Regulation: ΔV_{OS}	I_{LOAD} = 1mA to 1A, V_{IN} = -3.5V, V_{OUT} = -1.5V[3]		0.15	0.7	mV
Change in I_{SET} with V_{SET}	V_{SET} = -1.5V to -19V, V_{IN} = -20V, I_{LOAD} = 1mA		100	500	nA
Change in V_{OS} with V_{SET}	V_{SET} = -1.5V to -19V, V_{IN} = -20V, I_{LOAD} = 1mA[3]		0.08	0.3	mV
Change in I_{SET} with V_{SET}	V_{SET} = 0V to -1.5V, V_{IN} = -20V, I_{LOAD} = 1mA		250	500	nA
Change in V_{OS} with V_{SET}	V_{SET} = 0V to -1.5V, V_{IN} = -20V, I_{LOAD} = 1mA[3]		0.2	0.4	mV
Error Amplifier Switchover Point	V_{IN} = -3.5V, I_{LOAD} = 1mA, V_{SET} rising		-1.125		V
	V_{IN} = -3.5V, I_{LOAD} = 1mA, V_{SET} falling		-1.12		V
	Hysteresis		5		mV
Dropout Voltage[4]	I_{LOAD} = 1mA, 50mA		200	250	mV
	I_{LOAD} = 100mA		200	250	mV
	I_{LOAD} = 500mA		250	350	mV

(T_J = −40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, output capacitance (C_{OUT}) = one 10µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	I_{LOAD} = 1A		350	450	mV
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$[5]	I_{LOAD} = 10µA		2.9		mA
	I_{LOAD} = 1mA		3.0		mA
	I_{LOAD} = 50mA		3.5		mA
	I_{LOAD} = 100mA		4		mA
	I_{LOAD} = 500mA		7		mA
	I_{LOAD} = 1A		11		mA
Output Noise Spectral Density[3,6]	I_{LOAD} = 1A, Freq. = 10Hz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = -3.3V		800		nV/√Hz
	I_{LOAD} = 1A, Freq. = 10Hz, C_{OUT} = 10µF, C_{SET} = 4.7µF, -19V ≤ V_{OUT} ≤ -1.5V		140		nV/√Hz
	I_{LOAD} = 1A, Freq. = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, -19V ≤ V_{OUT} ≤ -1.5V		4		nV/√Hz
	I_{LOAD} = 1A, Freq. = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, -1.5V ≤ V_{OUT} ≤ 0V		7		nV/√Hz
Output Root mean square (RMS) Noise[3,6]	I_{LOAD} = 1A, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = -3.3V		2		μV_{RMS}
	I_{LOAD} = 1A, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, -19V ≤ V_{OUT} ≤ -1.5V		1.4		μV_{RMS}
	I_{LOAD} = 1A, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, -1.5V ≤ V_{OUT} ≤ 0V		2.5		μV_{RMS}
Reference Current RMS Output Noise[3,6]	BW = 10Hz to 100kHz		10		nA_{RMS}
Ripple Rejection -10V ≤ V_{OUT} ≤ -1.1V $V_{IN} - V_{OUT}$ = 2V (Average)[3,6] or $V_{IN(MIN)}$= -3.5V	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 1A, C_{OUT} = 10µF		96		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 1A, C_{OUT} = 10µF		80		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 1A, C_{OUT} = 10µF		60		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 1A, C_{OUT} = 10µF		65		dB
	V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 1A, C_{OUT} = 10µF		35		dB

(T_J = −40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, output capacitance (C_{OUT}) = one 10µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ripple Rejection $V_{OUT} \geq$ -1.1V V_{IN} = -3.5V[3,6]	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 1A, C_{OUT} = 10µF		90		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 1A, C_{OUT} = 10µF		75		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 1A, C_{OUT} = 10µF		55		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 1A, C_{OUT} = 10µF		60		dB
	V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 1A, C_{OUT} = 10µF		35		dB
EN/UV Pin Threshold	Positive EN/UV Trip Point Rising (Turn-On), V_{IN} = -3.5V		1.28		V
	Negative EN/UV Trip Point Rising (Turn-On), V_{IN} = -3.5V		-1.27		V
EN/UV Pin Hysteresis	Positive EN/UV Trip Point Hysteresis, V_{IN} = -3.5V		315		mV
	Negative EN/UV Trip Point Hysteresis, V_{IN} = -3.5V		330		mV
EN/UV Pin Current	$V_{EN/UV}$ = 0V, V_{IN} = -20V		0		µA
	$V_{EN/UV}$ = -1.5V, V_{IN} = -20V		-0.62		µA
	$V_{EN/UV}$ = -20V, V_{IN} = -20V		18		µA
	$V_{EN/UV}$ = 1.5V, V_{IN} = -20V		8		µA
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)	V_{IN} = -6V, V_{PG} = Open		5	15	µA
Internal Current Limit[7]	V_{IN} = -3.5V, V_{OUT} = 0V	1.43	1.55		A
	V_{IN} = -12V, V_{OUT} = 0V		890		mA
	V_{IN} = -20V, V_{OUT} = 0V		230		mA
Programmable Current Limit	Programming Scale Factor: -20V < V_{IN} < -3.5V[8]		8.2		A × kΩ
	V_{IN} = -3.5V, V_{OUT} = 0V, R_{ILIM} = 8.25kΩ	0.9	1	1.1	A
	V_{IN} = -3.5V, V_{OUT} = 0V, R_{ILIM} = 44.2kΩ	170	200	230	mA
PGFB Trip Point	PGFB Trip Point Rising	-330	-315	-300	mV
PGFB Hysteresis	PGFB Trip Point Hysteresis		7		mV
PGFB Pin Current	V_{IN} = -3.5V, V_{PGFB} = -290mV		25		nA

(T_J = −40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, output capacitance (C_{OUT}) = one 10µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PG Output Low Voltage	I_{PG} = 100µA		15		mV
PG Leakage Current	V_{PG} = 20V			1	µA
Voltage Input-to-Output Control (VIOC) Amplifier Gain	-20V ≤ V_{IN} ≤ -3.5V, V_{OUT} ≤ -1.5V		1		V/V
VIOC Sink Current	V_{IN} – V_{OUT} = -2V, V_{VIOC} = -1V	300			µA
VIOC Voltage for low output voltages[9]	V_{IN} = –3.5V, V_{OUT} > –1.5V		-2		V
Thermal Shutdown	T_J Rising		159		°C
	Hysteresis		5		°C
Start-Up Time	$V_{OUT(NOM)}$ = -5V, I_{LOAD} = 1A, C_{SET} = 0.47µF, V_{IN} = -6V, V_{PGFB} = -6V		55		ms
	$V_{OUT(NOM)}$ = -5V, I_{LOAD} = 1A, C_{SET} = 4.7µF, V_{IN} = -6V, V_{PGFB} = -6V		550		ms
	$V_{OUT(NOM)}$ = -5V, I_{LOAD} = 1A, C_{SET} = 4.7µF, V_{IN} = -6V, R_{PG1} = 50kΩ, R_{PG2} = 700kΩ (with Fast Start-Up to 90% of V_{OUT})		10		ms
Thermal Regulation	10ms Pulse		-0.01		%/W

1 The EN/UV pin threshold must be met to ensure device operation.

2 Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply to all possible combinations of input voltage and output current, especially due to the internal current limit foldback, which starts to decrease the current limit at V_{IN} – V_{OUT} > 8V. If operating at maximum output current, limit the input voltage range. If operating at maximum input voltage, limit the output current range.

3 The OUTS pin ties directly to the OUT pin.

4 Dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when the output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when V_{IN} = $V_{OUT(NOMINAL)}$. For lower output voltages (below -3.15V), the dropout voltage is limited by the minimum input voltage specification.

5 GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SET or ILIM pin current, but they are included in the Quiescent current.

6 Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise and the reference current's noise. The output noise then equals the error amplifier noise. The Use of a SET pin bypass capacitor also increases start-up time.

7 The internal backup current limit circuitry incorporates foldback protection that decreases the current limit for $V_{IN} - V_{OUT} > 8V$. Some output current level is provided at all $V_{IN} - V_{OUT}$ differential voltages. See the *Typical Performance Characteristics* graph for the current limit vs $V_{IN} - V_{OUT}$.

8 The current limit programming scale factor is specified while the internal backup current limit is inactive. Note that the internal current limit has foldback protection for $V_{IN} - V_{OUT}$ differentials greater than 8V.

9 The VIOC amplifier outputs a voltage equal to $V_{IN} - V_{OUT}$ or $V_{IN} + 1.5V$ (when V_{OUT} is between 0V and -1.5V). See the *Block Diagram* and the *Applications Information* for more information.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings[1]

PARAMETER	RATING
IN Pin Voltage with Respect to GND Pin	–22V, +0.3V
EN/UV Pin Voltage with Respect to IN Pin[2]	–0.3V, +30V
EN/UV Pin Voltage with Respect to GND Pin	±22V
PG Pin Voltage with Respect to IN Pin[2]	–0.3V, +30V
PG Pin Voltage with Respect to GND Pin	–0.3V, +22V
PGFB Pin Voltage with Respect to IN Pin[2]	–0.3V, +30V
PGFB Pin Voltage with Respect to GND Pin	±22V
PGFB Pin Current	±1mA
ILIM Pin Voltage with Respect to IN Pin[2]	–0.3V, +22V
VIOC Pin Voltage with Respect to IN Pin[2]	–0.3V, +22V
VIOC Pin Voltage with Respect to GND Pin	–2V, +0.3V
SET Pin Voltage with Respect to IN Pin[2]	–0.3V, +22V
SET Pin Voltage with Respect to GND Pin	–22V, +5V
SET Pin Current[3]	±10mA
OUTS Pin Voltage with Respect to IN Pin[2]	-0.3V, +22V
OUTS Pin Voltage with Respect to GND Pin	–22V, +5V
OUTS Pin Current[3]	±10mA
SET-to-OUTS Differential[4]	±22V
OUT Pin Voltage with Respect to IN Pin[2]	–0.3V, +22V
OUT Pin Voltage with Respect to GND Pin	–22V, +5V
OUT-to-OUTS Differential[5]	±1.2V
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature Range[6]	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

2 Parasitic diodes exist internally between the EN/UV, PG, VIOC, ILIM, PGFB, SET, OUTS, and OUT pins and the IN pin. Do not drive these pins more than 0.3V below the IN pin during a fault condition. These pins must remain at a voltage more positive than IN during normal operation.

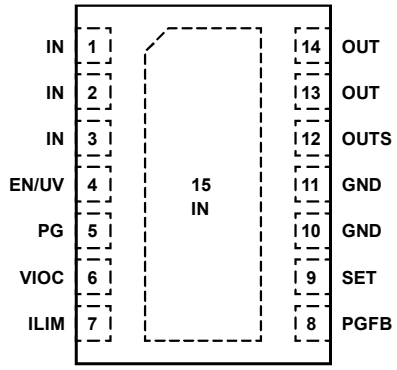
3 SET and OUTS pins are clamped using diodes and two 400Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current.

4 The current requirement for the maximum SET and OUTS pins must be satisfied.

[5] The maximum OUT to OUTS differential is guaranteed by design.

[6] The LT3099 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3099 is tested at T_A = 25°C. Performance of the LT3099 over the full –40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3099 is guaranteed over the full –40°C to 125°C operating T_J range.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



14-LEAD (4mm × 3mm) DUAL FLAT NO-LEAD (DFN) PACKAGE
EXPOSED PAD TIES TO IN, MUST BE SOLDERED TO PCB
$\theta_{JC(TOP)}$ = 42.8°C/W, $\theta_{JC(BOT)}$ = 4.7°C/W
002

Figure 3. Pin Configuration

Pin Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1-3, Exposed Pad Pin 15	IN	Input. These pins supply power to the regulator. The LT3099 requires a bypass capacitor at the IN pin. Generally, a battery's output impedance rises with frequency, so a bypass capacitor should be included in battery-powered applications. While a 10µF input bypass capacitor generally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop. See the *Applications Information* section for the proper use of an input capacitor and its effect on circuit performance.
4	EN/UV	Enable/UVLO. Pulling the LT3099's EN/UV pin low places the part in shutdown. The quiescent current in shutdown drops to 5µA, and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV, and GND.

PIN	NAME	DESCRIPTION
		The EN/UV pin is bi-directional and can be switched with either a positive or negative voltage. The LT3099 typically turns on when the EN/UV voltage exceeds 1.28V above ground (with a 315mV hysteresis on its falling edge) or 1.27V below ground (with a 330mV hysteresis). If unused, tie EN/UV to IN. Do not float the EN/UV pin.
5	PG	Power Good. PG is an open-drain flag that indicates output voltage regulation. PG pulls low if PGFB is more positive than -315mV. If the power good functionality is not needed, float the PG pin.
6	VIOC	Voltage for Input-to-Output Control. The LT3099 incorporates a tracking feature to control a circuit supplying power to the LT3099 to maintain the differential voltage across the LT3099. This function maximizes efficiency and performance while minimizing power dissipation. See the *Applications Information* section for more details.
7	ILIM	Current Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the LT3099's GND pin. The programming scale factor is nominally 8.2A × kΩ. If the programmable current limit functionality is not needed, tie ILIM to GND. Do not float the ILIM pin.
8	PGFB	Power Good Feedback. The PG pin pulls high if PGFB goes more negative than -315mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB, and GND sets the programmable power good threshold with the following transfer function: -0.315V × (1 + R_{PG2}/R_{PG1}). PGFB also activates the fast start-up circuitry (See the *Applications Information* section for more details). If power good and fast start-up functionality are not needed, tie PGFB to IN.
9	SET	Set. This pin is the inverting input of the error amplifier and the regulation set-point for the LT3099. The SET pin sinks a precision 100µA current that flows through an external resistor connected between SET and GND. The LT3099's output voltage is determined by $V_{SET} = I_{SET} \times R_{SET}$. The output voltage range is from 0V to -19V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of increased start-up time.

PIN	NAME	DESCRIPTION
		For optimum load regulation, Kelvin connect the ground side of the SET pin directly to the load.
10, 11	GND	Ground.
12	OUTS	Output Sense. This pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. Exercise care regarding the placement of input capacitors relative to output capacitors. See the *Applications Information* section for more information on capacitor placement and board layout.
13, 14	OUT	Output. This pin supplies power to the load. For stability, use a minimum 10µF output capacitor with an ESR below 30mΩ and an ESL below 1.5nH. Large load transients require larger output capacitance to limit peak voltage transients. See the *Applications Information* section for more details on output capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless otherwise noted.

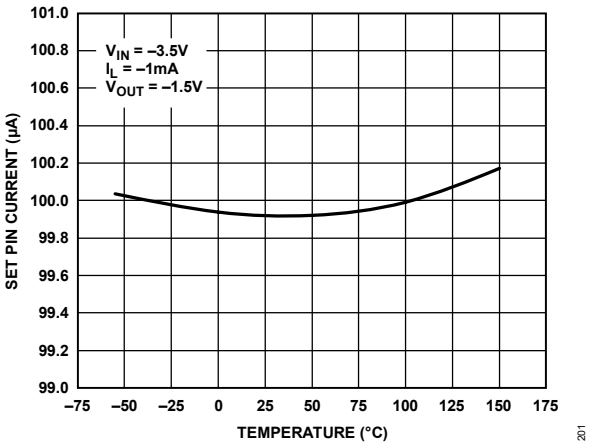


Figure 4. SET Pin current vs. Temperature

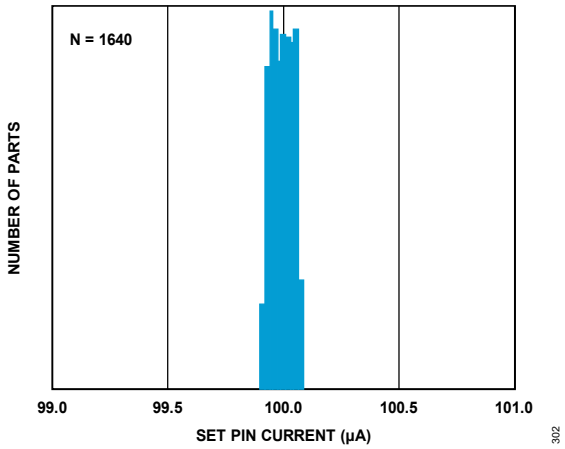


Figure 5. SET Pin Current Distribution

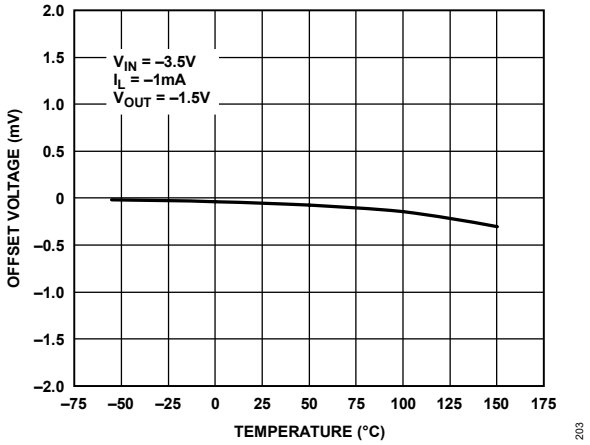


Figure 6. Offset Voltage (V_{OUT}–V_{SET}) vs. Temperature

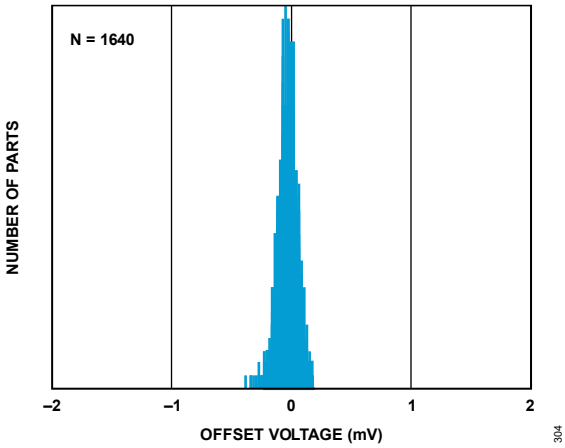


Figure 7. Offset Voltage (V_{OS}) Distribution

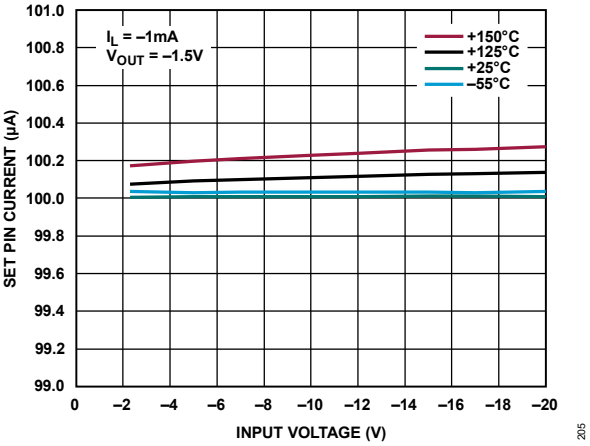


Figure 8. SET Pin Current vs. Input Voltage

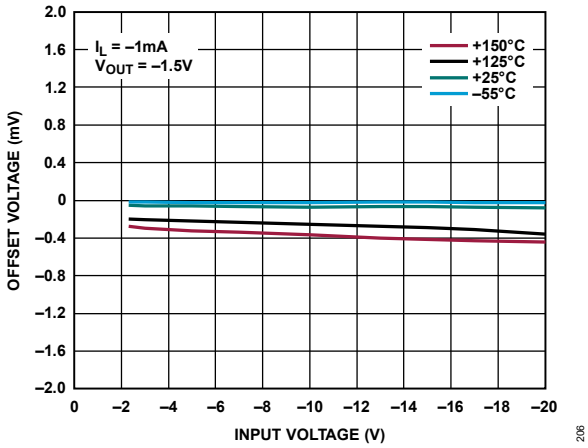


Figure 9. Offset Voltage (V_{OUT}–V_{SET}) vs. Input Voltage

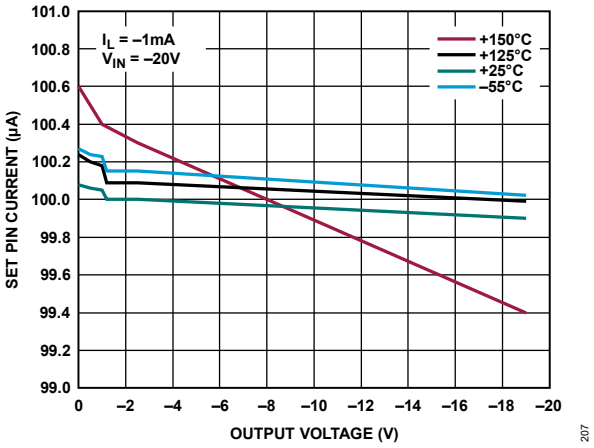


Figure 10. SET Pin Current vs. OUT Voltage

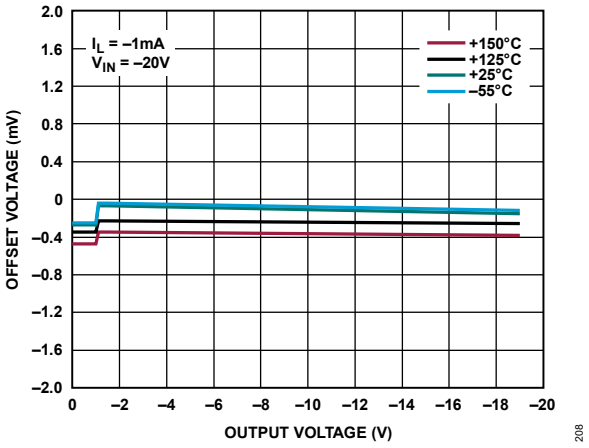


Figure 11. Offset Voltage (V_{OUT}–V_{SET}) vs. Output Voltage

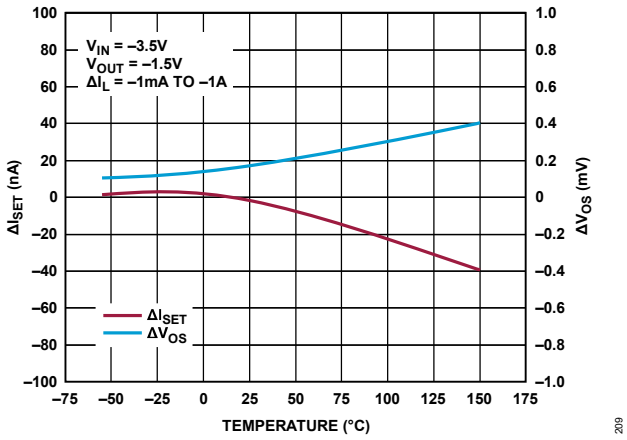


Figure 12. ΔI_{SET} and ΔV_{OS} Load Regulation vs. Temperature

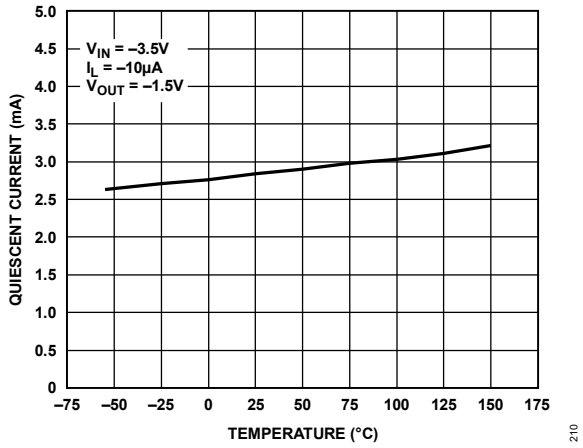


Figure 13. Quiescent Current (Operational) vs. Temperature

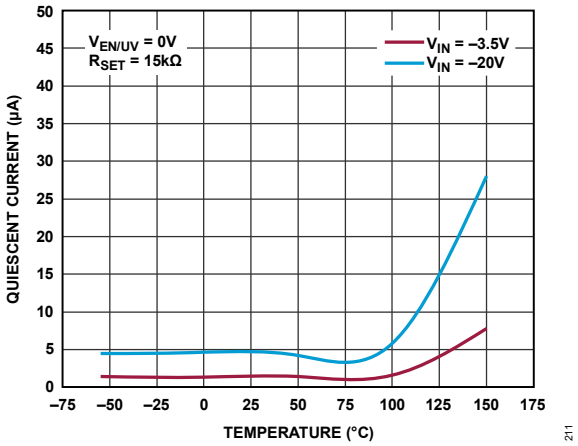


Figure 14. Quiescent Current (Shutdown) vs. Temperature

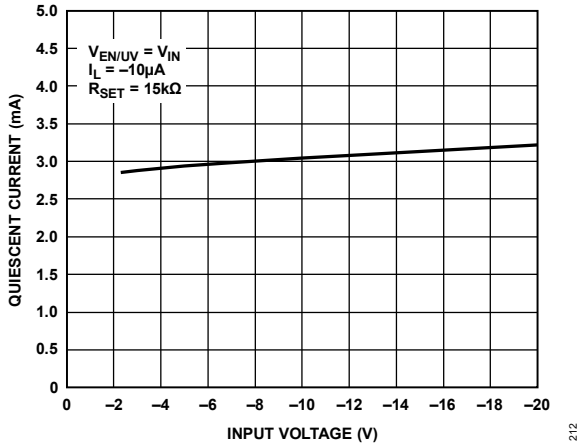


Figure 15. Quiescent Current (Operational) vs. IN Voltage

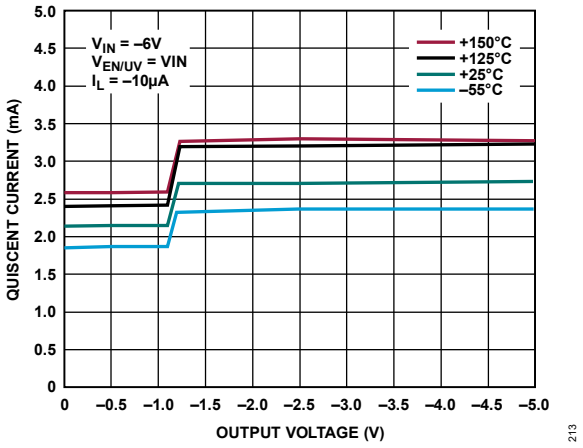


Figure 16. Quiescent Current (Operational) vs. OUT Voltage

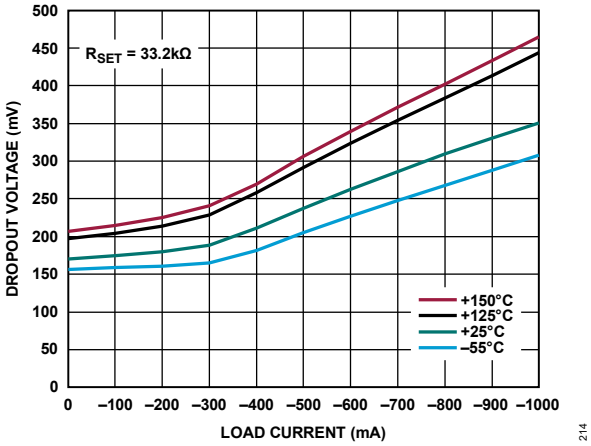


Figure 17. Typical Dropout Voltage vs. Load Current

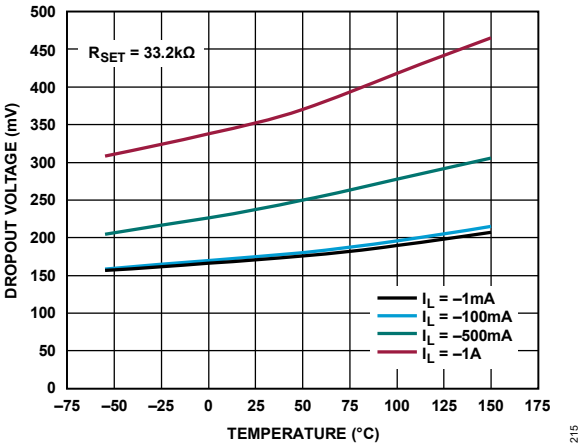


Figure 18. Dropout Voltage vs. Temperature

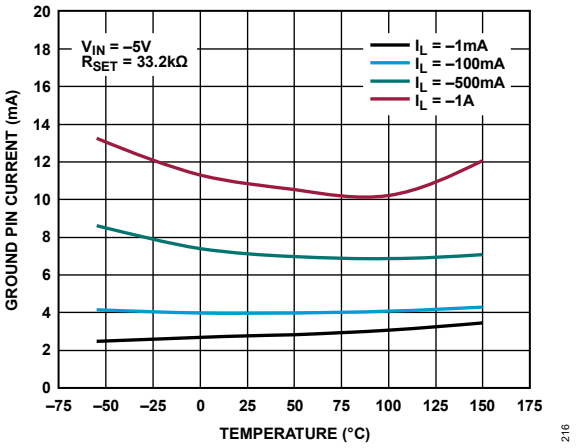


Figure 19. GND Pin Current vs. Temperature

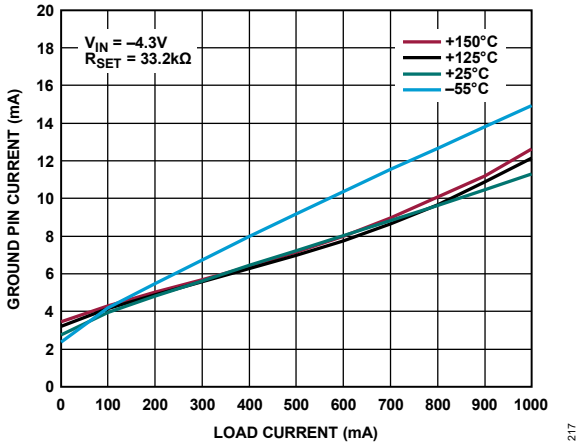


Figure 20. GND Pin Current vs. Load Current

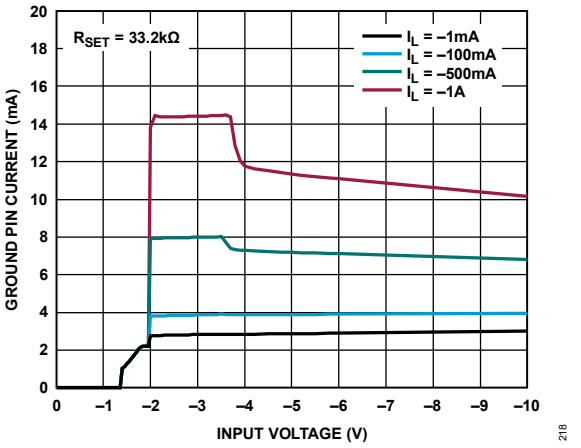


Figure 21. GND Pin Current vs. Input Voltage

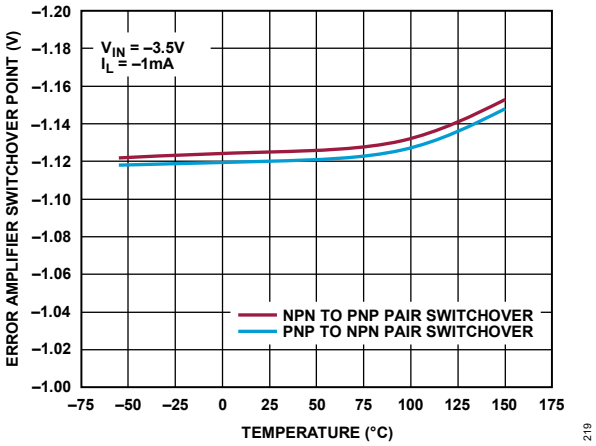


Figure 22. Error Amplifier Switchover Point vs. Temperature

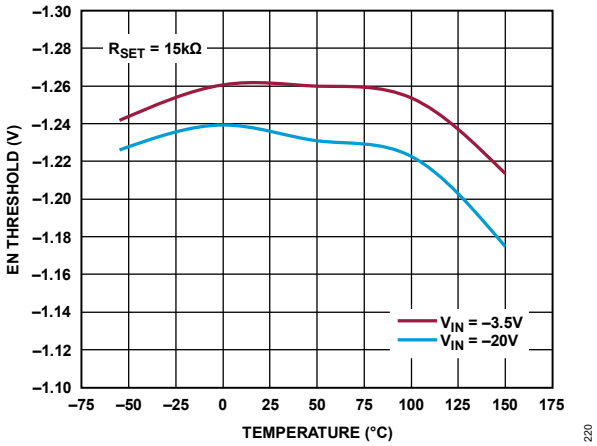


Figure 23. Negative EN/UV Turn-On Threshold vs. Temperature

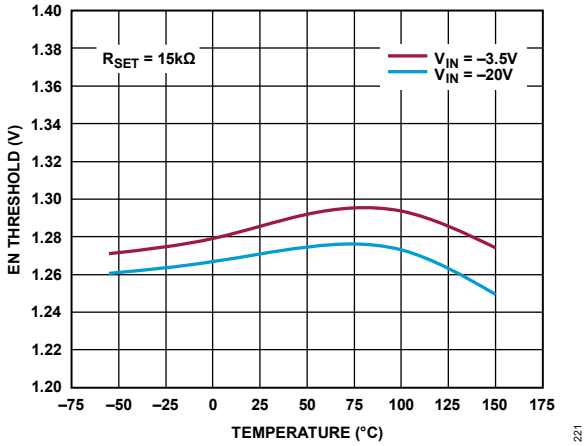


Figure 24. Positive EN/UV Turn-on Threshold vs. Temperature

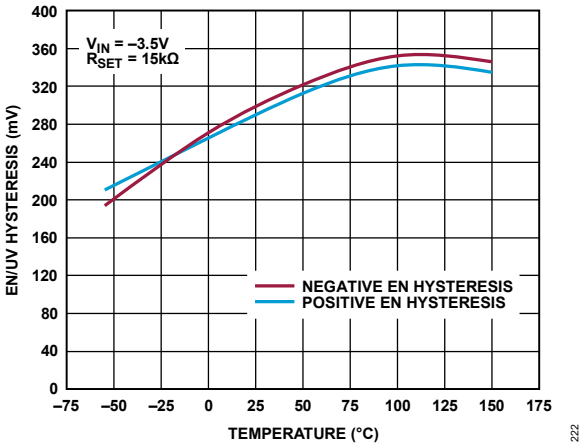


Figure 25. EN/UV Hysteresis vs. Temperature

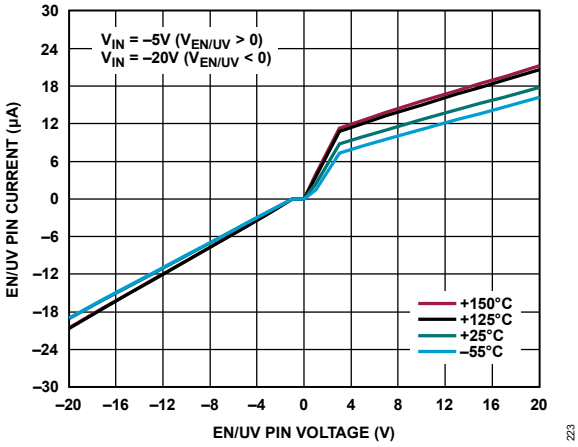


Figure 26. EN/UV Pin Current vs. EN/UV Pin Voltage

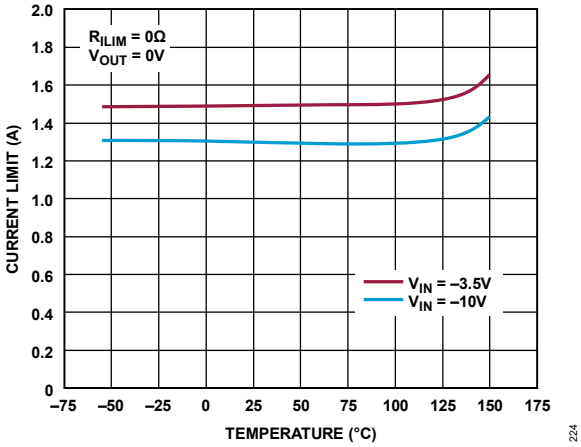


Figure 27. Internal Current Limit vs. Temperature

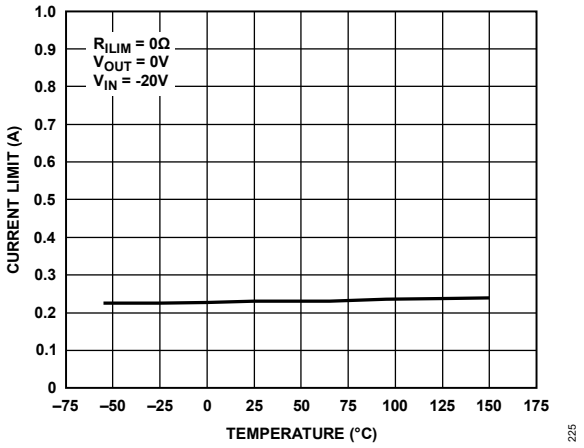


Figure 28. Internal Current Limit vs. Temperature

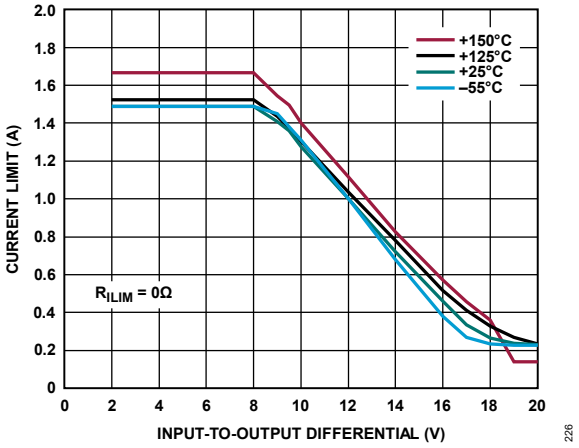


Figure 29.Internal Current Limit vs. Input-to-Output Differential

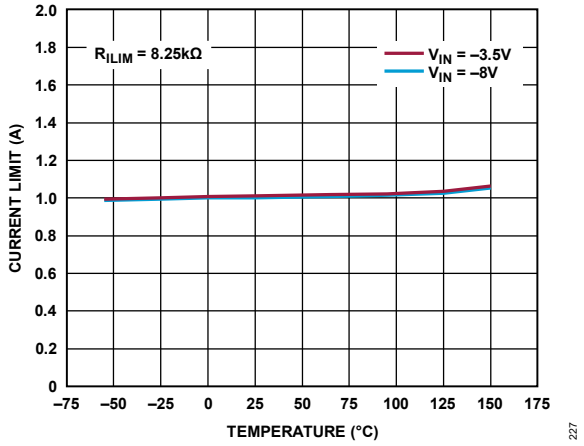


Figure 30. Programmable Current Limit vs. Temperature (1A)

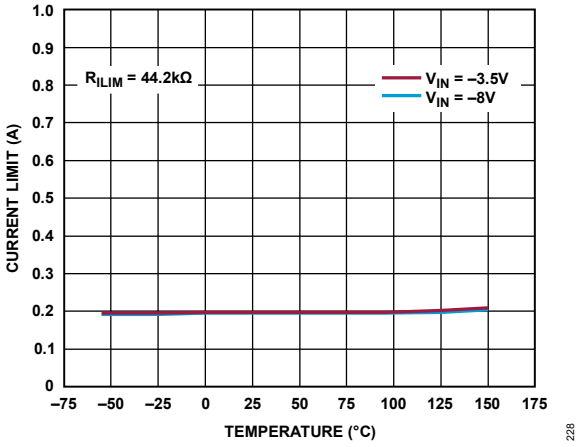


Figure 31. Programmable Current Limit vs. Temperature (200mA)

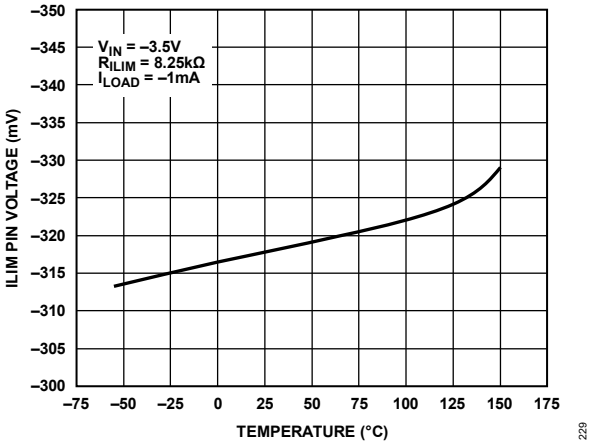


Figure 32. ILIM Pin Voltage vs. Temperature

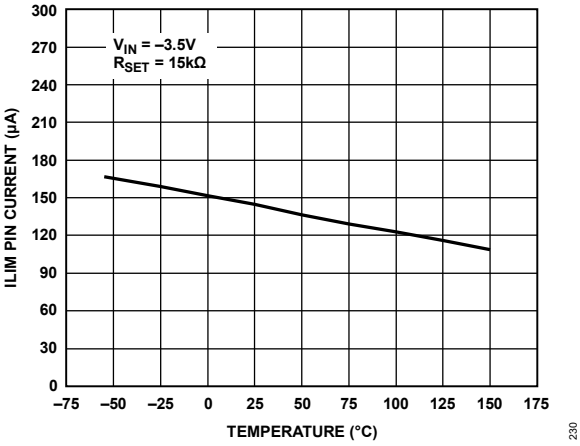


Figure 33. ILIM Pin Current vs. Temperature

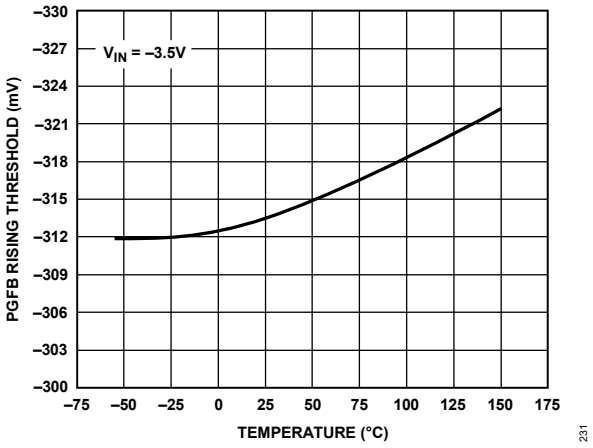


Figure 34. PGFB Rising Threshold vs. Temperature

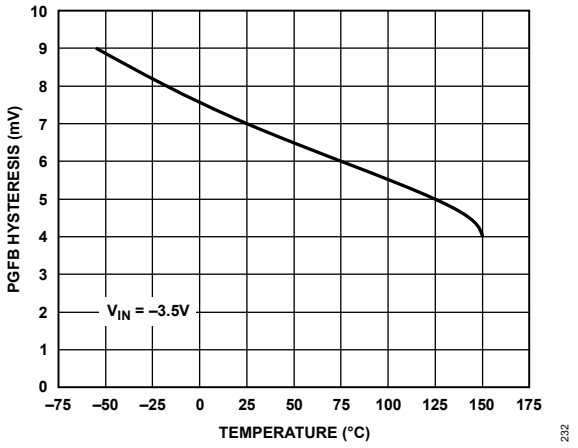


Figure 35. PGFB Hysteresis vs. Temperature

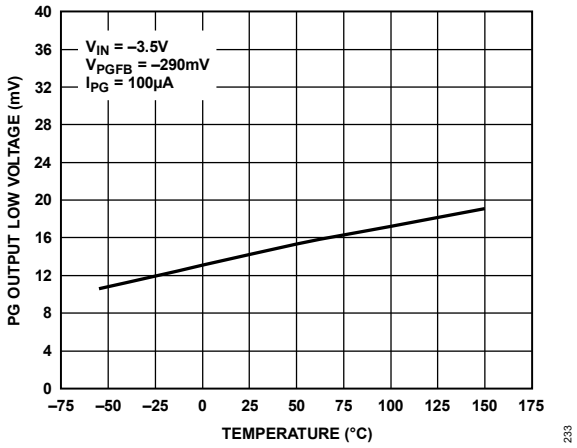


Figure 36. PG Output Low Voltage vs. Temperature

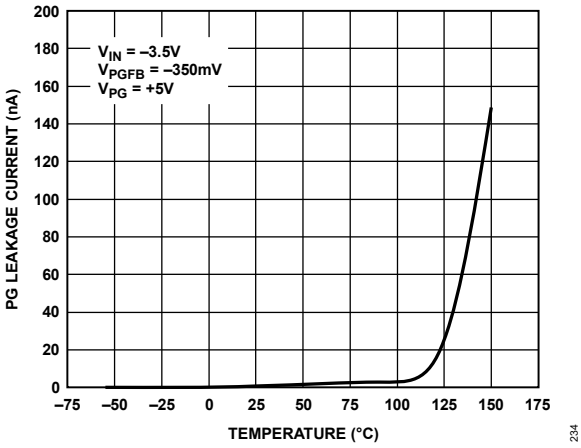


Figure 37. PG Pin Leakage Current vs. Temperature

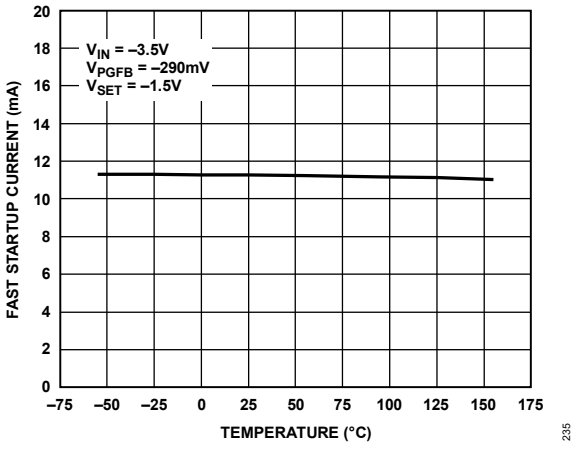


Figure 38. I_{SET} during Fast Startup with Fast Startup Enabled vs. Temperature

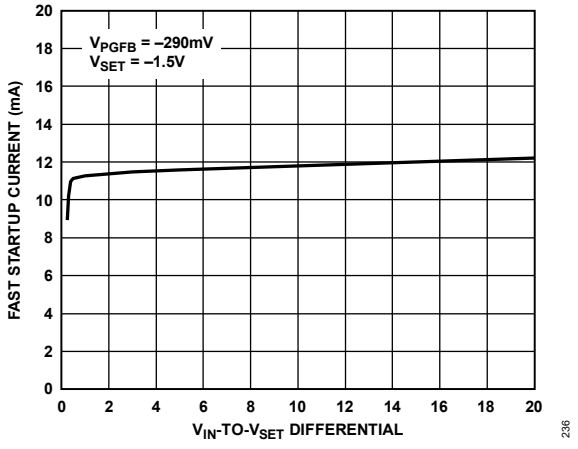


Figure 39. I_{SET} during Fast Startup with Fast Startup Enabled vs. V_{IN}–to–V_{SET} Differential

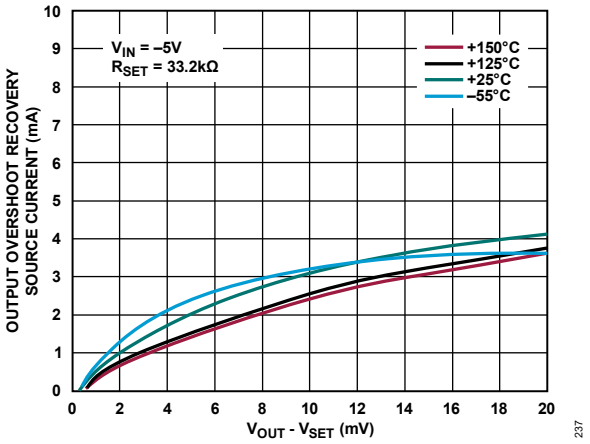


Figure 40. Output Overshoot Recovery Source Current vs. V_{OUT}–V_{SET}

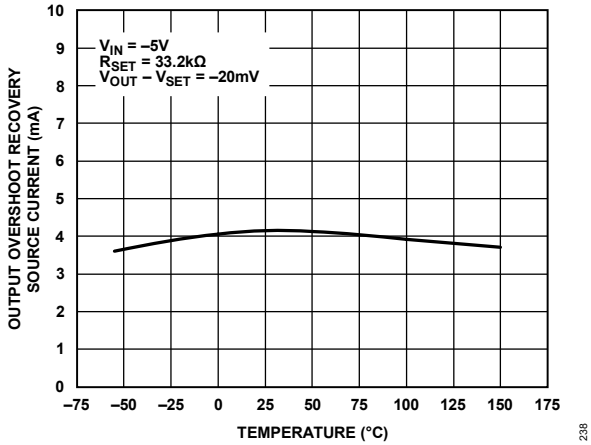


Figure 41. Output Overshoot Recovery Source current vs. Temperature

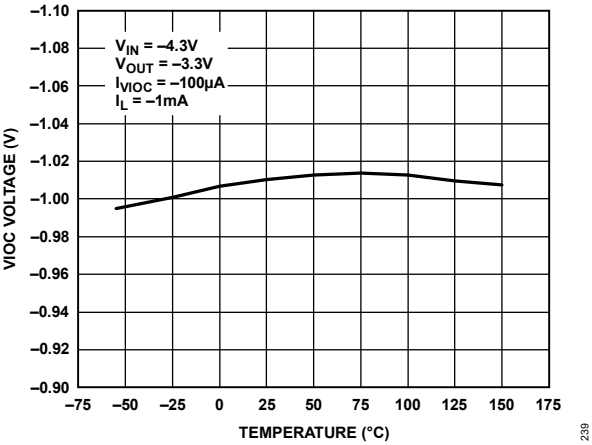


Figure 42. VIOC Voltage vs. Temperature

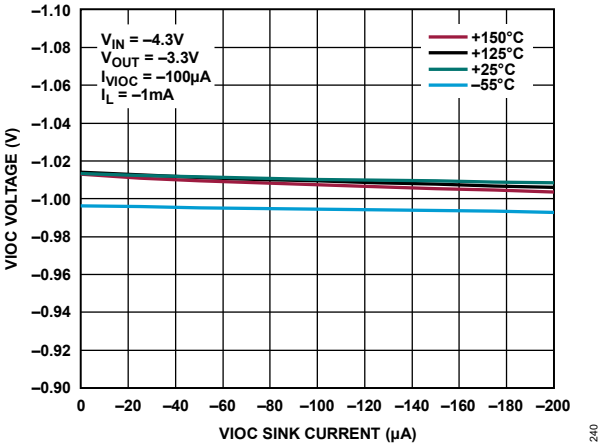


Figure 43. VIOC Voltage vs. VIOC Current

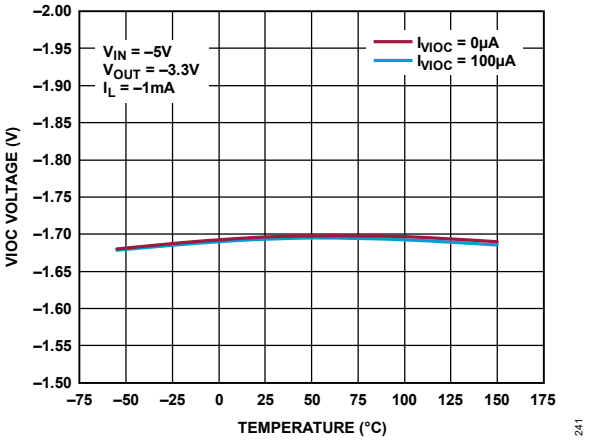


Figure 44. Maximum VIOC Voltage vs. Temperature

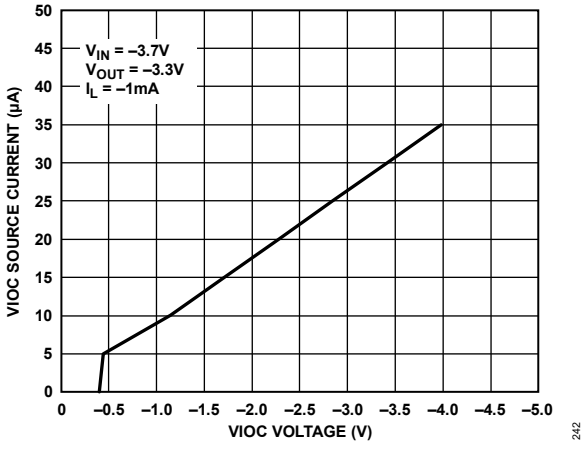


Figure 45. VIOC Source Current vs. VIOC Voltage

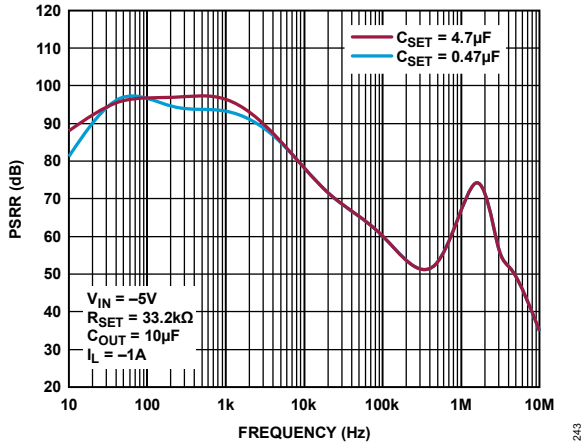


Figure 46. PSRR vs. Frequency (C_{SET} Steps)

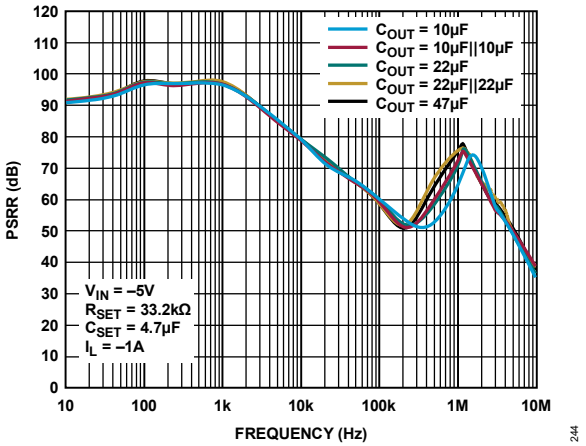


Figure 47. PSRR vs. Frequency (C_{OUT} Steps)

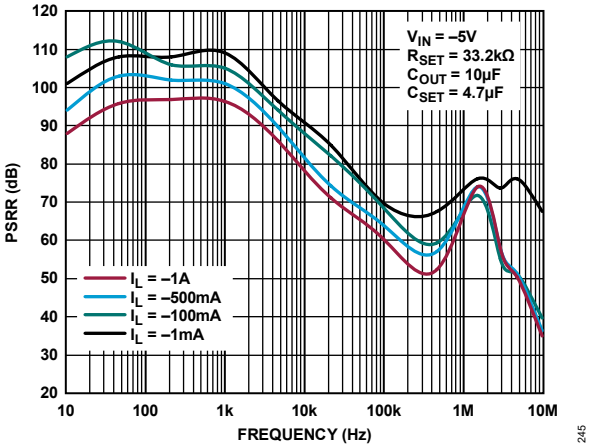


Figure 48. PSRR vs. Frequency (I_L Steps)

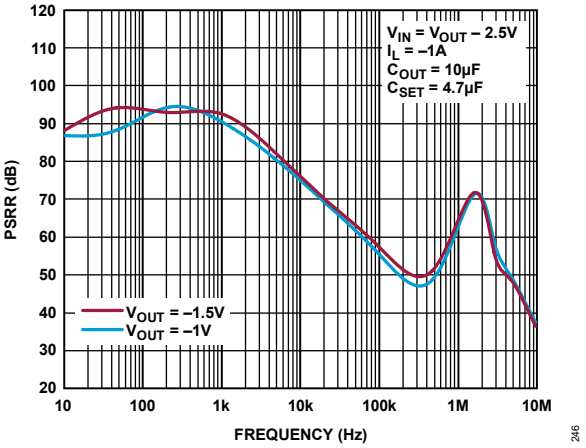


Figure 49. PSRR as a Function of EA Input Pair vs. Frequency

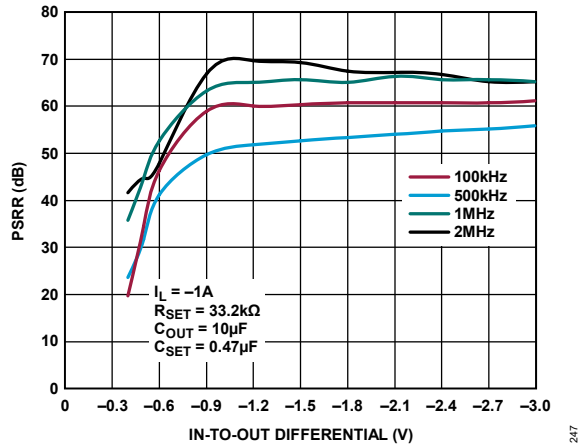


Figure 50. PSRR vs. IN–OUT Differential

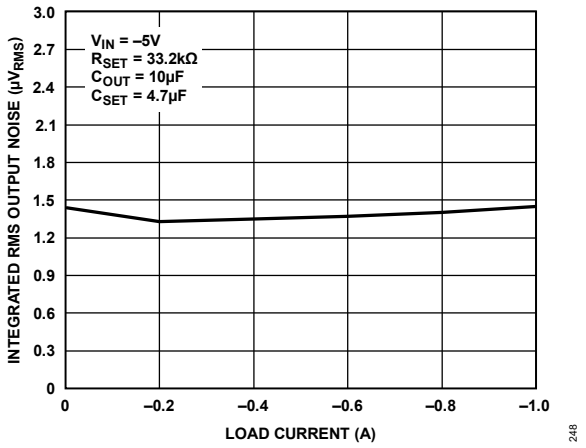


Figure 51. Integrated RMS Output Noise (10Hz–100kHz) vs. Load Current

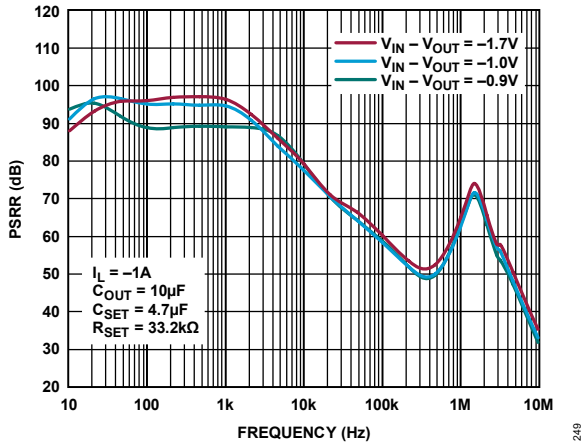


Figure 52. PSRR vs. Frequency (V_{IN}–V_{OUT} steps)

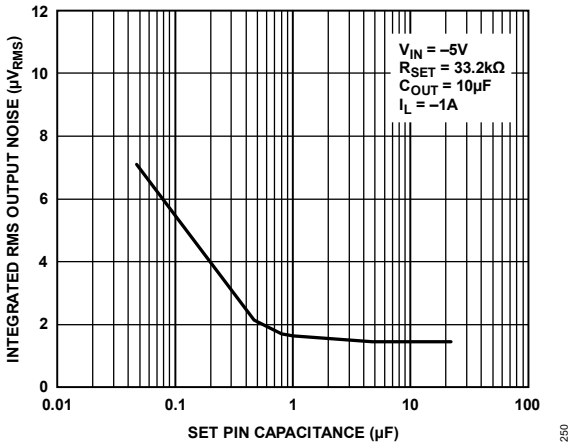


Figure 53. Integrated RMS Output Noise (10Hz–100kHz) vs. SET Pin Capacitance

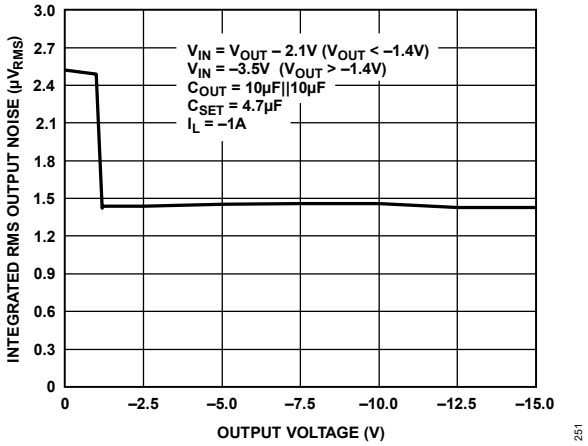


Figure 54. Integrated RMS Output Noise (10Hz–100kHz) vs. Output Voltage

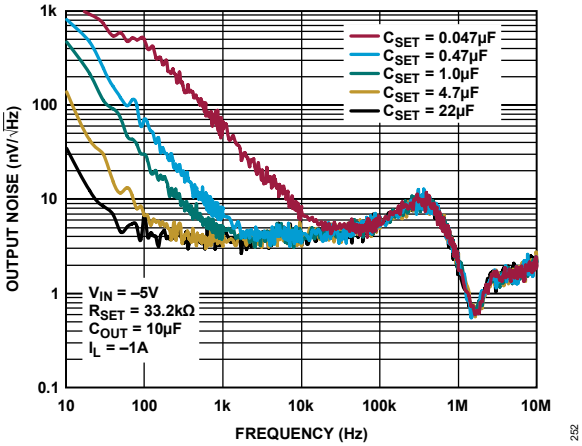


Figure 55. Output Noise vs. Frequency (C_{SET} Steps)

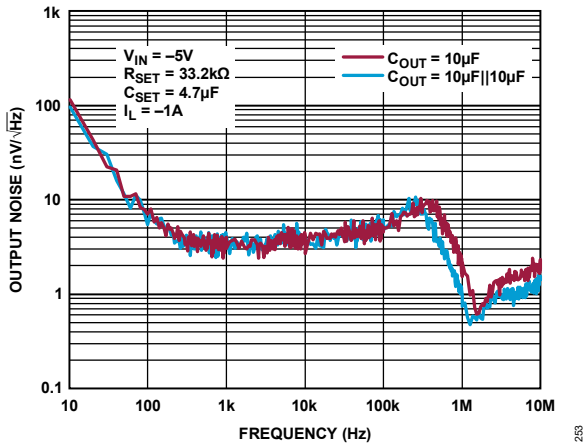


Figure 56. Output Noise vs. Frequency (C_{OUT} Steps)

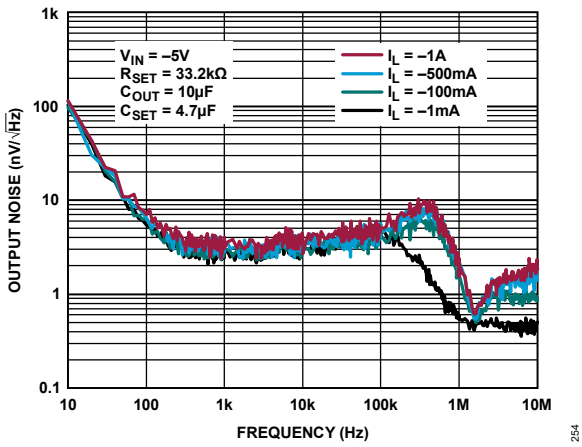


Figure 57. Output Noise vs. Frequency (I_L Steps)

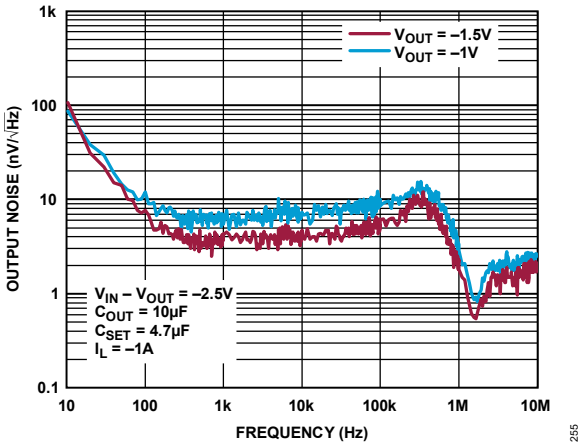


Figure 58. Output Noise as a Function of Error Amplifier Input Pair vs. Frequency

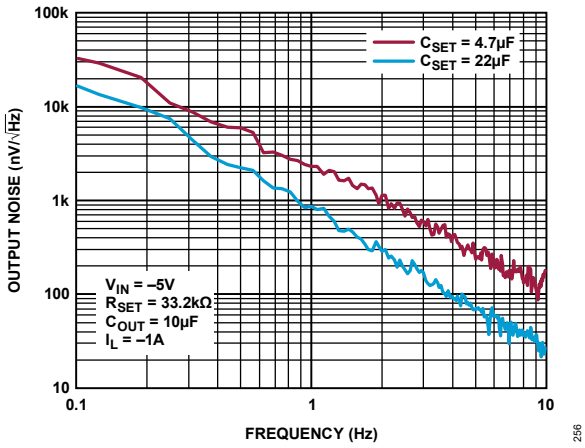


Figure 59. Output Noise (0.1Hz–10Hz) vs. Frequency

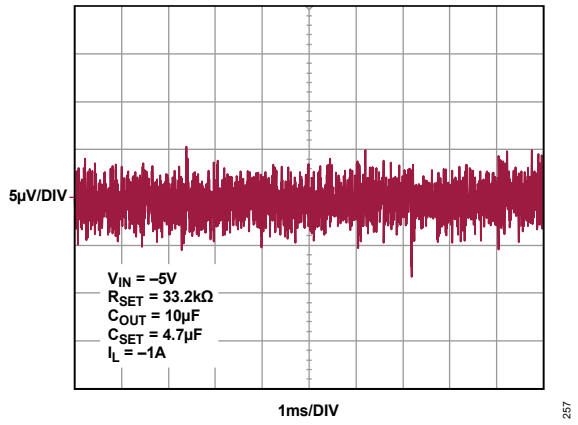


Figure 60. Output Noise (10Hz–100kHz)

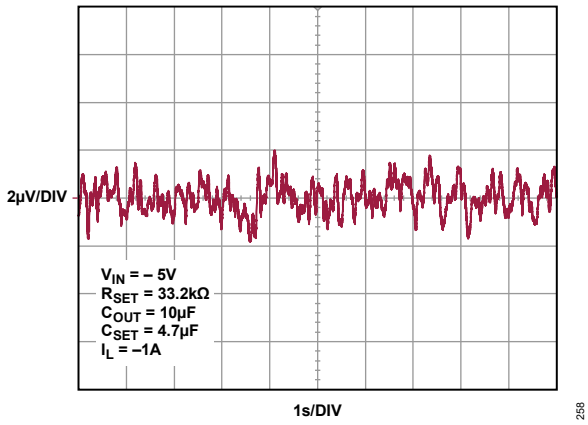


Figure 61. Output Noise (0.1Hz–10Hz), C_{SET} = 4.7µF

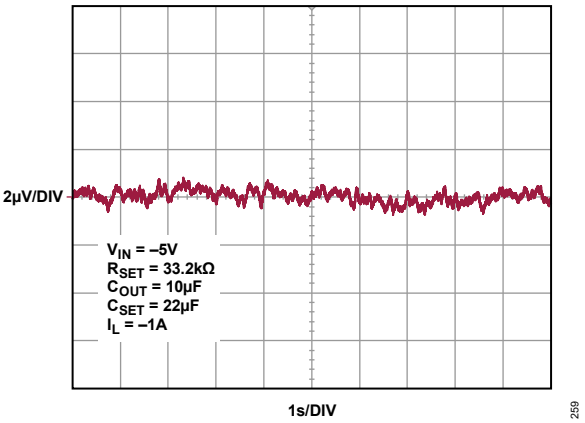


Figure 62. Output Noise (0.1Hz–10Hz), C_{SET} = 22µF

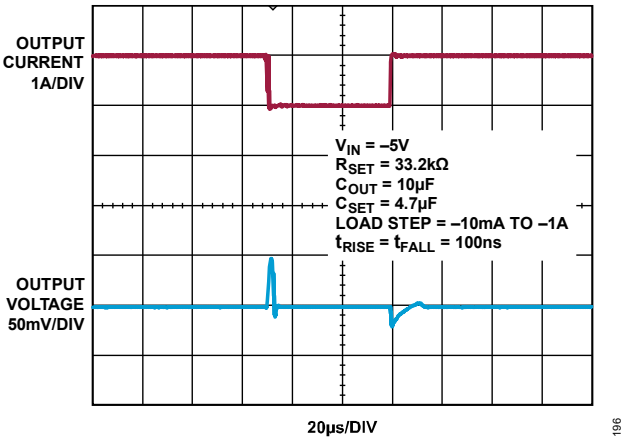


Figure 63. Load Transient Response

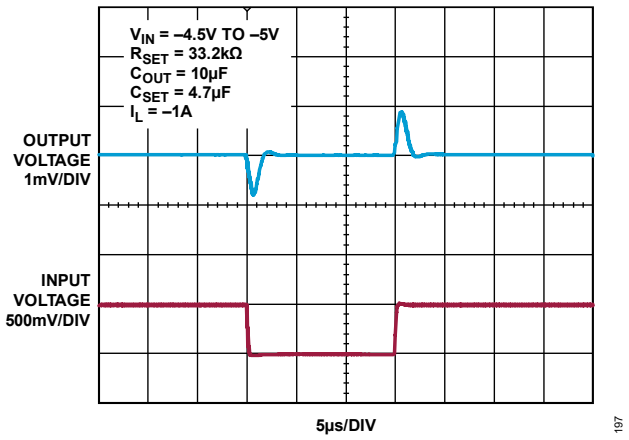


Figure 64. Line Transient Response

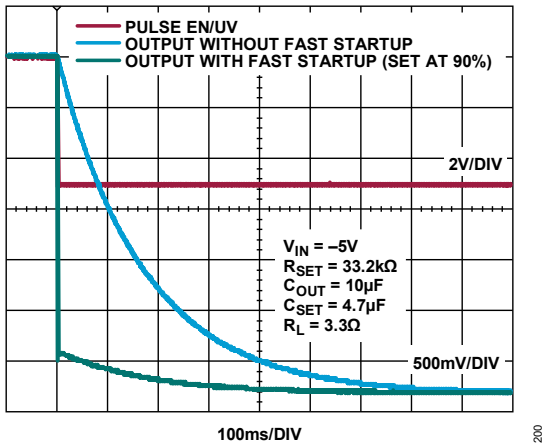


Figure 65. Startup Time with and without Fast Startup for large C_{SET}

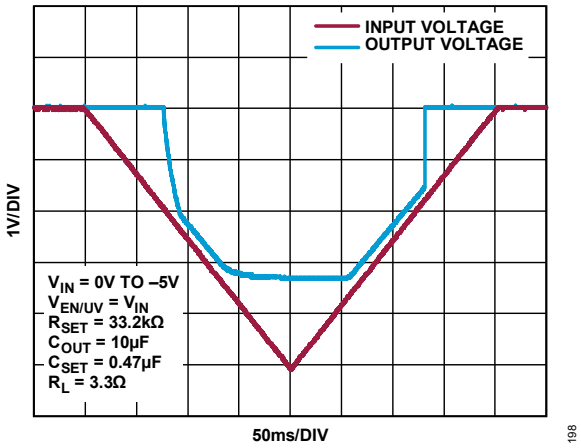


Figure 66. Input Supply Ramp-Up and Ramp-Down

BLOCK DIAGRAM

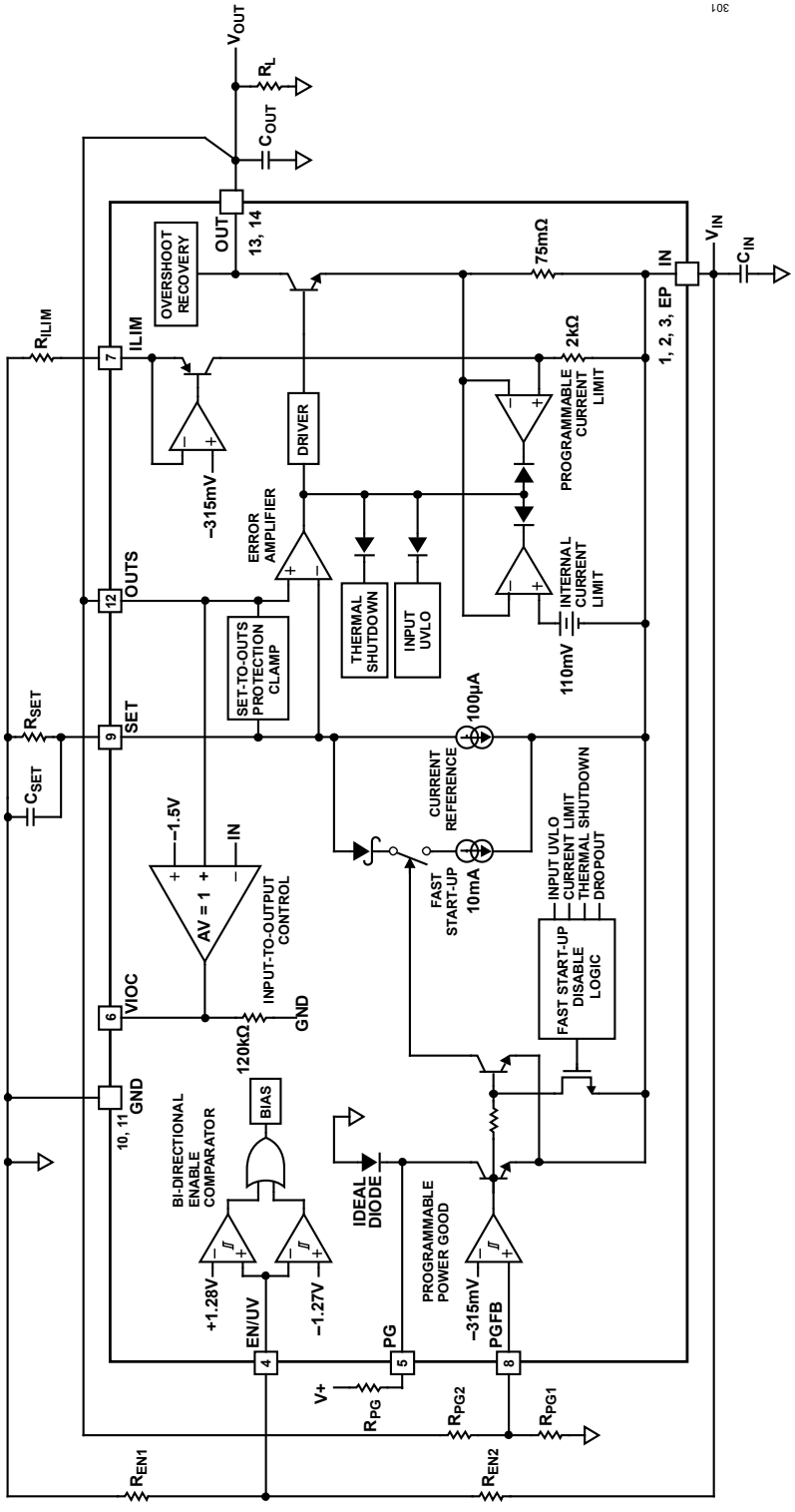


Figure 67. Block Diagram

APPLICATIONS INFORMATION

The LT3099 is a high-performance, low-dropout negative linear regulator featuring Analog Devices' ultralow noise (4nV/√Hz at 10kHz) and ultrahigh PSRR (75dB at 1MHz) architecture for powering noise-sensitive applications. Designed as a precision current reference followed by a high-performance rail-to-rail voltage buffer, the LT3099 can be easily paralleled to reduce noise, increase output current, and spread heat on the PCB. The device additionally features a programmable current limit, fast start-up capability, and programmable power good.

The LT3099 is easy-to-use and incorporates all the protection features expected in high-performance regulators. Short-circuit protection, safe operating area protection, and thermal shutdown with hysteresis are included.

Output Voltage

The LT3099 incorporates a precision 100µA current reference flowing into the SET pin, which also ties to the error amplifier's inverting input. *Figure 68* illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier's unity-gain configuration produces a low-impedance version of this voltage on its non-inverting input, i.e., the OUTS pin, which is externally tied to the OUT pin.

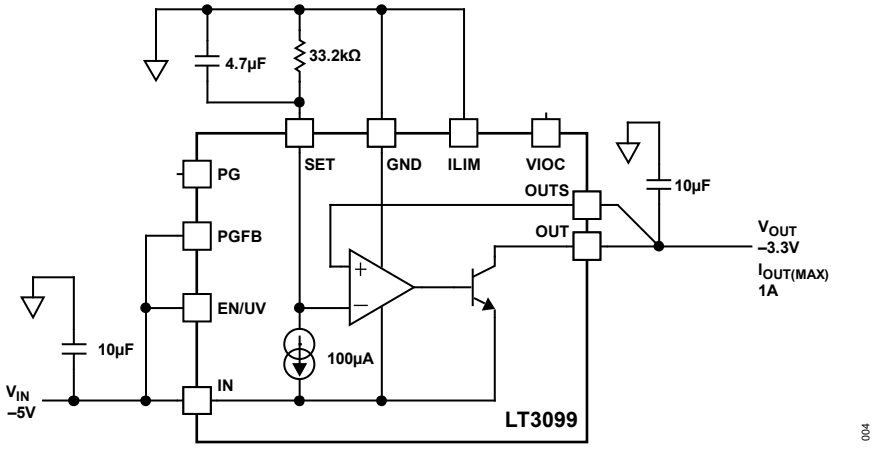


Figure 68. Basic Adjustable Regulator

The LT3099's rail-to-rail error amplifier and current reference architecture allow for a wide output voltage range from 0V (using a 0Ω resistor) to V_{IN} minus dropout. A negative-positive-negative (NPN) based input pair is active for 0V to -1.2V output, and a positive-negative-positive (PNP) based input pair is active for output voltages beyond -1.2V. While the PNP-based input pair is designed to offer the best overall performance, see *Table 1* (Electrical Characteristics table) for more details on offset voltage, SET pin current, output noise, and PSRR variation with the error amplifier input pair. *Table 4* lists many standard output voltages and their corresponding 1% R_{SET} resistors.

Table 4. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
-2.5	24.9
-3.3	33.2
-5	49.9
-12	121
-15	150

The benefit of using a current reference compared to a voltage reference as used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This allows the LT3099 to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR and transient performance do not change with output voltage. Moreover, since no error amplifier gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Since the zero TC current reference is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high-quality insulation (e.g., Teflon, Kel-F). Moreover, cleaning all insulating surfaces to remove fluxes and other residues may be required.

High-humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring operated at a similar potential—ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. A leakage of 100nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. *Figure 69* illustrates a typical guard ring layout technique.

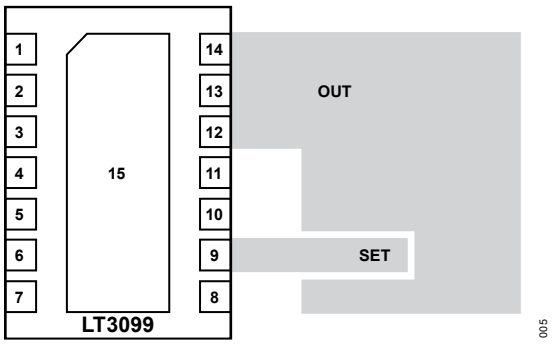


Figure 69. Guard Ring Layout

Since the SET pin is a high-impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue—10nF is sufficient.

For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltage source capable of sourcing 100µA. Connecting a precision voltage reference to the SET pin eliminates any errors in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The LT3099's OUTS pin provides a Kelvin sense connection to the output. The SET pin resistor's GND side provides a Kelvin sense connection to the load's GND side.

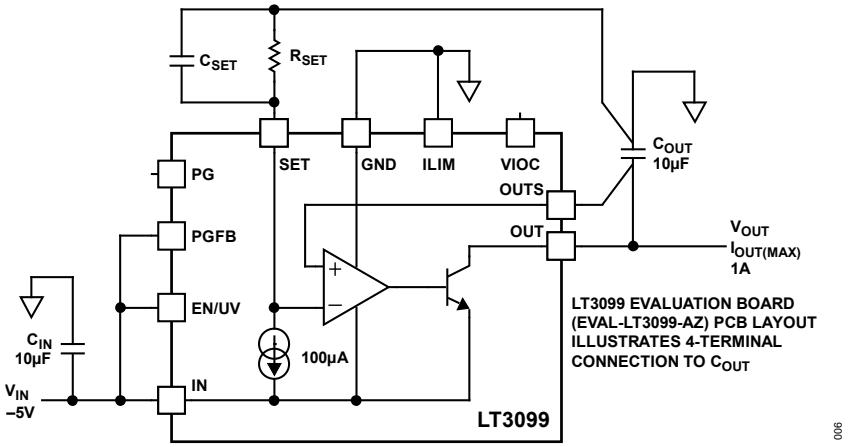


Figure 70. C_{OUT} and C_{SET} Connections for Best Performance

Additionally, for ultrahigh PSRR, the LT3099 bandwidth is made quite high (~1MHz), making it very close to a typical 10µF (1206 case size) ceramic output capacitor's self-resonance frequency (~1.6MHz). It is essential to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, as shown in *Figure 70*, minimize the effects of PCB trace and solder inductance by tying the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}. Either place the GND sides of C_{IN} and C_{OUT} reasonably close, or follow the guidance in the *PSRR and Input Capacitance* section for the highest PSRR performance. Refer to the *EVAL-LT3099* for more information on the recommended layout that meets these requirements. While the LT3099 is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase/gain margin, noise, and PSRR performance may degrade.

Stability and Output Capacitance

The LT3099 requires an output capacitor for stability. Given its high bandwidth, low Equivalent series resistance (ESR), and Equivalent series inductance (ESL), ceramic capacitors are recommended. A minimum of 10µF output capacitance with an ESR below 20mΩ and an ESL below 2nH is required for stability for output voltages lesser than -10V. For output voltages between -10V to -15V, a minimum of 20µF output capacitance is needed. For output voltages more negative than -15V, a minimum of 30µF output capacitance is needed.

Given the high PSRR and low noise performance attained by using a single 10µF ceramic output capacitor, larger values of output capacitor only marginally improve the performance because the regulator bandwidth decreases with increasing output capacitance—hence, there is little to be gained by using larger than the minimum 10µF output capacitor for output voltages less than -10V. Nonetheless, larger values of output capacitance do decrease peak output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3099 increase the effective output capacitance.

Give extra consideration to the type of ceramic capacitors used. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with the Electronic Industries Alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in small packages, but they tend to have stronger voltage and temperature coefficients, as shown in *Figure 71* and *Figure 72*. When used with a 5V regulator, a 16V 10µF

Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

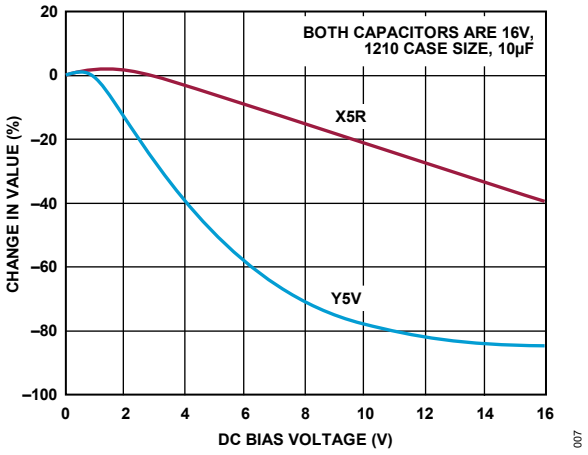


Figure 71. Ceramic Capacitor DC Bias Characteristics

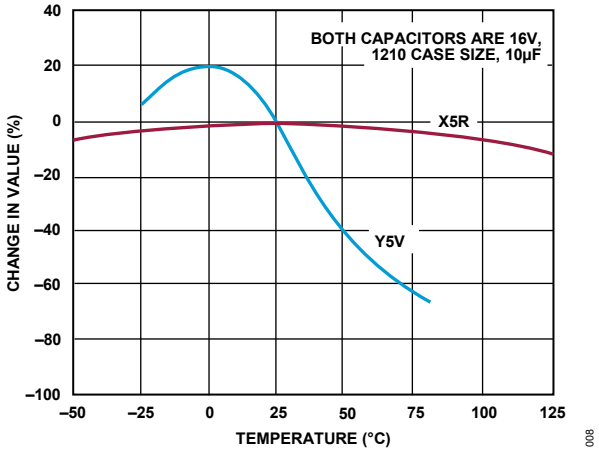


Figure 72. Ceramic Capacitor Temperature Characteristics

The X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for use with the LT3099. The X7R dielectric has better stability across temperatures, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify the operating temperature range and the maximum capacitance change over temperature. While capacitance change due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in *Figure 73* capacitor DC bias characteristics tend to improve as component case size increases, **but verification of expected capacitance at the operating voltage is highly recommended.** Due to its good voltage coefficient in small case sizes, it is recommended to use Murata's GCM series ceramic capacitor.

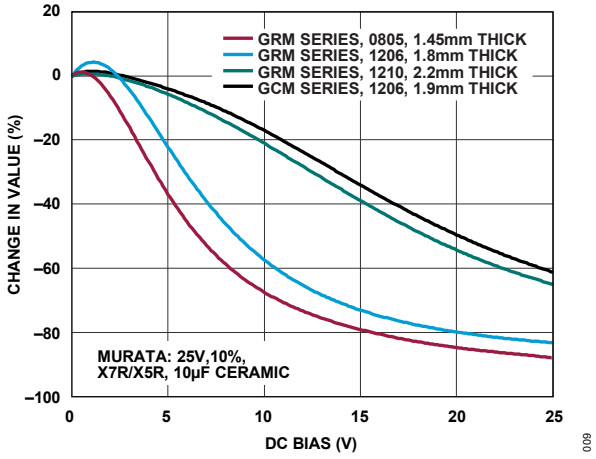


Figure 73. Capacitor Voltage Coefficient for Different Case Sizes

High-Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. This stress can be induced by mechanical vibrations within the system or thermal transients for a ceramic capacitor.

LT3099 applications in high-vibration environments have three distinct piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, due to the LT3099's very low output impedance over a wide frequency range, negligible output noise is generated using a ceramic output capacitor. Similarly, due to the LT3099's ultrahigh PSRR, negligible output noise is generated using a ceramic input capacitor. Given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise; peak-to-peak excursions of hundreds of µVs are possible. However, due to the SET pin capacitor's high ESR and ESL tolerance, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin; do note that electrolytic capacitors tend to have high 1/f noise. In any case, the use of surface-mount capacitors is highly recommended.

Stability and Input Capacitance

The LT3099 is stable with a minimum 10µF IN pin capacitor. Low ESR ceramic capacitors are recommended. Applications using long wires to connect the power supply to the LT3099's input and ground terminals, together with low ESR ceramic input capacitors, are prone to voltage spikes, reliability concerns, and application-specific board oscillations. The wire inductance and the low ESR ceramic input capacitor, form a high-Q LC resonant tank circuit. In some instances, the use of low-value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and input capacitor is the cause and not because of LT3099's instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-American wire gauge (AWG) isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing toward the LT3099 between two parallel conductors. In this case, placing the wire further apart reduces the inductance, up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self-inductance of the wires—therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted in close proximity powers the LT3099, a 10µF input capacitor suffices for stability. If a distantly located supply powers the LT3099, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 6" of wire length. The minimum input capacitance needed to stabilize the application also varies with the output capacitance and the load current. Placing additional capacitance on the LT3099's output helps. However, this requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the LT3099 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of the dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the LT3099 input in parallel with a 10µF ceramic capacitor.

PSRR and Input Capacitance

For applications utilizing the LT3099 for post-regulating switching converters, placing a capacitor directly at the LT3099 input results in AC (at the switching frequency) flowing near the LT3099. This relatively high-frequency switching current generates magnetic fields that couple to the LT3099 output, degrading the effective PSRR. While highly dependent on the PCB layout, the switching pre-regulator, input capacitor size, and other factors, the PSRR degradation can easily be over 30dB at 1MHz. This degradation is present even with the LT3099 desoldered from the board. It is a degradation in the PSRR of the PCB. While negligible for conventional low PSRR LDOs, the LT3099's ultrahigh PSRR requires careful attention to higher-order parasitics to realize the full performance the regulator offers.

To mitigate the flow of high-frequency switching current near the LT3099, the input capacitor can be removed as long as the switching converter's output capacitor is located more than an inch away from the LT3099. Magnetic coupling decreases rapidly with increasing distance. If the switching regulator is placed too far away (conservatively more than a couple of inches) from the LT3099, the lack of an input capacitor presents a high impedance at the input of the LT3099, and oscillation may occur. It is generally a common (and preferred) practice to bypass regulator inputs with some capacitance, so this option is fairly limited in its scope and not the most palatable solution.

To that end, it is recommended to refer to the *Printed Circuit Board (PCB) Layout* section in the *EVAL-LT3099* user guide for achieving the best possible PSRR performance. The LT3099 demo board layout utilizes magnetic field cancellation techniques to prevent PSRR degradation caused by the high-frequency current flow while keeping the input capacitor.

Filtering High Frequency Spikes

For applications where the LT3099 is used to post-regulate a switching converter, its high PSRR effectively suppresses any harmonic content present at the switching frequency (typically 100kHz to 4MHz). However, very high frequency (hundreds of MHz) "spikes" are associated with the switcher's power switch transition times that are beyond the LT3099's bandwidth and will almost directly pass through to the output. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (example: 0.5") PCB trace coupled with a capacitor with a low impedance at the transition frequency can serve as an LC filter to suppress these very high-frequency spikes.

Output Noise

The LT3099 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting the output voltage, and the noise gain created by this resistor divider. Many low-noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3099 does not use a voltage reference; instead, it uses a 100µA current reference. The current reference operates with a typical noise current level of 30pA/√Hz (10nARMS over the 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor values, which is then RMS summed with the error amplifier's noise and the resistor's Johnson noise of $\sqrt{4kTR}$ (k = Boltzmann's constant, 1.38 x 10^{-23} J/K, and T is absolute temperature) to give the net output noise.

One problem faced by conventional linear regulators is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the LT3099's unity-gain follower architecture presents no gain from the SET pin to the output. Therefore, using a capacitor to bypass the SET pin resistor allows output voltage noise to be independent of the programmed output voltage. The resultant output noise is then determined only by the error amplifier's noise, typically 4nV/√Hz from 1kHz to 1MHz and 1.4μV_{RMS} in the 10Hz to 100kHz bandwidth when using a 4.7µF SET pin capacitor. Paralleling multiple LT3099s further reduces noise by $\sqrt{N}$ for N parallel regulators.

See the *Typical Performance Characteristics* section for noise spectral density and RMS integrated noise performance over various load currents and SET pin capacitances.

SET Pin (Bypass) Capacitance: Noise, PSRR, Transient Response and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor improves PSRR and transient performance. Note that any bypass capacitor leakage deteriorates the LT3099's DC regulation. Capacitor leakage of as little as 100nA causes a 0.1% DC error. It is recommended to use a good quality, low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. The RC time constant formed by the SET pin resistor and capacitor determines the soft-start time. Without the use of fast start-up, the ramp-up rate from 0 to 90% of nominal V_{OUT} is:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \text{ (Fast Start} - \text{Up Disabled)}$$

Fast Start-Up

For ultralow-noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required; up to 22µF may be used. While this would normally significantly increase the regulator's start-up time, the LT3099 incorporates fast start-up circuitry that increases the SET pin current to about 10mA during start-up.

As shown in the *Block Diagram*, the 10mA current source remains engaged while PGFB is less than -315mV unless the regulator is in current limit, dropout, thermal shutdown, or input voltage is below the minimum V_{IN}.

If fast start-up capability is not used, tie PGFB to IN or to OUT (for output voltages more negative than -315mV). Note that doing so also disables power good functionality.

ENABLE/UVLO

The EN/UV pin puts the regulator into a micropower shutdown state. The LT3099 has an accurate -1.27V turn-on threshold on the EN/UV pin with 330mV of hysteresis. This threshold can be used in conjunction with a resistor divider from the input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The EN/UV pin current (I_{EN}) at the threshold must be considered when calculating the resistor divider network. See the *Electrical Characteristics* table and *Figure 26* for EN/UV pin characteristics. Use the following formula to determine resistor divider values (See *Figure 83* in *Typical Applications* section for more details).

$$V_{IN(UVLO)} = -1.27V(1 + \frac{R_{EN2}}{R_{EN1}}) - I_{EN}R_{EN2}$$

Since the EN/UV pin is bidirectional, it can also be pulled above 1.28V to turn on the LT3099. In bipolar supply applications, the positive EN/UV threshold can be used to sequence the turn-on of the LT3099 after the positive regulator has been turned on. If unused, tie the EN/UV pin to IN.

High-Efficiency Linear Regulator—Input-to-Output Voltage Control

The VIOC (voltage input-to-output control) pin is a function that controls a switching regulator and facilitates a design solution that maximizes system efficiency while providing good transient response, low noise, and high ripple rejection. This regulation loop also minimizes total power dissipation in fault conditions. If the output is overloaded and the LT3099 current limits, the VIOC amplifier will lower the switching regulator output voltage and limit the power dissipation in the LT3099.

The VIOC pin is the output of a fast unity-gain amplifier that regulates V_{IN} to a voltage that is a fixed voltage higher than the higher of V_{OUT} or -1.5V. Connect the VIOC pin to the feedback (FB) pin of the upstream switching converter ($V_{FBSWITCHER}$), which regulates the input-to-output differential of the LT3099 to the feedback voltage of the switching converter. When paralleling multiple LT3099 devices, connect the VIOC pin of one of the LT3099 devices to the feedback pin of the upstream switching converter and float the remaining VIOC pins. Targeting a differential voltage of -1V from input to output provides an optimum tradeoff between power dissipation and power supply rejection (see *Figure 50* for more details). The VIOC pin has a typical impedance to ground of 120kΩ when the LT3099 is disabled.

While the VIOC buffer is inside the feedback loop of the switching converter, given the high bandwidth of the VIOC buffer, the frequency compensation of the switching converter does not need adjustment. Phase delay through the VIOC buffer is typically less than 2° for frequencies as high as 100 kHz. Therefore, within the bandwidth (usually much less than 100 kHz) of the switching converter, the VIOC buffer is transparent and acts like an ideal wire. For example, for a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer, the phase margin degrades by at most 2°. Hence, the phase margin for the switching converter (using the VIOC pin) is at least 48°. Given that the VIOC buffer is inside the feedback loop of the switching converter, the total capacitance on the VIOC pin must be less than 20 pF. *Figure 74* shows a typical application utilizing the VIOC pin to control the output voltage of the upstream switching regulator.

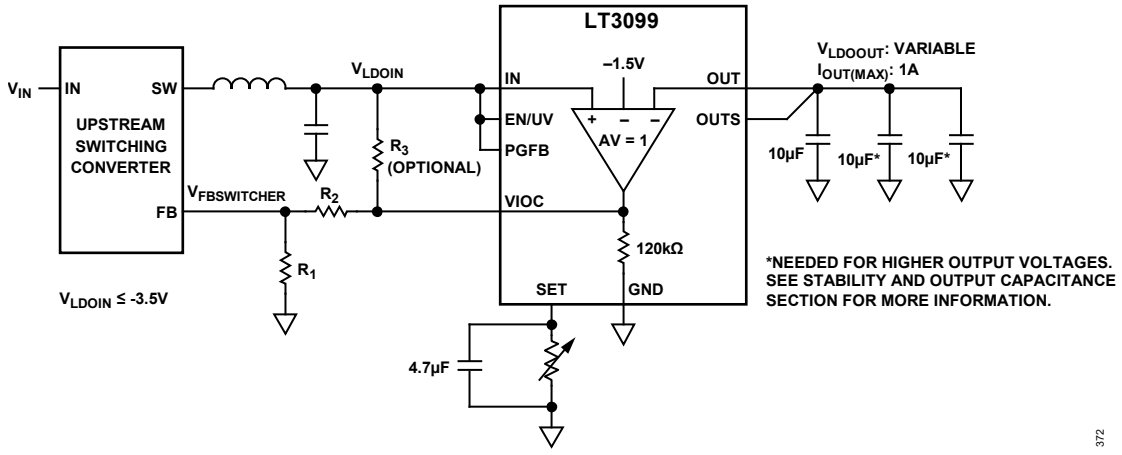


Figure 74. VIOC Operation and Programming Input-to-Output Differential

The input-to-output differential voltage is easily programmable to support different application needs by using the following equation:

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC(NOMINAL)} = V_{FBSWITCHER}\left(1 + \frac{R_2}{R_1}\right)$$

Furthermore, if the LT3099 SET pin opens up, the LT3099 input voltage can rise to the input voltage of the switching converter and, thus, potentially violate the *Absolute Maximum Ratings* of the LT3099. To prevent this violation, set the maximum LT3099 input voltage by using a resistor (R_3) between the VIOC and IN pins of the regulator such that:

$$V_{LDOIN(MAX)} = V_{FBSWITCHER}\left(1 + \frac{R_2 + R_3}{R_1}\right) + I_{SOURCE(VIOC)} \times R_3$$

$$I_{SOURCE(VIOC)} = \frac{V_{VIOC(NOMINAL)}}{120k\Omega}$$

where $I_{SOURCE(VIOC)}$ is the source current from the VIOC pin.

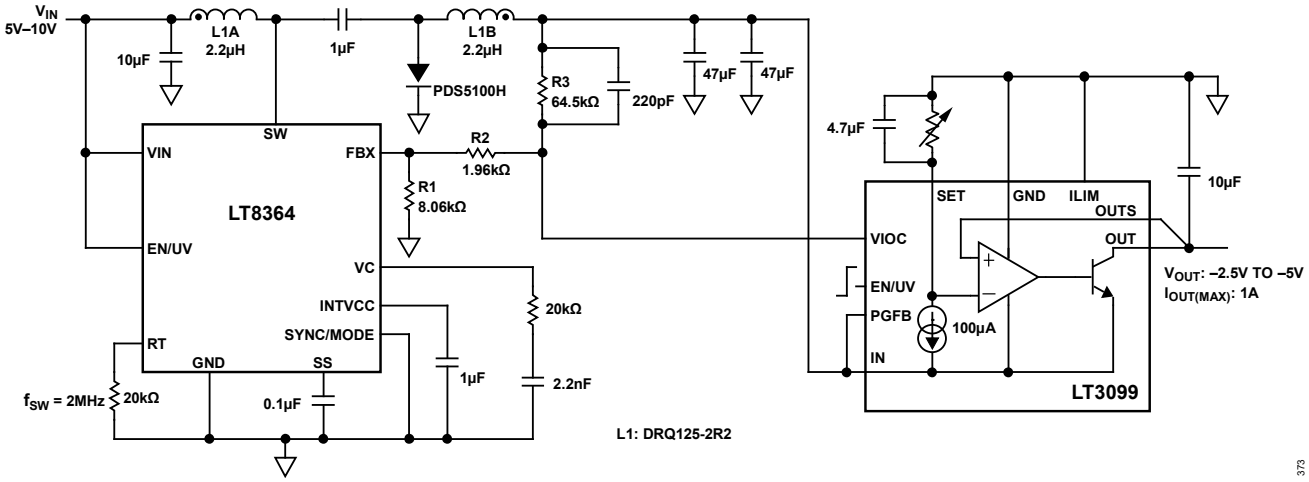


Figure 75. VIOC LT3099 Post-Regulating Application using LT8364

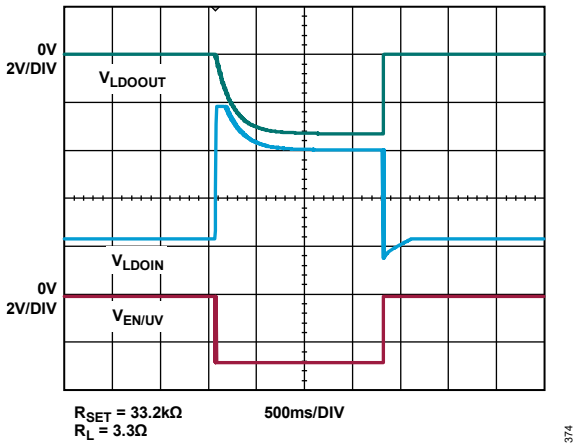


Figure 76. EN/UV Pulse (V_{LDOIN} is the Input of the LDO Regulator, and V_{LDOOUT} is the Output of the LDO Regulator)

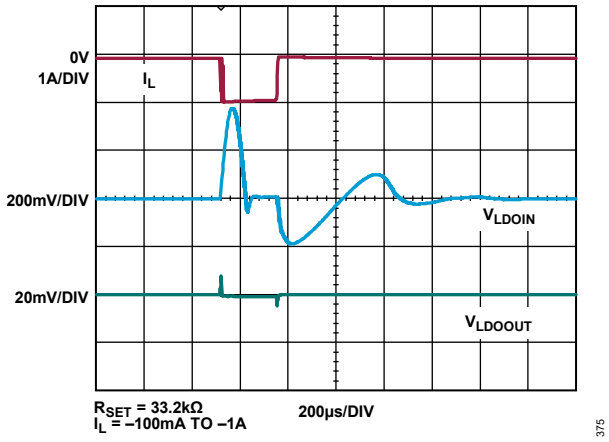


Figure 77. Load-Step Response using the VIOC Buffer

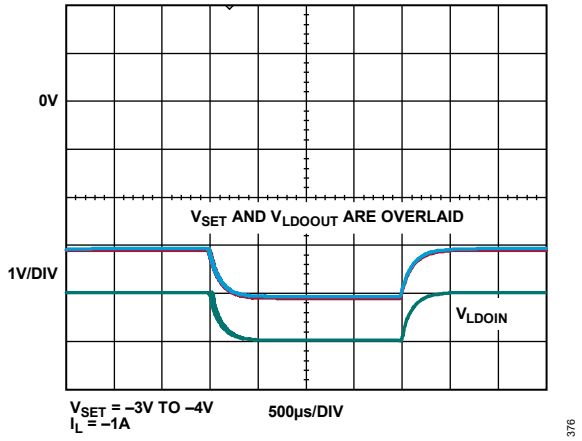


Figure 78. Stepping V_{SET} from -3V to -4V (and Back to -3V)

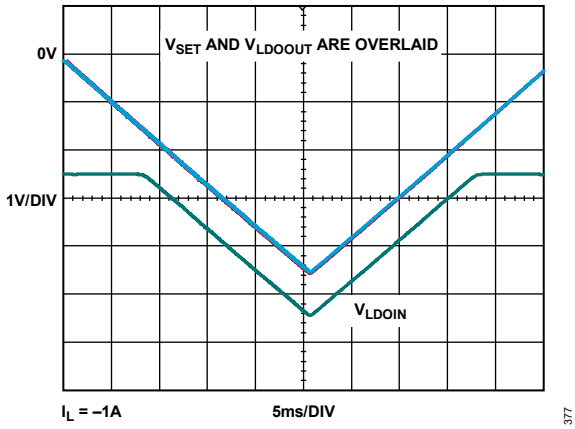


Figure 79. Ramping V_{SET} from 0V to -4.5V (and back to 0V)

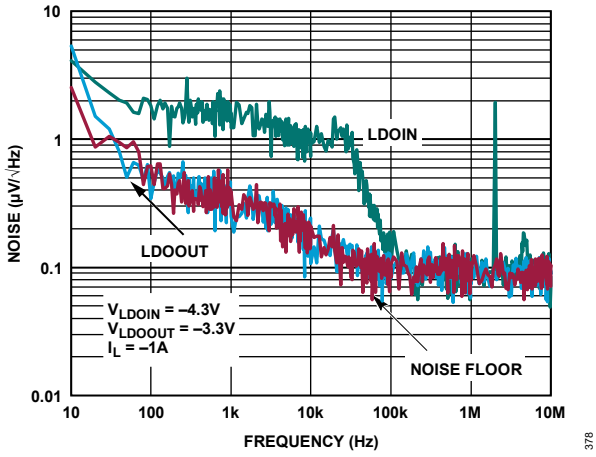


Figure 80. Input and Output Noise Spectral Density of the LT3099

Programmable Power Good

As illustrated in the *Block Diagram*, the power good threshold is user-programmable using the ratio of two external resistors, R_{PG1} and R_{PG2}:

$$V_{OUT(PG\_THRESH)} = -0.315V(1 + \frac{R_{PG2}}{R_{PG1}}) - I_{PGFB}R_{PG2}$$

If the PGFB pin becomes more negative than -315mV, the open-collector PG pin de-asserts and becomes high impedance. The power good comparator has 7mV hysteresis and 5µs of deglitching. If power good functionality is not used, float the PG pin. Note that the programmable power good and fast start-up capabilities are disabled for output voltages more positive than -315mV.

Externally Programmable Current Limit

The ILIM pin internally regulates to -315mV. Connecting a resistor from ground to ILIM sets the current flowing into the ILIM pin, which in turn programs the LT3099's current limit. With the programming scale factor, the current limit can be calculated as follows:

$$\text{Current Limit (A)} = \frac{8.2k\Omega \times A}{R_{ILIM}} + 0.015A$$

For example, an 8.25kΩ resistor programs the current limit to 1.01A, and a 44.2kΩ resistor programs the current limit to 200mA. For good accuracy, Kelvin connect this resistor to the LT3099's GND pin.

In cases where the IN-to-OUT differential is greater than 8V, the LT3099's foldback circuitry decreases the internal current limit. As a result, the internal current limit may override the externally programmed current limit to keep the LT3099 within its safe operating area (SOA). See the Internal Current Limit vs Input-to-Output Differential graph (*Figure 29*) in the *Typical Performance Characteristics* section. If not used, tie ILIM to GND.

Output Overshoot Recovery

During a load step from heavy load to very light or no load, the output voltage overshoots before the regulator responds to turn the power transistor off. It takes a long time to discharge the output capacitor with very light or no load.

The LT3099 incorporates an overshoot recovery circuit that turns on a current source to discharge the capacitor if OUTS is higher than SET. This current is typically 4mA.

If OUTS is externally held above SET, the current source turns on to restore OUTS to its programmed voltage. The current source remains on until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

A higher output current is obtained by paralleling multiple LT3099s. Tie all SET pins together and all IN pins together. Connect the OUT pins using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3099s. PCB trace resistance in mΩ/inch is shown in *Table 5*.

Table 5. PCB Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

The slight worst-case offset of 2mV for each paralleled LT3099 minimizes the required ballast resistor value. *Figure 81* illustrates that two LT3099s, each using a 10mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 10mΩ external resistors only add 10mV of output regulation drop with a 2A maximum current. A -3.3V output only adds 0.3% to the regulation accuracy. As discussed previously and shown in *Figure 70*, tie the OUTS pins directly to the output capacitors.

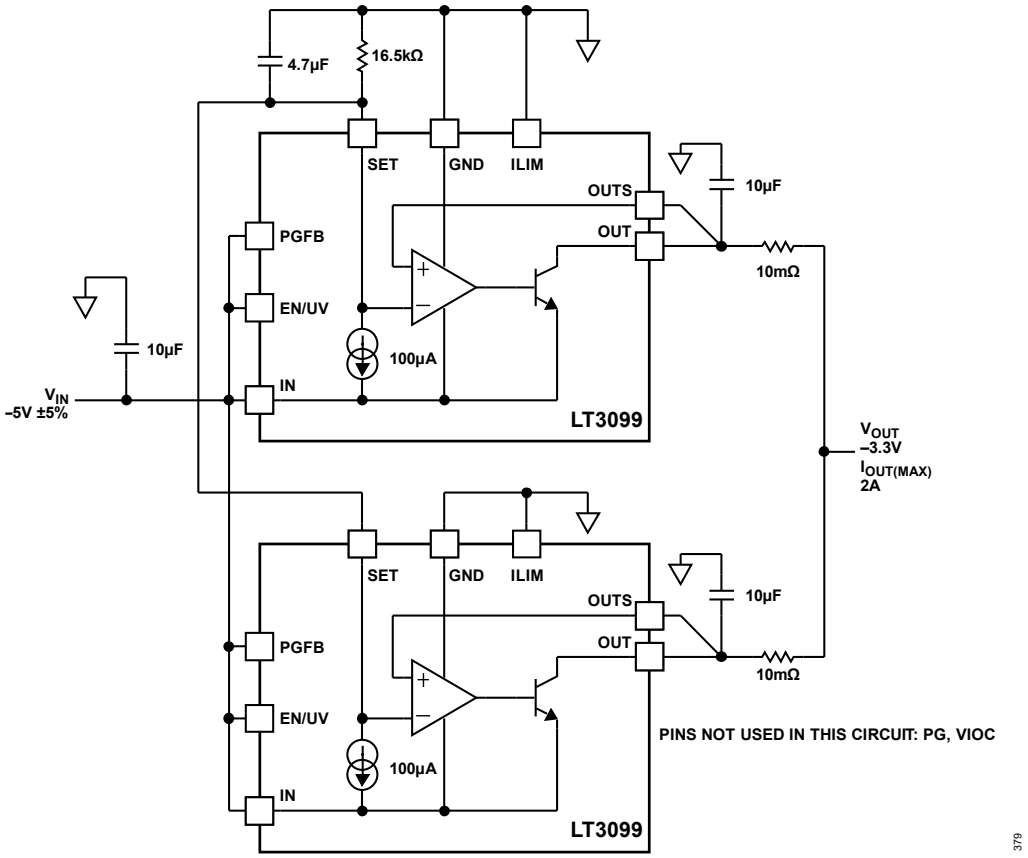


Figure 81. Parallel Devices

More than two LT3099s can be paralleled for higher output current and lower output noise. Paralleling multiple LT3099s is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or a resistor in parallel with the LT3099 can also spread heat.

PCB Layout Considerations

Given the LT3099's high bandwidth and ultrahigh PSRR, careful PCB layout must be employed to achieve full device performance. *Figure 82* shows a recommended layout that delivers the full performance of the regulator. Refer to the *EVAL-LT3099* user guide for further details.

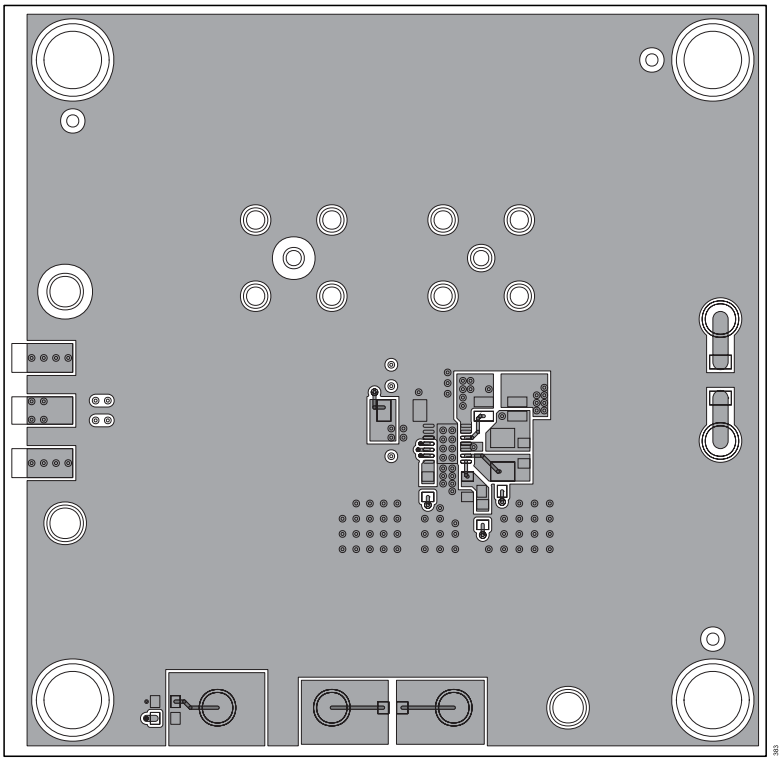


Figure 82. Recommended Layout

Thermal Considerations

The LT3099 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 159°C, with about 5°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature of 125°C. It is important to consider all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance, or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources close to the LT3099.

The underside of the package has exposed metal from the lead frame to the die attachment. The package allows heat to transfer directly from the die junction to the PCB metal to limit the maximum operating junction temperature. The dual, inline pin arrangement allows the metal to extend beyond the ends of the package on the top side (component side) of the PCB.

For surface mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can spread the heat generated by the regulator.

Table 6 lists thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and

high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 6. Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
TOP SIDE*	BOTTOM SIDE		
2500mm^2	2500mm^2	2500mm^2	34°C/W
1000mm^2	2500mm^2	2500mm^2	34°C/W
225mm^2	2500mm^2	2500mm^2	36°C/W
100mm^2	2500mm^2	2500mm^2	37°C/W

*Device is mounted on topside

Calculating Junction Temperature

Example: Given an output voltage of -3.3V and input voltage of -5V ±5%, output current range from -1mA to -1A, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The LT3099's power dissipation is:

$$P_{DISS} = I_{OUT(MAX)} (V_{IN(MAX)} - V_{OUT}) + I_{GND} V_{IN(MAX)}$$

where:

$I_{OUT(MAX)}$ = -1A

$V_{IN(MAX)}$ = -5.25V

I_{GND} (at I_{OUT} = -1A and V_{IN} = -5.25V) = -11.3mA

Therefore:

$$P_{DISS} = -1A \times (-5.25V + 3.3V) + 11.3mA \times 5.25V = 2W$$

For the DFN package, the thermal resistance ranges from 34°C/W to 37°C/W, depending on the copper area. Therefore, the junction temperature rise above the ambient approximately equals:

$$2W \times 35°C/W = 70°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{J(MAX)} = 50°C + 70°C = 120°C$$

Overload Recovery

Like many IC power regulators, the LT3099 incorporates SOA protection. The SOA protection activates at input-to-output differential voltages greater than 8V. The SOA protection decreases the current limit as the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the LT3099's *Absolute Maximum Ratings*. The LT3099 provides some output current level for all input-to-output differential voltage values. See the Current Limit Curves in the *Typical Performance Characteristics* section. When power is first applied and input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the regulator to supply large output current and start-up into high current loads.

Due to current limit foldback, however, a problem can occur at high input voltages if the output voltage is low and the load current is high. Such situations occur after removing a short-circuit or if the EN/UV pin is pulled high after the input voltage has turned on. The load line, in such cases, intersects the output current profile at two points. The regulator now has two stable operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought back up again to make the output recover. Other linear regulators with foldback current limit protection, such as the *LT3094* and *LT3090*, also exhibit this phenomenon, which is not unique to the LT3099.

Protection Features

The LT3099 incorporates several protection features for sensitive applications. Precision current limit and thermal overload protection safeguard the LT3099 against overload and fault conditions at the device's output. For normal operation, do not allow the junction temperature to exceed 125°C.

Pulling the LT3099's output above ground induces no damage to the part. If IN is left open circuit or grounded, OUT can be pulled 5V above GND. In this condition, a maximum current of 30mA flows into the OUT pin and out of the GND pin. If IN is powered by a voltage source, OUT sinks the LT3099's (foldback) short circuit current and protects itself by thermal limiting. In this case, however, grounding the EN/UV pin turns off the device and stops OUT from sinking the short-circuit current.

TYPICAL APPLICATIONS

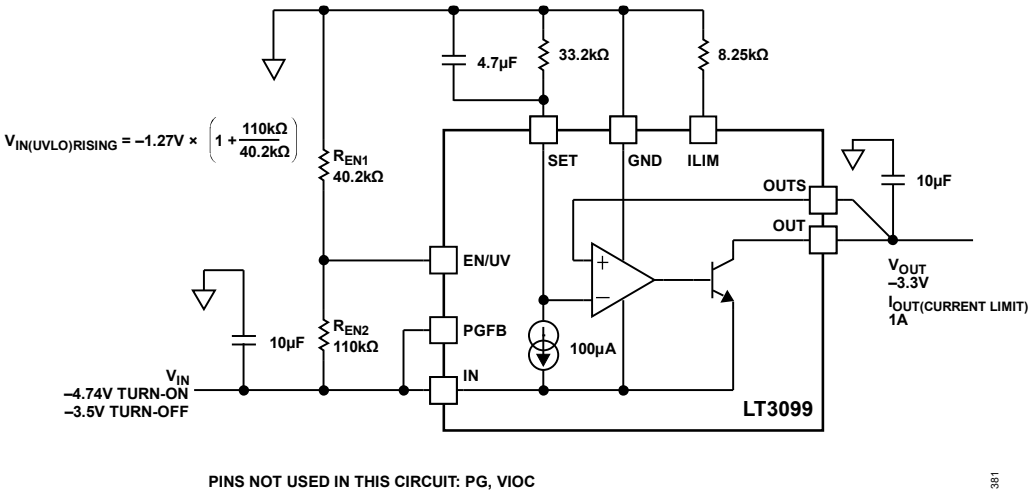


Figure 83. Programming Undervoltage Lockout

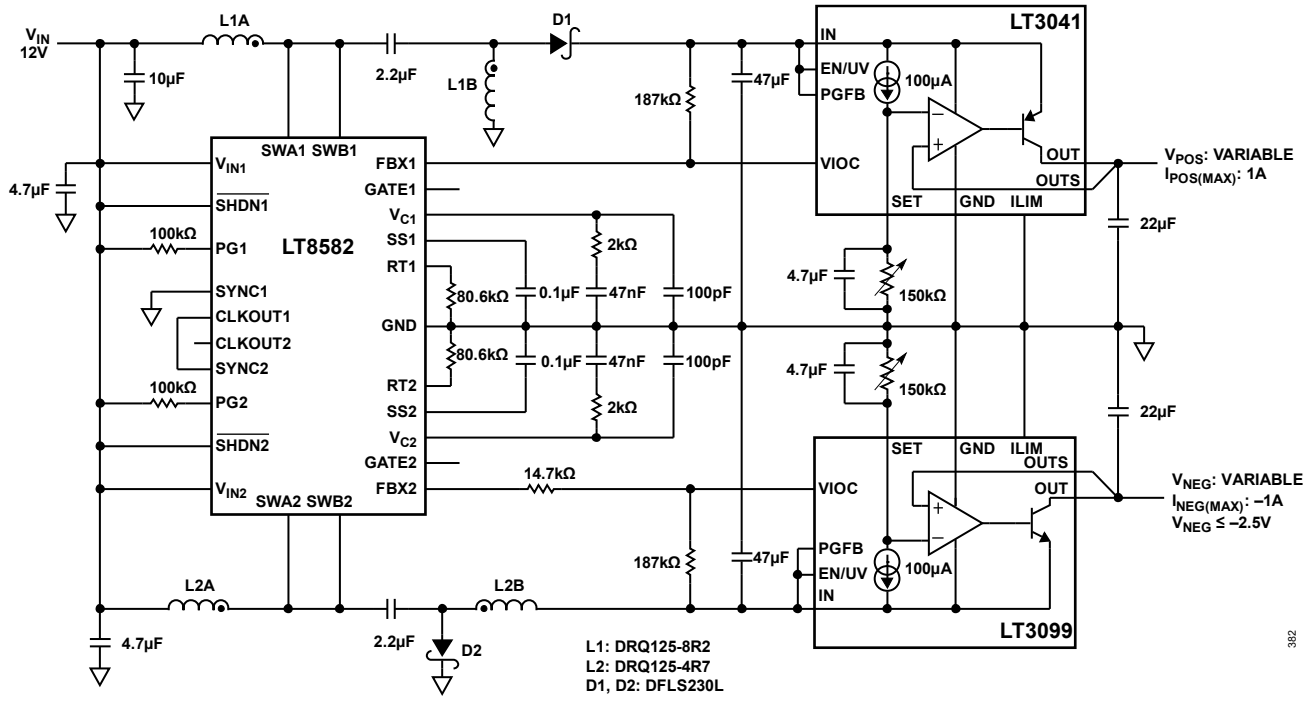
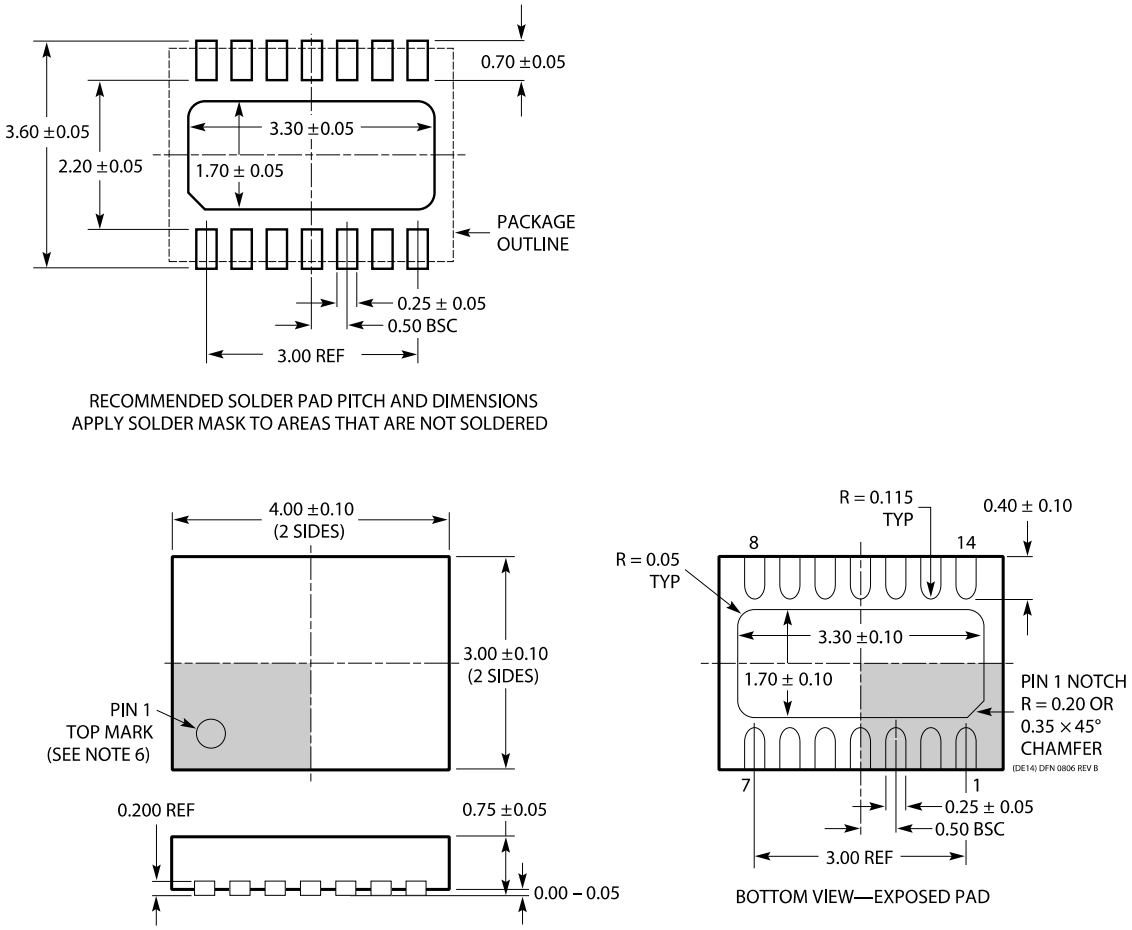


Figure 84. Positive and Negative Variable Supply

OUTLINE DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 85. 14-Lead, 4mm × 3mm, Plastic DFN (05-08-1708) (Dimensions shown in millimeters)

ORDERING INFORMATION

Table 7. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING, QUANTITY	PACKAGE OPTION
LT3099ADE#PBF	-40°C to 125°C	14-Lead Plastic DFN (4mm x 3mm)	Tray, 490	05-08-1708
LT3099ADE#TRPBF	-40°C to 125°C	14-Lead Plastic DFN (4mm x 3mm)	Reel, 2500	05-08-1708

[1]All models are RoHS compliant parts.

EVALUATION BOARDS

Table 8. Evaluation Boards

MODEL[1]	DESCRIPTION
EVAL-LT3099-AZ	Evaluation Board

[1]The EVAL-LT3099-AZ is a RoHS compliant part.

RELATED PRODUCTS

MODEL	DESCRIPTION	COMMENTS
LT3094	−20V, 500mA, ultralow noise, ultrahigh PSRR negative linear regulator	0.8µV_{RMS} noise and 74dB PSRR at 1MHz, V_{IN} = –1.8V to –20V, 235mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
LT3093	−20V, 200mA, ultralow noise, ultrahigh PSRR negative linear regulator	0.8µV_{RMS} noise and 73dB PSRR at 1MHz, V_{IN} = –1.8V to –20V, 190mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
LT3090	–36V, 600mA Negative Linear Regulator with Programmable Current Limit	18µV_{RMS} noise and 25dB PSRR at 1MHz, VIN = –1.5V to –36V, 300mV dropout voltage, programmable current limit, 3mm × 3mm DFN and MSOP packages
LT3041	20 V, 1 A, Ultra-Low Noise, Ultra-High PSRR Linear Regulator with VIOC Control	1µV_{RMS} noise and 80dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, 310mV dropout voltage, programmable current limit and power good, 4mm × 3mm DFN package
LT3046	20 V, 200 mA, Ultra-Low Noise, Ultra-High PSRR Linear Regulator	0.8µV_{RMS} noise and 82dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, 300mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN package
LT3042	20V, 200mA, ultralow noise, ultrahigh PSRR RF linear regulator	0.8µV_{RMS} noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
LT3045	20V, 500mA, ultralow noise, ultrahigh PSRR linear regulator	0.8µV_{RMS} noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV dropout voltage, 3mm × 3mm DFN and MSOP packages
LT3045-1	20V, 500mA, ultralow noise, ultrahigh PSRR linear regulator with VIOC control	0.8µV_{RMS} noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV dropout voltage, 3mm × 3mm DFN and MSOP packages
LT3040	20V, 200mA, ultralow noise, ultrahigh PSRR precision DAC/reference buffer	1.2µV_{RMS} noise and 73dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV dropout voltage, 3mm × 3mm DFN and MSOP Packages
ADP1761	1A, Low V_{IN}, low noise, CMOS linear regulator	2µV_{RMS} noise and 41dB PSRR at 1MHz, V_{IN} = 1.10V to 1.98V, 30mV dropout voltage, soft-start and power good, 3mm x 3mm LFCSP package
ADP7156	1.2A, ultralow noise, high PSRR, fixed output, RF linear regulator	1.6µV_{RMS} noise and 60dB PSRR at 1MHz, V_{IN} = 2.3V to 5.5V, 120 mV dropout voltage, 3mm × 3mm LFCSP and 8-lead SOIC packages
ADP7157	1.2A, ultralow noise, high PSRR, adjustable output, RF linear regulator	1.6µV_{RMS} noise and 55dB PSRR at 1MHz, V_{IN} = 2.3V to 5.5V, 120mV dropout voltage, 3mm × 3mm LFCSP and 8-lead SOIC packages
ADM7150	800mA, ultralow noise, high PSRR, fixed output, RF linear regulator	1.6µV_{RMS} noise and 60dB PSRR at 1MHz, V_{IN} = 4.5V to 16V, 600mV dropout voltage, 3mm × 3 mm LFCSP and 8-lead SOIC packages
ADM7151	800mA, ultralow noise, high PSRR, adjustable output, RF linear regulator	1.6µV_{RMS} noise and 60dB PSRR at 1MHz, V_{IN} = 4.5V to 16V, 600mV dropout voltage, 3mm × 3mm LFCSP and 8-lead SOIC packages

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