EVAL-LTC9105-AZ

LTC9105, MAX5974C, LT4321, and ADuM1252 IEEE 802.3bt Powered Device with I²C Telemetry

FEATURES

- IEEE 802.3bt-compliant Class 6 PD
- Port telemetry with an isolated I²C interface
- 5V/9.2A isolated synchronous forward converter

EVALUATION KIT CONTENTS

- EVAL-LTC9105-AZ
- 14-pin ribbon cable

ADDITIONAL HARDWARE NEEDED

- IEEE 802.3bt PSE
- Electronic load supporting 5V/9.2A
- Optional: DC power supply supporting 55V/1.2A
- Optional: DC590B I²C interface board

SOFTWARE NEEDED

- Optional: EVAL-LTC9105-AZ GUI for evaluating telemetry

GENERAL DESCRIPTION

The EVAL-LTC9105-AZ is an IEEE 802.3bt-compliant Type 3, Class 6 Power over Ethernet (PoE) powered device (PD) with port telemetry via I²C. The evaluation board features the LTC9105 PD interface controller, MAX5974C switching regulator controller, the LT4321 PoE ideal diode bridge controller, and the ADuM1252 I²C isolator.

The LTC9105 provides IEEE 802.3af-, IEEE 802.3at-, and IEEE 802.3bt-compliant interfacing with port voltage and current telemetry via I²C. It utilizes an external, low channel resistance, $R_{DS(ON)}$ (34mΩ typical), N-channel, hot-swap metal-oxide semiconductor, field-effect transistor (MOSFET), and 50mΩ sense resistor. Automatic maintain power signature (MPS) keeps the port connected when the current drops to a low level.

The MAX5974C controls a DC/DC converter utilizing a highly efficient active-clamp forward converter topology with synchronous rectification and provides an isolated 5V/9.2A output. The LT4321 controls eight low $R_{DS(ON)}$ (57mΩ typical), N-channel MOSFETs to further improve end-to-end power delivery efficiency and ease thermal design. The ADuM1252 isolates I²C data between the LTC9105 and a host controller on a nonisolated ground domain.

The EVAL-LTC9105-AZ is configured as a Class 6 PD and accepts up to 51W of delivered power from a power sourcing equipment (PSE) via its RJ45 connector (J1). The EVAL-LTC9105-AZ can be powered by a local 55V DC power supply using the auxiliary supply input terminals. With the DC590B I²C interface board connected to the EVAL-LTC9105-AZ, the EVAL-LTC9105-AZ graphical user interface (GUI) displays port telemetry and configuration options.

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Table 1. EVAL-LTC9105-AZ Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	Measured +PVOUT to DGND		5		V
Output Current	I_{OUT}	Class 6 (default)			9.2	A
Output Voltage Ripple		Port voltage (V_{PORT}) = 57V, I_{OUT} = 9.2A		100		mV p-p
Switching Frequency				300		kHz
Load Regulation		I_{OUT} = 0A to 9.2A		0.1		%
Line Regulation		V_{PORT} = 43V to 57V		0.1		%
Efficiency		V_{PORT} = 43V, I_{OUT} = 9.2A, DC-DC converter only (PVIN to V_{OUT})		93.1		%
		V_{PORT} = 43V, I_{OUT} = 9.2A, after bridge (V_{PORT} to V_{OUT})		92.2		%
		V_{PORT} = 43V, I_{OUT} = 9.2A, end-to-end (RJ45 to V_{OUT})		91.3		%

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

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REVISION HISTORY

2/2025—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

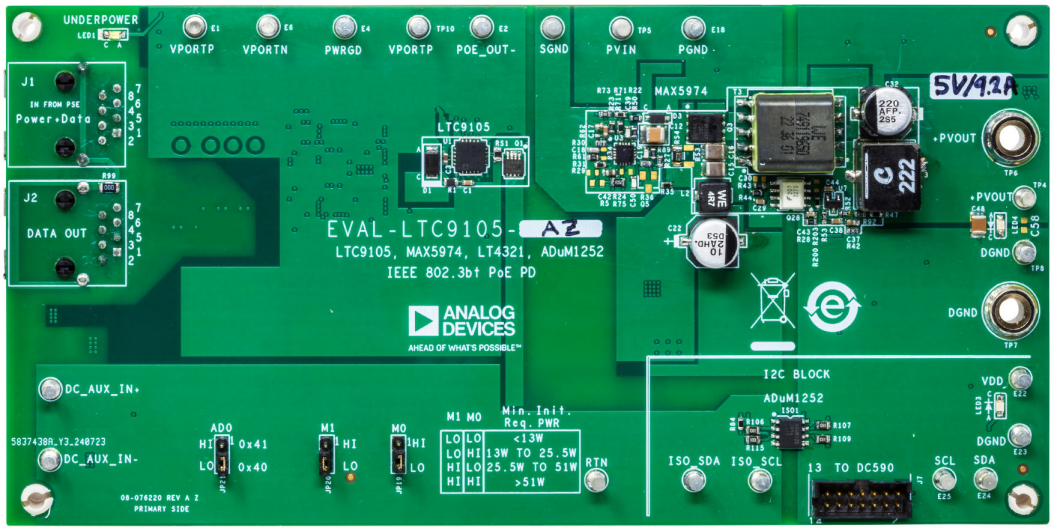

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Figure 1. EVAL-LTC9105-AZ Evaluation Board Photograph

QUICK START PROCEDURE

EVAL-LTC9105-AZ OPERATION

This quick start procedure shows how to connect the EVAL-LTC9105-AZ. Take the following steps and refer to Figure 2, Table 2, and Table 3 for the proper equipment setup and default configuration. Note that the default setup is Class 6 (IEEE 802.3bt, Type 3) with I²C Address 0x40 and <13W minimum initial required power:

1. Set the minimum initial required power to <13W with the mark count jumpers (JP19 and JP20). With this configuration, the LTC9105 applies power to the downstream circuitry if it receives 13W or more from the PSE. Refer to Table 2 for the mark count jumper settings and minimum initial required power for each PSE type.
2. Set the I²C address of the LTC9105 to 0x40 with the AD0 jumper (JP21). Refer to Table 3 for the AD0 jumper configurations.
3. Connect a load to the EVAL-LTC9105-AZ between +PVOUT and DGND.
4. Optionally, connect a ribbon cable from the DC590B 14-pin header (J4) to the EVAL-LTC9105-AZ 14-pin header (J6) and connect the USB Type B cable from the DC590B to the PC of the user for evaluation with the EVAL-LTC9105-AZ GUI.
5. Connect the output of the IEEE 802.3bt PSE to the RJ45 connector (J1) of the EVAL-LTC9105-AZ using a CAT5e or CAT6 Ethernet cable.
6. After connection is established, verify the output light-emitting diode (LED), LED4, is lit, which indicates that the DC-DC output is present.
7. Enable the load.

Table 2. Minimum Initial Required Power and Mark Count Settings

		Mark Count Jumpers	
Minimum PSE Type	**Minimum Initial Required Power**	**M1, JP20**	**M0, JP19**
Type 1	<13W	**LO**	**LO**
Type 2	13W to 25.5W	**LO**	**HI**
Type 3	25.5W to 51W	**HI**	**LO**
Type 4	51W to 71.3W	**HI**	**HI**

Table 3. I²C Address Settings

I²C Address	**I²C Address Jumper: AD0, JP21**
0x40	**LO**
0x41	**HI**

QUICK START PROCEDURE

SETUP DIAGRAM

See Figure 2 for the evaluation board setup.

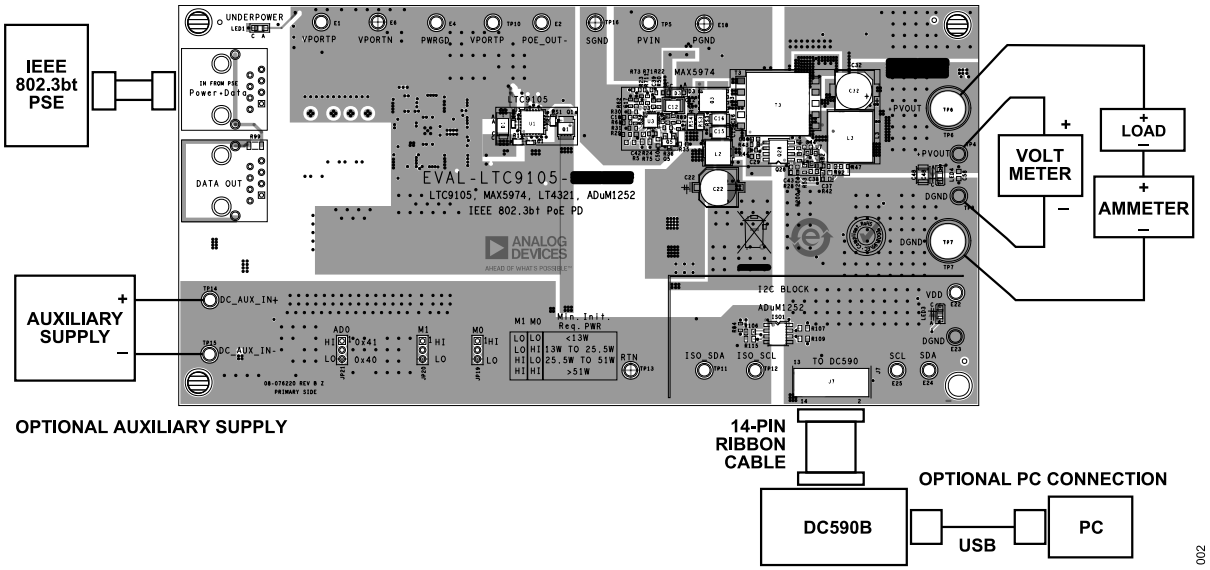

Figure 2. EVAL-LTC9105-AZ Setup

EVALUATION BOARD FEATURES

MINIMUM INITIAL REQUIRED POWER

When a PD is connected to an IEEE 802.3af, IEEE 802.3at, or IEEE 802.3bt PSE, the PSE can perform classification after the initial detection. Classification allows for the PSE to determine the requested power of the PD. In turn, the PD can determine the allocated power of the PSE by the number of mark events during classification. A PSE can demote the PD and allocate less power than the PD requested.

IEEE 802.3 requires a demoted PD to not exceed its power allocation. For some PD applications, the demoted power is less than the required boot-up power or normal operation power. The LTC9105 can be configured to block the downstream circuitry from powering on while providing an active indication that it is underpowered. The LTC9105 powers the downstream circuitry if sufficient allocated power is present.

To determine if the LTC9105 must apply power to the downstream circuitry, the LTC9105 compares the number of mark events provided by the PSE to the minimum initial required power as set by the mark count pins (M1 and MO). If the allocated power is less than the minimum initial required power, the LTC9105 draws the MPS current to keep the port connected while keeping its hot-swap MOSFET off. The UNDERPOWERED LED (LED1) turns on to indicate that the LTC9105 is underpowered and has received less than its minimum initial required power.

An underpowered LTC9105 does not power the downstream circuitry unless reconfigured via the I^2C interface. If the AUX pin goes high, the LTC9105 transitions to cold secondary mode. In cold secondary mode, the LTC9105 continues to draw MPS current until the AUX pin transitions low, at which point, the MPS current turns off for a PSE port reset.

CLASS SETTINGS AND OUTPUT POWER

The EVAL-LTC9105-AZ is configured for Class 6 by default with the RCLSA and RCLSB resistors. The PD class can be customized by changing these resistors. The on-board MAX5974C forward converter was optimized for 5V/9.2A targeting Class 6. This circuit can support 5V/11.2A (Class 7) and 5V/13A (Class 8); however, it may require additional thermal relief.

PSE ALLOCATED POWER

The host controller determines the PSE allocated power by reading the **mark_type** field via the I^2C interface and comparing it to the requested class of the PD. Refer to Table 4.

Table 4. PSE Allocated Power Based on PD Requested Class and mark_type

PD Requested Class	mark_type Value			
	0	**1**	**2**	**3**
0	13W			
1	3.84W			
2	6.49W			
3	13W			
4	13W	25.5W		
5	13W	25.5W	40W	
6	13W	25.5W	51W	
7	13W	25.5W	51W	62W
8	13W	25.5W	51W	71.3W

AUXILIARY INPUT

The EVAL-LTC9105-AZ accepts a DC auxiliary input between DC_AUX_IN+ and DC_AUX_IN−. This supply diode ORs with the PSE supply to the LTC9105. If the PSE is connected first, whichever supply has the highest voltage between the PoE port or the DC auxiliary supply powers the LTC9105. Otherwise, the auxiliary supply has priority and blocks the PSE from detecting or classifying the PD. The auxiliary supply operating range is 45V to 57V as programed by the AUX pin resistor divider.

Note: For DC auxiliary operation with the EVAL-LTC9105-AZ, the mark count jumpers must both be set to low to set <13W for the minimum initial required power.

EVALUATION BOARD FEATURES

PORT TELEMETRY

Via the I²C interface, the LTC9105 provides port telemetry including current, voltage, or power; PSE mark response; auxiliary status; and brownout status. Voltage and current are continuously measured by dedicated Δ-Σ analog-to-digital converters (ADCs) with 14-bit resolution and are individually read back by the host when the **padc_data** bit is cleared. Optionally, the voltage and current can be mixed to produce a power reading instead of a voltage reading when the **padc_data** bit is set. Priority status, standby mode, power ADC enable, and the AUX pin threshold are all configurable via the I²C interface.

EVAL-LTC9105-AZ GUI OPERATION

The EVAL-LTC9105-AZ GUI allows users to evaluate the LTC9105 telemetry and configuration options. Use a 14-pin ribbon cable between the DC590B and EVAL-LTC9105-AZ evaluation board and a Type-B USB cable to connect from the DC590B to the PC of the user. Open the EVAL-LTC9105-AZ GUI to display the window shown in Figure 3. Installation of Analog Devices, Inc., QuikEval software is required prior to operation. If an error occurs when opening the GUI, verify that the DC590B is connected directly to the PC of the user.

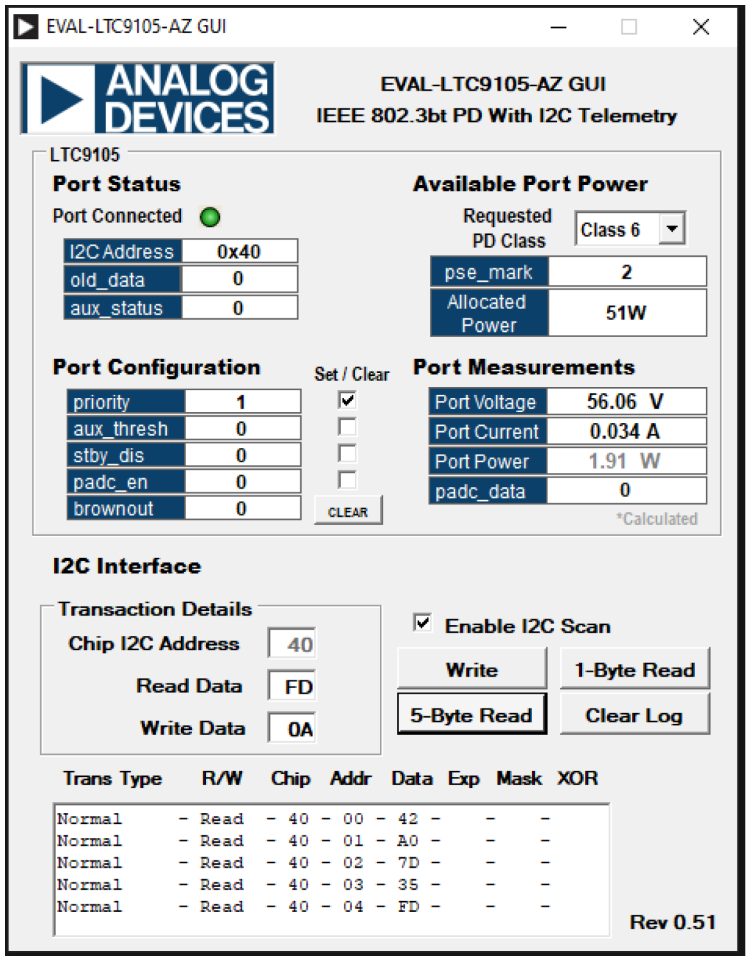

Figure 3. EVAL-LTC9105-AZ GUI Window

EVALUATION BOARD FEATURES

Port Status

The **Port Status** section indicates if an LTC9105 was detected by the GUI, information about the LTC9105 status, and the I^2C transaction. The I^2C address field displays the active I^2C address. If **old_data** is set, it indicates that the telemetry data was already read within the current sampling interval (100ms typical), and if **aux_status** is set, it indicates that another power source is present.

Available Port Power

The **Available Port Power** section displays the result of the physical layer classification and the allocated power. **pse_mark [1:0]** contains the result of physical layer classification, and determines allocated power based on the requested class of the PD. The EVAL-LTC9105-AZ default is Class 6; the class of the PD can be changed by replacing the RCLSA and RCLSB resistors. The GUI compares the **Requested PD Class** dropdown menu with **pse_mark** to identify the allocated power.

Port Configuration

The **Port Configuration** shows several ways to modify the behavior of the LTC9105. The four read/write bit states are shown with a corresponding checkbox that is checked when the bit is **1** and unchecked if it is **0**. The bit state may be changed by clicking the **Set/Clear** checkbox adjacent to each bit. The last bit is write one to clear and has a **CLEAR** button. **priority** indicates whether the PD is the primary power source, or if it is in standby mode. Setting **stby_dis** disables the hot-swap MOSFET of the PD, and the MPS current is only drawn if an auxiliary power source is present. Setting **aux_thresh** increases the AUX pin threshold voltage. **padc_enable** configures the ADCs for either voltage or power. Note, it may take up to 200ms (typical) for **padc_enable** to change the **padc_data** state. **brownout** indicates if the port voltage of the PD dropped to less than the off voltage (V_{OFF}) but has stayed more than the reset voltage (V_{RESET}). Click the **CLEAR** button next to the **brownout** bit to clear.

Port Measurements

The **Port Measurements** include port voltage, current, and power. **padc_data** indicates that Register 4 and Register 5 contain voltage or power data. The default configuration has **padc_data** cleared indicating that the registers contain voltage data, while if **padc_data** is set, the registers contain power data. The GUI automatically calculates voltage or power based on the ADC configuration. The calculated value is shown in gray, while the directly measured value is shown in black.

I^2C Interface

The **I2C Interface** section allows users to manually configure the I^2C interface and logs user I^2C transactions. The GUI automatically scans I^2C Address 0x40 and I^2C Address 0x41 for a LTC9105 and displays data from the first address detected. To disable the I^2C scan, uncheck the **Enable I2C Scan** box to allow user input into the **Chip I2C Address** field. **Write**, **1-Byte** (first LTC9105 register), and **5-Byte** (all five LTC9105 registers) read transactions each have buttons, while the write and read data have text fields. The user's I^2C transactions are logged, and the log can be cleared by clicking the **Clear Log** button.

TYPICAL PERFORMANCE CHARACTERISTICS

EVAL-LTC9105-AZ TEST DATA

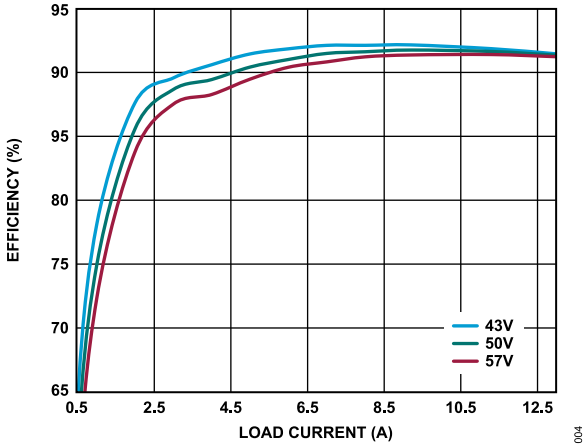

Figure 4. EVAL-LTC9105-AZ Efficiency vs. Load Current (After Bridge to V_{OUT})

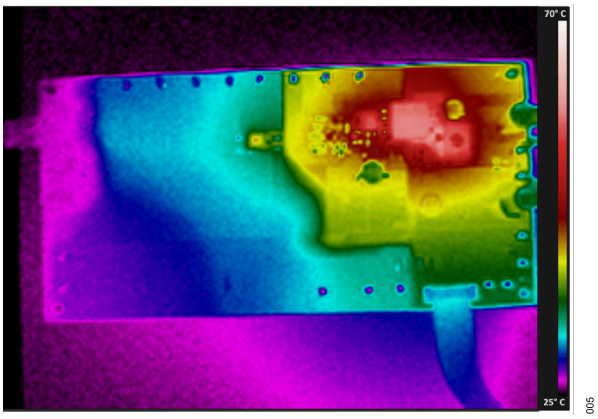

Figure 5. Front Thermal Image (Test Conditions: V_{PORT} = 52V and I_{OUT} = 9.2A)

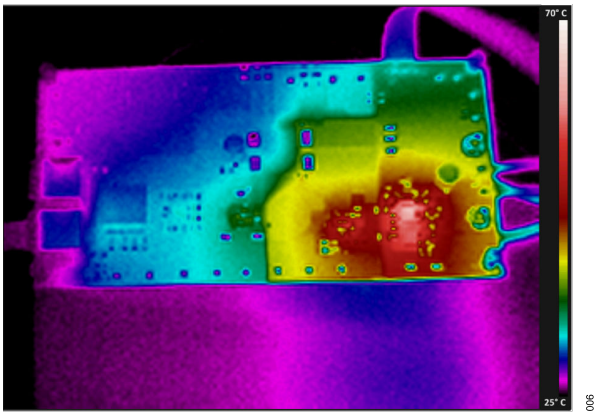

Figure 6. Back Thermal Image (Test Conditions: V_{PORT} = 52V and I_{OUT} = 9.2A)

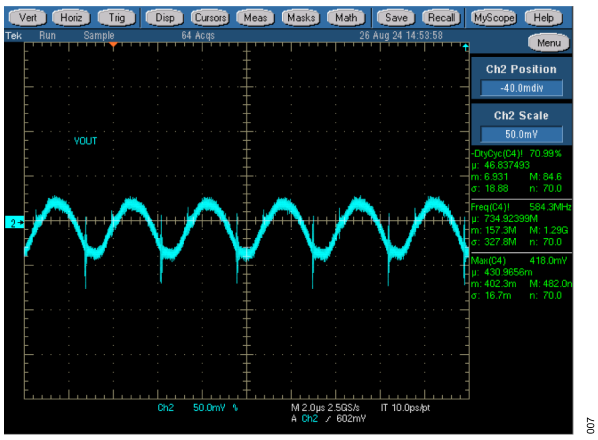

Figure 7. Output Voltage Ripple (Test Conditions: V_{PORT} = 50V and I_{OUT} = 9.2A)

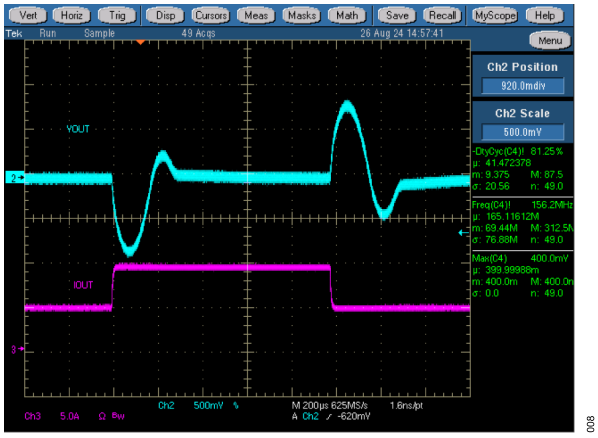

Figure 8. Load Transient Response (Test Conditions: V_{PORT} = 50V and Load Step: 4.6A to 9.2A DC Load)

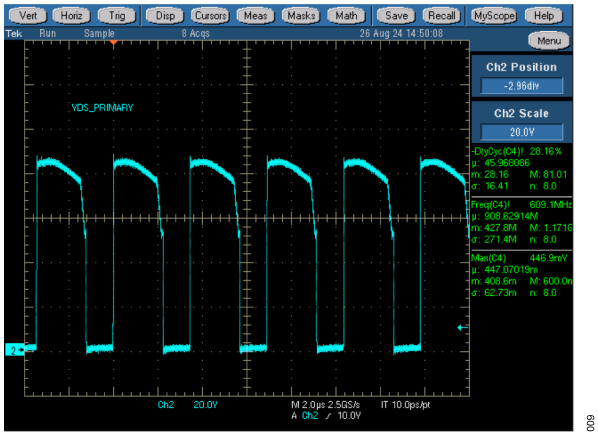

Figure 9. Switch Node Waveforms: Primary Side (Test Conditions: V_{PORT} = 57V and I_{OUT} = 9.2A)

TYPICAL PERFORMANCE CHARACTERISTICS

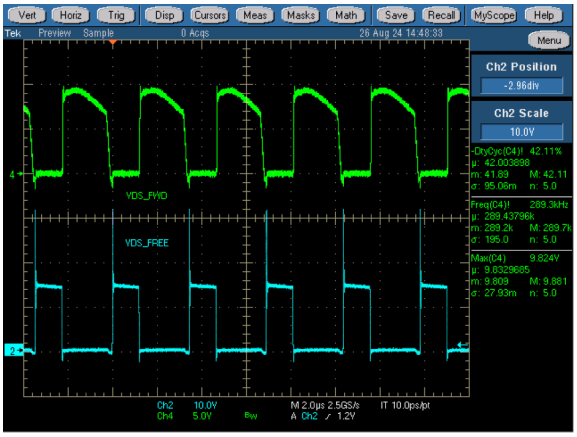

Figure 10. Switch Node Waveforms: Secondary Side
(Test Conditions: V_{PORT} = 57V and I_{OUT} = 9.2A)

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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