Evaluating the ADAQ4380-4/ADAQ4370-4/ADAQ4381-4 Quad, 16-/14-Bit, 4/2 MSPS, Simultaneous Sampling, µModule Data Acquisition Solutions

FEATURES

- ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 quad, 16-/14-bit, 4/2 MSPS, µModule® evaluation boards
- Versatile analog signal conditioning circuitry
- On-board LDO and power supply circuits
- PC software for control and data analysis of time and frequency domain
- System demonstration platform-compatible (SDP-H1, high-speed controller board (EVAL-SDP-CH1Z))

EVALUATION BOARD KIT CONTENTS

- EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ evaluation board

EQUIPMENT NEEDED

- PC running Windows® 10 or higher
- SDP-H1 (EVAL-SDP-CH1Z) controller board
- Low noise, precision signal source (such as APX500 series)
- Standard USB A to USB mini-B
- Band-pass filter suitable for 16-bit testing (optional, value based on signal frequency)

SOFTWARE NEEDED

- ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 ACE plug-in
- SDP-H1 driver

GENERAL DESCRIPTION

The EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards (see Figure 1) enable a simple evaluation of the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 quad, 16-/14-bit, 4/2 MSPS, simultaneous sampling, µModule data acquisition solutions, respectively. The evaluation boards demonstrate the performance of the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 µModules and are versatile tools for variety of applications.

The ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 µModules combine multiple common signal processing and conditioning blocks into a single device that includes a low noise, fully differential analog-to-digital converter (ADC) drivers, a high precision 3.3 V reference chip, low-noise reference buffer, high resolution, quad, 16-/14-bit, 4/2 MSPS simultaneous sampling successive approximation register (SAR) ADC, and all the critical passive components necessary for optimum performance.

The EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards interface with high-speed system demonstration platform SDP-H1 (EVAL-SDP-CH1Z) board through a 160-pin FMC connector, as shown in Figure 2.

Refer to the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 data sheets for full specifications, which must be consulted in conjunction with this user guide when using the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards. For the current schematic, layouts, and bill of materials, refer to the EVAL-ADAQ4380-4, EVAL-ADAQ4370-4, or EVAL-ADAQ4381-4 product page.

EVALUATION BOARD PHOTOGRAPH

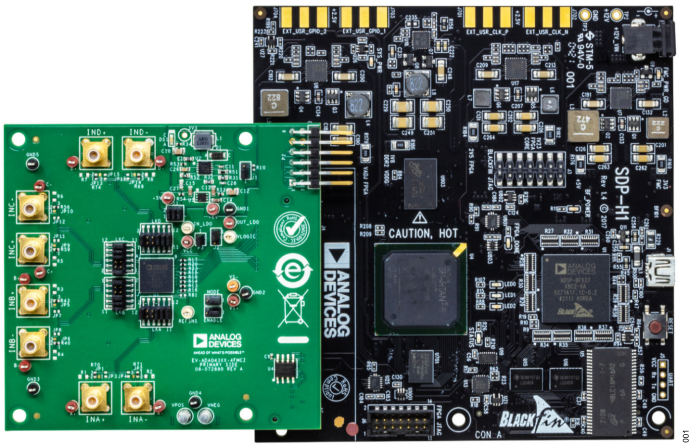

Figure 1. Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Rev. A to Rev. B

Changes to User Guide Title ... 1
Added EV-ADAQ4381-4FMCZ and ADAQ4381-4 (Universal) ... 1
Changes to Features Section ... 1
Changes to General Description Section ... 1
Changes to Launching the Software Section ... 11

9/2024—Rev. 0 to Rev. A

Changes to User Guide Title ... 1
Added EV-ADAQ4370-4FMCZ (Universal) ... 1
Changes to Features Section ... 1
Changes to Software Needed Section ... 1
Changes to General Description Section ... 1
Changes to Setting Up the Evaluation Board Section ... 4
Changes to Power Supplies Section ... 4
Changes to Analog Inputs Section, Table 2, and Table 3 ... 5
Changes to Link Configuration For Different Gain Options Section ... 6
Changes to Software Installation Section ... 8
Changes to Troubleshooting Section ... 10
Changed Connecting the EV-ADAQ4380-4FMCZ and the SDP-H1 to the PC Section to Connecting the Evaluation Board and the SDP-H1 to the PC Section ... 10
Changes to Connecting the Evaluation Board and the SDP-H1 to the PC Section ... 10
Changed Disconnecting the EV-ADAQ4380-4FMCZ Section to Disconnecting the Evaluation Board and the SDP-H1 to the PC Section ... 10
Changes to Board Layout Guidelines Section ... 10
Changes to Launching the Software Section ... 11
Changes to Description of the Analysis Window Section ... 14
Changes to CAPTURE Pane Section ... 14
Changes to Waveform Graph Section ... 15

TABLE OF CONTENTS

5/2024—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

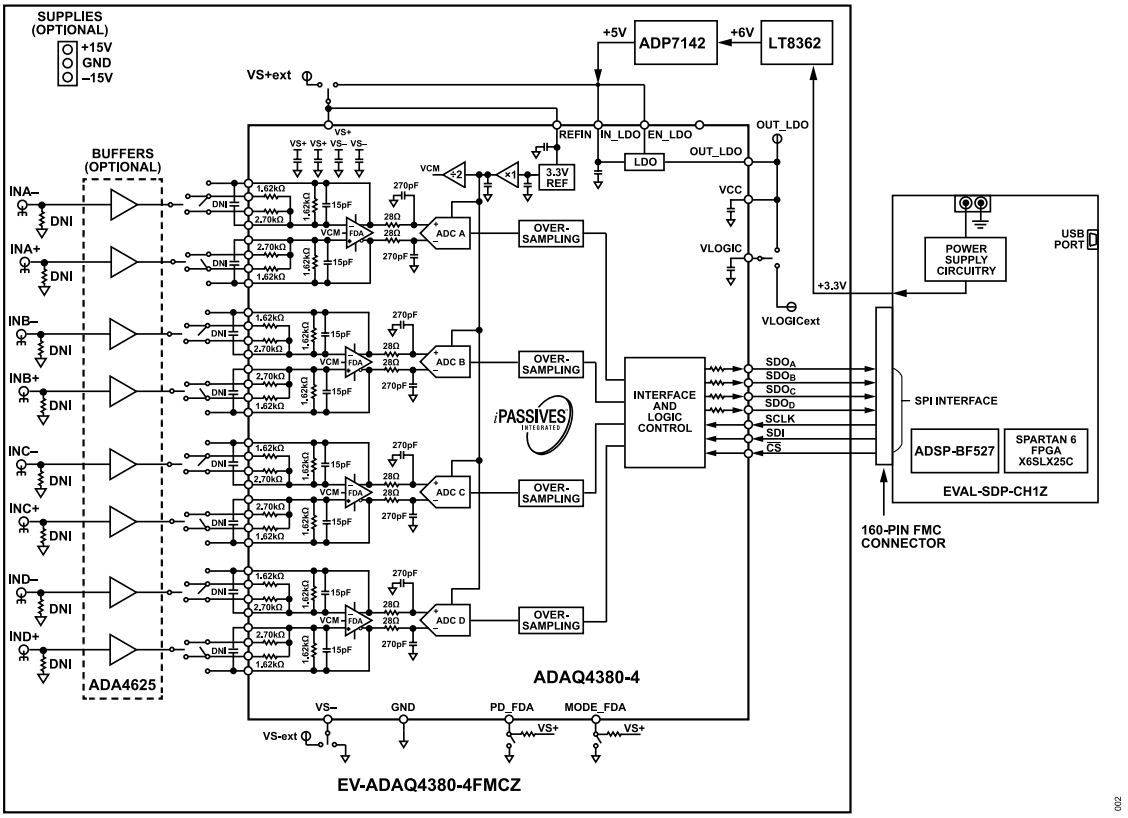

Figure 2. Simplified Evaluation Block Diagram

SETTING UP THE EVALUATION BOARD

Figure 2 shows the simplified evaluation board block diagram of the EV-ADAQ4380-4FMCZ connected to the SDP-H1 controller board. The board consists of one µModule (U1, ADAQ4380-4), on-board power supplies to derive the necessary supply rails using the LT8362 (U2), and the ADP7142 (U3). Provision for optional buffer amplifiers is available when evaluating the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4, where sensors require high input impedance and/or further amplification is required.

SDP-H1 CONTROLLER BOARD

The EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation kits use a serial-port interface (SPI) and require the system demonstration platform (SDP-H1) controller board to capture the data through a graphic user interface (GUI), see Figure 1. The SDP-H1 board requires power from a 12 V wall adapter. The SDP-H1 has a Xilinx® Spartan 6 and an ADSP-BF527 processor with connectivity to the PC through a USB 2.0 high speed port. The controller boards allow the configuration and capture of data on the daughter boards from the PC through a USB.

The SDP-H1 has an FMC low pin count (LPC) connector with full differential LVDS and singled-ended low voltage CMOS support. It also features the 120-pin connector that exposes the Blackfin® processor peripherals. This connector provides a configurable serial, parallel I²C and SPI, and general-purpose input/output (GPIO) communications lines to the attached daughter boards for the functional description of the on-board power supplies.

POWER SUPPLIES

All necessary supply rails on the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ are powered by a 3.3 V rail coming from the SDP-H1 board. The evaluation boards can be powered from an external 3.3 V supply applied using the 3V3 pin header. For an external 3.3 V supply configuration change J1 header position, see Table 2.

The board positive rails, 5 V (+VS), 3.45 V (VCC), and 3.45 V (VLOGIC), are generated from a combination of the on-board power supplies, U2 (LT8362), U3 (ADP7142-5.0), and the internal 3.45 V low dropout (LDO) linear regulator. Decoupling capacitors for the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 supply pins are integrated within the µModule, adding external capacitors are not necessary. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 1. On-Board Power Supplies

Power Supply (V)	Function
+6.0	Supply rail from LT8362.

EVALUATION BOARD HARDWARE

Table 1. On-Board Power Supplies (Continued)

Power Supply (V)	Function
+5.0 (default)	VS+, REFIN, IN_LDO, and EN_LDO supply rail from ADP7142-5.0.
+3.45 (default)	VCC and VLOGIC supply rail from the internal LDO.

ANALOG INPUTS

The SMA connectors (INA+ and INA−, INB+ and INB−, INC+ and INC−, and IND+ and IND−) on the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards are used to provide analog inputs from a low noise, audio precision signal source (such as the SYS-2700 or the APX-500 series). Analog inputs are directly feed through the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4, as shown in Figure 2. The provision for optional amplifiers (A1, A2, A3, and A4), can be set up to any gain configuration to drive the inputs of the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 for high input impedance applications. In the default board configuration, analog input signals are fed directly to the inputs of the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4.

To evaluate dynamic performance, a fast Fourier transform (FFT), integral non-linearity (INL), differential non-linearity (DNL), or time domain (waveform and histogram) test can be performed by applying a very-low distortion AC source.

For low-input frequency testing below 100 kHz, it is recommended to use a low noise, audio-precision signal source, APX-500, set at high-performance sine generator. A different precision signal source can be used alternatively with additional band-pass filtering. The filter bandwidth depends on input bandwidth of interest.

Multiple link options must be set correctly for the appropriate operating setup before applying the power and signal to the evaluation board.

The EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards are factory configured to provide the appropriate input signal type, single-ended or fully differential, and different gain/attenuation or input range scaling.

Table 2 and Table 3 lists the necessary link options and jumper positions for different configurations.

Table 2. Link Options with Factory Default Setting

Link	Default	Function	Comment
LKA, LKB, LKC, LKD	1 to 2, 7 to 8, 9 to 10, 11 to 12	µModule gain configuration	Gain = 0.3. For the link configuration on different gain options, see Figure 3 to Figure 6.
J1	1 to 2	3.3 V input	Takes 3.3 V from the FMC. Change shunt to Pin 2 and Pin 3 when using external 3.3 V supply.
J2	1 to 2	VLOGIC input	Utilizes the 3.45 V from the internal LDO. Change shunt to Pin 2 and Pin 3 when external VLOGIC supply is required.
J3	1 to 2, 3 to 4, 5 to 6	µModule power supply	Utilizes the on-board +5 V power supply. Disconnect shunts when supplying external voltages to VS+, VS−, and IN_LDO thru respective header pins.
MODE	1 to 2	MODE_FDA control voltage	FDA power mode. Change shunt to Pin 2 and Pin 3 to enter low power mode.
ENABLE	1 to 2	PD_FDA control voltage	FDA enable. Change shunt to Pin 2 and Pin 3 to disable the FDAs (ADC Drivers).

Table 3. Jumper Positions with Factory Default Setting

Jumper	Default	Function	Comment
JP1, JP5, JP10, JP14	2 to 3	Optional buffers	Change to **2 to 1** to utilize optional buffers provision.
JP2, JP6, JP9, JP13	2 to 1	Optional buffers	Change to **2 to 3** to utilize optional buffers provision.
JP3, JP4, JP7, JP8, JP11, JP12, JP15, JP16	Not installed	Optional buffers	Install 0 Ω when using the provision for optional buffers.
R2, R4, R6, R8	Not installed (fully differential input)	µModule input configuration	Install 0 Ω for single-ended input configuration.

EVALUATION BOARD HARDWARE

LINK CONFIGURATION FOR DIFFERENT GAIN OPTIONS

Multiple link options must be set correctly for appropriate gain configuration of the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4. Table 4 details the different gain positions for the links of the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards.

LKA, LKB, LKC, and LKD connections are designed such that different link positions and combinations are identical on Channels A and B, whereas Channels C and D connections are mirror of Channels B and A, respectively. Figure 3 to Figure 6 link connections are applicable for Channels A and B.

Table 4. Different Gain Configurations for the Links of the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ

Gain	Input Range	Input Signal on Pins	Test Conditions
0.3	±11 V	INx2+ and INx2−	For LKA, LKB, LKC, and LKD, install shunt 1 to 2, 7 to 8, 9 to 10, and 11 to 12. See Figure 3.
0.6	±5.5 V	INx2+ and INx2−	For LKA, LKB, LKC, and LKD, install shunt 1 to 2, and 7 to 8. See Figure 4.
1.0	±3.3 V	INx1+ and INx1−	For LKA and LKB (Channel A and B), install shunt 1 to 3, and 5 to 7. For LKC and LKD (Channel C and D), install shunt 2 to 4, and 6 to 8. See Figure 5.
1.6	±2.06 V	INx1+ and INx2+, and INx1− and INx2−	For LKA, LKB, LKC, and LKD, install shunt 1 to 2, 3 to 4, 5 to 6, and 7 to 8. See Figure 6.

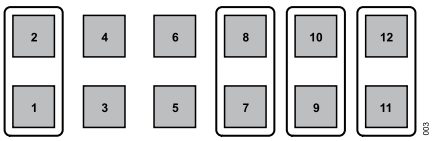

Figure 3. Gain = 0.3

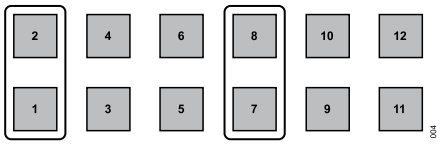

Figure 4. Gain = 0.6

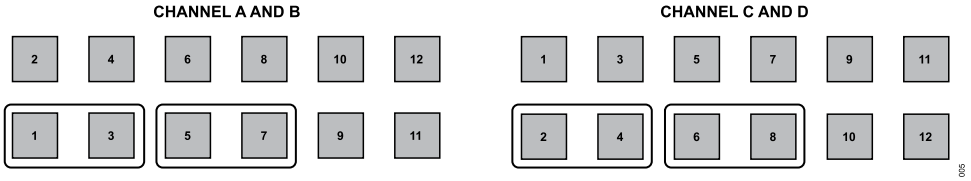

Figure 5. Gain = 1.0

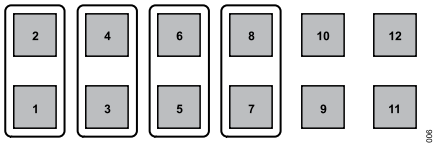

Figure 6. Gain = 1.6

EVALUATION BOARD HARDWARE

OPTIONAL BUFFERS AND FILTERS CONFIGURATION

The EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, and EV-ADAQ4381-4FMCZ evaluation boards include optional amplifiers for further amplification and filtering. By default, these amplifiers are bypassed and not connected to the analog-input signal path.

If evaluation requires, utilize these amplifiers by installing jumpers JP1 to JP16 (refer to the evaluation board schematic attached in the EVAL-ADAQ4380-4, EVAL-ADAQ4370-4, or EVAL-ADAQ4381-4 product page). Optional buffer provisions A1 to A4 are intended for high impedance buffering, amplification, and filtering. The filters can be configured as either low-pass (see Figure 7) or high-pass (see Figure 8) Sallen-Key filter.

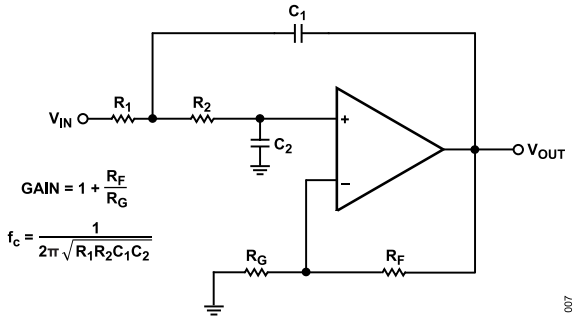

Figure 7. 2nd Order Low-Pass Filter Topology

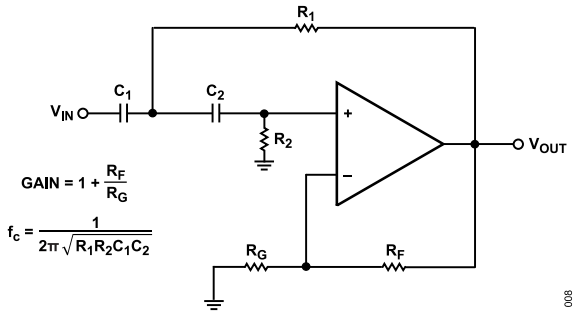

Figure 8. 2nd Order High-Pass Filter Topology

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

Before using the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ evaluation kit, download and install the ACE software. In addition, download the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 ACE plug-in from the **ACE Evaluation Board Plug-ins** section of the **ACE Software** page or from the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ product page.

To complete the installation process, do the following steps:

1. Install the ACE evaluation software.
2. Install the SDP-H1 drivers.
3. Install the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 plug-in. The ACE Quickstart page shows the plug-in installation guide.

Warning

To ensure that the evaluation system is properly recognized when it is connected to the PC, install the ACE software and the SDP-H1 driver before connecting the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ, and the SDP-H1 controller board to the USB port of the PC.

Installing the ACE Software

To install the ACE software, do the following steps:

1. Download the ACE software to a Windows®-based PC.
2. Double-click the **ACEInstall.exe** file to begin the installation. By default, the software is saved at **C:\Program Files (x86)\Analog Devices\ACE.**
3. A dialog box appears seeking permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. Click **Next >** to continue the installation, as shown in Figure 9.

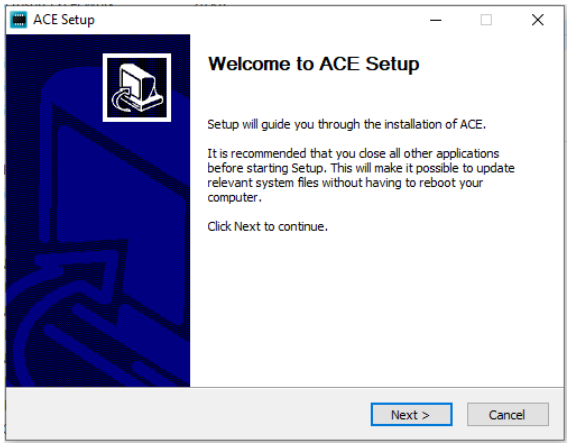

Figure 9. Evaluation Software Install Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 10).

Figure 10. License Agreement

6. Click **Browse...** to choose the installation location and click **Next>** (see Figure 11).

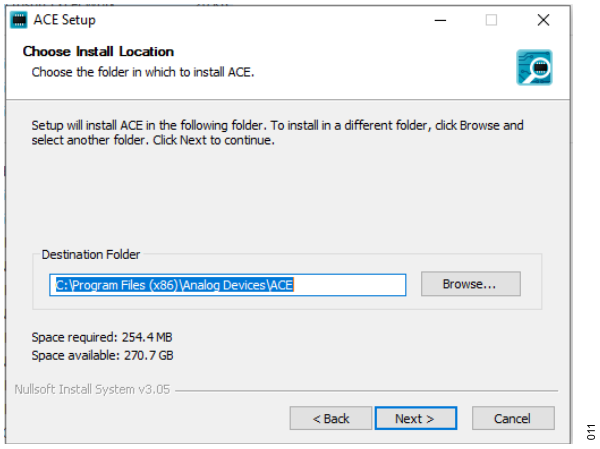

Figure 11. Choose Install Location

EVALUATION BOARD SOFTWARE

7. The ACE software components to install are preselected. Click **Install** (see Figure 12).

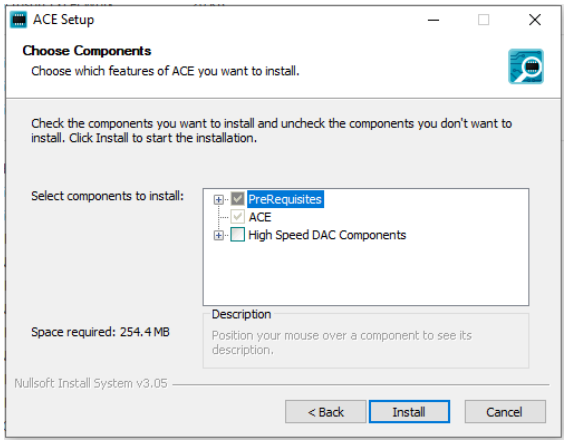

Figure 12. Choose Components

8. The installation is in progress. No action is required (see Figure 13).

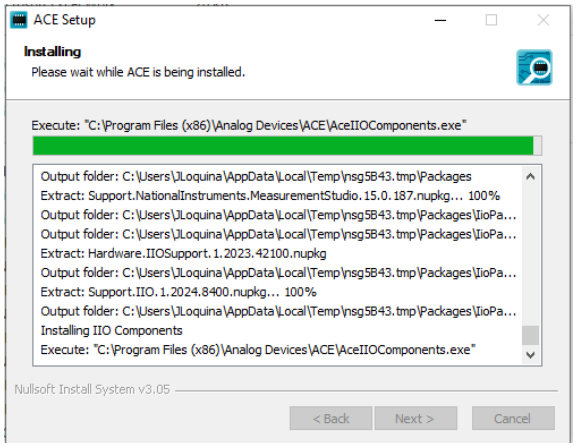

Figure 13. Installation in Progress

9. The installation is complete (see Figure 14). Click **Next >** and then click **Finish** (see Figure 15) to complete.

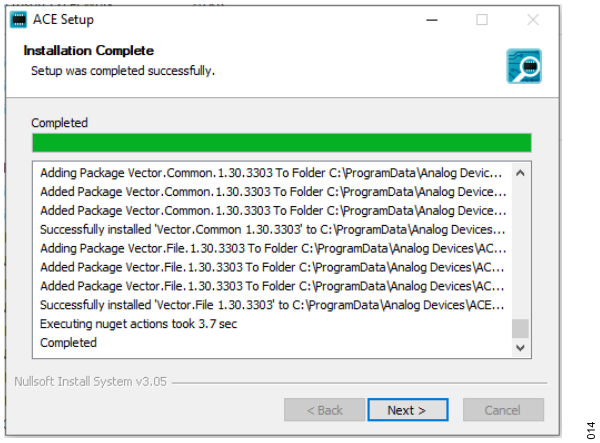

Figure 14. Installation Complete

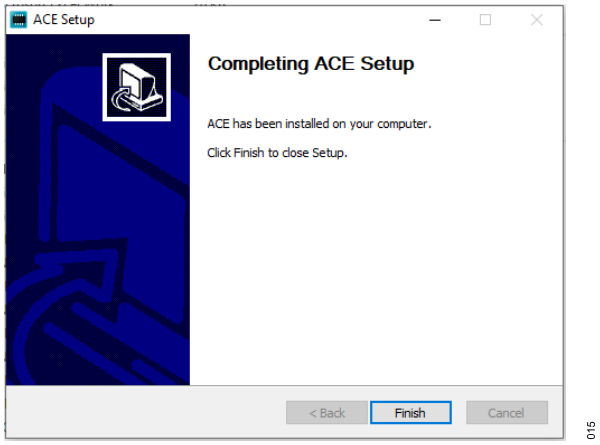

Figure 15. Completing ACE Setup

TROUBLESHOOTING

The SDP-H1 board is the communication link between the PC and the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ. Figure 2 shows a diagram of the connections between the evaluation board and the SDP-H1 board.

To ensure that the evaluation system is correctly recognized when it is connected to the PC, install the ACE software and the SDP-H1 driver before connecting the evaluation board and the SDP-H1 board to the USB port of the PC.

When the software installation is complete, set up the evaluation board and the SDP-H1 board as explained in the following sections.

CONNECTING THE EVALUATION BOARD AND THE SDP-H1 TO THE PC

To connect the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ, and the SDP-H1 board to the PC, do the following steps:

1. Ensure that all configuration links are in the appropriate positions, as shown in Table 2.
2. Connect the EV-ADAQ43XX-4FMCZ securely to the 160-pin FMC connector on the SDP-H1 board. The EV-ADAQ43XX-4FMCZ does not require an external power supply adapter.
3. Connect the SDP-H1 board to the PC through the USB cable enclosed in the SDP-H1 kit, see Figure 2.

VERIFYING THE BOARD CONNECTION

To verify the board connection, do the following steps:

1. Run the **Found New Hardware Wizard** after the SDP-H1 board is plugged into the PC. If using Windows XP, then search for the SDP-H1 drivers. Choose to automatically search for the drivers for the SDP-H1 board if prompted by the operating system.
2. A dialog box appears asking for permission to allow the program to make changes to the computer. In this case, click **Yes**. The **Computer Management** window appears.
3. From the list of **System Tools**, click **Device Manager** and use the **Device Manager** window to ensure that the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ is connected to the PC properly.
4. If the SDP-H1 driver software is installed and the board is connected to the PC properly, then in the **Device Manager** window, **Analog Devices SDP-H1** appears under **ADI Development Tools**, as shown in Figure 16.

DISCONNECTING THE EVALUATION BOARD AND THE SDP-H1 TO THE PC

Always remove power from the SDP-H1 board or press the Reset Tact switch located along the mini USB port before disconnecting the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ from the SDP-H1 board.

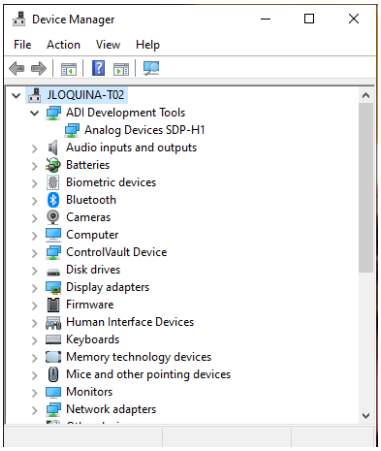

Figure 16. Device Manager Window

MECHANICAL STRESS

The mechanical stress of mounting a device to a board can cause subtle changes to the signal-to-noise ratio (SNR) and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended.

BOARD LAYOUT GUIDELINES

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4. A multilayer board with an internal and clean ground plane in the first layer beneath the µModule is recommended. Care must be taken with the placement of individual components and routing of various signals on the board. It is highly recommended to route input and output signals symmetrically. Solder the ground pins directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes under the analog input/output and digital input/output pins of the µModule to avoid undesired parasitic capacitance. Any undesired parasitic capacitance could impact the distortion and linearity performance.

The sensitive analog and digital sections must be separated on the PCB while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as SCLK or SDI, and digital outputs SDOA to SDOD must not run near or cross over analog signal paths to prevent noise coupling to the µModule.

Good quality ceramic bypass capacitors of at least 2.2 µF (0402, X7R) must be placed at the output of LDO generating the µModule supply rails (VS+, REFIN, and IN_LDO) to GND to minimize electromagnetic interference (EMI) susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the µModule to save extra board space and cost.

ACE SOFTWARE OPERATION

LAUNCHING THE SOFTWARE

When the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ, and SDP-H1 boards are properly connected to the PC, launch the ACE Software. To launch the **ACE Software**, do the following steps:

1. From the **Start** menu, select **All Programs** > **Analog Devices > ACE > ACE.exe** to open the main software window, as shown in Figure 17.
2. The **ADAQ4380-4 Eval Board**, **ADAQ4370-4 Eval Board**, or **ADAQ4381-4 Eval Board** icon appears in the **Attached Hardware** section.
3. If the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ is not connected to the USB port through the SDP-H1 board when the software is launched, the **ADAQ4380-4 Eval Board**, **ADAQ4370-4 Eval Board**, or **ADAQ4381-4 Eval Board** icon does not appear in the **Attached Hardware** section. Connect the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ, and SDP-H1 board to the USB port of the PC and wait a few seconds, then continue following these instructions.
4. Double-click the **ADAQ4380-4 Eval Board**, **ADAQ4370-4 Eval Board**, or **ADAQ4381-4 Eval Board** icon to open the board view window, as shown in Figure 18.
5. Double-click the **ADAQ4380-4**, **ADAQ4370-4**, or **ADAQ4381-4** chip icon to open the chip view window, as shown in Figure 19.
6. Click **Proceed to Analysis** in the chip view window to open the analysis view window, as shown in Figure 20.

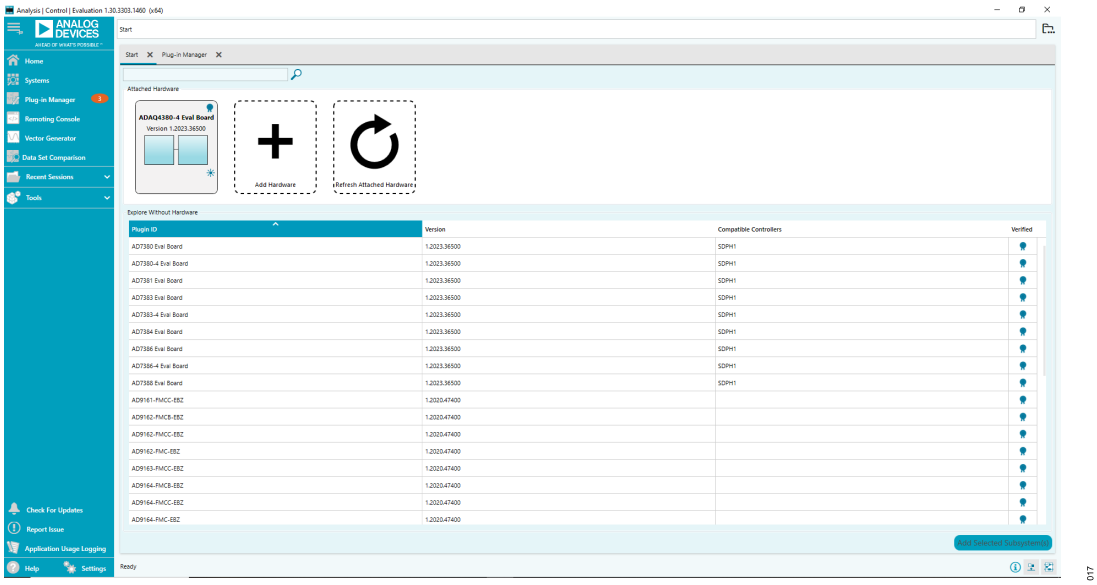

Figure 17. EVAL-ADAQ4380-4 ACE Software Main Window

ACE SOFTWARE OPERATION

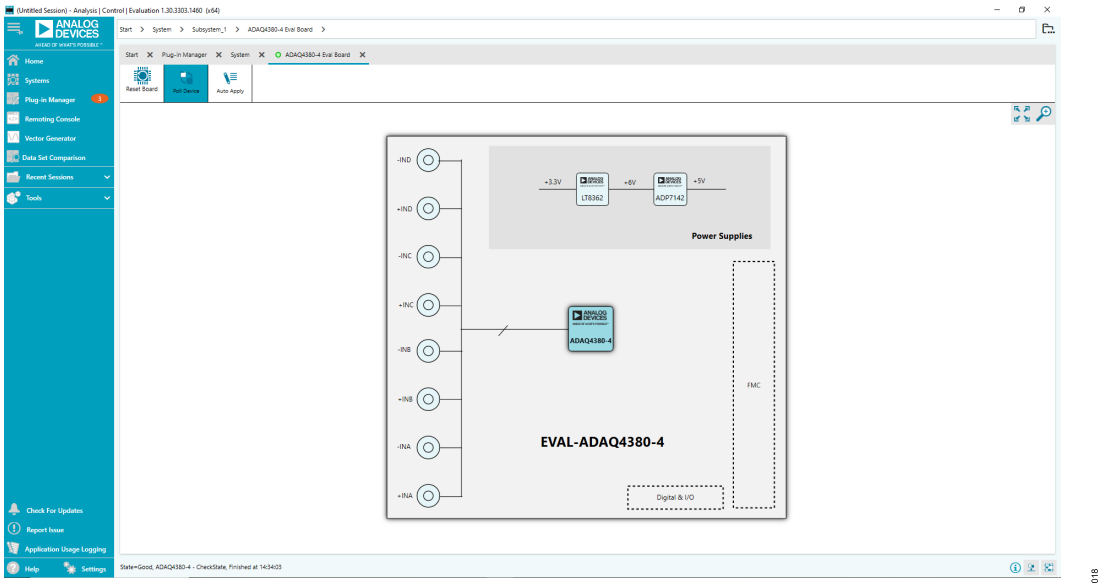

Figure 18. EVAL-ADAQ4380-4 Board View Window

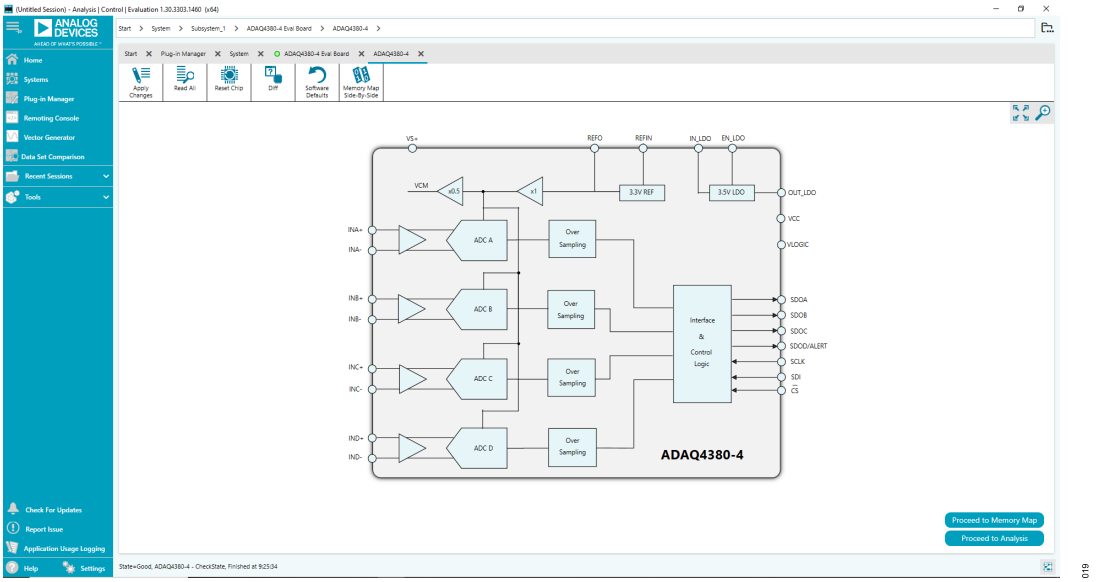

Figure 19. ADAQ4380-4 Chip View Window

ACE SOFTWARE OPERATION

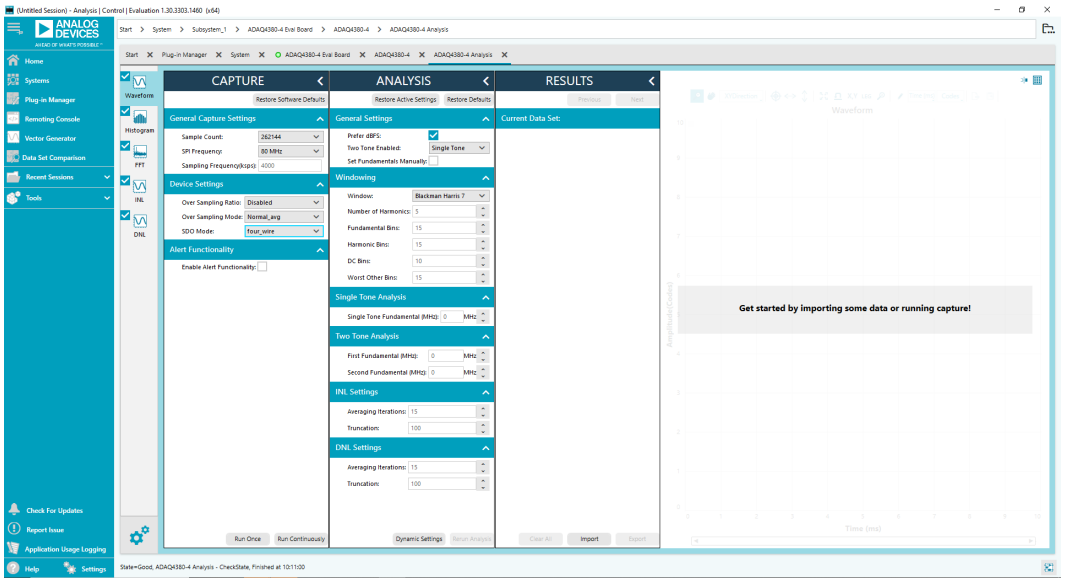

Figure 20. ADAQ4380-4 Analysis View Window

ACE SOFTWARE OPERATION

EXITING THE SOFTWARE

To exit the software, click **File** icon on the upper right tab and then click **Close ACE**.

DESCRIPTION OF THE ANALYSIS WINDOW

Click **Proceed to Analysis** in the **ADAQ4380-4**, **ADAQ4370-4**, or **ADAQ4381-4** chip view window to open the **ADAQ4380-4**, **ADAQ4370-4**, or **ADAQ4381-4** analysis view window, as shown in Figure 19. The **ADAQ4380-4**, **ADAQ4370-4**, or **ADAQ4381-4** analysis view window contains the **Waveform** (see Figure 21), **Histogram** (see Figure 22), **FFT** (see Figure 23), **INL** (see Figure 25), and **DNL** (see Figure 26) tabs.

In the **Device Settings** section, click the **SDO Mode** drop-down list and select **four_wire**. Click **Run Once** to update the register settings.

CAPTURE Pane

The **CAPTURE** pane contains the capture settings. These settings reflect onto the registers automatically before data capture.

In the **General Capture Settings** section, the **Sampling Frequency (ksps)** or **Throughput (ksps)** field allows the user to set the throughput rate of the µModule. The ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 has a maximum throughput rate of 4/2 MSPS. By default, the throughput rate is set to 2 MSPS since the **SDO Mode** in the **Device Settings** section is in **Two_wire** mode. To change that, click the drop-down list and select **four_wire** to enable maximum throughput rate.

In the **General Capture Settings** section, the **Sample Count** drop-down list allows the user to select the number of samples per capture.

The ADAQ4380-4, ADAQ4370-4, and ADAQ4381-4 have on-chip oversampling features. In the **Device Settings** section, click the **Over Sampling Mode** drop-down list to select between **Normal Average** and **Rolling Average** oversampling. Click the **Over Sampling Ratio** drop-down list to enable device oversampling. The device oversampling section can be set between 2× and 8× for rolling average oversampling, and between 2× and 32× for normal average oversampling. For the detailed explanation on the device on-chip oversampling feature, refer to the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 data sheet.

In the **CAPTURE** pane, click **Run Once** to start a data capture of the samples at the sample rate specified in the **Sample Count** drop-down list. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

In the **CAPTURE** pane, click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time, which runs the **Run Once** operation continuously.

ANALYSIS Pane

In the **ANALYSIS** pane, the **General Settings** section allows the user to set up the preferred configuration of the FFT analysis. This configuration sets the number of tones to analyze and if the fundamental is set manually (see Figure 20).

The **Windowing** section allows the user to set up the preferred **Window** type to use in the FFT analysis. This section also configures the other parameters to include in the analysis (that is, the **Number of Harmonics**, **Fundamental Bins**, **Harmonic Bins**, **DC Bins**, and **Worst Other Bins**).

The **Single Tone Analysis** and the **Two Tone Analysis** sections set up the fundamental frequencies included in the FFT analysis. When analyzing one frequency, use the **Singe Tone Analysis** section and when analyzing two frequencies, use the **Two Tone Analysis** section.

The **INL Settings** section allows the user to set the **Averaging Iterations** and **Truncation** settings during the INL measurement.

The **DNL Settings** section allows the user to set the **Averaging Iterations** and **Truncation** settings during the DNL measurement.

RESULTS Pane

The **Channels** section allows the user to select which channels to capture. The data for a specific channel is only shown if that channel is selected before the capture.

The **Results** section displays amplitude, sample frequency, and noise analysis data for the selected channels.

Click **Export** to export captured data. The waveform, histogram, and FFT data are stored in .xml files along with the values of the parameters at capture.

ACE SOFTWARE OPERATION

WAVEFORM TAB

In the **RESULTS** pane, the **Waveform Results** section displays time domain characteristics of the signal, such as **Sample Frequency**, **Sample Count**, **Min (LSB)**, **Max (LSB)**, **Range (LSB)**, **Average (LSB)**, **Rms (LSB)**, and **Transition-noise (LSB)**, as shown in Figure 21. The **CAPTURE** pane contains the **General Capture Settings**, which reflect in the registers automatically before data capture.

Waveform Graph

The data waveform graph shows each successive sample of the ADAQ4380-4, ADAQ4370-4, or ADAQ4381-4 output. The user can zoom in on and pan across the waveform using the embedded waveform tools. In the **Channels** section, select the channels to display.

Click the display units drop-down list (shown with the **Codes** option selected in Figure 21) to select whether the data graph displays in units of hexadecimal, volts, or codes. The axis controls are dynamic.

When selecting either y-scale dynamic or x-scale dynamic, the corresponding axis width automatically adjusts to show the entire range of the results after each batch of samples.

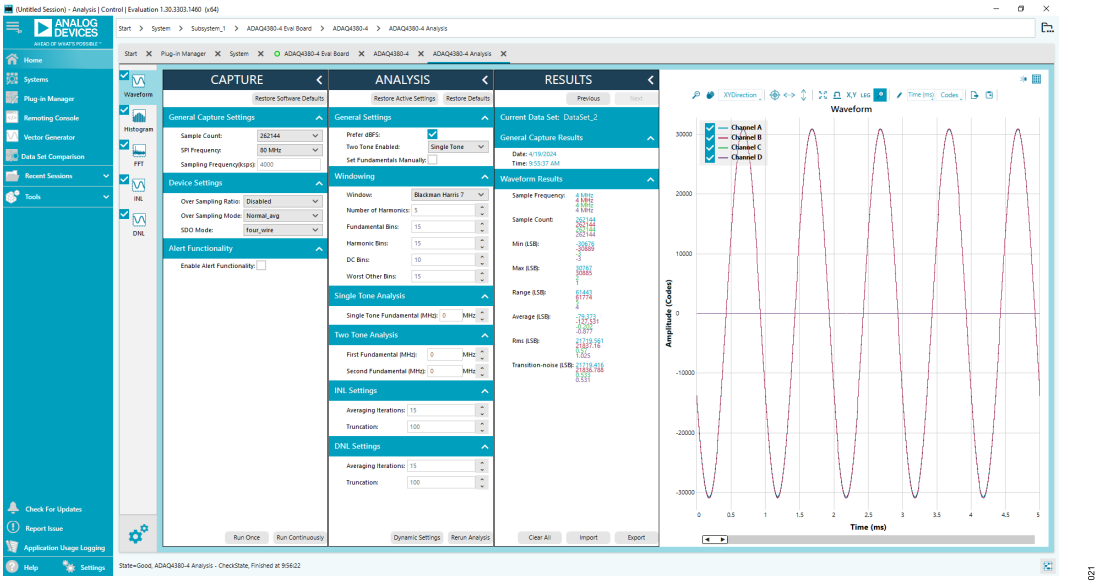

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Figure 21. EVAL-ADAQ4380-4 Waveform

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HISTOGRAM TAB

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 22.

The **RESULTS** pane displays the information related to the DC performance.

The **Histogram** graph displays the number of hits per code within the sampled data. This graph is useful for DC analysis and indicates the noise performance of the device.

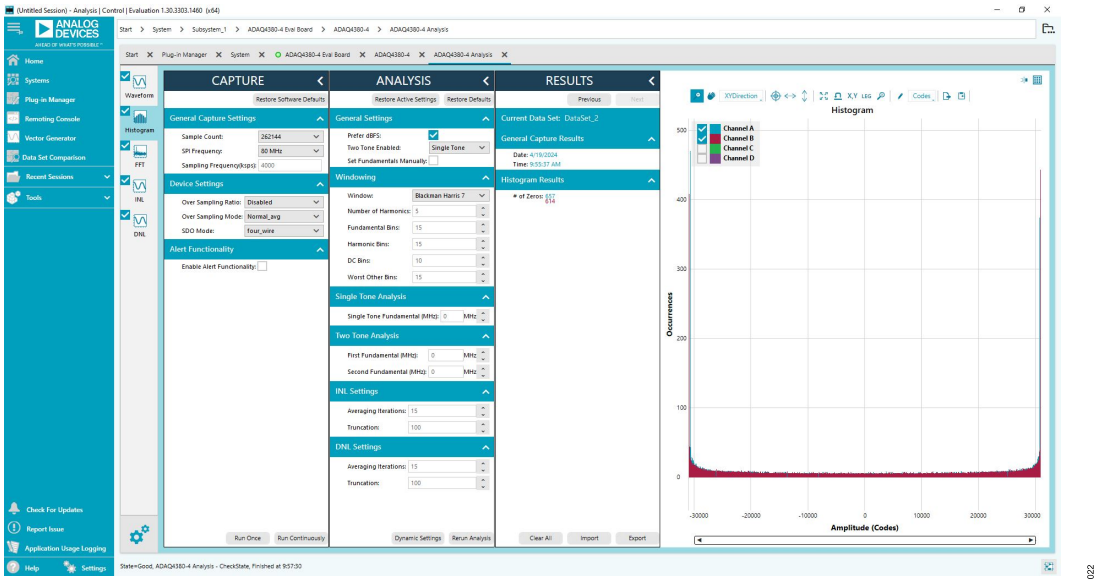

Figure 22. EVAL-ADAQ4380-4 Histogram

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FFT TAB

The **FFT** tab displays the FFT information for the last batch of samples gathered, as shown in Figure 23. The FFT also allows the oversampling function with OSR up to 8× for rolling average oversampling, as shown in Figure 24.

In the **RESULTS** pane, the **Signal** section displays the **Sample Frequency**, fundamental frequency (**Fund Frequency**), and fundamental power (**Fund Power**).

In the **RESULTS** pane, the **Noise** section displays the SNR and other noise performance results.

In the **RESULTS** pane, the **Distortion** section displays the harmonic content of the sampled signal and **DC Power** when viewing the FFT analysis.

Click the **Log** icon to display the FFT plot in logarithmic scale. Adjust the x-scale and y-scale ranges to display the frequency and amplitude of interest.

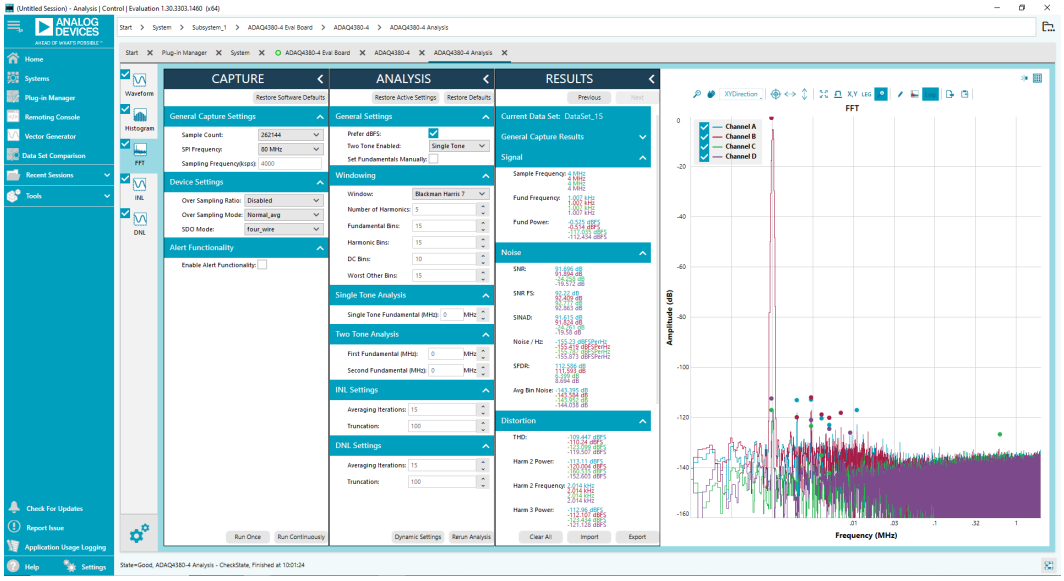

Figure 23. EVAL-ADAQ4380-4 FFT Plot

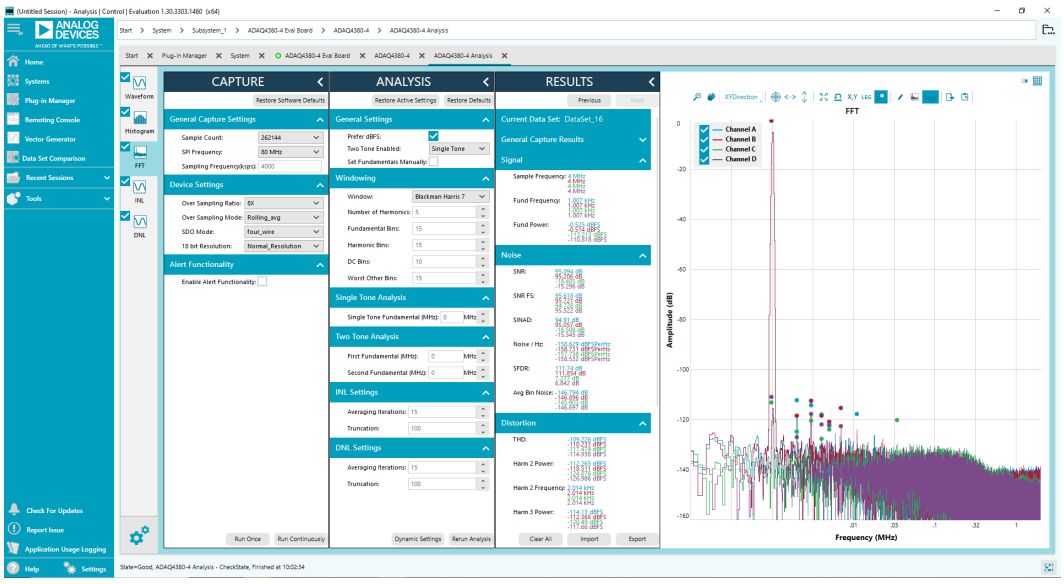

Figure 24. EVAL-ADAQ4380-4 FFT Plot with 8× Rolling Average Oversampling

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INL AND DNL TAB

The **INL** and **DNL** tab displays linearity analysis. INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

To perform a linearity test, apply a sinusoidal signal with 0.5 dB above full scale to the EV-ADAQ4380-4FMCZ, EV-ADAQ4370-4FMCZ, or EV-ADAQ4381-4FMCZ board at INA+ and INA−, INB+ and INB−, INC+ and INC−, and IND+ and IND− SMB inputs. Using a large number of averaging iterations results in more accurate INL and DNL readings but in a significant test time. Click **Run Continuously** to perform INL and DNL test.

Figure 25 and Figure 26 show the captured data that includes the ±INL and ±DNL performance of the ADAQ4380-4 taken at 50 averaging iterations.

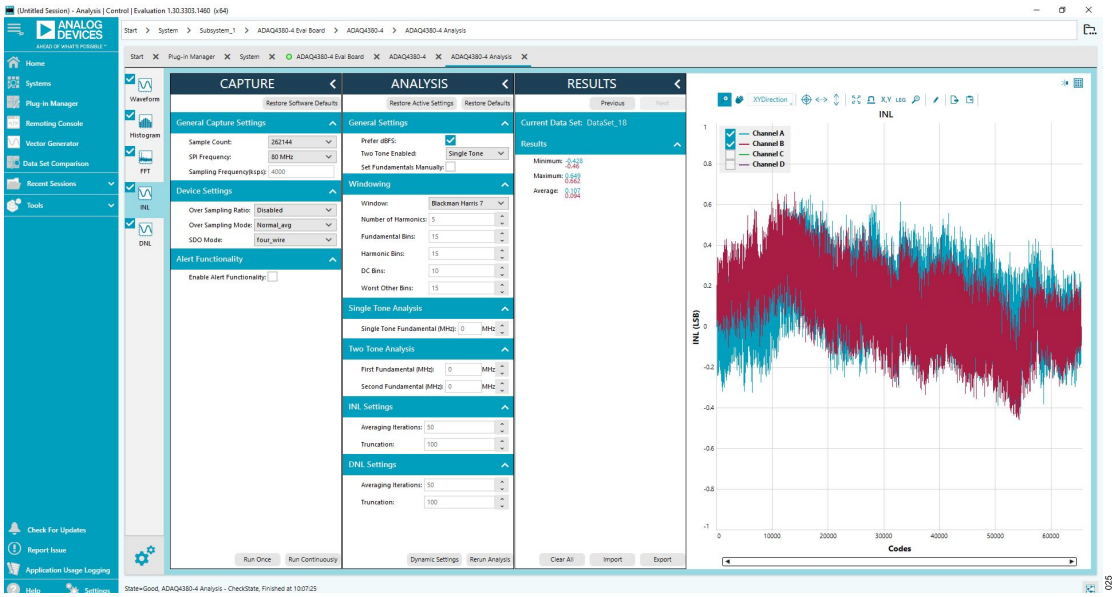

Figure 25. EVAL-ADAQ4380-4 INL

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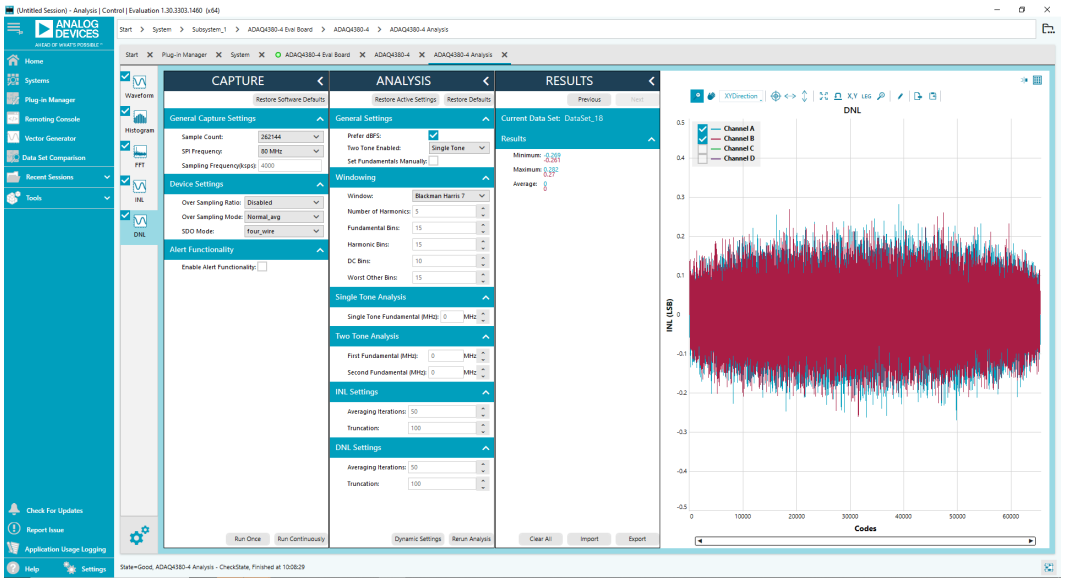

Figure 26. EVAL-ADAQ4380-4 DNL

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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