Compact, Low Power, 12-Bit, Easy Drive SAR ADC with I3C Interface

FEATURES

- Small footprint, big performance
  - INL: ±0.1 LSB maximum
  - SNR: 73.8dB with V_{REF} = 3.3V
  - 1.35nJ per conversion
  - 405μW at 300kSPS in sample mode
  - 370μW/112μW at 1MSPS/300kSPS in autonomous modes
  - 4.1μW standby power
- Versatile signal conditioning integration
  - Easy Drive features enable small, low-power AFE designs
  - Compatible with differential and single-ended signal chains
  - Wide common-mode input range
- Minimizes digital host activity and power dissipation
  - Autonomous sampling with window comparator and interrupt generation
  - Averaging filter with burst sampling support
  - Power cycling synchronization for companion devices
- 2-wire I3C Interface compatible with 1.8V to 3.3V logic
- 2.00mm × 2.6mm LFCSP and 1.67mm × 1.97mm WLCSP
- Wide operating temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered data acquisition
- Vital signs monitoring
- Biological and chemical analysis
- Geologic and seismic sensing
- Motion and robotics

GENERAL DESCRIPTION

The AD4060 is a versatile, 12-bit, successive approximation register (SAR) analog-to-digital converter (ADC) that enables low-power, high-density data acquisition solutions without sacrificing precision. This ADC offers a unique balance of performance and power efficiency, plus innovative features for seamlessly switching between high-resolution and low-power modes tailored to the immediate needs of the system. The AD4060 is ideal for battery-powered, compact data acquisition and edge sensing applications.

The Easy Drive features enable highly efficient analog front end (AFE) designs. The small sampling capacitors (3.4pF) maximize input impedance, thus reducing the dependence on high-bandwidth, power-hungry amplifiers typically required by SAR ADCs. The wide input common-mode range grants inherent support for both differential and single-ended signals.

The AD4060 supports microcontrollers with power-down modes and interrupt-driven firmware. The autonomous modes enable out-of-range event detection while the digital host sleeps. The burst averaging mode delivers on-demand, high-resolution measurements while offloading computations from the host processor. The self-timed device enable signal (DEV_EN) synchronizes AFE device power cycling to the ADC sampling instant, optimizing system power consumption while minimizing power-up settling error artifacts. The AD4060 also supports power cycling the voltage reference and using the supply as the ADC reference voltage (V_{REF}) for additional power savings.

The device configuration and ADC data readback is supported via a robust, 2-wire I3C interface with cyclic redundancy check (CRC) supported for all data transfers. The AD4060 is available in compact 14-Lead Lead Frame Chip Scale [LFCSP] and 16-Ball Wafer Level Chip Scale [WLCSP] packages and operates across a wide temperature range, making it ideal for a diverse set of applications.

FUNCTIONAL BLOCK DIAGRAM

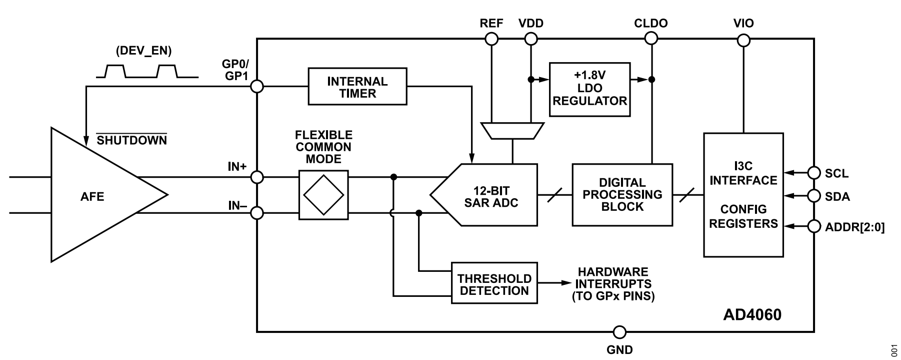

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2025—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3V to 3.6V, V_{REF} = 2.3V to 3.6V, VIO = 1.71V to 3.6V, reference capacitance (C_{REF}) = 2.2µF, and operating at the maximum specified sample rate (f_S), unless otherwise specified. All other features in default configuration, minimum and maximum values at T_A = −40°C to +125°C, and typical values at T_A = +25°C, unless otherwise specified.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION					
ADC Resolution		12			Bits
Averaging Filter Resolution	Burst averaging mode	14			Bits
Comparator Mode Resolution	Autonomous modes	12			Bits
SAMPLING DYNAMICS					
Sampling Rate (f_S)[1]				2	MSPS
Aperture Delay			0.3		ns
ANALOG INPUT					
Input Voltage (V_{IN}) Range[2]	$V_{IN} = V_{IN+} - V_{IN-}$				
	Differential mode	$-V_{REF}$		$+V_{REF}$	V
	Single-ended mode	0		$+V_{REF}$	V
Absolute Input Voltage[2]	V_{IN+}, V_{IN-}	−0.1		VDD + 0.1	V
Common-Mode Input Voltage (V_{CM}) Range[3]	$V_{CM} = (V_{IN+} + V_{IN-})/2$	−0.1		VDD + 0.1	V
Analog Input Leakage Current	IN+, IN−		6		nA
Sampling Capacitance (C_{IN})			3.4		pF
Analog Input Capacitance[4]	IN+, IN−				
Track Phase			5.4		pF
Hold Phase			2.0		pF
DC ACCURACY	V_{REF} = 3.3 V				
No Missing Codes		12			Bits
Transition Noise	Sample mode (no averaging)				
	Differential mode		0.08		LSB rms
	Single-ended mode		0.16		LSB rms
Integral Nonlinearity (INL)		−0.1	±0.03	+0.1	LSB
Differential Nonlinearity (DNL)[5]		−0.1	±0.03	+0.1	LSB
Zero Error		−900	±75	+900	µV
Zero-Error Drift			±0.05		ppm/°C
Gain Error		−0.06	±0.002	+0.06	%FS
Gain Error Drift			±0.2		ppm/°C
Total Unadjusted Error (TUE)[6]		−600	±20	+600	ppm
Autonomous Mode TUE[7]			±7		mV
REFERENCE					
V_{REF} Input Range		2.3		VDD	V
REF Standby Current	V_{REF} = 3.3V		8		nA
REF Average Input Current[8]	V_{REF} = 3.3V, f_S = 300kSPS		9	10	µA
AC PERFORMANCE	V_{REF} = 3.3V				
Total RMS Noise	Sample mode (no averaging)		476		µVrms
Signal-to-Noise Ratio (SNR)	V_{IN} = −0.5dBFS, input frequency (f_{IN}) = 1kHz				
Differential Mode	Sample mode (no averaging)		73.8		dB
Single-Ended Mode	Sample mode (no averaging)		73.5		dB
Total Harmonic Distortion (THD)	V_{IN} = −0.5dBFS, f_{IN} = 1kHz, sample mode		−105	−90	dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Signal-to-Noise and Distortion (SINAD)	V_{IN} = −0.5dBFS, f_{IN} = 1kHz, sample mode				
Differential Mode			73.8		dB
Single-Ended Mode			73.5		dB
−3dB Input Bandwidth			200		MHz
DIGITAL INPUTS					
Input Low Voltage (V_{IL})		−0.1 × VIO		+0.3 × VIO	V
Input High Voltage (V_{IH})		0.7 × VIO		1.1 × VIO	V
Input Low Current (I_{IL})		−1		+1	µA
Input High Current (I_{IH})		−1		+1	µA
Digital Input Capacitance			3		pF
DIGITAL OUTPUTS					
Output Low Voltage (V_{OL})					
SDA	Digital output current = +3mA			0.3	V
GP0, GP1	Digital output current = +500µA			0.3	V
Output High Voltage (V_{OH})					
SDA[9]	Digital output current = −3mA	VIO − 0.3			V
GP0, GP1	Digital output current = −500µA	VIO − 0.3			V
Digital Output Short-Circuit Current	VIO = 3.3V				
Sourcing	Logic high shorted to 0V		48		mA
Sinking	Logic low shorted to 3.3V		38		mA
POWER REQUIREMENTS					
VDD		2.3		3.6	V
VIO		1.71		3.6	V
POWER SUPPLY CURRENT	VDD = 3.3V				
Sleep Mode Current	f_S = 0SPS				
VDD			10		nA
VIO	VIO = 1.8V		20		nA
	VIO = 3.3V		120		nA
Standby Current	f_S = 0SPS				
VDD			990		nA
VIO	VIO = 1.8V		50		nA
	VIO = 3.3V		260		nA
VDD Active Supply Current[10]					
Sample Mode	f_S = 10kSPS		4		µA
	f_S = 300kSPS		120	160	µA
Autonomous Modes	f_S = 10kSPS		1.12		µA
	f_S = 300kSPS		34		µA
	f_S = 1MSPS		112		µA
	f_S = 2MSPS		224	300	µA
POWER DISSIPATION	VDD = VIO = 3.3V				
Sleep Mode Power Dissipation	f_S = 0SPS		430		nW
Standby Power Dissipation	f_S = 0SPS		4.1		µW
VDD Energy per Conversion			1.35		nJ
VDD Active Power Dissipation[10]					

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Sample Mode	f_S = 10kSPS		13.6		μW
	f_S = 300kSPS		405	528	μW
Autonomous Modes	f_S = 10kSPS		3.7		μW
	f_S = 300kSPS		112		μW
	f_S = 1MSPS		370		μW
	f_S = 2MSPS		740	990	μW

[1] Sampling rate specifies the maximum sample rate capabilities of the AD4060 ADC. Output data rate is the number of ADC samples that can be transmitted over the serial interface per second and is a function of the I3C interface timing specifications. In sample mode, the I3C interface bottlenecks the AD4060 output data rate to <2MSPS. In burst averaging mode and autonomous modes, the output data rate requirements are reduced, and the AD4060 ADC core can operate at the full 2MSPS. See the Calculating Serial Interface Output Data Rate section for guidelines for estimating AD4060 I3C output data rate for each operating mode.

[2] V_{IN+} and V_{IN-} represent the voltages on the IN+ and IN− pins, respectively. The AD4060 samples and converts the difference between V_{IN+} and V_{IN-}.

[3] See the Wide Input Common-Mode Range section for a detailed description of the AD4060 common-mode input voltage range.

[4] In the track phase, the total input capacitance is the sum of C_{IN} and the pin capacitance. In the hold phase, C_{IN} is disconnected from the inputs, and the input capacitance is only the pin capacitance. See Figure 40.

[5] The minimum and maximum DNL specifications are guaranteed by design.

[6] TUE is defined as the largest deviation from the ideal DC transfer function over the full input range for any individual device. TUE includes the combined effects of zero-error, gain error, and INL error for each device.

[7] Autonomous mode TUE applies to the comparator operation. See the Comparator Operation and the Autonomous Modes sections.

[8] The averaging REF input current scales linearly with f_S (see Figure 23).

[9] For push-pull operation only.

[10] VDD supply current and power dissipation scale linearly with f_s (see the VDD Power Dissipation section, Figure 26, and Figure 29).

SPECIFICATIONS

TIMING SPECIFICATIONS

VDD = V_{REF} = 2.3V to 3.6V, VIO = 1.71V to 3.6V, I3C bus capacitance (C_{BUS}) = 50pF, and all other features in default configuration. Minimum and maximum limits at T_A = −40°C to +125°C and typical values at T_A = +25°C, unless otherwise indicated.

Table 2. ADC Parameters

Parameter[1]	Symbol	Min	Typ	Max	Unit
Sampling Rate[2]	f_s			2	MSPS
Sample Period[2]	t_{CYC}	500			ns
Conversion Time	t_{CONV}		270	320	ns
Acquisition Time[3][4]	t_{ACQ}				
f_s = 2MSPS		290	327		ns
f_s = 300kSPS		3123.3	3160.3		ns
Internal Timer Frequency[5]	f_{OSC}	−15%	f_{OSC}	+15%	ns

1 The t_{CONV} specifications is production tested. All other timing specifications in this table are guaranteed by characterization and design.

2 Sampling rate specifies the maximum sample rate capabilities of the AD4060 ADC. Output data rate is the number of ADC samples that can be transmitted over the serial interface per second and is a function of the I3C interface timing specifications. In sample mode, the I3C interface bottlenecks the AD4060 output data rate to <2 MSPS. In burst averaging mode and autonomous modes, the output data rate requirements are reduced, and the AD4060 ADC core can operate at the full 2 MSPS. See the Calculating Serial Interface Output Data Rate section for guidelines for estimating AD4060 I3C output data rate for each operating mode.

3 The t_{ACQ} specification is the time available for the input sampling capacitors to acquire the input voltage for a given sample rate. The t_{ACQ} specification is equivalent to the time the ADC spends in track phase. The t_{ACQ} specification is inversely proportional to the sample rate. Therefore, the t_{ACQ} specification increases as the sample rate decreases. The minimum t_{ACQ} specification for any given sample period rate is given by the following equation:

$$t_{ACQ} = t_{CYC} - 210\text{ ns} \quad (1)$$

4 See the Device Enable Signal section for a description of acquisition time while using the DEV_EN signal to power cycle the analog front end.

5 The internal timer sets the sampling frequency in burst averaging mode and autonomous modes. The AD4060 is guaranteed to operate at the maximum f_{OSC} specification. See Table 52 for the nominal sampling frequency options.

Table 3. Open Drain Parameters

Parameter[1]	Symbol	Min	Typ	Max	Unit
SCL Low Time	t_{LOW_OD}	200			ns
SCL High Time	t_{HIGH_OD}	32			ns
SDA Fall Time	t_{FDA_OD}			4.2	ns
SDA Rise Time	t_{RDA_OD}			120	ns
SDA Data Setup Time	t_{SU_OD}	1.5			ns
Clock After Start Time	t_{CAS}	38.4			ns
Clock Before Stop Time	t_{CBP}	19.2			ns
Bus Available Condition	t_{AVAL}	1			μs

1 The t_{LOW_OD}, t_{HIGH_OD}, t_{CAS} and t_{CBP} specifications are production tested. All other timing specifications in this table are guaranteed by characterization and design.

SPECIFICATIONS

Table 4. Push-Pull Parameters

Parameter[1]	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency	f_{SCL}	0.01	12.5	12.9	MHz
SCL Clock Low Time	t_{LOW}	24			ns
SCL Clock High Time	t_{HIGH}	24			ns
SDA Data Out Hold Time	t_{HD_PP}	10			ns
SDA Data Valid Delay	t_{DSDA}			34	ns
Time Delay to Switch from Push-Pull to High-Z State	t_{SCO}			12	ns
SDA Data In Setup Time	t_{SU_PP}	1.5			ns
Clock Before Repeated Start	t_{CASr}	19.2			ns
Clock After Repeated Start	t_{CBSr}	19.2			ns

1 The t_{LOW}, t_{HIGH}, t_{CASr} and t_{CBSr} specifications are production tested. All other timing specifications in this table are guaranteed by characterization and design.

Table 5. Device Specific/Other Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Stop and Start	t_{BUF}	38			ns
IBI Delay[1]	t_{IBI_ISSUE}		28		μs
Reset Delay for Fuse Reload	$t_{RESET\_FUSE\_RELOAD}$		5		ns
Reset Delay for Peripheral Reset	$t_{RESET\_PERIPHERAL}$		60		ns

1 Time between IBI event happening and the AD4060 pulling SDA low to indicate the occurrence of an IBI event.

Timing Diagrams

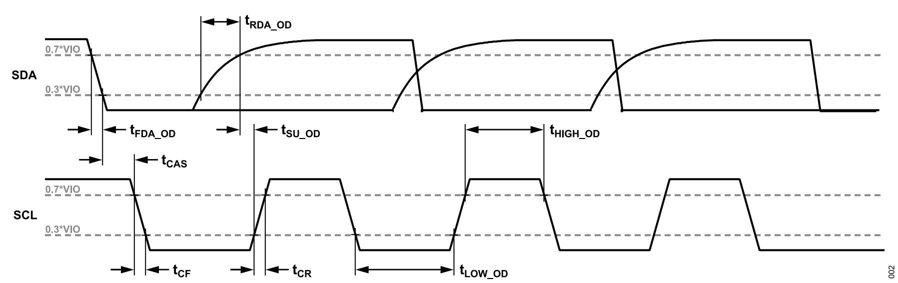


Figure 2. Open Drain Parameters

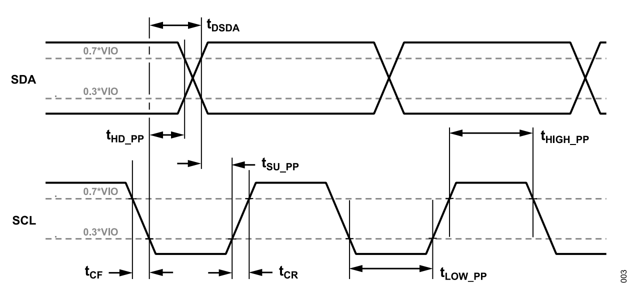


Figure 3. Push-Pull Parameters

SPECIFICATIONS

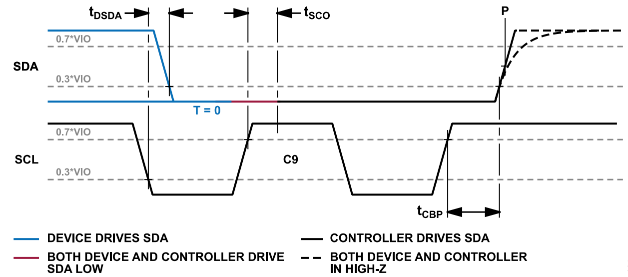


Figure 4. T-Bit When AD4060 Ends Read and Controller Generates Stop

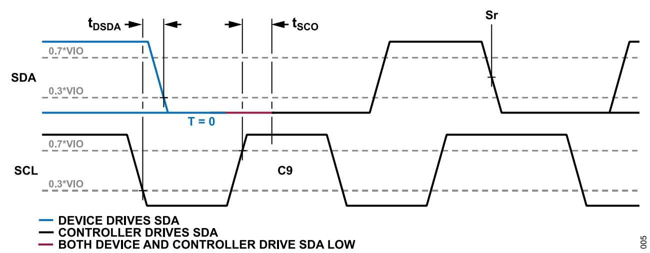


Figure 5. T-Bit When AD4060 Ends Read and Controller Generates Repeated Start

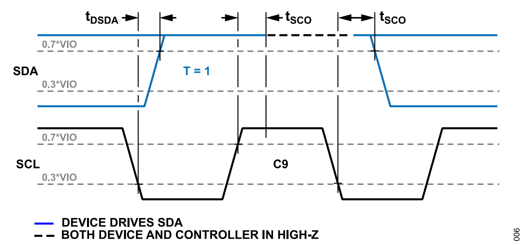


Figure 6. T-Bit When AD4060 and Controller Agree to Continue Reading Message

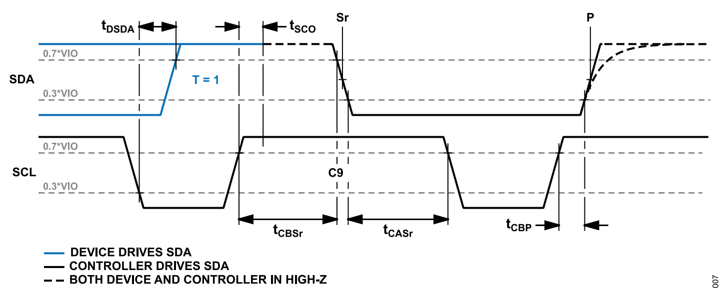


Figure 7. T-Bit When Controller Ends Read With Repeated Start and Stop

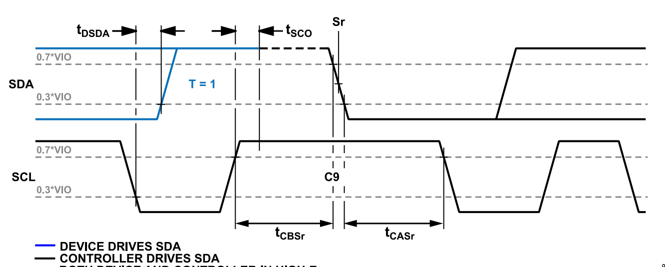


Figure 8. T-Bit When Controller Ends Read Via Repeated Start and Further Transfer

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
IN+, IN−, and REF to GND	−0.3V to VDD + 0.3V
Supply Voltages	
VDD and VIO to GND	−0.3V to +3.96V
CLDO to GND	−0.3V to +2.1V
Digital Inputs to GND	−0.3V to VIO + 0.3V
Digital Outputs to GND	−0.3V to VIO + 0.3V
Temperature	
Storage	−55°C to +150°C
Operating T_J Range	−40°C to +125°C
Maximum Reflow (Package Body)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Unit
CP-14-7	73.9	52.3	°C/W
CB-16-26	49.6	0.6	°C/W

1 Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB.

2 θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

3 θ_{JC} is the junction-to-case thermal resistance.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

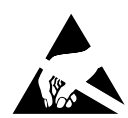
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4060

Table 8. AD4060, 14-Lead LFCSP and 16-Ball WLCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	4	3A
FICDM	1.25	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

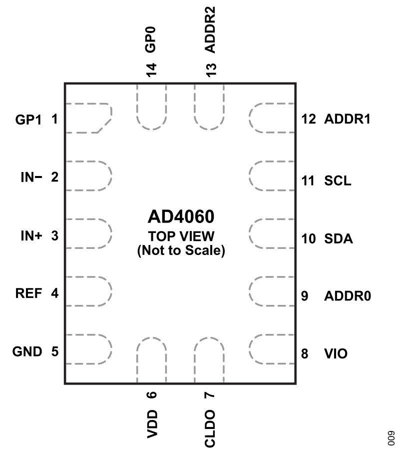


Figure 9. AD4060 LFCSP Pin Configuration

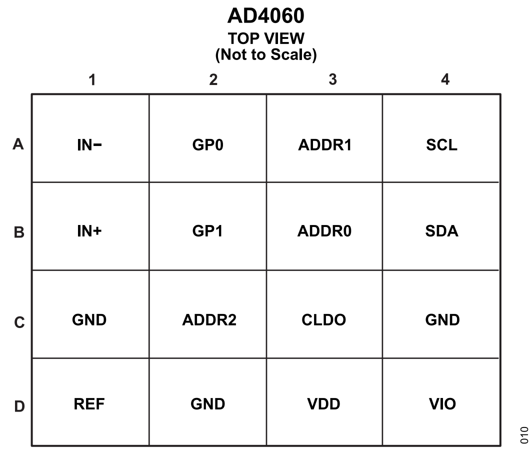


Figure 10. AD4060 WLCSP Pin Configuration

Table 9. AD4060 LFCSP and WLCSP Pin Function Descriptions

LFCSP Pin No.	WLCSP Pin No.	Mnemonic	Type	Description
1	B2	GP1	DO	General Purpose Output 1. The GP1 pin is a digital output that can be configured as multiple device interrupt signals. See the Interrupts and Control Signals section.
2	A1	IN−	AI	Negative Analog Input. See the Analog Inputs section.
3	B1	IN+	AI	Positive Analog Input. See the Analog Inputs section.
4	D1	REF	AI	Reference Input. Decouple the REF pin with a 2.2μF capacitor to GND. See the Voltage Reference section.
5	C1, C4, D2	GND	P	Power Supply Ground.
6	D3	VDD	P	Analog Power Supply. Decouple the VDD pin with a 1μF capacitor to GND. The VDD pin is also the input to the +1.8V internal LDO regulator that supplies the CLDO pin supply voltage. See the Power Supplies section.
7	C3	CLDO	P	ADC Core Power Supply. The CLDO pin is powered by the +1.8 V internal low-dropout (LDO) regulator. Decouple the CLDO pin with a 1μF capacitor to GND. See the Power Supplies section.
8	D4	VIO	P	Logic Voltage Supply. The VIO pin sets the logic voltage levels for digital inputs and digital outputs. Decouple the VIO pin with a 1μF capacitor to GND. See the Power Supplies section.
9	B3	ADDR0	DI	Address 0 Input. Sets Bit[0] of the part instance in 48-bit provisional ID. See the Table 19 section.[1]
10	B4	SDA	DI/DO	Serial Data I/O
11	A4	SCL	DI	Serial Data Clock Input.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. AD4060 LFCSP and WLCSP Pin Function Descriptions (Continued)

LFCSP Pin No.	WLCSP Pin No.	Mnemonic	Type	Description
12	A3	ADDR1	DI	Address 1 Input. Sets Bit[1] of the part instance in 48-bit provisional ID. See the Table 19 section.[1]
13	C2	ADDR2	DI	Address 2 Input. Sets Bit[2] of the part instance in 48-bit provisional ID. See the Table 19 section.[1]
14	A2	GP0	DO	General Purpose Output 0. The GP0 pin is a digital output that can be configured as multiple device control or interrupt signals. See the Interrupts and Control Signals section.

[1] The ADDR[2:0] pins enable the assignment of up to eight unique part instance values to support up to eight AD4060 devices on one I3C bus.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 3.3V, V_{REF} = 3.3V, VIO = 3.3V, C_{REF} = 2.2µF, maximum f_S, T_A = 25°C, and all features in default configuration, unless otherwise specified.

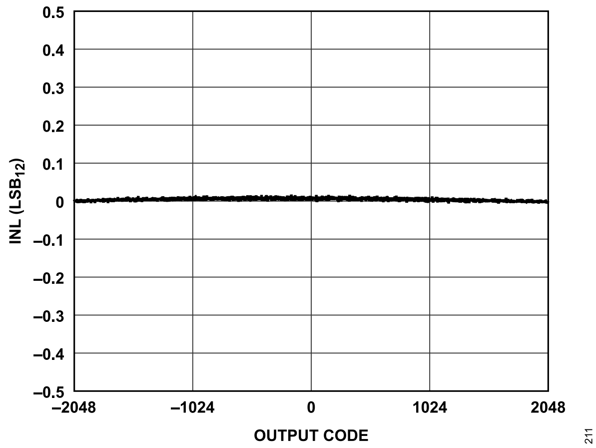


Figure 11. INL vs. Output Code

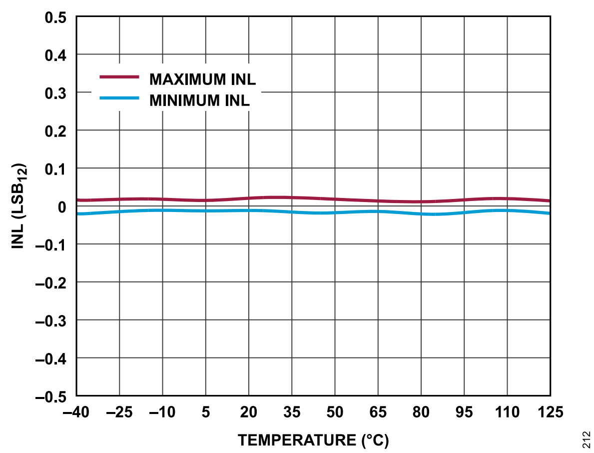


Figure 12. INL vs. Temperature

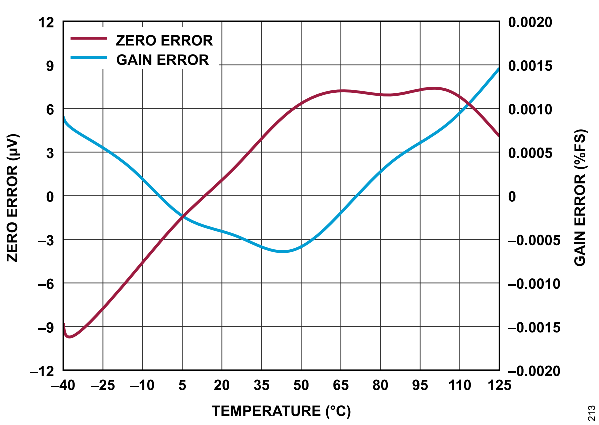


Figure 13. Zero Error and Gain Error vs. Temperature

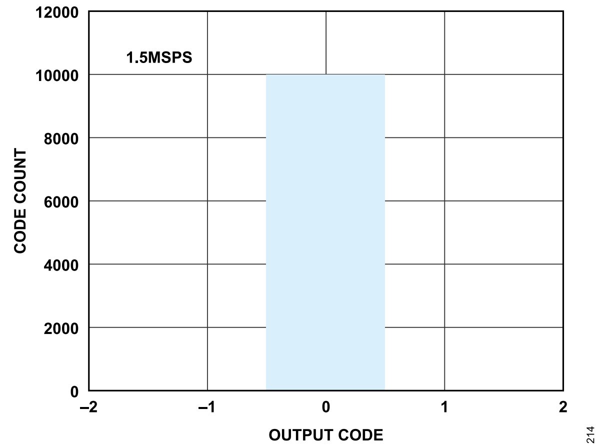


Figure 14. Histogram, Sample Mode (No Averaging)

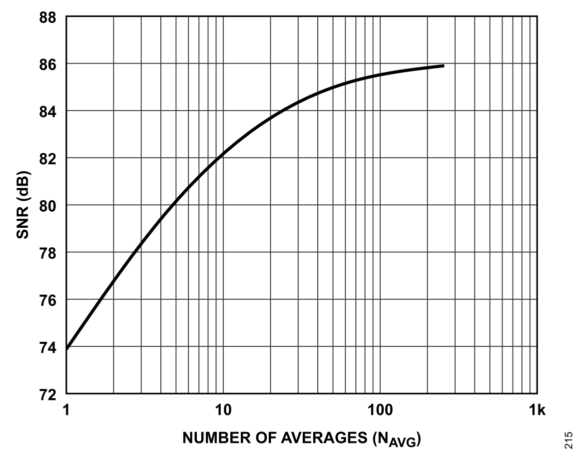


Figure 15. SNR vs. Number of Averages

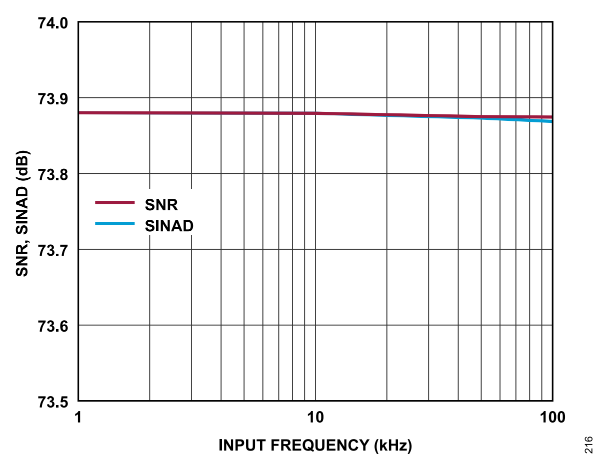


Figure 16. SNR, SINAD vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

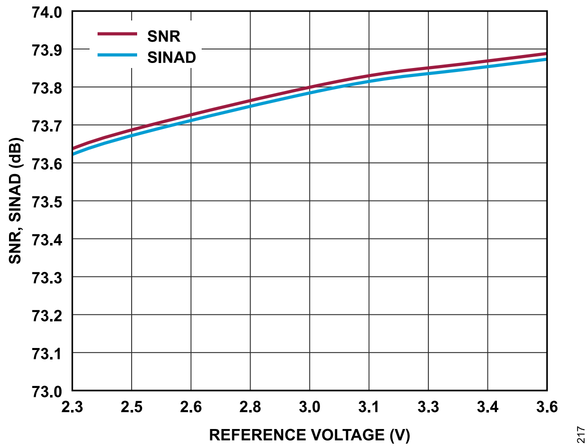


Figure 17. SNR, SINAD vs. Reference Voltage

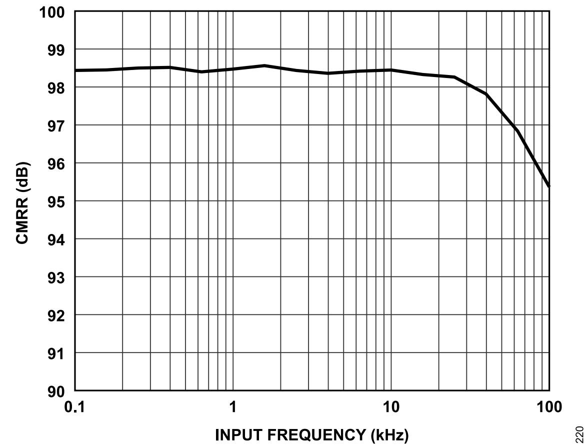


Figure 20. Common-Mode Rejection Ratio (CMRR) vs. Input Frequency

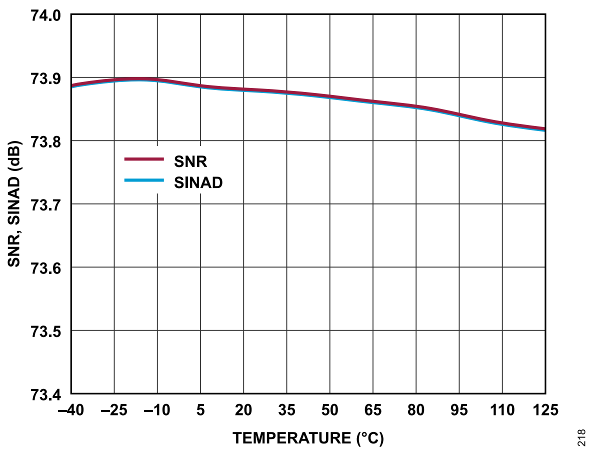


Figure 18. SNR, SINAD vs. Temperature

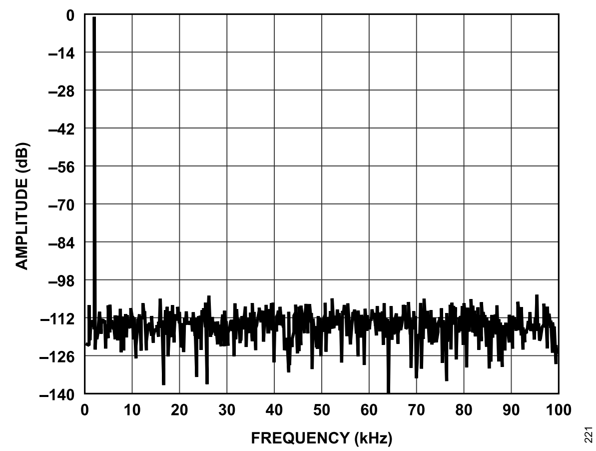


Figure 21. Fast Fourier Transform (FFT), f_S = 200kSPS, f_{IN} = 1kHz

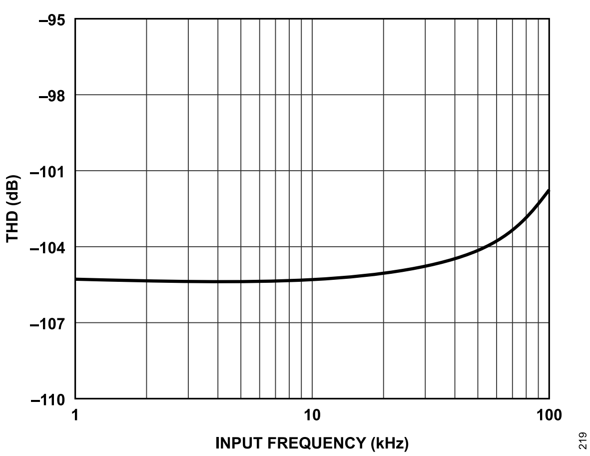


Figure 19. THD vs. Input Frequency, V_{IN} = −1dBFS

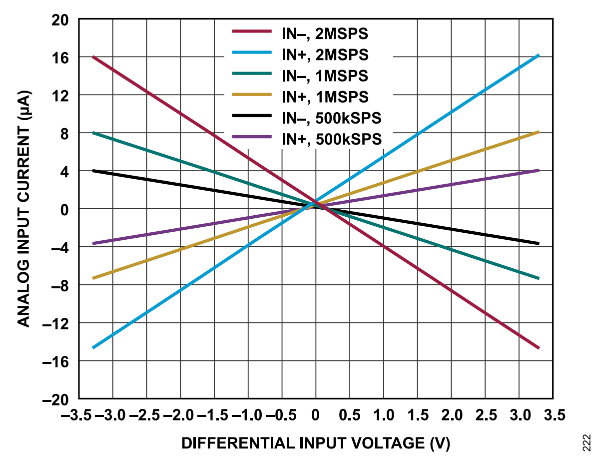


Figure 22. Analog Input Current vs. Differential Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

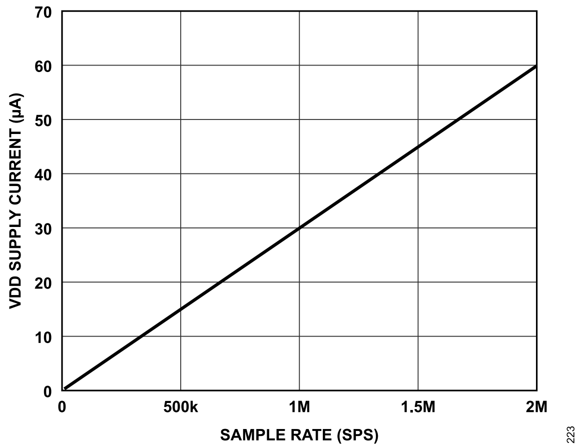


Figure 23. Reference Input Current vs. Sample Rate

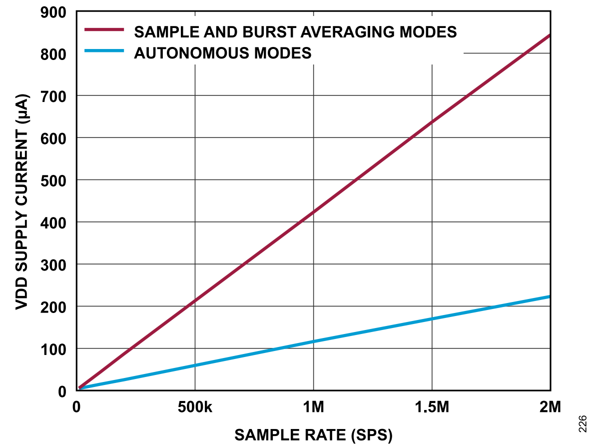


Figure 26. VDD Supply Current vs. Sample Rate

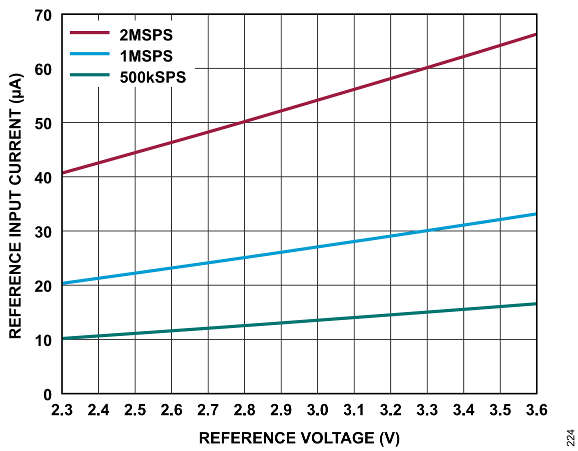


Figure 24. Reference Input Current vs. Reference Voltage

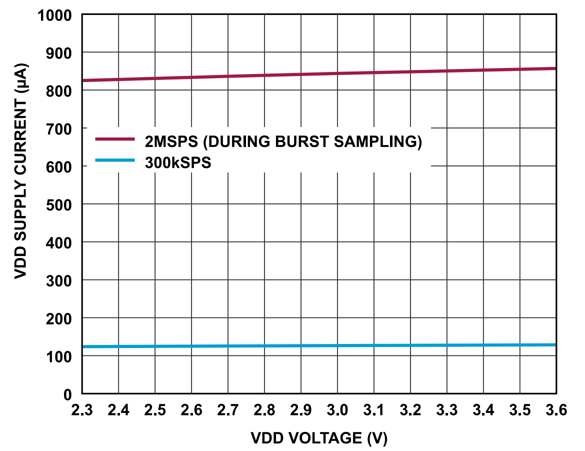


Figure 27. VDD Supply Current vs. VDD Voltage

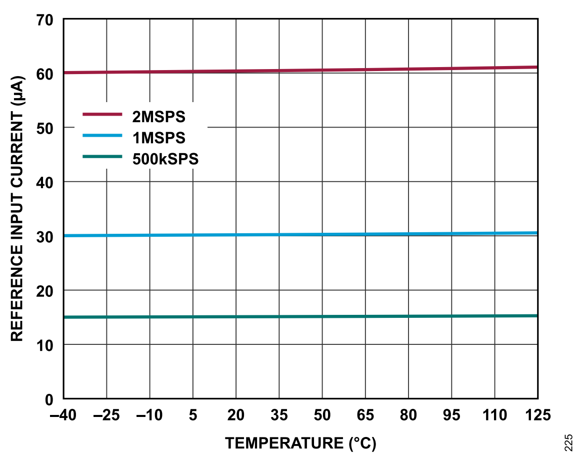


Figure 25. Reference Input Current vs. Temperature

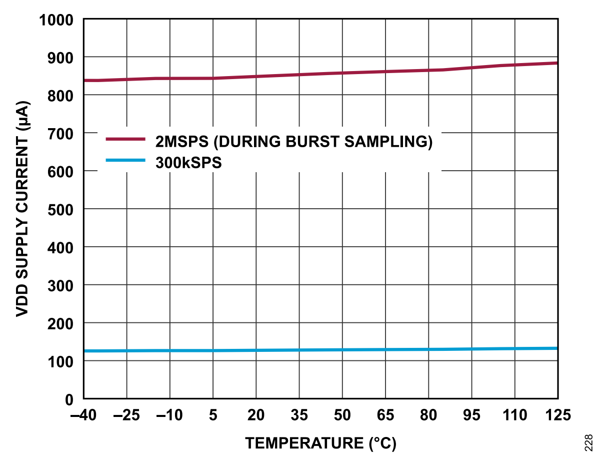


Figure 28. VDD Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

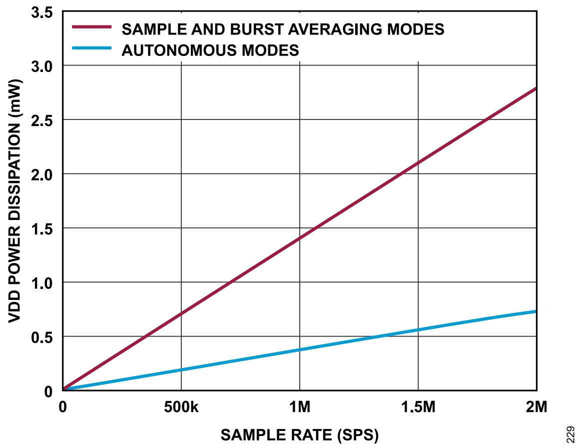


Figure 29. VDD Power Dissipation vs. Sample Rate

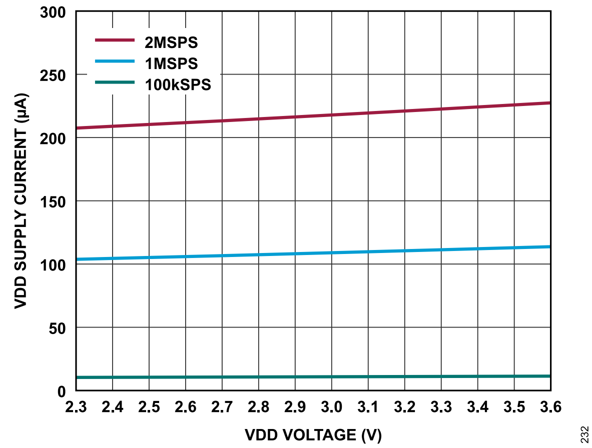


Figure 32. VDD Supply Current vs. VDD Voltage (Autonomous Modes)

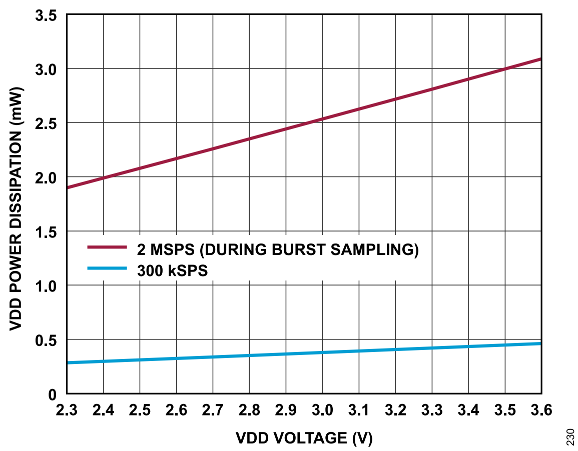


Figure 30. VDD Power Dissipation vs. VDD Voltage

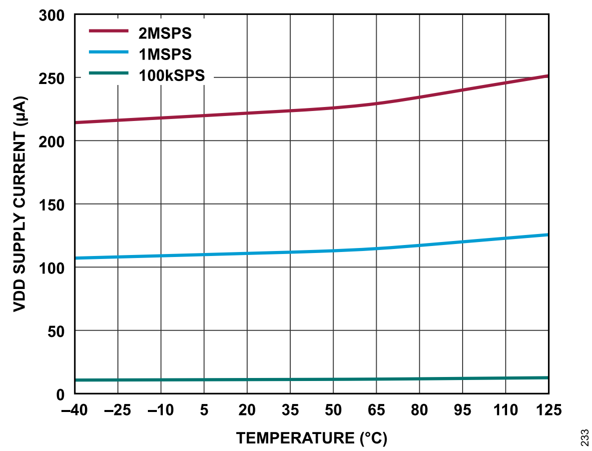


Figure 33. VDD Supply Current vs. Temperature (Autonomous Modes)

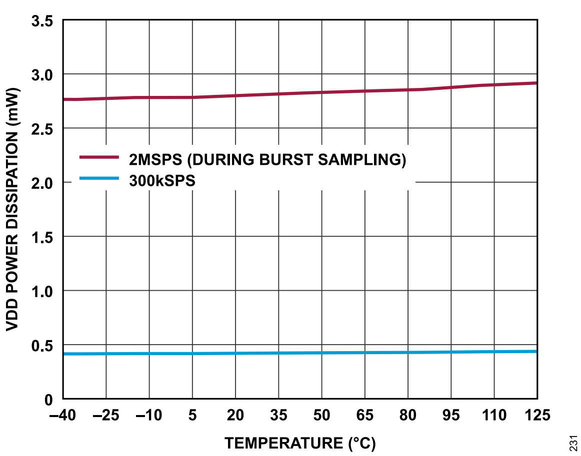


Figure 31. VDD Power Dissipation vs. Temperature

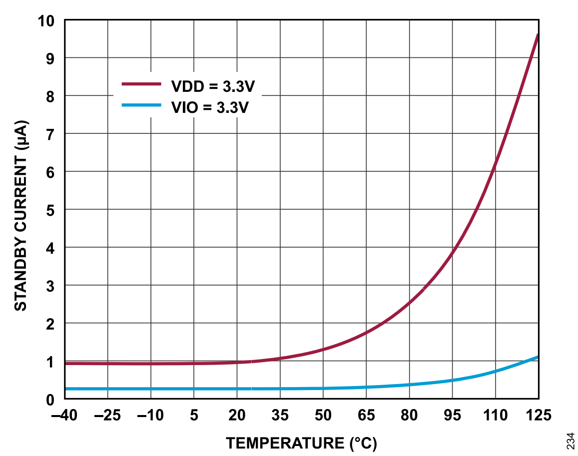


Figure 34. Standby Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

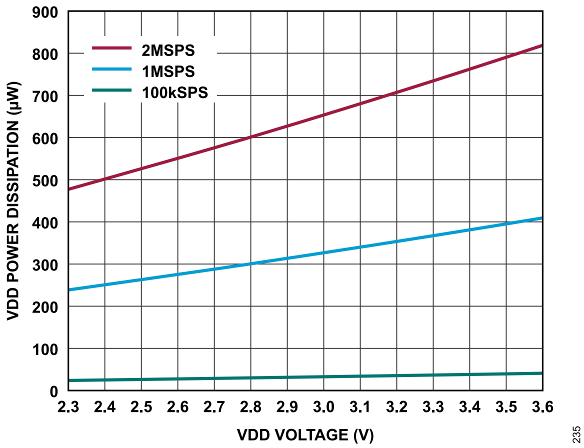


Figure 35. VDD Power Dissipation vs. VDD Voltage (Autonomous Modes)

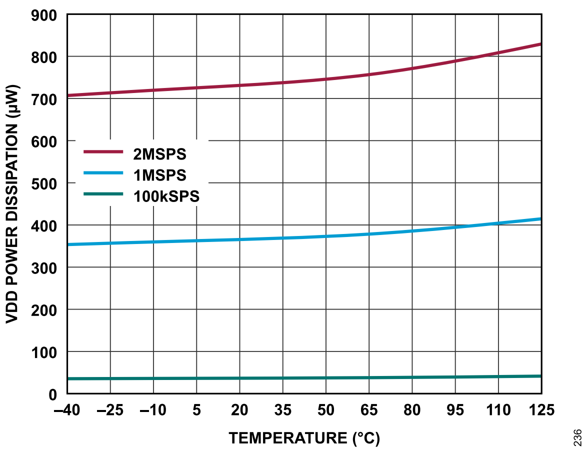


Figure 36. VDD Power Dissipation vs. Temperature (Autonomous Modes)

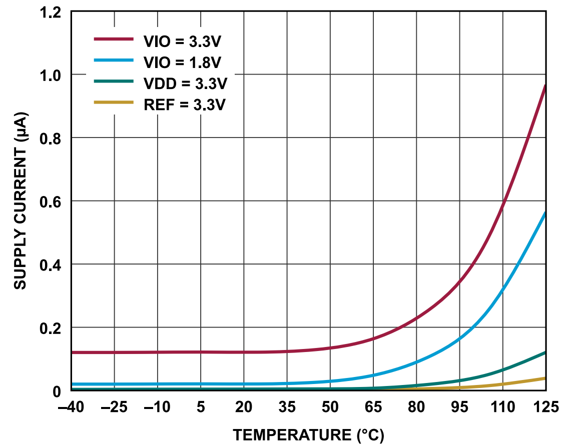


Figure 37. Supply Current (Sleep Mode) vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL) Error

INL is the deviation of each individual code from a line drawn from the negative full scale through the positive full scale. The point used as the negative full scale occurs ½ LSB before the first code transition. The positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from each code center to the true straight line.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error (ZE)

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Gain Error (GE)

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above the nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Total Unadjusted Error (TUE)

TUE is the worst-case measured deviation from the ideal ADC transfer function over the full input range, specified in ppm of full-scale. TUE includes the combined effects of zero error, gain error, and INL error for any given device.

Dynamic Range (DR)

Dynamic range is the RMS voltage of a full-scale sine wave to the total RMS voltage of the noise measured. The value for dynamic range is expressed in decibels. Dynamic range is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the RMS amplitude of a full-scale input signal and the peak spurious signal.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS voltage of a full-scale sine wave to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonic components to the RMS value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the RMS voltage of a full-scale sine wave to the RMS sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value of SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD as follows:
ENOB = (SINAD dB − 1.76)/6.02.
ENOB is expressed in bits.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a −1 dBFS sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR(dB) = 10 \times \log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

Aperture Delay

Aperture delay is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

THEORY OF OPERATION

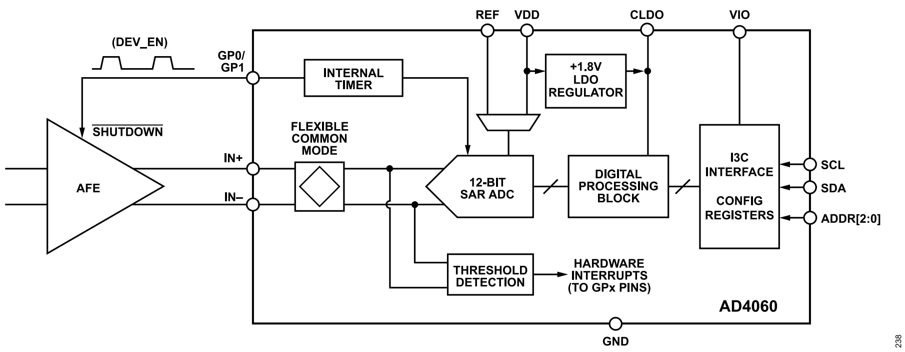


Figure 38. AD4060 Functional Block Diagram

OVERVIEW

The AD4060 is a compact, ultra-low power, 12-bit, Easy Drive SAR ADC. The AD4060 feature set eases the design of low-power precision measurement systems by reducing the AFE design constraints and minimizing the digital host overhead. The low input capacitance and wide common-mode input range broaden the selection of compatible AFE components, allowing for simpler and lower power signal chain solutions. The block averaging filter provides noise reduction while offloading computations from the host processor. The internal timer block enables autonomous monitoring modes, burst sampling, and device power cycling controls synchronized to the ADC sampling instant. Various hardware interrupts allow the digital host to sleep between user-defined events.

The AD4060 offers a unique balance of performance and power efficiency, with 73.8dB of SNR and guaranteed INL of ±0.1 LSBs at only 1.35nJ per conversion. The AD4060 only consumes 2.7mW at 2MSPS when operated on a single 3.3V supply. The power dissipation scales linearly with sample rate for the AD4060 (see Figure 29). The devices consume 4.1μW standby power while not performing conversions. A sleep mode is available to further reduce standby power to 430nW during long periods of idle operation.

The AD4060 features 2-wire I3C with CRC for device configuration and ADC data readback, and the I3C is compatible with 1.8V to 3.3V logic levels.

The AD4060 has several operating modes, each optimized for either high precision measurement or power-efficient signal monitoring. The Theory of Operation section describes the AD4060 functional blocks, and the Modes of Operation section describes the utilization of the functional blocks in each operating mode. The Serial Interface section describes the I3C protocols for accessing configuration registers and ADC data. The AD4060 Register Summary section documents the configuration registers.

CONVERTER OPERATION

The AD4060 operates in two phases, the acquisition phase and the conversion phase. In the acquisition phase, the internal track-and-hold circuitry is connected to each input pin (IN+ and IN−) and acquires the voltage on each pin independently. The AD4060 remains in the acquisition phase until the CONV_READ or CONV_TRIGGER register initiates a conversion. At the start of the conversion phase, the track-and-hold circuitry samples the acquired analog input signal, and the SAR ADC core generates a corresponding 12-bit digital code. The conversion phase ends when the 12-bit conversion result is ready, which is given by the t_{CONV} specification in ADC Timing Specifications. The AD4060 acquisition and conversion phases overlap to maximize acquisition time (t_{ACQ}).

In sample mode and burst averaging mode, the conversions are initiated by accessing either the CONV_READ or the CONV_TRIGGER registers (see the Register Address Pointer, CONV_READ Register, and CONV_TRIGGER Register sections for more detail).

The AD4060 offers several modes where the convert start is triggered by an internal oscillator, including the autonomous modes. Refer to the Modes of Operation section for specific ADC timing information for each of the relevant operating modes.

Transfer Function

Figure 39 shows the ideal transfer function of the AD4060 SAR ADC core. The AD4060 encodes the sampled voltage difference between IN+ and IN− as a fraction of the full-scale range (FSR) into a 12-bit digital code. The unit of 1 LSB refers to the smallest discrete voltage step that can be resolved by the ADC and is a function of the V_{REF} voltage. In burst averaging mode, the block averaging filter averages multiple 12-bit samples into one 14-bit code. Table 10 and Table 11 summarize the mapping of input voltages to digital output codes.

THEORY OF OPERATION

Following the conversions, the ADC data are stored in the CONV_READ and CONV_TRIGGER registers. CONV_READ and CONV_TRIGGER are accessed in 8-bit segments via the I3C Interface. (See the CONV_READ Register and CONV_TRIGGER Register sections for more detail.)

As described in the Wide Input Common-Mode Range section, the AD4060 supports arbitrary input common-mode voltages, therefore the devices inherently support both differential and single-ended type signals. The AD4060 supports both twos complement (signed) and straight binary (unsigned) formats to map either differential signals or single-ended signals to the full 12-bit ADC transfer function. The DATA_FORMAT bit in the ADC_MODES register selects between the differential mode and single-ended mode transfer functions as seen in Table 10 and Table 11.

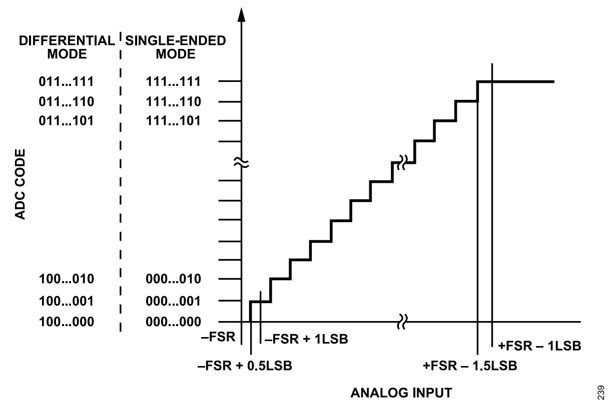


Figure 39. ADC Ideal Transfer Function

Table 10. ADC Input Voltage to Output Code Mapping (Sample Mode)

	Differential Mode		Single-Ended Mode	
Description	V_{IN}	Digital Output Code	V_{IN}	Digital Output Code
FSR − 1 LSB	(2047/2048) × V_{REF}	0x7FF	(4095/4096) × V_{REF}	0xFFF
...	...	...	...	...
Midscale + 1 LSB	(1/2048) × V_{REF}	0x001	(2049/4096) × V_{REF}	0x801
Midscale	0 V	0x000	(½) × V_{REF}	0x800
Midscale − 1 LSB	−(1/2048) × V_{REF}	0xFFF	(2047/4096) × V_{REF}	0x7FF
...	...	...	...	...
−FSR + 1 LSB	(−2047/2048) × V_{REF}	0x801	(1/2048) × V_{REF}	0x001
−FSR	$-V_{REF}$	0x800	0 V	0x000

Table 11. ADC Input Voltage to Output Code Mapping (Burst Averaging Mode)

	Differential Mode		Single-Ended Mode	
Description	V_{IN}	Digital Output Code	V_{IN}	Digital Output Code
FSR − 1 LSB	(8191/8192) × V_{REF}	0x1FFF	(16383/16384) × V_{REF}	0x3FFF
...	...		...	...
Midscale + 1 LSB	(1/8192) × V_{REF}	0x0001	(8193/16384) × V_{REF}	0x2001
Midscale	0 V	0x0000	(½) × V_{REF}	0x2000
Midscale − 1 LSB	(−1/8192) × V_{REF}	0xFFFF	(8191/16384) × V_{REF}	0x1FFF
...	...	...	...	...
−FSR + 1 LSB	(−8191/8192) × V_{REF}	0x2001	(1/16384) × V_{REF}	0x0001
−FSR	$-V_{REF}$	0x2000	0 V	0x0000

THEORY OF OPERATION

ANALOG INPUTS

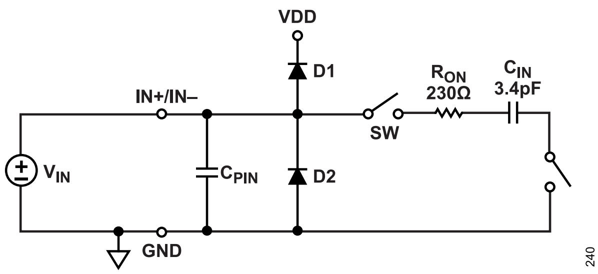


Figure 40. Equivalent Analog Input Circuit

Figure 40 shows an equivalent circuit for each of the AD4060 analog inputs (IN+ and IN−). The analog inputs are modeled as a switched capacitive load. During the acquisition phase, the sampling switch (SW) connects each input pin to the 3.4pF sampling capacitor (C_{IN}) in series with the 230Ω switch on resistance (R_{ON}). During the conversion phase, SW disconnects to sample the voltages on the IN+ and IN− pins onto the sampling capacitors. D1 and D2 represent the ESD diodes from the IN+ and IN− pins to the VDD supply and GND, respectively. C_{PIN} represents the pin capacitance of each input pin to GND and is typically 2pF.

See the AD4060 Equivalent Analog Input Model section for more information on the effective loading characteristics of the AD4060 analog inputs.

Easy Drive Features

The AD4060 Easy Drive analog inputs are designed to enable compact, low-power precision signal chains by minimizing dependence on specialized high-speed, low-noise, high-power ADC driver amplifiers. The small sampling capacitors minimize the transient current glitches typical of SAR ADCs, and the long acquisition phase maximizes the settling time—even at high sample rates. The RC kickback filter uses smaller capacitors and larger resistors, alleviating amplifier stability concerns and enabling the use of tiny passive components (for example, 0201 NP0/C0G capacitors). These Easy Drive features ensure the AD4060 interface with front-end circuits with high output impedance without incurring settling errors, expanding compatibility with low-power amplifiers and sensors (see the Analog Front-End Design section).

The AD4060 is available in the LTspice component library and support cosimulation with a wide variety of companion amplifiers. The LTspice model emulates the input-referred noise spectral density and input transient loading for system noise and settling accuracy simulations.

VOLTAGE REFERENCE

The V_{REF} voltage sets the ADC FSR (see the Transfer Function section). The AD4060 V_{REF} range is 2.3 V to VDD, where the maximum VDD supply voltage is 3.6 V (see Table 1).

The V_{REF} voltage is polled during the SAR bit trials to determine the ADC output code. During the bit trials, the SAR core exhibits transient charge draw. To ensure the V_{REF} voltage remains stable during the SAR bit trials, place a 2.2 µF decoupling capacitor as close to the REF pin as possible. Lower decoupling capacitance values (for example, 1 µF) may be used with slight performance degradations. See the Reference Circuit Design section for more recommendations for pairing voltage references with the AD4060.

Reference Selection Modes

The AD4060 V_{REF} voltage can be sourced from either the REF input pin or the VDD supply pin. By default, the REF pin acts as the V_{REF} source, and this setting is the intended mode to achieve the performance specifications given in Table 1. The VDD supply option is provided to support low-power measurements where accuracy is not critical or to allow the system to power cycle the voltage reference for long periods of time to save system power. The V_{REF} source option is controlled with the REF_SEL bit in the ADC_CONFIG register (see Table 48).

The AD4060 includes an automated gain scaling function, where the ADC core samples the REF voltage as a fraction of the VDD supply voltage and stores the appropriate gain scaling value into the MON_VAL register, such that using VDD as the V_{REF} source has the same ADC transfer function as REF. This allows the system to power down the voltage reference circuitry for extended periods of time with similar levels of performance. See the Achieving High Accuracy with Reference Shutdown section for a detailed description of the automated gain scaling feature.

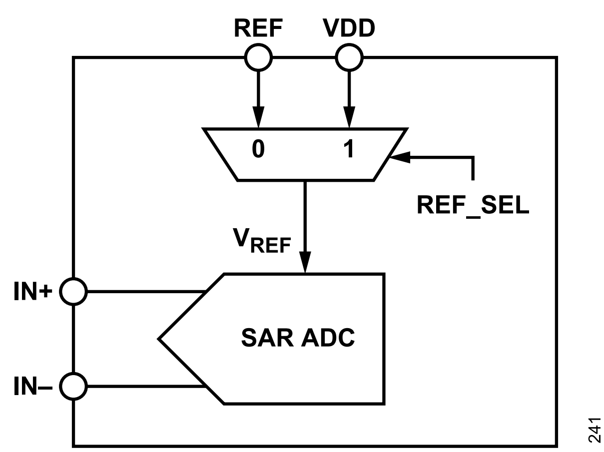


Figure 41. Reference Source Selection

THEORY OF OPERATION

DIGITAL PROCESSING FEATURES

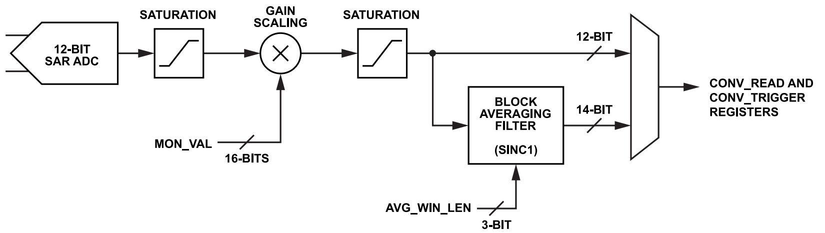


Figure 42. AD4060 Digital Processing Functionality

The AD4060 includes several data processing features that can be applied to ADC data to offload computations from the digital host processor. Figure 42 shows a block diagram of the available data processing functions. Functionality and configuration of each block is described in detail in following sections. Note that these digital processing functions are not used in the autonomous modes.

Gain Scaling

The gain scaling function applies a 16-bit unsigned digital gain factor to the 12-bit ADC results. Gain scaling can be applied to calibrate out system gain error. The gain scaling factor is set by the MON_VAL bit field in the MON_VAL scaling register with the following equation:

$$Code_{OUT} = Code_{IN} \times \left({}^{MON\_VAL}/_{0x8000}\right) \qquad (2)$$

where 0x0000 ≤ MON_VAL ≤ 0xFFFF, giving an effective gain range of 0 to 1.99997.

Gain scaling can also be used to scale the ADC transfer function when using the VDD supply as the V_{REF} source (see the Reference Selection Modes section). The AD4060 can be configured to measure the ratio of the VDD supply and the REF input voltage and automatically adjust the MON_VAL register value to set the transfer functions to be the same. The external voltage reference circuitry can then be powered down to reduce system power dissipation. See the Achieving High Accuracy with Reference Shutdown section for more information.

Note that applying gain to the samples can cause numerical saturation when $Code_{OUT}$ in Equation 2 exceeds the 12-bit full scale (see the Full-Scale Saturation section). Ensure the MON_VAL bit field is set accordingly to prevent the gain scaling block output from saturating.

Gain scaling is disabled by default and enabled by setting the SCALE_EN bit field in the ADC_CONFIG register to 1 (see Table 48).

Full-Scale Saturation

The conversion results saturate digitally (prior to any data processing) when the sampled analog input voltage exceeds the input range limits specified in Table 1. The AD4060 includes saturation blocks at the output of the ADC core and the output of the gain scaling block that detect when the digital output codes or the ADC core and gain scaling block reach the maximum or minimum values, respectively.

The OVER_RNG_ERR and UNDER_RNG_ERR flags in the DEVICE_STATUS register are set when either of the saturation blocks detect a maximally or minimally saturated code. In differential mode, the 12-bit results saturate maximally at 0x7FF and minimally at 0x800. In single-ended mode the 12-bit results saturate maximally at 0xFFF and minimally at 0x000. (See the Transfer Function section for a description of differential and single-ended modes.)

The OVER_RNG_ERR and UNDER_RNG_ERR flags can be periodically polled when using the block averaging filter to verify none of the filter input data has saturated. The OVER_RNG_ERR and UNDER_RANGE_ERR flags are write-1-to-clear bits and, therefore, hold their states until the digital host is able to poll them.

Block Averaging Filter

The AD4060 includes a block averaging filter with programmable averaging ratios (N_{AVG}) from 2 to 256. The block averaging filter is automatically enabled when the device is in burst averaging mode. The block averaging filter exhibits a SINC1 frequency response. Figure 43 shows the frequency response of the averaging filter for N_{AVG} of 2, 4, 8, 16, and 32.

When enabled, the block averaging filter accumulates a block of 12-bit ADC results before generating a 14-bit averaged result. N_{AVG} refers to the number of ADC samples per averaged result. The block averaging filter is reset (cleared) after processing each block of N_{AVG} samples. The N_{AVG} configuration is set by the AVG_WIN_LEN bit field in the AVG_CONFIG register (see Table 49) using the following equation:

$$N_{AVG} = 2^{AVG\_WIN\_LEN\,+\,1} \qquad (3)$$

THEORY OF OPERATION

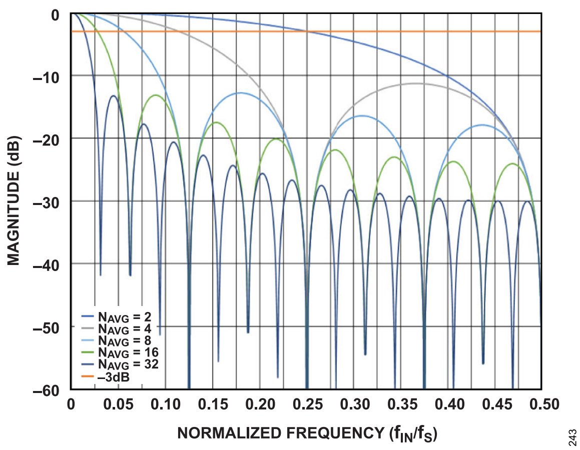


Figure 43. Frequency Response Examples for the Block Averaging Filter

INTERNAL TIMER

The AD4060 includes an internal timer to generate the ADC sampling clock in burst averaging mode and both the autonomous modes (monitor mode and trigger mode). The sampling frequency in these modes is set by the FS_BURST_AUTO bit field in the TIMER_CONFIG register and ranges from 2MSPS to 111SPS. See Table 52 in the Register Details section for the full set of nominal sampling clock frequencies (f_{OSC}) offered on the AD4060. The actual sampling frequency in these modes is guaranteed to be within ±15% of f_{OSC} (see Timing Specifications).

The internal timer also controls the DEV_EN signal delay (see theDevice Enable Signal section). The t_{PWR_ON} delay is set by the TIMER_PWR_ON bit field, which is also in the TIMER_CONFIG register. The t_{PWR_ON} settings range from 0.5µs to 9000µs. See Table 52 in the Register Details section for the full set of nominal t_{PWR_ON} delay options.

In monitor mode, threshold detection events do not disable the internal sampling clock, and the device continues sampling even after the MAX/MIN threshold interrupt bit fields and signals are asserted . See the Monitor Mode section for detail.

In trigger mode, threshold detection events do disable the internal sampling clock. Simultaneously, the ADC is enabled and performs an N-bit conversion, and updates the contents of MAX_SAMPLE, MIN_SAMPLE, MAX_THRESH_INTR, MIN_THRESH_INTR, and THRESH_OVERRUN bit field/registers. See the Trigger Mode section for detail.

POWER SUPPLIES

The AD4060 has the following three power domains, the ranges for which are given in Table 1:

- VDD is the analog supply rail.
- CLDO is the +1.8V ADC core supply rail, generated by an internal +1.8V LDO regulator.
- VIO is the digital interface logic supply rail.

The VDD and VIO supplies must be supplied externally. The CLDO supply is generated internally by an internal +1.8V LDO regulator sourced by the VDD rail. The VDD supply current is a function of the ADC sampling rate, because it supplies the internal LDO regulator that then supplies the SAR ADC core (see the VDD Power Dissipation section). In sleep mode, the internal LDO regulator is powered down to reduce the VDD standby current to 10nA (see Table 1 and the Sleep Mode section).

The AD4060 has no power supply sequencing requirements. The minimum allowable rise time for the VDD and VIO supplies is 100µs. It is recommended to perform a device reset after the VDD and VIO supplies are stable (see the Power-On Reset section).

It is recommended to decouple the VDD, CLDO, and VIO pins to GND each with a 1µF capacitor. When selecting VDD as the V_{REF} source (as described in the Reference Selection Modes section), or when driving the VDD and REF pins with a common external source, it is recommended to decouple VDD and REF with a shared 2.2µF capacitor.

COMPARATOR OPERATION

The AD4060 ADC core offers a lower power, 12-bit window comparator mode for autonomous threshold detection and monitoring. Figure 44 shows a simplified schematic of the window comparator used in the autonomous modes.

The AD4060 has two autonomous sampling modes, as described in the Autonomous Modes section. When either of the autonomous modes are enabled, the ADC enters comparator mode, and the internal timer acts as the sampling clock (see the Internal Timer section). The comparator steps through a sequence of comparisons against four user-programmable threshold regions on each sample and generates alert flags and hardware interrupts when the signal enters those regions.

Figure 45 illustrates the out-of-bounds regions set by the maximum and minimum threshold values. The maximum and minimum thresholds are user-programmable via the MAX_LIMIT and MIN_LIMIT bit fields. The MAX_LIMIT and MIN_LIMIT fields are each 12 bits wide for 12-bit comparator resolution. There are also independent hysteresis settings for maximum and minimum limits, set by the MAX_HYST and MIN_HYST fields, respectively, that define a second set of limits for autoclearing the alert signals. See the Autonomous Modes section for more information.

The data format of the MAX_LIMIT and MIN_LIMIT fields corresponds to the selected input range mode (as described in the Transfer Function section). The MAX_LIMIT and MIN_LIMIT fields are in twos complement in differential mode (DATA_FORMAT = 1'b1) and straight binary in single-ended mode (DATA_FORMAT = 1'b0). The MAX_HYST and MIN_HYST fields are always straight binary regardless of input mode setting.

The comparator includes two alert signals and two sticky alert bits in the register map. The MAX_INTR and MIN_INTR signals are the alert signals for maximum and minimum threshold events,

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respectively. The MAX_INTR and MIN_INTR signals may be routed to either or both of the GP0 and GP1 pins (see the Interrupts and Control Signals section). The MAX_FLAG and MIN_FLAG bits are sticky, write 1 to clear the bits in the DEVICE_STATUS register. The DEVICE_STATUS register also includes a threshold overrun bit (THRESH_OVERRUN) that is set whenever the comparator tries to set either the MAX_FLAG or MIN_FLAG bits before they have been cleared.

Maximum and minimum threshold events also trigger the MAX_IBI and MIN_IBI respectively if these IBIs are enabled. See In-Band Interrupts for more detail.

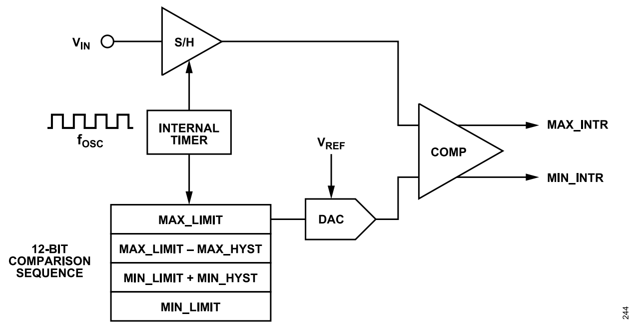

Figure 44. Simplified Schematic of Autonomous Mode Window Comparator

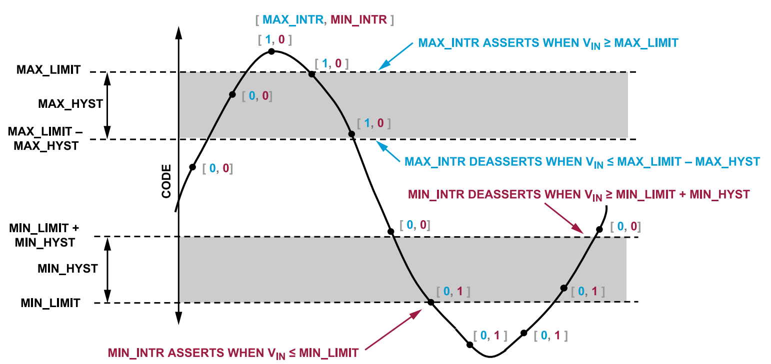

Figure 45. Threshold Event Regions

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INTERRUPTS AND CONTROL SIGNALS

The AD4060 generates several digital signals for synchronizing the analog front-end and digital back-end processes to the ADC sampling. These signals can be assigned to the two general purpose pins (GP0 and GP1) via the GP0_MODE and GP1_MODE fields in the GP_CONFIG register, respectively. The following sections describe the functionality and timing details for each of the AD4060 digital signals. Table 12 and Table 50 list the GPx signal assignments that correspond to each GPx_MODE bit field setting.

Table 12. GP0 and GP1 Signal Assignment Control

GPx_MODE Setting	GP0 Signal Assignment	GP1 Signal Assignment
3'h0	Disabled/high-Z (default)	Disabled/high-Z
3'h1	GP0_INTR	GP1_INTR
3'h2	$\overline{\text{RDY}}$	$\overline{\text{RDY}}$
3'h3	DEV_EN	DEV_EN
3'h4	Invalid	Invalid
3'h5	Logic low	Logic low
3'h6	Logic high	Logic high
3'h7	Invalid	DEV_RDY (default)

In-Band Interrupts

The AD4060 includes In-Band Interrupts (IBIs) as per the MIPI I3C specification in response to specific events. When an IBI event is triggered, the AD4060 sends an interrupt request to the digital host. The AD4060 conforms to the I3C specification for standards and rules about when an I3C target device is allowed to transmit an IBI over the I3C bus.

According to Section 5.1.3.2.2 of the MIPI I3C specifications, the I3C bus must be in the bus available state (see t_{IBI_ISSUE} in Table 5) for the target device to issue the start of an IBI transmission. When IBIs are enabled, it is recommended to precede each I3C frame with the broadcast address 0x7E to allow the AD4060 to drive its TGT_ADDR to initiate an IBI request.

IBIs can be enabled or disabled using the ENEC and DISEC CCCs respectively. (See Common Command Codes (CCCs) for more detail). Table 13 lists the AD4060 IBIs along with their trigger conditions, and the enable bits. Each IBI can be individually enabled or disabled. (See the Interface Error IBI Enable Register section and the ADC IBI Enable Register section for more detail.)

The IBI_PENDING bit field in the IBI_STATUS register indicates whether the AD4060 has a pending IBI. The IBI stays pending until the controller services the IBI request. Section 5.1.6.2 of the MIPI I3C specification outlines the ways in which a controller can service a target device's IBI request. The IBI_EN bit field in the IBI_STATUS register indicates whether IBIs are currently enabled or disabled. (See the IBI Status Register section for more detail.)

The MAX_IBI indicates the occurrence of a MAX threshold event which means the input signal value has exceeded the limit stored in the MAX_LIMIT register

The MIN_IBI indicates the occurrence of a MIN threshold event which means the input signal value is lower than the limit stored in the MIN_LIMIT register

The DATA_READY_IBI is defined for the event where new ADC data are ready to read from the CONV_TRIGGER register. The DATA_READY_IBI is triggered by the end-of-conversion events in both the sample mode and burst averaging modes when the single conversion or the burst of conversions are complete, and the data is ready to be read by the controller on the I3C bus.

The INTERFACE_ERROR_IBI occurs when there is an error in the I3C bus interface. This IBI can be triggered by any of the enabled interface error sources including parity error, SCL error, CRC error, write invalid error, and address invalid error.

Table 13. IBI Triggers and Enable Bits

IBI	IBI Trigger	IBI Enable Bit
MAX_IBI	MAX Threshold Event	MAX_IBI_EN
MIN_IBI	MIN Threshold Event	MIN_IBI_EN
DATA_READY_IBI	End of Conversion/ Data Valid (Address Pointer → CONV_TRIGGER)	DATA_READY_IBI_EN
INTERFACE ERROR IBI	Parity Error	PARITY_ERROR_IBI_EN
	SCL Error	SCL_ERROR_IBI_EN
	CRC Error	CRC_ERROR_IBI_EN
	Write Invalid Error	WRITE_INVALID_IBI_EN
	Address Invalid Error	ADDR_INVALID_IBI_EN

Mandatory Data Byte

The AD4060 will transmit a Mandatory Data Byte (MDB) on the I3C bus as defined by the MIPI I3C specification when the controller reads the IBI generated by a target device. The MDB indicates what type of IBI has been generated through the interrupt group identifier field (MDB[7:5]) and the specific group identifier field (MDB[4:0]).

The INTERFACE_ERR asserts when an interface error has been detected on the I3C bus. When an interface error occurs, the user will have to check the INTERFACE_STATUS register to find the specific field associated with the error. The INTERFACE_ERR is cleared when the user writes a 1 to it via a register write.

The MAX_THRESH_INTR asserts when the input signal is greater than MAX_LIMIT.

The MIN_THRESH_INTR asserts when the input signal is less than MIN_LIMIT.

MAX_THRESH_INTR and MIN_THRESH_INTR are sticky bits which means that once they are set to 1, they do not self-clear

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even when the input signal goes back in range as dictated by the MAX_ HYST and MIN_ HYST registers. They are cleared when the user writes a 1 to them via a register write. (see the Autonomous Modes section for more detail).

The MAX_THRESH_INTR and MIN_THRESH_INTR bit fields are not to be confused with the MAX_INTR and MIN_INTR signals which are optionally output on the GP1 or GP0 pins. MAX_INTR and MIN_INTR are defined to self-clear when input voltage is back in range as defined by the MAX _HYST and MIN _HYST registers.

Table 14. Mandatory Data Byte - Interrupts Group Identifier Field

IBI	Interrupt Group Identified Field	MDB[7:5]
MAX_IBI (Monitor Mode)	User Defined	3'b000
MIN_IBI (Monitor Mode)	User Defined	3'b000
MAX_IBI (Trigger Mode)	Pending Read Notification[1]	3'b101
MIN_IBI (Trigger Mode)	Pending Read Notification	3'b101
DATA_READY_IBI	Pending Read Notification	3'b101
INTERFACE_ERROR_IBI	Either User Defined or Pending Read Notification[2]	3'b000 or 3'b101

1 Section 5.1.6.2.2 of the MIPI I3C specifications explains what the controller's responsibilities are when a target device sends an IBI request and an MDB with a pending read notification

2 The INTERFACE_ERROR_IBI can occur independent of the ADC Operating mode, and at times, this IBI can exhibit either of the interrupt group identifier codes. Thus, if the Interface Error flag (MDB[3]) gets set to '1'(see Table 15), then any pending read shall be treated as invalid, and ADC data should not be read until the interface error has been cleared

Table 15. Mandatory Data Byte - Specific Interrupt Identifier Field

MDB[4]	MDB[3]	MDB[2]	MDB[1]	MDB[0]
1'b1	INTERFACE_ERR	1'b0	MAX_THRESH_INTR	MIN_THRESH_INTR

Static Logic Outputs

The AD4060 GP0 and GP1 digital outputs can be set to a static logic low or logic high level. This function allows the digital host to control logic settings for external devices through the AD4060 and reduces the required number of GPIO resources. The logic output voltage specifications and corresponding load current conditions are given by V_{OL} and V_{OH} in Table 1.

Data Ready Signal

The data ready signal ($\overline{RDY}$) is an active-low interrupt signal that indicates when new ADC data are ready to read via the I3C interface.

$\overline{RDY}$ is always driven high following any form of device reset. $\overline{RDY}$ is also driven high when the ADDR_PTR is pointing to any address besides the CONV_READ and CONV_TRIGGER registers.

When the ADDR_PTR is pointing to CONV_READ or CONV_TRIGGER, $\overline{RDY}$ gets driven high at the convert-start instant, and transitions from high to low any time a new conversion result is ready to read. In sample mode, $\overline{RDY}$ goes low at the end of the conversion phase to indicate a new 12-bit result is available (see Sample Mode Timing Diagram). In burst averaging mode, RDY goes low after N_{AVG} conversions to indicate a new 14-bit averaged result is available (see Burst Averaging Mode Timing Diagram).

Threshold Alert Signals

The comparator threshold alert signals MAX_INTR and MIN_INTR can be routed to the GP0 or GP1 pins via the GP0_INTR and GP1_INTR signals (see the Autonomous Modes section). Either of the GPx_INTR signals can be assigned to the MAX_INTR signal, the MIN_INTR signal, or the logical OR of both, giving the flexibility to either drive independent hardware interrupts for maximum and minimum crossings or to combine together for a single interrupt. By default, MAX_INTR is assigned to GP1_INTR and MIN_INTR is assigned to GP0_INTR.

The mapping of the alert signals to the GPx pins is controlled via the GP0_INTR_EN and GP1_INTR_EN bit fields in the INTR_CONFIG register (see Table 16 and Table 51).

Table 16. GPx_INTR Settings

GPx_INTR_EN Setting	GPx_INTR Signal Assignment
2'h0	Neither interrupt
2'h1	MIN_INTR
2'h2	MAX_INTR
2'h3	(MAX_INTR) OR (MIN_INTR)

Device Ready Signal

The device ready signal (DEV_RDY) is an active-high signal that indicates when the AD4060 completes power-up or reset routines and is ready to accept serial interface communications. The DEV_RDY signal is routed to the GP1 pin after power-up or reset, so the digital host can monitor it to know when the AD4060 is active. See the Device Reset section for timing diagrams of the DEV_RDY signal.

Device Enable Signal

The AD4060 includes a signal chain power-cycling control signal called DEV_EN. The DEV_EN signal synchronizes the enable and power-down states of signal chain devices (such as amplifiers, sensors, and voltage references) with the ADC sampling instant, optimizing system power consumption while minimizing sampling error from power-on delays. Figure 46 shows a typical application

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circuit utilizing the DEV_EN signal to power down an amplifier between samples.

When the DEV_EN signal is enabled, the internal timer acts as a one-shot timer triggered by the ADC convert-start rising edge. The timer delay (t_{PWR_ON}) controls how long the amplifier is powered on before the ADC sampling instant and is programmable to tailor to the connected device's specific power-on settling time specifications. Table 52 in the Register Details section shows the nominal t_{PWR_ON} settings available via the TIMER_PWR_ON bit field.

The DEV_EN signal is enabled by assigning it to either the GP0 or GP1 digital outputs (see Table 12). The DEV_EN signal can be configured as active high or active low via the DEV_EN_POL bit field in the GP_CONFIG register (see Table 50). DEV_EN is active high by default.

Figure 51, and Figure 55 show timing diagrams of the DEV_EN signal and the ADC sampling instant relative to the ADC convert-start.

When using the CONV_READ register to trigger ADC conversions, the convert-start happens on the SDA rising edge of the stop (P) at the end of the read command (see CONV_READ Register). The DEV_EN signal asserts at this convert-start instant. When using the CONV_TRIGGER register to trigger ADC conversions, the convert-start happens on the SDA rising edge of the stop (P) at the end of the write command (see CONV_TRIGGER Register). The DEV_EN signal asserts at this convert-start instant.

In sample mode, DEV_EN deasserts after each conversion. In burst averaging mode, DEV_EN remains asserted until the last conversion in the burst of samples. DEV_EN is not supported in the autonomous modes.

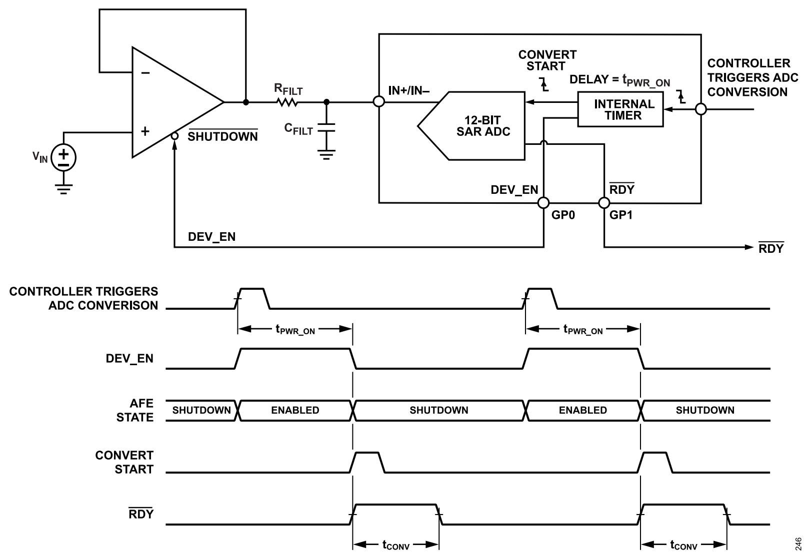

Figure 46. Typical Application Circuit with DEV_EN Signal

MODES OF OPERATION

Table 18 shows an overview of the AD4060 functional modes. The ADC and serial interface functionality for each mode is given in the subsequent sections.

The AD4060 ADC code is idle following power-up and device resets. The operating modes are selected via the configuration registers as shown in Table 18. The I3C protocol for register writes and reads is described in the Register Reads and Register Writes sections.

Figure 47 shows the AD4060 operating mode selection as a state machine diagram.

Table 17 shows the recommended address pointer setting for reading ADC data in each functional mode.

Table 17. Address Pointer Recommended Values

Mode	Conversion Register	Recommended Address Pointer Value
Sample Mode	CONV_READ	0x51
	CONV_TRIGGER	0x57
Burst Averaging Mode	CONV_READ	0x51
	CONV_TRIGGER	0x57
Monitor Mode	CONV_TRIGGER	0x57
Trigger Mode	CONV_TRIGGER	0x57

Table 18. AD4060 Functional Modes

Mode	ADC_MODE	AUTO_MODE	POWER_MODE
Sample Mode	2'b00	Don't care	2'b00
Burst Averaging Mode	2'b01	Don't care	2'b00
Monitor Mode	2'b11	1'b0	2'b00
Trigger Mode	2'b11	1'b1	2'b00
Sleep Mode	Don't care	Don't care	2'b11

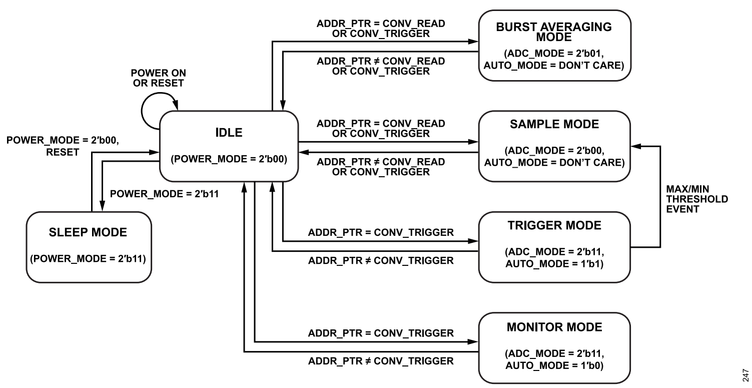

Figure 47. AD4060 State Machine Diagram

MODES OF OPERATION

SAMPLE MODE

In sample mode, a convert-start triggers a single conversion. At the end of the conversion, the AD4060 generates a 12-bit result that the controller device reads via the I3C bus. Table 18 lists the configuration register settings to select sample mode. Figure 48 shows a typical connection diagram for the AD4060 digital interface.

Figure 49 and Figure 50 show interface timing diagrams for sample mode using the CONV_READ and CONV_TRIGGER registers respectively. The t_{CONV} specification quantifies the time delay between the convert-start and the end of conversion. The controller must wait for the maximum t_{CONV} delay before reading the result over the I3C bus. The $\overline{RDY}$ signal acts as an optional hardware interrupt to synchronize I3C reads to the ADC sampling phases (see the Data Ready Signal section).

When reading from the CONV_READ register to trigger ADC conversions, each conversion result is output on each subsequent read on the I3C bus (see the CONV_READ Register section). When using the CONV_TRIGGER register to trigger ADC conversions, the conversion result must be read from the register after each conversion, or else the next write (and convert-start) will overwrite the conversion results from the previous conversion (see the CONV_TRIGGER Register section).

It is recommended to read the lower 16-bits of the CONV_READ and CONV_TRIGGER registers in sample mode for the most efficient readback. See Table 17 for the recommended ADDR_PTR setting for data readback in sample mode.

In sample mode, the maximum sampling rate (f_S) is limited by the output data rate of the I3C bus, which is a function of the output data length and the I3C bus characteristics. The fastest output data rate is achieved by repeatedly reading from the CONV_READ register, as shown in Figure 63. See the Calculating Serial Interface Output Data Rate section for details on estimating the maximum achievable f_S for the given operating conditions.

When the DEV_EN signal is enabled, the start of the conversion is delayed by the programmable t_{PWR_ON} delay relative to the convert-start. See the Device Enable Signal section and Figure 51 for specific timing details when using the DEV_EN signal.

If enabled, the DATA_READY_IBI occurs at the end-of-conversion for the CONV_TRIGGER register and indicates that the ADC data is ready to be read from the CONV_TRIGGER register by the controller. (See In-Band Interrupts for more detail.)

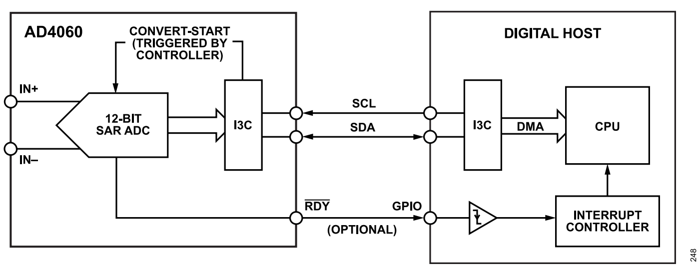

Figure 48. Sample Mode Example Connection Diagram

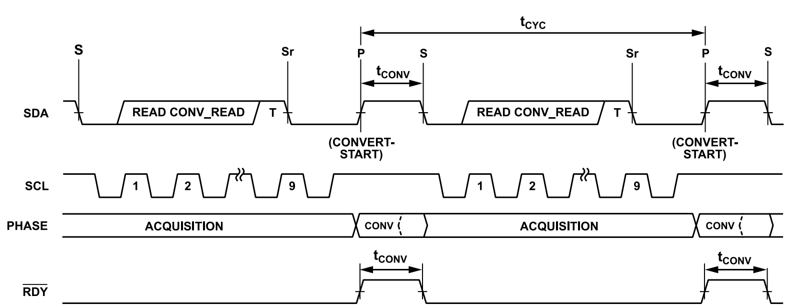

Figure 49. Sample Mode Timing Diagram Using CONV_READ

MODES OF OPERATION

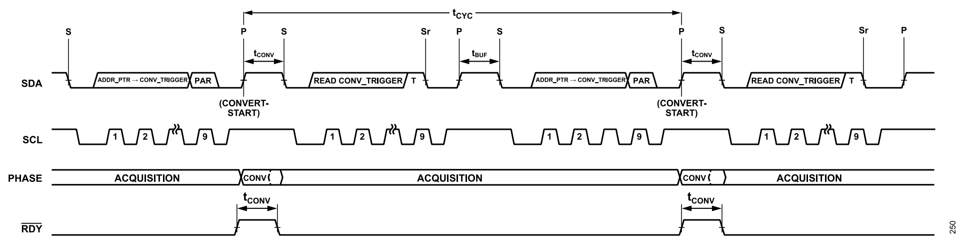

Figure 50. Sample Mode Timing Diagram Using CONV_TRIGGER

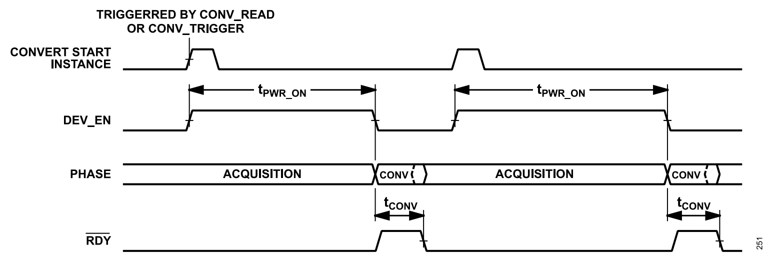

Figure 51. Sample Mode Timing with DEV_EN Enabled

MODES OF OPERATION

BURST AVERAGING MODE

In burst averaging mode, a convert-start triggers the internal timer to perform a burst of conversions for the averaging filter to accumulate and generate a 14-bit averaged result. Table 18 lists the configuration register settings to select burst averaging mode. Figure 52 shows a typical connection diagram for the AD4060 digital interface.

Figure 53 and Figure 54 show interface timing diagrams for burst averaging mode using the CONV_READ and CONV_TRIGGER registers respectively. The ADC sampling period (t_{CYC}) is set by the internal timer frequency (f_{OSC}) and the number of samples per burst is set by the averaging ratio (N_{AVG}). Table 52 lists the options for f_{OSC}. The averaging filter supports averaging ratios from 2 to 256 and is set by the AVG_WIN_LEN bit field, as described in the Block Averaging Filter section.

The controller must wait for the averaged result to be ready before reading the results on the I3C bus. The $\overline{\text{RDY}}$ signal acts as an optional hardware interrupt to synchronize the I3C data reads to the ADC sampling phases (see the Data Ready Signal section).

The total latency between the convert-start trigger and data ready is given by the following equation:

$$\frac{(N_{AVG}-1)}{f_{OSC}} + t_{CONV} \quad (4)$$

It is recommended to read the lower 16-bits of the CONV_READ and CONV_TRIGGER registers in burst-averaging mode for the most efficient readback. See Table 17 for the recommended ADDR_PTR setting for data readback in burst-averaging mode.

When the DEV_EN signal is enabled, the start of the burst of conversions is delayed by the programmable t_{PWR_ON} delay, relative to the convert-start trigger. The DEV_EN signal remains asserted until the end of the burst of samples. See the Device Enable Signal section and Figure 55 for specific timing details when using the DEV_EN signal.

If enabled, the DATA_READY_IBI occurs at the end-of-conversion for the CONV_TRIGGER register and indicates that the ADC data is ready to be read from the CONV_TRIGGER register by the controller. (See In-Band Interrupts for more detail)

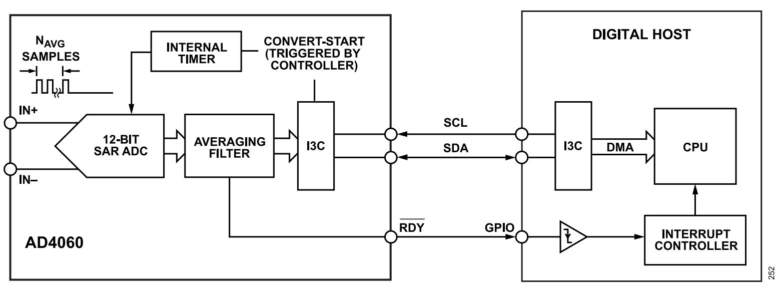

Figure 52. Burst Averaging Mode Example Connection Diagram

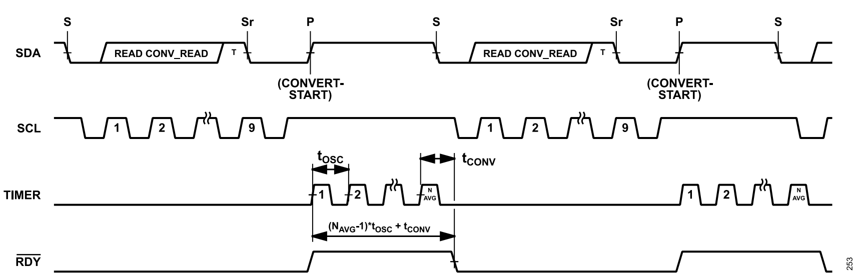

Figure 53. Burst Averaging Mode Timing Diagram Using CONV_READ

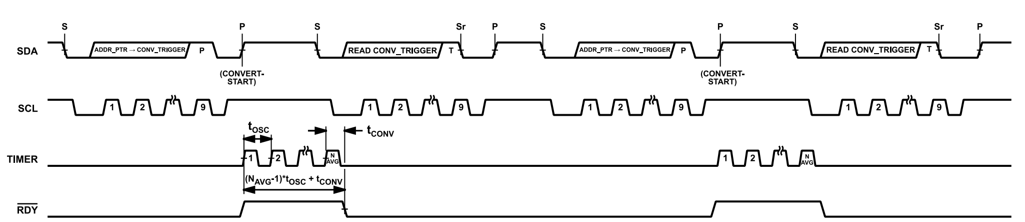

Figure 54. Burst Averaging Mode Timing Diagram Using CONV_TRIGGER

MODES OF OPERATION

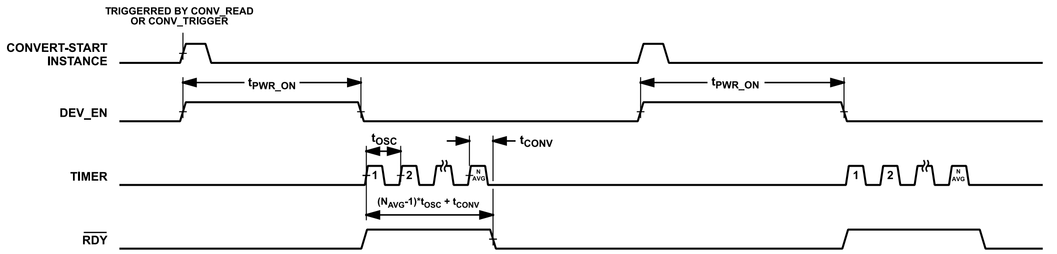

Figure 55. Burst Averaging Mode Timing with DEV_EN Enabled

MODES OF OPERATION

AUTONOMOUS MODES

The autonomous modes allow the AD4060 to autonomously monitor the input signal to detect out-of-range events. The autonomous modes feature lower power dissipation than nonautonomous modes, because the ADC core enters a low-power comparator mode, as described in the Comparator Operation section (see Table 1 for power dissipation specifications for each mode).

The AD4060 offers two autonomous modes named monitor mode and trigger mode. Both autonomous modes are described in the subsequent sections. When either autonomous mode is selected, the ADC core functions as a window comparator, and the ADC sampling clock is driven by the internal timer, as described in the Comparator Operation section. The sampling clock frequency is set by the FS_BURST_AUTO bit field in the TIMER_CONFIG register (see Table 52).

The comparator performs the following four sample-and-comparison operations in a repeated sequence, each taking one sample period to execute, for a total sequence time of four sample periods as follows:

1. $V_{IN} \geq$ MAX_LIMIT
2. $V_{IN} \leq$ MAX_LIMIT − MAX_HYST
3. $V_{IN} \geq$ MIN_LIMIT + MIN_HYST
4. $V_{IN} \leq$ MIN_LIMIT

The comparator includes two hardware alert signals for the maximum and minimum threshold events (MAX_INTR and MIN_INTR, respectively). These signals can be assigned to either or both of the GP0 and GP1 pins, as described in the Threshold Alert Signals section. Figure 58 shows a typical connection diagram for a microcontroller using these alert signals as hardware interrupts.

Monitor Mode

Table 18 shows the ADC_MODE and AUTO_MODE bit field settings for entering monitor mode. After setting the ADC_MODE and the AUTO_MODE bits, setting the ADDR_PTR to CONV_TRIGGER enables the internal timer, and the AD4060 starts autonomously functioning as a window comparator. The AD4060 continuously operates in autonomous mode until the controller changes the ADDR_PTR from the CONV_TRIGGER register to a different value (see Figure 47). Monitor mode makes use of the user-programmable hysteresis settings to self-clear the MAX_INTR and MIN_INTR signals when the input signal goes back in range (see Figure 45).

Figure 56 shows a flowchart for register configuration, the comparison sequence operations, and the behavior of the hardware interrupts and alert flags following threshold crossings in monitor mode.

When the maximum or minimum threshold crossings are detected, the MAX_INTR or MIN_INTR signal asserts, respectively. The internal timer continues to generate the sampling clock, and the MAX_INTR or MIN_INTR signal is deasserted when the sampled input signal is back in bounds as set by the MAX_HYST and MIN_HYST bit fields, respectively.

The MAX_FLAG or MIN_FLAG bit is also asserted when MAX_INTR or MIN_INTR asserts, respectively. The MAX_FLAG and MIN_FLAG are sticky and do not self-clear when the signal goes back in range. It is recommended to reset the MAX_FLAG and MIN_FLAG bits after exiting and before returning to monitor mode.

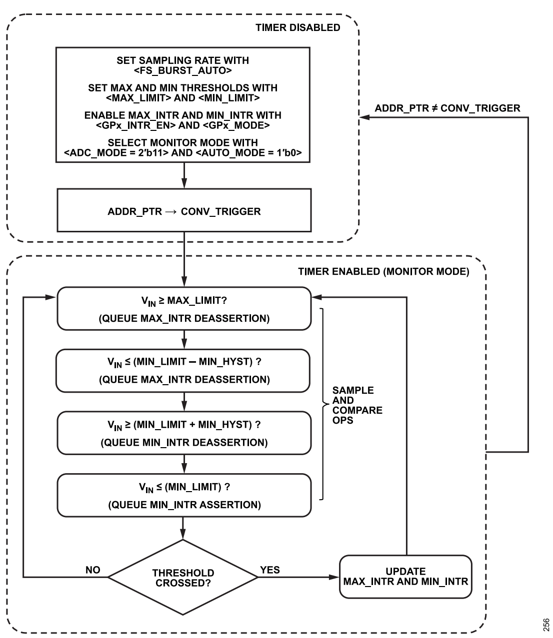

Figure 56. Monitor Mode Flowchart

MODES OF OPERATION

Trigger Mode

Table 18 shows the ADC_MODE and AUTO_MODE bit field settings for entering trigger mode. After setting the ADC_MODE and the AUTO_MODE bits, setting the ADDR_PTR to CONV_TRIGGER enables the internal timer, and the AD4060 starts autonomously functioning as a window comparator. In trigger mode, threshold crossings trigger the AD4060 to automatically perform a 12-bit conversion of the input signal and transition into sample mode. The corresponding alert signals and status bits are asserted to send the MAX or MIN IBI on the I3C bus. The controller can then read the 12-bit result from the MAX_SAMPLE_REG or MIN_SAMPLE_REG registers in configuration mode.

Figure 57 shows a flowchart for register configuration, the comparison sequence operations, and the behavior of the hardware interrupts and alert flags following threshold crossings in trigger mode.

When a maximum or minimum crossing is detected, the MAX_INTR or MIN_INTR signal asserts, respectively. The internal timer is disabled to stop autonomous sampling, and the ADC core powers up to convert the input signal. Figure 59 shows a timing diagram for the threshold detection and ADC sampling in trigger mode. Following the threshold event, the firmware can either continue operating the AD4060 in sample mode to perform more conversions, or the firmware can set the ADDR_PTR to a different value besides the CONV_TRIGGER register to exit sample mode and read the alert registers. The MAX_INTR and MIN_INTR signals hold their states until the ADDR_PTR is updated to a different value besides CONV_TRIGGER.

Note that following the transition to sample mode, the ADC_MODE bit field in the register map is internally overwritten to 2'h0 and must be rewritten to 2'h3 to reenter autonomous mode.

The MAX_FLAG or MIN_FLAG bit is also asserted when MAX_INTR or MIN_INTR asserts, respectively. The MAX_FLAG and MIN_FLAG bits are sticky and do not clear until the host sets them to 1'b1 with a register write. It is recommended to reset the MAX_FLAG and MIN_FLAG bits before returning to autonomous mode.

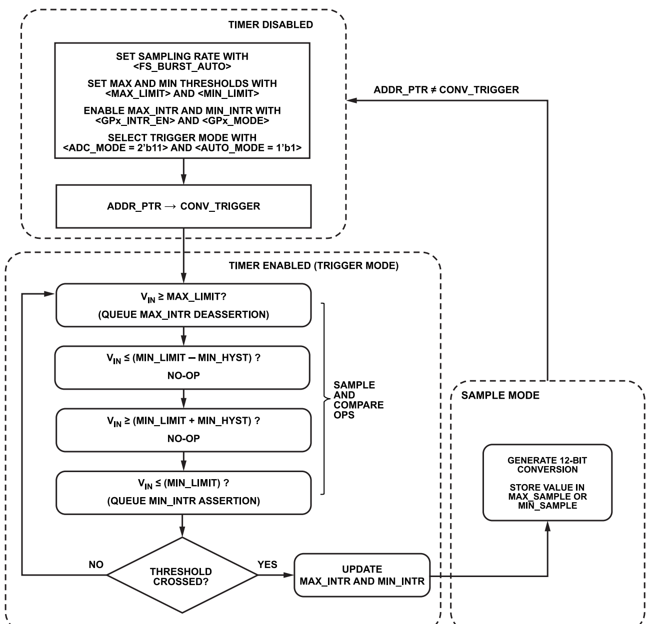

Figure 57. Trigger Mode Flowchart

MODES OF OPERATION

Autonomous Mode Diagrams

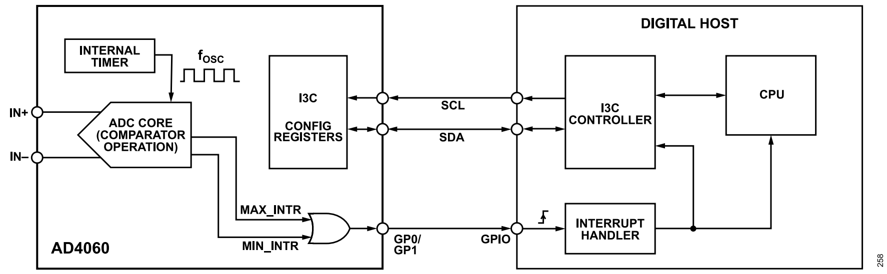

Figure 58. Autonomous Mode Example Connection Diagram

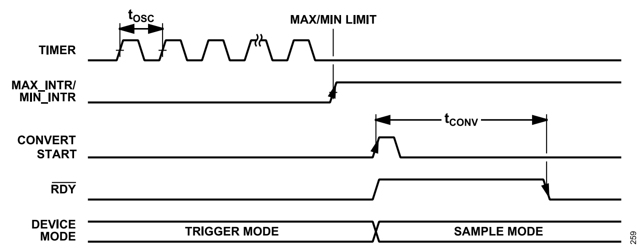

Figure 59. Trigger Mode Timing Diagram

SLEEP MODE

In sleep mode, the AD4060 powers down all functional blocks, except the digital interface, to achieve an ultra-low power consumption of 430nW for extended periods of idle time (see Table 1). Set the POWER_MODE bit field in the DEVICE_CONFIG register to 2'h3 to put the AD4060 into sleep mode.

The internal LDO regulator is powered down and stops supplying the +1.8V CLDO supply while in sleep mode. This feature powers down the ADC core and most other functional blocks. The digital interface remains active, so the digital host can rewrite the POWER_MODE bit field to 2'h0 to exit sleep mode and power up the device. When the device exits sleep mode, it enters configuration mode. The configuration register states persist, so the digital host does not need to reprogram the device configuration after exiting sleep mode.

SERIAL INTERFACE

The AD4060 digital interface includes a 2-wire I3C interface for serial data transfer, and two general-purpose digital outputs, GP0 and GP1. The I3C interface is primarily used for reading and writing the AD4060 configuration registers and for reading the ADC results. The Modes of Operation sections describe the I3C functionality and protocols for each operating mode.

The AD4060 adheres to the I3C specifications as defined by MIPI I3C v1.1 that are also referenced throughout this document. Section 4.2.2 of the MIPI I3C specifications outlines the role of an I3C target device. The AD4060 is an SDR-only target and does not support HDR modes. The AD4060 supports the common command codes (CCCs) listed in the Common Command Codes (CCCs) section, and in-band Interrupts (IBIs) as described in the In-Band Interrupts section. The AD4060 does not support the hot-join mechanism and is not capable of functioning as an I3C controller device. The AD4060 is not compatible with I2C controllers.

Refer to Section 5.1.3.1 of the MIPI specifications for guidance on the open drain pull-up requirements for SDA and SCL.

The SDA data are read on the SCL rising edge and updated on the SCL falling edge.

The AD4060 includes a CRC for register reads and writes supporting robust data transfers (see the Register Access CRC section for more detail). The ADC data are formatted to integer multiples of bytes to maximize compatibility with microcontroller internal memory transfer operations such as direct memory access (DMA).

The interface logic level is set by the VIO supply voltage, as specified in Specifications. The AD4060 supports 1.8V, 2.5V, and 3.3V logic systems.

DYNAMIC ADDRESSING

The AD4060 is addressed by the I3C controller with a unique dynamic address (TGT_ADDR). Following each start or repeated start, the AD4060 compares the first byte against its TGT_ADDR to determine if it is being addressed.

Following a device reset, and at the start of the I3C bus initialization, the controller must initiate the dynamic address assignment (DAA) procedure by sending the broadcast ENTDAA CCC on the bus indicating to all the target devices to enter the DAA mode (See the Common Command Codes (CCCs) section for more detail).

During the DAA routine, the AD4060 (along with any other I3C targets on the bus) sends its unique 48-bit Provisional ID (PID) to the controller. Table 19 shows the contents of the AD4060 48-bit PID. The controller then assigns a unique 7-bit dynamic address to each target device on the bus (section 5.1.4 of the MIPI I3C specifications describes the DAA Procedure in detail).

The TGT_ADDR is stored in the TGT_ADDR_REG after it is assigned.

The AD4060 includes three address logic inputs called ADDR0, ADDR1, and ADDR2 (see Table 19). The ADDRx pins allow up to eight unique PIDs, enabling up to eight AD4060 devices to be populated on one I3C bus without address conflicts.

The AD4060 supports group addressing, allowing an I3C controller to write to multiple devices simultaneously. Group addressing can be used to trigger simultaneous sampling of multiple AD4060 devices via the CONV_TRIGGER register, for example. Group addresses are assigned with the SETGRPA CCC (see the SETGRPA section).

The AD4060 does not include a static I2C address.

Table 19. AD4060 48-Bit Provisional ID Definition

PID[1] Bit Field Name	PID Bit Field Offset	Value	Description
MIPI Manufacturer ID (MID)	PID[47:33]	15'h0177	ADI MIPI assigned vendor ID.
PID Type Selector	PID[32]	1'b0	Vendor fixed value.
Part ID	PID[31:16]	16'h007A	ADI product ID.
Instance ID	PID[15:12]	PID[15] = 1'b0	
		PID[14:12] = [ADDR2, ADDR1, ADDR0]	Allows pin-strap selection of up to eight unique device instances. (See the Pin Configuration and Function Descriptions section for more detail.)
Vendor-Defined	PID[11:0]	PID[11:8] = 4'b0	Device revision number.
		PID[7:0] = DCR[7:0]	Device characteristics register (DCR) byte. See the Register Details section for more detail.

[1] Fixed by vendor.

SERIAL INTERFACE

REGISTER ADDRESS POINTER

The register address pointer (ADDR_PTR) is a one byte long standalone register for selecting the active AD4060 register for reading or writing. When an I3C read command is initiated, the controller will read data from the register address currently stored in the ADDR_PTR. Similarly, when an I3C write is initiated, the controller will write data to the register address currently stored in the ADDR_PTR. The ADDR_PTR register itself is not directly addressable for readback.

The ADDR_PTR is updated during the instruction phase of an I3C write command (see Figure 60). The ADD_PTR holds the value written to it until it is updated, or until a device reset.

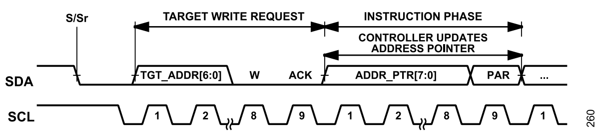

Figure 60. Updating the Address Pointer

REGISTER WRITES

The register write process for the AD4060 on an I3C bus consists of three separate phases—target write request phase, instruction phase, and data phase.

Figure 61 shows a register write sequence for the AD4060.

In the target write request phase, the controller initiates a register write by sending a start (S) or a repeated start (Sr) with the device's dynamic target or group address with the RnW bit = '0'. The device acknowledges this by sending an ACK by pulling SDA low. If the controller addresses multiple AD4060 devices via a group address, then the subsequent register write data shall be applied to all AD4060 devices on the I3C bus.

In the instruction phase, the controller updates the ADDR_PTR. If CRC is enabled, a CRC byte is included in the ADDR_PTR. Both the ADDR_PTR Byte(s) and the CRC byte each have their own parity bit (see the Data Phase Ninth SDA Bit section).

In the data phase, the controller sends write-data (plus CRC if enabled) to consecutive-addressed registers one byte at a time. The first data byte (plus CRC) corresponds to the data in the register at address = <ADDR_PTR>. Each subsequent data byte (plus CRC) corresponds to the next-lowest addressed register after <ADDR_PTR> and so on.

The write frame is concluded when the controller initiates a repeated start (Sr) or a stop (P).

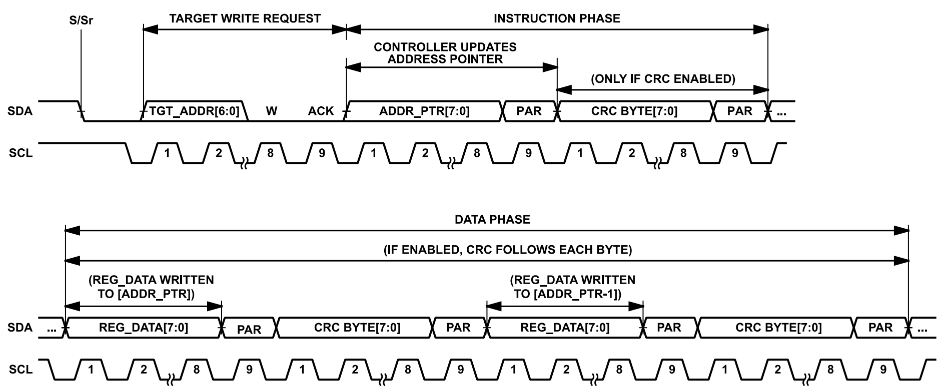

Figure 61. AD4060 Register Write Sequence

SERIAL INTERFACE

REGISTER READS

The register read process for the AD4060 on an I3C bus consists of three separate phases—a write to update the ADDR_PTR, target read request phase, and data phase.

Figure 62 shows a register read sequence for the AD4060.

The ADDR_PTR specifies which register will be read back during the target read request. Set the ADDR_PTR to the desired register address value prior to sending a target read request (see the Register Address Pointer section).

In the target read request phase, the controller initiates a register read by sending a start (S) or a repeated start (Sr) with the device's TGT_ADDR with the RnW bit = '1'. The device acknowledges this by sending an ACK by pulling SDA low.

In the data phase, the AD4060 outputs read-data (plus CRC if enabled) from consecutive-addressed registers one byte at time. The first data byte (plus CRC) corresponds to the data in the register at address = <ADDR_PTR>. Each subsequent data byte (plus CRC) corresponds to the data in the next-lowest addressed register after <ADDR_PTR> and so on.

The read frame is concluded when the controller initiates a repeated start (Sr). Each register read byte is terminated with a T-bit. The T-bit is always = '1' for register reads, so the controller is responsible for ending the register read frame (see Figure 7 and Figure 8).

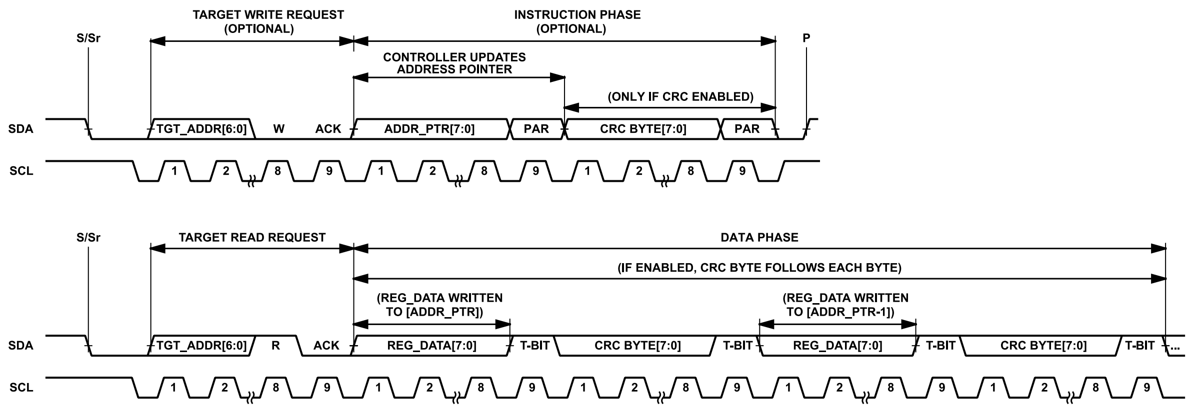

Figure 62. AD4060 Register Read Sequence

SERIAL INTERFACE

REGISTER ACCESS CRC

The AD4060 includes optional error checking for register reads and writes based on CRC-8, using the following polynomial:

$$x^8 + x^2 + x + 1 \quad (5)$$

The CRC is enabled by setting the CRC_EN and CRC_EN_B bit fields to 0x1 and 0x2, respectively. When the CRC is enabled, an 8-bit checksum code is appended to each register data byte. The value of the checksum is calculated from the data read or written over the I3C bus, which allows the AD4060 and the controller to detect corrupted serial communications.

The CRC bytes are half duplex and are only sent by the controller or the target at any one time. The CRC-8 calculation is seeded by a nonzero value to detect if the SDA is stuck low. The seed for the first CRC following each ACK bit is 0xA5. Table 20 summarizes the data and seed values for all possible register read and write transactions in configuration mode.

When the AD4060 receives a checksum that is inconsistent with its corresponding I3C transaction, the transaction is considered invalid, and the CRC_ERR bit in the INTERFACE_STATUS register is set to 1. The CRC_ERR bit is a write-1-to-clear bit (R/W1C). When the CRC is enabled, it is recommended to check the CRC_ERR bit after each register read and write attempt.

For register writes and ADDR_PTR writes, the controller must send a valid CRC byte following each byte of data. The CRC bytes following the register writes and ADDR_PTR writes also have a parity bit that the AD4060 verifies before updating the write data. When a register write has an invalid CRC, the contents of the register are not updated, and the CRC_ERR bit is asserted.

For register reads, the AD4060 calculates and sends a CRC byte following the register data. The CRC byte transmitted by the AD4060 following the first register read data byte factors in its dynamic address so that the controller can validate that it is accessing data from the intended device. When the controller receives an invalid CRC, the data must be assumed corrupted. The controller should ignore the received data and retry the register read.

Table 20. CRC Data and Seed Values for I3C Writes

Instruction Phase CRC		Data Phase CRCs	
Seed Input	Data Input	Seed Input	Data Input
0xA5	TGT_ADDR, RnW Bit, ADDR_PTR[7:0] Byte	LSByte of Current Register Address	Data Phase Byte(s)

Table 21. CRC Data and Seed Values for I3C Reads

First Data Phase CRC		Subsequent Data Phase CRCs	
Seed Input	Data Input	Seed Input	Data Input
0xA5	TGT_ADDR, RnW Bit, Data Phase Byte(s)	LSByte of Current Register Address	Data Phase Byte(s)

SERIAL INTERFACE

CONV_READ REGISTER

The CONV_READ register can be used to trigger continuous ADC conversions in a loop where reading the conversion results of one ADC conversion initiates the next ADC conversion.

To trigger ADC conversions using the CONV_READ register, update the ADDR_PTR to point to any of the register addresses of the CONV_READ register (from 0x50 to 0x53). Then, perform a dummy I3C read from the AD4060 and issue a repeated start (Sr) followed by a stop (P) at the end of the data phase. The SDA rising edge of the stop (P) triggers an ADC convert-start as shown in Figure 63. In sample mode, the convert-start trigger results in a single conversion. In burst averaging mode, the convert-start trigger results in a burst of multiple conversions which are used to generate a single averaged result (see the Modes of Operation section).

When the next I3C read is performed, the data bits read from the target will be the ADC conversion results stored in CONV_READ. The repeated start (Sr) followed by a stop (P) of this read will trigger the next ADC conversion, and therefore the host can repeatedly read from CONV_READ to continuously generate and read back ADC samples.

Note that before reading conversion results from CONV_READ, it is important to ensure that the correct number of data bytes will be read from the AD4060 depending on the operating mode. Table 22 shows the contents of the CONV_READ register for sample mode, trigger mode, and burst averaging mode. Table 17 shows the recommended ADDR_PTR setting for reading out data in each mode to minimize the number of bytes to be read per conversion.

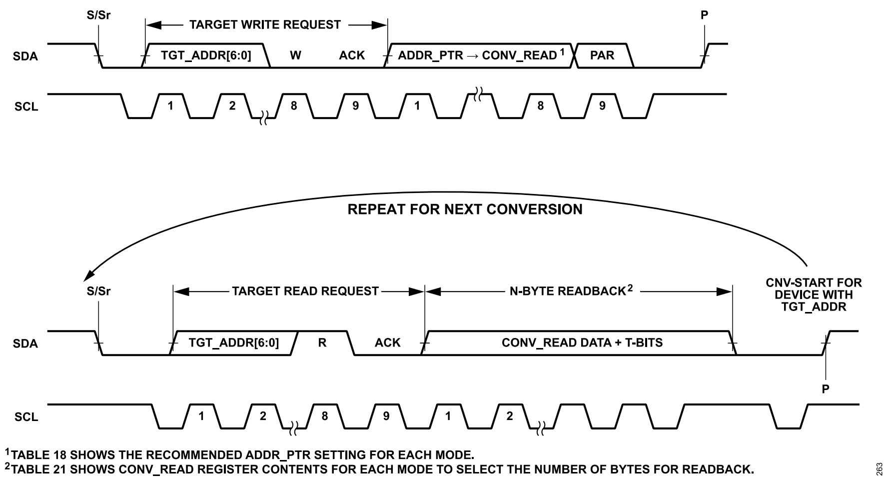

Figure 63. Triggering ADC Conversions Using CONV_READ

Table 22. CONV_READ Register Contents

ADC Mode	Byte 0x53 (CONV_READ [31:24])	Byte 0x52 (CONV_READ [23:16])	Byte 0x51 (CONV_READ [15:8])	Byte 0x50 (CONV_READ [7:0])
Sample Mode and Trigger Mode	SE[15:8][1]	SE[7:0]	SE[3:0], DATA[11:8]	DATA[7:0]
Burst Averaging Mode	SE[15:8]	SE[7:0]	SE[1:0], DATA[13:8]	DATA[7:0]

[1] SE refers to the Sign Extension bits. When the ADC is in differential mode, the value of the SE bits is the same as the most significant data bit. When the ADC is in single-ended mode, the SE bits are always = 0.

SERIAL INTERFACE

CONV_TRIGGER REGISTER

The CONV_TRIGGER register is an alternative to the CONV_READ register that allows for triggering ADC conversions or entering autonomous modes. CONV_TRIGGER allows the controller to trigger simultaneous sampling of multiple AD4060 devices on the same bus using group addressing.

To trigger an ADC conversion using the CONV_TRIGGER register, perform an I3C write to the target device, and update the ADDR_PTR to point to any of the register addresses of CONV_TRIGGER (0x56 to 0x59). The convert-start trigger occurs on the SDA rising edge of the stop (P) as shown in Figure 64. In sample mode, the convert-start trigger results in a single conversion. In burst averaging mode, the convert-start trigger results in a burst of multiple conversions which are used to generate a single averaged result (see the Modes of Operation section).

While the ADDR_PTR is still pointing to CONV_TRIGGER, the results of the previous conversion can be read by performing an I3C read from the target device after the data is ready. Table 23 shows the contents of the CONV_TRIGGER register for sample mode, trigger mode, and burst averaging mode. Table 17 shows the recommended ADDR_PTR setting for reading out data in each mode.

If IBIs are enabled, performing ADC conversions via the CONV_TRIGGER register results in the DATA_READY_IBI (see the In-Band Interrupts section for detail).

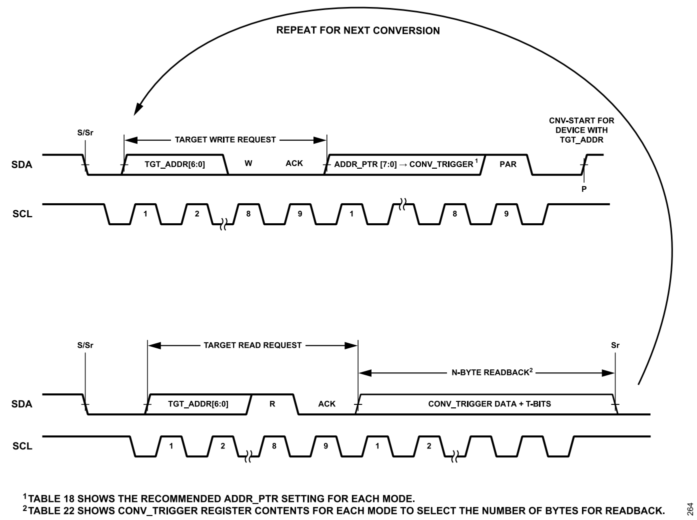

Figure 64. Using CONV_TRIGGER to trigger ADC conversions

Table 23. CONV_TRIGGER Register Contents

ADC Mode	Byte 0x59 (CONV_TRIGGER [31:24])	Byte 0x58 (CONV_TRIGGER [23:16])	Byte 0x57 (CONV_TRIGGER [15:8])	Byte 0x56 (CONV_TRIGGER [7:0])
Sample Mode and Trigger Mode	SE[15:8][1]	SE[7:0]	SE[3:0], DATA[11:8]	DATA[7:0]
Burst Averaging Mode	SE[15:8]	SE[7:0]	SE[1:0], DATA[13:8]	DATA[7:0]

1 SE refers to the Sign Extension bits. When the ADC is in differential mode, the value of the SE bits is the same as the most significant data bit. When the ADC is in single-ended mode, the SE bits are always = 0.

SERIAL INTERFACE

DATA PHASE NINTH SDA BIT

In the data phase of an I3C read or write command, the data is sent or received by the AD4060 in 8-bit packets.

In an I3C write command, each byte of data is followed by the parity bit which is calculated using odd parity and is sent form the controller to the target during the ninth SCL clock period. This data byte along with the parity bit is used by the AD4060 to determine if any errors occurred during the transmission of this data. If the AD4060 receives an even number of 1s in the data plus parity bits, then this data byte is discarded and treated as an invalid write. The AD4060 then waits for the controller to issue a stop (P) or a repeated start (Sr). When a parity error is detected, the PARITY_ERROR bit field in the INTERFACE_STATUS_A register is set to 1. PARITY_ERROR is a W1C field and needs to be cleared by the user before proceeding.

In an I3C read command, the data byte is followed the T-bit which is sent from the AD4060 to the controller during the ninth SCL high period. T = 0 forces the digital host to end the current readback, while T = 1 allows the digital host to either continue or end the current readback.

During register reads, the AD4060 always outputs T = 1, so the controller can decide to continue reading the next register byte (as shown in Figure 6) or end the frame (as shown in Figure 7 and Figure 8).

During direct CCCs that involve the target device sending data to the controller (for example, GETPID, GETBCR, GETDCR, GET-STATUS, and GETCAPS), the T-bit is set to 0 after the last required data byte is sent to the controller to force the end of the CCC.

COMMON COMMAND CODES (CCCS)

Common Command Codes (CCCs) are the I3C command set as described by MIPI specifications in Section 5.1.9. Table 24 shows the CCCs that the AD4060 supports. CCCs are categorized as either broadcast (sent to all targets on the I3C bus) or direct (sent to one specific target on the bus). Section 5.1.9.1 of the MIPI specifications describes the I3C frame format for a broadcast vs a direct CCC.

Table 24. Common Command Code Support for the AD4062

CCC	Description	Supported Format	Command Code(s)
ENEC	Enable Events	Direct Broadcast	0x80 0x00
DISEC	Disable Events	Direct Broadcast	0x81 0x01
RSTDAA	Reset Dynamic Address Assignment	Broadcast	0x06
ENTDAA	Enter Dynamic Address Assignment	Broadcast	0x07

Table 24. Common Command Code Support for the AD4062 (Continued)

CCC	Description	Supported Format	Command Code(s)
RSTACT	Target Reset Action	Broadcast	0x2A, 0x9A
RSTGRPA	Reset Group Address	Direct Broadcast	0x9C 0x2C
SETNEWDA	Set New Dynamic Address	Direct	0x88
GETPID	Get Provisioned ID	Direct	0x8D
GETBCR	Get Bus Characteristics Register	Direct	0x8E
GETDCR	Get Device Characteristics Register	Direct	0x8F
GETSTATUS	Get Device Status	Direct	0x90
GETCAPS	Get Optional Feature Capabilities	Direct	0x95
SETGRPA	Set Group Address	Direct	0x9B

The following sections describe each CCC and its format in more detail.

ENEC/DISEC

The ENEC and DISEC direct or broadcast CCCs can be used to enable or disable target driven IBIs, respectively.

Figure 67 shows the target events byte that is transmitted by the controller to the target during the ENEC/DISEC CCC. Setting the ENINT bit = 1 in the ENEC command byte enables IBIs for the AD4060. Setting DISINT = 1 in the DISEC Command Byte disables IBIs for the AD4060. The ENHJ, ENCR, DISHJ, and DISCR bits are don't care for the AD4060.

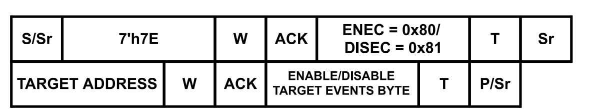

Figure 65. ENEC/DISEC Direct Format

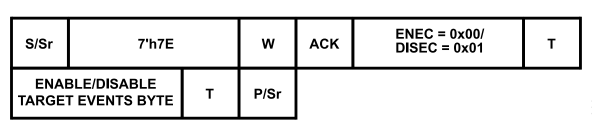

Figure 66. ENEC/DISEC Broadcast Format

SERIAL INTERFACE

TARGET EVENTS BYTE FOR ENEC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RESERVED				ENHJ (DON'T CARE)	RESERVED	ENCR (DON'T CARE)	ENINT

TARGET EVENTS BYTE FOR DISEC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RESERVED				DISHJ (DON'T CARE)	RESERVED	DISCR (DON'T CARE)	DISINT

Figure 67. ENEC/DISEC Target Events Byte

RSTDAA

The RSTDAA broadcast CCC indicates all target devices connected on the I3C bus to clear/reset their controller-assigned dynamic addresses

S/Sr	7'h7E	W	ACK	RSTDAA = 0x06	T	P/Sr

Figure 68. RSTDAA Broadcast Format

RSTACT

The RSTACT CCC can be used to configure the reset actions that will be performed by a target device when it is commanded to perform a reset by the controller (see the Reset Bits and Reset Pattern sections for more detail). MIPI specifications define RSTACT as a broadcast, direct read or a direct write type CCC. However, the AD4060 only supports the broadcast version of the RSTACT CCC.

S/Sr	7'h7E	W	ACK	RSTACT = 0x2A	T
DEFINING BYTE	T	P/Sr			

Figure 69. RSTACT Broadcast Format

In the broadcast format of RSTACT, the controller sends a defining byte (DByte) to the target devices which indicates the target reset action. Section 5.1.9.3.26 of the MIPI specifications lists the DByte values available for the controller to use. The AD4060 only supports DByte values of 0x00, 0x01, and 0x02. Table 25 highlights the reset actions for the AD4060 based on the DByte value received from the controller.

Table 25. AD4060 RSTACT Actions

RSTACT Defining Byte Value	Reset Action
0x00	No Reset
0x01	I3C Peripheral Only Reset[1]
0x02	I3C peripheral, fuse reload, register map, and address pointer reset.

[1] An I3C peripheral reset resets the target's dynamic assigned address (both target and group), as well as other fields set by the CCC commands. It does not include the register memory map, hence none of the registers/bit fields are reset, nor are the fuses reloaded. The controller must perform the dynamic address assignment routine again following an I3C peripheral reset.

ENTDAA

The ENTDAA broadcast CCC indicates all target devices connected on the I3C bus to enter the dynamic address assignment mode as described in Section 5.1.4 of the MIPI specifications.

S/Sr	7'h7E	W	ACK	ENTDAA = 0x07	P/Sr	ACK
DAA MODE	P					

Figure 70. ENTDAA Broadcast Format

SETNEWDA

The SETNEWDA direct CCC can be used to assign a new dynamic address to a target device on the I3C bus that already has a controller-assigned dynamic address. The use of this CCC is invalid if the target device does not already have a dynamic address. After the use of this CCC, the target device shall only respond to its newly assigned dynamic address and ignore the previous one.

S/Sr	7'h7E	W	ACK	SETNEWDA = 0x88	T	Sr
CURRENT TARGET ADDRESS	W	ACK	NEW 7-BIT DYNAMIC ADDRESS	1'b0	T	P/Sr

Figure 71. SETNEWDA Direct Format

RSTGRPA

The RSTGRPA direct or broadcast CCC indicates target devices to reset/clear their controller-assigned group addresses. This CCC gives the controller the ability to disband any created groups. When used in direct (individual) mode, a target that receives this command shall clear the group address assigned to it, thus removing itself from the group. When used in direct (group) mode, all devices in the group shall clear their group address, thus disbanding the group. In broadcast mode, all targets shall clear all of their group addresses thus removing all groups from the I3C bus.

S/Sr	7'h7E	W	ACK	RSTGRPA = 0x9C	T	Sr
TARGET ADDRESS	W	ACK	P/Sr			

Figure 72. RSTGRPA Direct (Individual) Format

S/Sr	7'h7E	W	ACK	RSTGRPA = 0x9C	T	Sr
GROUP ADDRESS	W	ACK	P/Sr			

Figure 73. RSTGRPA Direct (Group) Format

S/Sr	7'h7E	W	ACK	RSTGRPA = 0x2C	T	P/Sr

Figure 74. RSTGRPA Broadcast Format

SETGRPA

The SETGRPA direct CCC can be used to assign a group address to a target device on the I3C bus that already has a dynamic

SERIAL INTERFACE

address assigned. The use of this CCC is invalid for a target device that does not already have a controller-assigned dynamic address. The target's dynamic address is be used to initiate this CCC and then it can be assigned a group address as well. After assigning a group address to a target, it shall respond to both its dynamic address and the group address when addressed by the controller.

Once the AD4060 has been assigned a group address after the successful use of the SETGRPA CCC, this group address can be read from the GRP_ADDR_REG register. Until group address has been assigned, the GRP_ADDR_REG always returns its default value of 7'h7E.

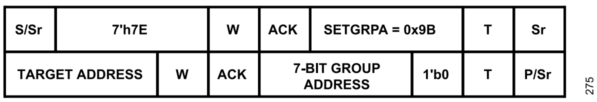

Figure 75. SETGRPA Direct Format

GETPID

The GETPID direct CCC can be used by the controller to obtain the 48-bit provisional ID (PID) from a target device. The PID is used in the dynamic address assignment procedure as described in Section 5.1.4 of the MIPI specifications. Upon receiving this CCC, the target device transmits six bytes of the PID with the MSB first. (See the Dynamic Addressing section for more detail about the AD4060's 48-bit PID).

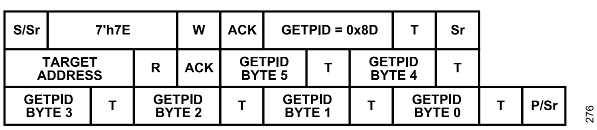

Figure 76. GETPID Direct Format

GETBCR

The GETBCR direct CCC can be used by the controller to obtain the bus characteristics register (BCR) value from a target device on the I3C bus. The BCR is transmitted by the target as one byte with the MSB first.

Upon receiving the GETBCR CCC, the AD4060 transmits the values described in Table 26 as its BCR.

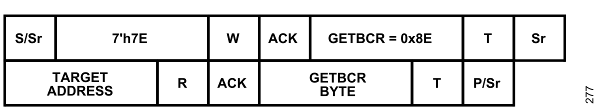

Figure 77. GETBCR Direct Format

Table 26. AD4060 Bus Characteristics Register Byte

Bit Field Offset	Bit Field Name	Value	Characteristic
BCR[7:6]	Device Role [1:0]	2'b00	I3C target only
BCR[5]	Advanced Capabilities	1'b1	Supports some advances capabilities. See the GETCAPS section

Table 26. AD4060 Bus Characteristics Register Byte (Continued)

Bit Field Offset	Bit Field Name	Value	Characteristic
BCR[4]	Virtual Target Support	1'b0	No virtual target support
BCR[3]	Offline Capable	1'b0	Always responds to I3C commands
BCR[2]	IBI Payload	1'b1	IBIs contain one mandatory data byte
BCR[1]	IBI Request Capable	1'b1	Capable of sending IBIs
BCR[0]	Max Data Speed Limitation	1'b0	No limitation

GETDCR

The GETDCR direct CCC can be used by the controller to obtain the device characteristics register (DCR) value from a target device on the I3C bus. The BCR is transmitted by the target as one byte with the MSB first.

Upon receiving the GETDCR CCC, the AD4060 transmits an 8'b00 as the GETDCR byte indicating a generic device type as defined by MIPI.

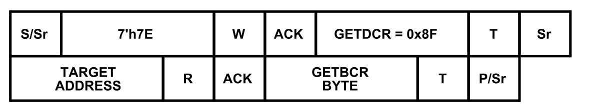

Figure 78. GETDCR Direct Format

GETSTATUS

The GETSTATUS direct CCC can be used by the controller to obtain the status bytes of a target on the I3C bus. The GETSTATUS CCC has two formats as described in Section 5.1.9.3.15 of the MIPI specifications. The AD4060 only supports Format 1 and does not support Format 2. If the AD4060 receives the GETSTATUS CCC with Format 2, it NACKs its address on the SDA line.

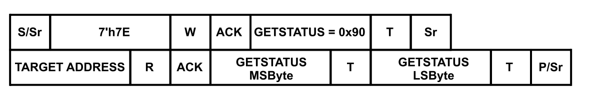

Figure 79. GETSTATUS Direct Format

Upon receiving the GETSTATUS CCC Format 1, the AD4060 transmits the following two bytes to the controller as defined in Table 27.

Table 27. AD4060 GETSTATUS Bytes

Byte	Bits	Field	Value	Description
MSB	15:8	Vendor Reserved	DEVICE_STATUS[7:0]	Bit fields in the device status register
LSB	7:6	Activity Mode	2'b00	Power mode bit field in the DEVICE_CONFIG register

SERIAL INTERFACE

Table 27. AD4060 GETSTATUS Bytes (Continued)

Byte	Bits	Field	Value	Description
	5	Protocol Error	1'b1: Protocol Error Detected 1'b0: No Protocol Error	Indicates if the target detected a protocol error since the last status read
	4	Reserved	1'b0	Reserved by MIPI
	3:0	Pending Interrupt	MDB[3:0]	Lowest four bits of the mandatory data byte register

GETCAPS

The GETCAPS direct CCC allows the controller to obtain the optional feature set support for a target device on the I3C bus. The GETCAPS CCC has two formats as described in Section 5.1.9.3.19 of the MIPI specifications. The AD4060 only supports GETCAPS Format 1. If the AD4060 receives a GETCAPS Format 2 CCC, it NACKs its address on the SDA line.

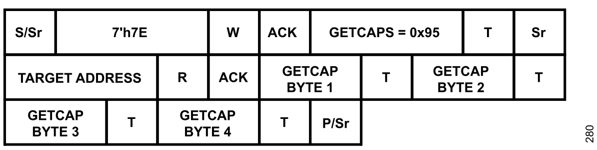

Figure 80. GETCAPS Direct Format

Upon receiving the GETCAPS CCC Format 1, the AD4060 transmits the four GETCAPS bytes described in Table 28.

Table 28. AD4060 GETCAPS Byte

GETCAPS Byte	Bit Field	Value	Description
GETCAP1	7:0	8'b00	No HDR support
GETCAP2	7:6	2'b00	No HDR support
	5:4	2'b01	Support for one group address
	3:0	4b'0001	Conforms to I3Cv1.1 specifications
GETCAP3	7	1'b0	Reserved by MIPI
	6	1'b1	Support for pending read notification
	5	1'b0	No HDR support
	4	1'b0	No GETSTATUS Format 2 support
	3	1'b0	No GETCAPS Format 2 support
	2	1'b0	No support for device-to-device transfer IBI
	1	1'b0	No support for device-to-device transfers
	0	1'b0	No support for multilane data transfer
GETCAP4	7:0	8'b00	Reserved by MIPI

DEVICE RESET

A device reset returns the device registers to the default settings and resets the AD4060 target address. The following sections describe the AD4060 device reset mechanisms.

The AD4060 includes a hardware interrupt signal (DEV_RDY) that indicates when the device reset is complete. The DEV_RDY signal is active high and is assigned to the GP1 pin by default, so the digital host can monitor the GP1 pin for a rising edge to inform the firmware that the AD4060 is ready for operation. See the Device Ready Signal for more information.

The DEVICE_RESET bit in the DEVICE_STATUS register indicates when a device reset has occurred. The DEVICE_RESET bit is a write-1-to-clear bit and holds its state until the host writes it to the value 1'b1. The DEVICE_RESET bit can be referenced to confirm a reset executed as expected or if an unintended reset occurred (for example, if the power supplies failed during operation).

Reset Bits

A reset is initiated by setting both the SW_RESET_MSB and SW_RESET_LSB bits in the INTERFACE_CONFIG_A register to 1'b1 in the same write instruction (see the Interface Configuration A Register section). Two reset bit fields are used to reduce the likelihood of an unintended reset from interference on the I3C bus. Using these reset bits performs a fuse reload and resets the register map and the address pointer values. It does not reset the I3C peripheral.

Figure 81 shows the timing diagram for resetting the AD4060 with the reset bits. The digital host must wait for the $t_{RESET\_FUSE\_RELOAD}$ delay to elapse before initiating I3C transactions (see Timing Specifications).

Reset Pattern

The reset pattern shown in Figure 82 allows the digital host to reset the AD4060 from any of its operating modes.

The reset pattern is described in Section 5.1.11.3 of the MIPI specifications and is equivalent to fourteen SDA transitions while SCL is kept low, followed by a repeated start (Sr) and a stop (P). Figure 82 shows the timing diagram for resetting the AD4060 with the reset pattern. The digital host must wait for the delay time associated with the reset action of the device (see the Table 5) to elapse before initiating I3C transactions.

The RSTACT CCC is used to assign a reset action for the AD4060 (see RSTACT section). If the AD4060 does not have a reset action defined yet, sending the reset pattern once only resets the I3C peripheral, and a second time performs a full device reset.

If the AD4060 does have a reset action defined, then the AD4060 takes the reset action mentioned in Table 25 when the reset pattern is issued.

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Power-On Reset

The AD4060 is designed to generate a power-on reset (POR) when the VDD and VIO rails are first applied or when the rails are power cycled. A POR on the VDD or VIO supplies resets the state of the user configuration registers. The configuration registers are not reset when the AD4060 enters sleep mode and disables the internal LDO regulator (see the Sleep Mode section).

Figure 83 shows the timing diagram for the AD4060 PORs. The controller must wait for the $t_{RESET\_FUSE\_RELOAD}$ delay after the power supplies are stable. Then the controller can send the broadcast RSTACT CCC with DByte = 0x02 followed by a reset pattern, or the controller can send the reset pattern twice to perform a full reset (see Figure 83 and Figure 84). Finally, an additional $t_{RESET\_FUSE\_RELOAD}$ delay must elapse before performing other I3C transactions.

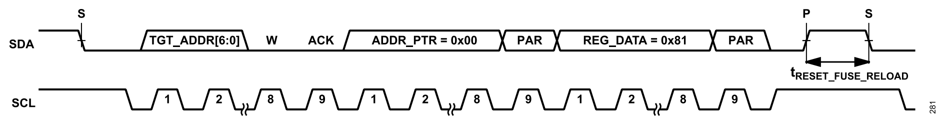

Figure 81. Reset Bit Timing Diagram

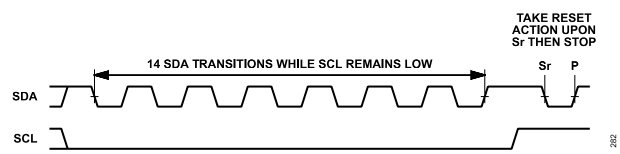

Figure 82. Reset Pattern Timing Diagram

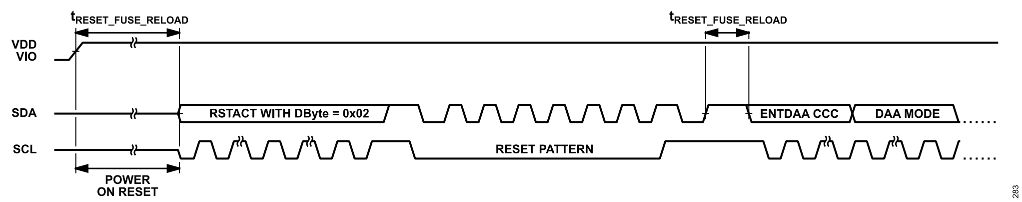

Figure 83. POR Timing Diagram with RSTACT

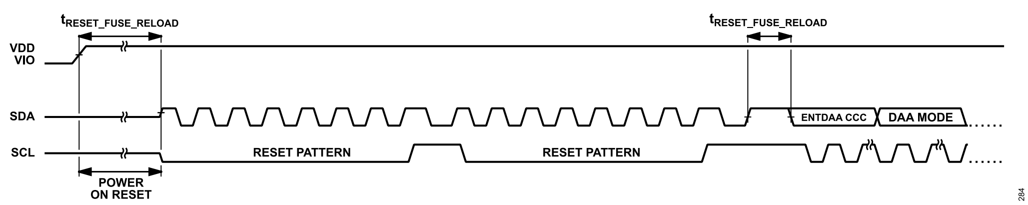

Figure 84. POR Timing Diagram with 2 Reset Patterns

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TYPICAL APPLICATIONS DIAGRAM

Figure 85 shows an example connection diagram with the AD4060. Common companion circuitry for the AD4060 includes power management, voltage reference circuitry, analog front-end and signal conditioning circuitry, and an I3C-compatible digital host (such as a microcontroller or a field programmable gate array (FPGA)).

The components shown in Figure 85 are general recommendations for best performance when operating the AD4060 and not intended for all use cases. The following sections provide more guidelines for component selection.

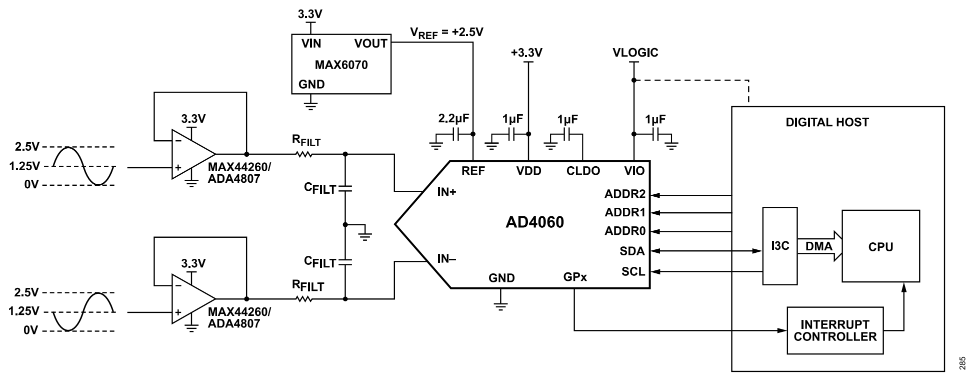

Figure 85. AD4060 Typical Application Diagram

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ANALOG FRONT-END DESIGN

Wide Input Common-Mode Range

The AD4060 analog inputs feature a wide common-mode input voltage range that is only restricted by the absolute voltage range for each input (see Table 1). The IN+ and IN− signals can span anywhere between 0V and V_{REF} without violating the common-mode input voltage specification (V_{CM}), ensuring compatibility with both differential and single-ended type signals. The V_{CM} voltage is given in the following equation and illustrated in Figure 86.

The AD4060 convert the differential voltage between IN+ and IN−, and the common-mode signal is attenuated by the CMRR (see Table 1 and Figure 20).

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \quad (6)$$

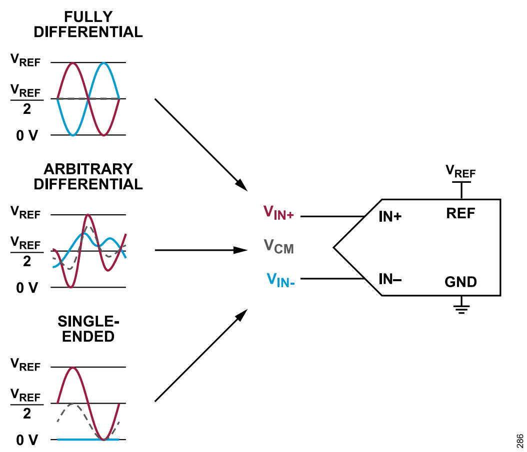

Figure 86. AD4060 Wide Input Common-Mode Range

AD4060 Equivalent Analog Input Model

As described in the Analog Inputs section, the AD4060 analog inputs can be modeled as switched capacitive loads, with the IN+ and IN− inputs each connected to a 3.4 pF sampling capacitor through a set of sampling switches (SW1). As part of each conversion phase, the SW1 switch disconnects and reconnects the sampling capacitors (C_{IN}) from the IN+ and IN− pins, causing transient input current and voltage glitches at the output of the AFE circuit. The small C_{IN} of the AD4060 ensures the magnitude of the transient current and voltage spikes is minimal compared to other SAR ADCs, but the AFE must still be designed to settle these glitches quickly enough (before the next conversion) to meet the accuracy and performance specifications in Specifications.

AD4060 Equivalent Analog Input Model shows an equivalent load circuit model of the AD4060 IN+ and IN− inputs. SW1 represents the sampling switches and SW2 represents the C_{IN} reset switch. The SW1 switch opens at the beginning of the conversion phase to sample the IN+ and IN− voltages on the C_{IN} capacitors. Before the start of the acquisition phase, the SW2 switch shorts the sampling capacitors together to reset them to a known, predictable state. Because the C_{IN} capacitance is the same for both IN+ and IN−, the reset voltages on each capacitor are equivalent and are given by the following equation:

$$\frac{V_{IN+} + V_{IN-}}{2} \quad (7)$$

where V_{IN+} and V_{IN-} are the sampled IN+ and IN− voltages, respectively. Note that this formula is the same as the common-mode input voltage formula given in Wide Input Common-Mode Range.

As mentioned in the Converter Operation section, the AD4060 acquisition and conversion phases overlap. The acquisition phase starts 210ns after the start of the conversion phase. At the start of the acquisition phase, the SW2 switch opens and the SW1 switch closes to reconnect C_{IN} to the AD4060 inputs to acquire the signal. At the instant SW1 closes, the IN+ and IN− inputs sink or source some charge from the AFE circuit to recharge the C_{IN} capacitors to the intended signal voltage. The transient current spike causes transient voltage glitches on each pin, with magnitudes that are a function of the amount of charge pulled by the C_{IN} capacitors and the output impedance of the AFE circuit.

The SW2 switch is implemented to minimize linearity errors if the AFE cannot completely settle the input glitch before the next conversion phase. The SW2 switch ensures the charge transfer per sample is linearly related to the input signal voltage. The worst-case current and voltage glitch magnitude occur when the differential input voltage is equal to V_{REF}. For example, when V_{IN-} = 0V, and V_{IN+} = V_{REF} = 3.3V, the charge transfer per sample is 5.6pC into the IN− input and out of the IN+ input. The steady-state input current is, therefore, also linearly related to input voltage, as shown in Figure 22. Settling error with the AD4060, therefore, appears as additional gain error rather than degradation in INL and THD.

An RC kickback filter is recommended on each of the IN+ and IN− pins to attenuate the voltage glitch on the output of the AFE circuit (see Figure 85). The Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter article provides guidance for selecting the RC components of the kickback filter to ensure proper settling. Table 29 provides general RC component recommendations for the AD4060 for several sample rates (R_{FILT} and C_{FILT} are the resistor and capacitor values in the RC kickback filter, respectively). The values in Table 29 are provided for initial guidance, and the system designer must verify the companion amplifier is stable driving these RC loads. The values corresponding to sample rates of 500kSPS and above are only applicable for the burst of conversions during the burst averaging mode.

The AD4060 LTspice model emulates the equivalent analog input model shown in Figure 87 when configured for transient simulations.

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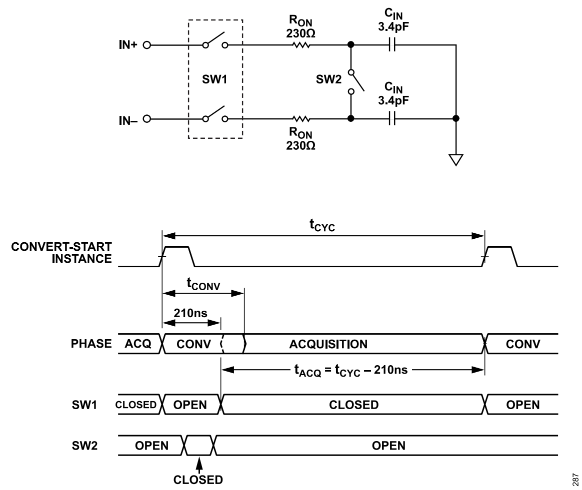

Figure 87. AD4060 Equivalent Input Load Model

Table 29. AD4060 RC Kickback Filter Recommendations

Sample Rate	t_{ACQ}	R_{FILT}	C_{FILT}	−3dB Bandwidth
2MSPS	290ns	100Ω	1nF	1.59MHz
		200Ω	360pF	2.21MHz
1MSPS	790ns	250Ω	1nF	636.61kHz
		523Ω	360pF	845.30kHz
500kSPS	1790ns	665Ω	1nF	239.33kHz
		1270Ω	360pF	348.10kHz
100kSPS	9790ns	3.57kΩ	1nF	44.5kHz
		6.81kΩ	360pF	64.91kHz

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Noise and Distortion Considerations

The noise and distortion specifications of the AFE circuit must be considered, because they combine with the AD4060 noise and distortion specifications to determine the overall system performance. The total system noise ($v_{N,TOTAL}$) is the root sum of squares (RSS) of the AFE RMS noise ($v_{N,AFE}$) and ADC RMS noise ($v_{N,ADC}$), referred to the inputs of the AD4060 as shown the following equation:

$$v_{N,TOTAL} = \sqrt{v_{N,AFE}^{2} + v_{N,ADC}^{2}} \quad (8)$$

MT-049 and *MT-050* describe how to estimate $v_{N,AFE}$ for operational amplifier circuits, as a function of the amplifier and passive component noise specifications and amplifier configuration. The *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter* article describes how to estimate system SNR vs. $v_{N,AFE}$ and $v_{N,ADC}$.

As noted in the AD4060 Equivalent Analog Input Model section, the primary purpose of the RC kickback filter between the AFE and the ADC is to minimize settling error and not to filter AFE noise or perform anti-aliasing. The RC kickback filter bandwidth cannot be set arbitrarily low, and it is recommended to implement any additional noise or anti-alias filtering before or within the amplifier circuit instead of the RC kickback filter. NP0/C0G type dielectric capacitors are recommended for all capacitors used in the AFE circuit to minimize signal distortion artifacts caused by capacitor voltage and temperature derating.

REFERENCE CIRCUIT DESIGN

Equivalent REF Input Model

The AD4060 requires an external voltage reference to define the input range of the device. A low-noise, stable reference is critical for maximizing accuracy and performance.

The AD4060 REF pin draws charge (Q_{CONV}) from the external reference circuit during each conversion phase to perform the SAR ADC bit trials. The REF input current (I_{REF}) can, therefore, be expressed as a transient current load that occurs once per conversion and as an equivalent average DC current load that is a function of the sample rate (see Table 1 and Figure 23). The voltage reference circuit must maintain a stable and accurate V_{REF} voltage, despite the charge transient from the AD4060 REF pin, to prevent gain error or stuck bits in the conversion results.

A reference decoupling capacitor (C_{REF}) is strongly recommended to supply the instantaneous charge drawn by the REF pin while maintaining the V_{REF} voltage to within an LSB. For optimal performance, populate C_{REF} with a 2.2 µF capacitor with a case size of 0402 or larger to ensure suitable capacitor voltage coefficient. For space-constrained applications, a 1µF capacitor in a case size of 0201 may be used with slight degradation to gain error and INL. Place the C_{REF} capacitor on the same PCB layer and as close to the REF pin as possible with a wide trace to minimize series impedance (see the Layout Recommendations section).

While the AD4060 is idling (not performing conversions), the REF pin draws only a small standby current (8 nA). In applications where the AD4060 intermittently switches between idling and performing bursts of conversions (for example, when using burst averaging mode), the I_{REF} quickly shifts from near-zero current to 60µA/15µA for f_S = 2MSPS/500kSPS. This step in load current triggers an output load transient response in the reference circuit that must be considered if V_{REF} varies by more than ½ LSB. The MAX6070 voltage reference is recommended for its exceptional transient response with low power dissipation. Figure 88 illustrates the transient loading effects on the reference circuit in response to a burst of conversions.

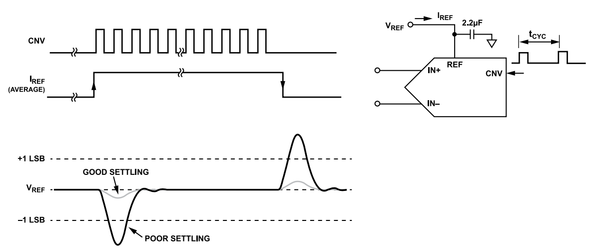

Figure 88. Burst Sampling and Voltage Reference Settling

Reference Noise Considerations

The voltage reference circuit noise is critical for achieving the system-level dynamic range and SNR target specifications. For large input signals near full scale, any noise from the reference circuit will couple into the conversion results and modulate around the fundamental frequency. Reference noise will also limit the SNR and resolution improvements gained from using high averaging ratios in burst averaging mode.

SYNCHRONIZED AMPLIFIER SHUTDOWN AND ADC SAMPLING

The DEV_EN signal is an amplifier power-down signal generated by the AD4060 and synchronized to the ADC to maximize amplifier power-up settling time prior to the sampling instant. Figure 46 shows a typical connection diagram when using the AD4060 DEV_EN signal with an operational amplifier. The DEV_EN signal is assigned to the GP0 output pin in this example.

When the DEV_EN signal is asserted (see the Device Enable Signal section), it enables the connected amplifier. The sampling instant is delayed until the user-programmable t_{PWR_ON} delay elapses. After the t_{PWR_ON} delay elapses, the DEV_EN signal is deasserted to power down the amplifier. Consult the amplifier data sheet for its shutdown pin logic levels to ensure compatibility with the AD4060 logic levels that are set by the VIO voltage and given in Specifications.

To ensure the amplifier output settles before the ADC sampling instant, set the t_{PWR_ON} delay to be longer than the amplifier turn-on time specification. Turn-on time indicates the time needed for the amplifier output to settle to a specified accuracy following assertion of its ENABLE/$\overline{\text{SHUTDOWN}}$ input. Note that turn-on time varies

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for different loads and amplifier configurations. The *Introduction to Dynamic Power Scaling* article provides guidance on configuring and evaluating operational amplifier power cycling relative to the SAR ADC sampling.

See Figure 51 and Figure 55 for timing diagrams using DEV_EN in the various AD4060 operating modes.

ACHIEVING HIGH ACCURACY WITH REFERENCE SHUTDOWN

Low-noise, high-accuracy voltage references are generally recommended to pair with precision SAR ADCs to maximize system-level performance. The voltage reference circuit also needs to have low output impedance and fast transient response to deal with the SAR ADC REF input transient load, especially when performing bursts of samples (see the Reference Circuit Design section). Low-power voltage references generally cannot satisfy all of these requirements simultaneously, which often forces system designers to add a reference buffer amplifier, increasing overall system power dissipation.

The MAX6070 is an exceptionally low-power voltage reference that can drive the AD4060 REF pin directly without an intermediate reference buffer amplifier. For extremely power-sensitive applications, however, the AD4060 offer unique features that allow the voltage reference to be disabled without degrading precision.

The AD4060 can select the VDD supply as the V_{REF} source, as described in the Reference Selection Modes section. To maintain accuracy while using VDD as the V_{REF}, the AD4060 can directly measure the ratio between the VDD supply and the REF input voltages and calculate a corresponding digital correction factor to automatically scale the ADC samples accordingly. The digital correction uses the MON_VAL field described in the Gain Scaling section to scale the ADC transfer function between the REF and VDD domains.

The automatic MON_VAL scaling calculation consist of two phases. Figure 89 illustrates the AD4060 configuration while measuring and calculating the MON_VAL digital correction factor. Figure 90 shows the configuration after MON_VAL is updated and the AD4060 begin sampling the inputs with VDD as the V_{REF} source. Table 30 gives the relevant configuration settings for both phases.

In the MON_VAL calculation phase, the REF pin is driven by an accurate voltage reference, like the MAX6070, and the REF pin is selected as the V_{REF} source. The VDD voltage is internally scaled by ½ and sampled by the ADC. When the controller triggers the AD4060 to perform a burst of samples in burst averaging mode, and the averaged result is generated, the AD4060 automatically calculates a 16-bit digital correction factor and loads it into the MON_VAL field. The $\overline{RDY}$ signal can optionally be assigned to the GP0 or GP1 pins to indicate when the calculation is complete.

In the MON_VAL application phase, the ADC is reconfigured to sample the input signal via the IN+ and IN− pins, with VDD selected as the V_{REF} source. The external voltage reference is powered down to reduce system power. When the ADC samples the inputs, the MON_VAL scaling factor is applied to the digital output codes to scale them to the transfer function set by the REF voltage instead of the VDD voltage.

Depending on the stability of the VDD supply circuit, the MON_VAL calculation may need to be repeated periodically to maintain system accuracy targets.

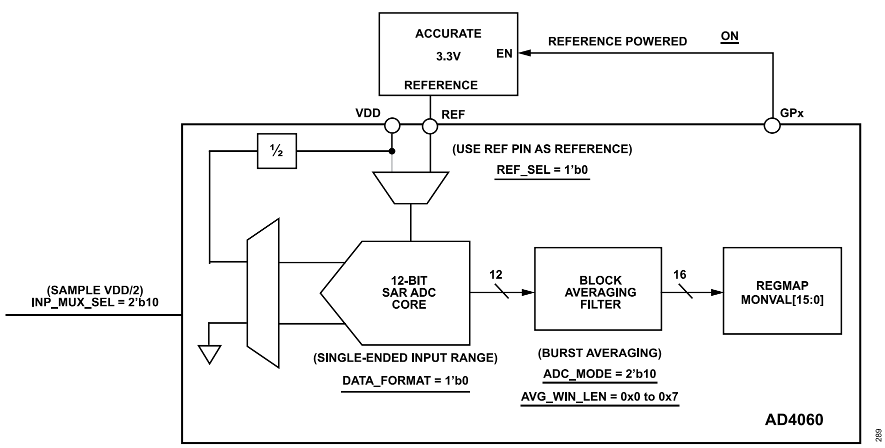

Figure 89. MON_VAL Calculation Configuration

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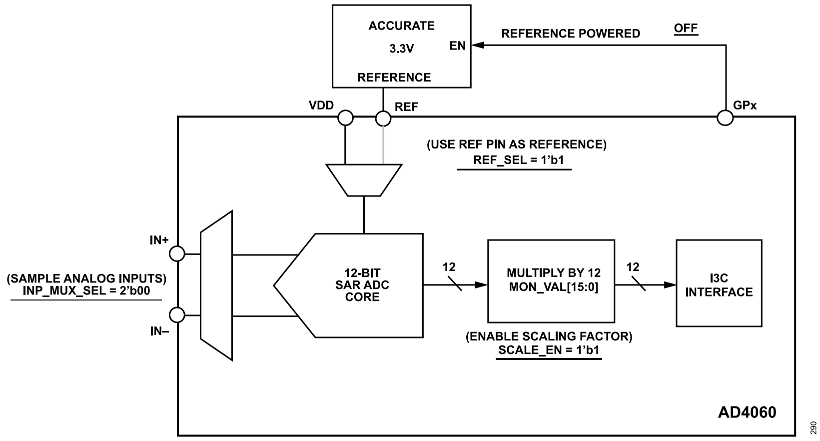

Figure 90. MON_VAL Application Configuration

Table 30. Configuration Settings for MON_VAL Scaling

Bit Field Name	MON_VAL Calculation	MON_VAL Application
REF_SEL	1'b0: V_{REF} = REF	1'b1: V_{REF} = VDD
DATA_FORMAT	1'b0: Single-ended mode	Don't care
INP_MUX_SEL	2'b10: Sample VDD/2	2'b00: sample IN+ and IN−
ADC_MODE	2'b10: Burst averaging mode	Don't care
AVG_WIN_LEN	Don't care[1]	Don't care
SCALE_EN	1'b0: Scaling disabled	1'b1: scaling enabled
GP0_SEL	3'b010: $\overline{\text{RDY}}$ on GP0[2]	Don't care
GP1_SEL	3'b110: Logic high on GP1[3]	3'b011: logic low on GP1[3]

1 MON_VAL calculations do not require a specific value for N_{AVG}, but it is recommended to set N_{AVG} based on the VDD supply circuit noise and the system accuracy targets.

2 Optional. The $\overline{\text{RDY}}$ signal can act as a hardware interrupt to notify the digital host when MON_VAL calculation is complete.

3 Optional. The static logic levels can act as the voltage reference enable pin if its input logic levels are consistent with the AD4060 output logic levels.

VDD POWER DISSIPATION

SAR ADCs such as the AD4060 are ideal for precision measurement applications with tight power dissipation budgets. The ADC core is effectively duty-cycled and only consumes active power while performing a conversion, so the effective power dissipation is lower at slower sample rates. Figure 91 illustrates the instantaneous and average VDD input current (I_{DD}) vs. ADC sampling. Table 1 gives the average supply current and power dissipation for several operating modes and sample rates.

The AD4060 ADC core is exceptionally power efficient and can operate in several lower power operating modes. As described in the Analog Front-End Design section, slower sampling rates also relax the load drive requirements for the AFE and reference circuitry, allowing the AD4060 to interface with low-power amplifiers and voltage references for overall system power optimization.

While the AD4060 is idle, VDD draws only 990nA standby current (see Figure 34). In sample mode, the AD4060 average VDD current is 400µA at 1MSPS, and 120µA at 300kSPS, equivalent to 400pC per conversion. In the autonomous modes, the VDD current is reduced to 112µA at 1MSPS, and 56µA at 500kSPS, equivalent to 112pC per comparison operation. Figure 26 and Figure 29 show the average I_{DD} and power dissipation vs. the ADC sample rate and operating mode. The supply current and power dissipation scale linearly with the sample rate.

In burst averaging mode, the AD4060 performs a burst of conversions to generate an averaged result. The average power dissipation in burst averaging mode is, therefore, a function of the average number of conversions performed per second over many bursts of samples. This is a function of the burst sampling rate, N_{AVG}, and the period of the conversion instances. Figure 92 illustrates the VDD power dissipation over the burst sampling and idle phases in burst averaging mode.

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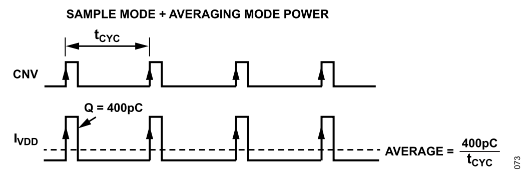

Figure 91. I_{DD} vs. Conversion Periods in Sample Mode

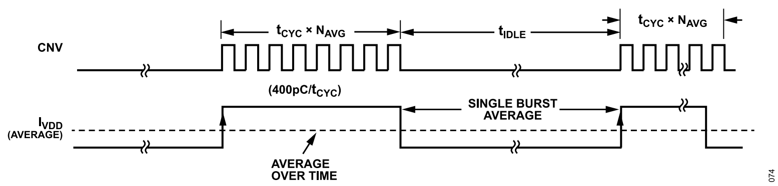

Figure 92. I_{DD} vs. Burst Conversions in Burst Averaging Mode

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CALCULATING SERIAL INTERFACE OUTPUT DATA RATE

The AD4060 ADC core performance is specified for f_S up to 2MSPS, but the maximum achievable output data rate (f_{ODR_MAX}) is a function of the operating conditions and serial interface specifications and may limit the practical f_S, especially in sample mode.

When using CONV_READ to trigger ADC conversions, each read of the conversion result (followed by a repeated start and a stop) results in another ADC conversion. When using CONV_TRIGGER to trigger ADC conversions requires sending a write command to update the Address Pointer to trigger each conversion, followed by a read command to read the conversion results before the triggering the next conversion. Reading from CONV_READ therefore enables a faster f_{ODR_MAX}.

Table 31 shows the maximum serial interface output data rate in sample mode using the CONV_READ and CONV_TRIGGER registers. The maximum output data rate numbers are obtained by assuming all the specifications mentioned in Equation 9 through Equation 19 at their specified minimum values, and using the maximum conversion time of 320ns. t_{OD_Clock} is assumed to be = $t_{LOW\_OD\_Min} + t_{HIGH\_OD\_Min}$ = 232ns. t_{PP_Clock} is assumed to be = 80ns using an f_{SCL} value of 12.5MHz (see Timing Specifications). Since the AD4060 does not have any SDA falling or rising edge rate detection restrictions when SDA is driven by the controller, the controller driven SDA rise and fall times are assumed to be = 0.

Equation 9 to Equation 13 can be used to estimate f_{ODR_MAX} in sample mode using CONV_READ. Equation 14 to Equation 19 can be used to estimate f_{ODR_MAX} in sample mode using CONV_TRIGGER.

Table 31. Maximum Serial Interface Output Data Rate

Conversion register	f_{ODR_MAX}
CONV_READ	251.03kSPS
CONV_TRIGGER	146.88kSPS

$$t_{OD} = t_{CAS} + 9 \times (t_{OD\_Clock}) \quad (9)$$

$$t_{PP} = 18 \times (t_{PP\_Clock}) \quad (10)$$

$$t_{Transition} = t_{CBSr} + t_{CASr} + \tfrac{1}{2}(t_{PP\_Clock}) + t_{CBP} + t_{CONV} \quad (11)$$

$$t_{CYC\_MIN} = t_{OD} + t_{PP} + t_{Transition} \quad (12)$$

$$f_{ODR\_MAX} = {}^{1}/_{t_{CYC}} \quad (13)$$

$$t_{OD} = t_{CAS} + 9 \times (t_{OD\_Clock}) \quad (14)$$

$$t_{PP} = 9 \times (t_{PP\_Clock}) \quad (15)$$

$$t_{Transition} = t_{CBP} + t_{CONV} \quad (16)$$

$$t_{Read} = t_{CAS} + 9 \times (t_{OD\_Clock}) + 18 \times (t_{PP\_Clock}) + t_{CBP} + t_{BUF} \quad (17)$$

$$t_{CYC\_MIN} = t_{OD} + t_{PP} + t_{Transition} + t_{Read} \quad (18)$$

$$f_{ODR\_MAX} = {}^{1}/_{t_{CYC}} \quad (19)$$

where:
t_{CYC} is the minimum achievable sample period.
f_{ODR_MAX} is the maximum achievable output data rate.
t_{CAS} is the clock wait time after a start.
t_{OD_Clock} is a clock period in open drain (see Table 3)
t_{PP_Clock} is a clock period in push pull (see Table 4)
t_{CBSr} is the clock wait time before a repeated start.
t_{CASr} is the clock wait time after a repeated start.
t_{CBP} is the clock wait time before a stop.
t_{CONV} is the ADC conversion time.
t_{BUF} is the wait time between a stop and a start.

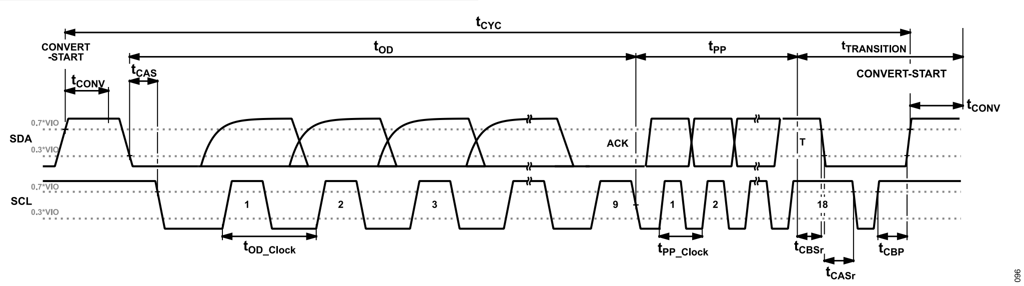

Figure 93. Calculating f_{ODR_MAX} Using CONV_READ

APPLICATIONS INFORMATION

LAYOUT RECOMMENDATIONS

The following PCB layout guidelines are recommended to maximize performance using the AD4060:

- Include a solid ground plane in the PCB layer underneath the AD4060. Ensure there are low-impedance connections between the AD4060 GND pins and the ground plane layer.
- Ensure the analog input and REF traces are physically separated from the digital interface traces to minimize crosstalk from digital signal edges. Include a GND fill between the analog and digital traces. Avoid routing the digital interface traces underneath the AD4060 or the analog signal traces without including a solid ground plane layer in between.
- Ensure the impedance between the voltage reference circuitry and the AD4060 REF pin is as low as possible to prevent V_{REF} settling issues. Place a low effective series resistance (ESR) decoupling capacitor as close to the AD4060 REF pin as possible (see the Reference Circuit Design section). Use wide traces between the voltage reference and the AD4060 REF pin.
- Place the RC kickback filter capacitors as close to the IN+ and IN− pins as possible (see the Analog Front-End Design section).
- Place the supply decoupling capacitors as close to the VDD, CLDO, and VIO pins as possible (see the Power Supplies section).

AD4060 REGISTER SUMMARY

Table 32. AD4060 Register Summary

Address	Name	Description	Reset	Access
0x00	INTERFACE_CONFIG_A	Interface Configuration A.	0x00	R/W
0x01	INTERFACE_CONFIG_B	Interface Configuration B.	0x08	R/W
0x02	DEVICE_CONFIG	Device configuration.	0xF0	R/W
0x03	DEVICE_TYPE	Device type.	0x07	R
0x04	PRODUCT_ID_L	Product identification (LSByte).	0x7A	R
0x05	PRODUCT_ID_H	Product identification (MSByte).	0x00	R
0x06	DEVICE_GRADE	Device grade.	0x00	R
0x0A	SCRATCH_PAD	Scratch pad.	0x00	R/W
0x0C	MANUFACTURER_ID_L	MIPI manufacturer ID (LSByte).	0x77	R
0x0D	MANUFACTURER_ID_H	MIPI manufacturer ID (MSByte).	0x01	R
0x0E	LOOP_COUNT	Reserved.	0x00	R/W
0x0F	TRANSFER_CONFIG	Reserved.	0x00	R/W
0x10	INTERFACE_CONFIG_C	Interface Configuration C.	0x03	R/W
0x11	INTERFACE_STATUS	Interface status.	0x00	R/W
0x21	ADC_MODES	ADC operating mode configuration.	0x80	R/W
0x22	ADC_CONFIG	ADC setup configuration.	0x00	R/W
0x23	AVG_CONFIG	Averaging filter configuration.	0x00	R/W
0x24	GP_CONFIG	General purpose pin configuration.	0xF0	R/W
0x25	INTR_CONFIG	Interrupt configuration.	0x21	R/W
0x27	TIMER_CONFIG	Timer configuration.	0x00	R/W
0x28	MAX_LIMIT_REG	Maximum threshold configuration.	0x0000	R/W
0x2A	MIN_LIMIT_REG	Minimum threshold configuration.	0x0000	R/W
0x2C	MAX_HYST_REG	Maximum threshold hysteresis.	0x00	R/W
0x2D	MIN_HYST_REG	Minimum threshold hysteresis.	0x00	R/W
0x2E	MON_VAL_REG	MON_VAL scaling.	0x0000	R/W
0x30	INTERFACE_IBI_EN	Interface error IBI enable.	0x00	R/W
0x31	ADC_IBI_EN	ADC IBI enable.	0x00	R/W
0x40	FUSE_CRC	Fuse CRC.	0x00	R/W
0x41	DEVICE_STATUS	Device status.	0x40	R/W
0x42	MAX_SAMPLE_REG	Maximum interrupt sample.	0x0000	R
0x44	MIN_SAMPLE_REG	Minimum interrupt sample.	0x0000	R
0x46	TGT_ADDR_REG	Target address.	0x00	R
0x47	GRP_ADDR_REG	Group address.	0xFF	R
0x48	IBI_STATUS	IBI status.	0x00	R
0x50	CONV_READ	Conversion read result.	0x00000000	R
0x56	CONV_TRIGGER	Conversion trigger.	0x00000000	R

REGISTER DETAILS

INTERFACE CONFIGURATION A REGISTER

Interface configuration settings.

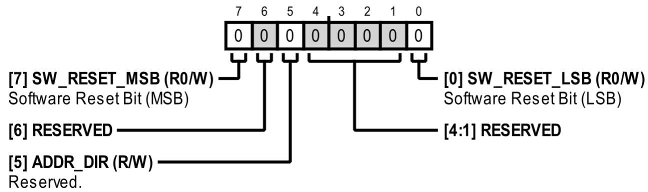

Figure 94. Address: 0x00, Reset: 0x00, Name: INTERFACE_CONFIG_A

Table 33. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET_MSB	Software Reset Bit (MSB). Set both SW_RESET_MSB and SW_RESET_LSB to 1 in the same register write to initiate a software reset of the device.	0x0	R0/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_DIR	Reserved. This bit must be set to 0. This bit is not reset by software resets, and must be reset by the software reset pattern or power-on reset.	0x0	R/W
[4:1]	RESERVED	Reserved.	0x0	R
0	SW_RESET_LSB	Software Reset Bit (LSB). Set both SW_RESET_MSB and SW_RESET_LSB to 1 in the same register write to initiate a software reset of the device.	0x0	R0/W

INTERFACE CONFIGURATION B REGISTER

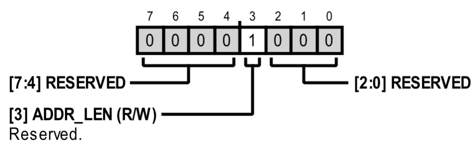

Figure 95. Address: 0x01, Reset: 0x08, Name: INTERFACE_CONFIG_B

Table 34. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	ADDR_LEN	Reserved. This bit must be set to 1.	0x1	R/W
[2:0]	RESERVED	Reserved.	0x0	R

DEVICE CONFIGURATION REGISTER

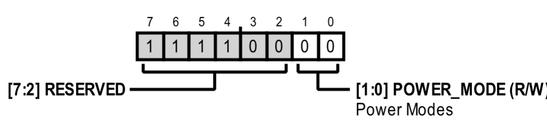

Figure 96. Address: 0x02, Reset: 0xF0, Name: DEVICE_CONFIG

Table 35. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x3C	R
[1:0]	POWER_MODE	Power Modes. 00: Active Mode. 11: Sleep Mode (Low Power).	0x0	R/W

REGISTER DETAILS

DEVICE TYPE REGISTER

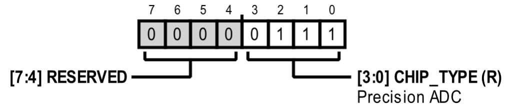

Figure 97. Address: 0x03, Reset: 0x07, Name: DEVICE_TYPE

Table 36. Bit Descriptions for DEVICE_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

PRODUCT IDENTIFICATION (LSBYTE) REGISTER

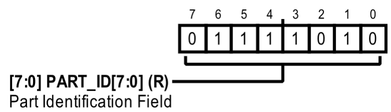

Figure 98. Address: 0x04, Reset: 0x7A, Name: PRODUCT_ID_L

Table 37. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PART_ID[7:0]	Part Identification Field.	0x7A	R

PRODUCT IDENTIFICATION (MSBYTE) REGISTER

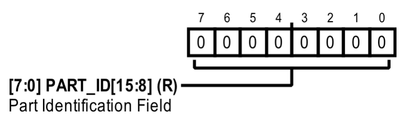

Figure 99. Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 38. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PART_ID[15:8]	Part Identification Field.	0x0	R

DEVICE GRADE REGISTER

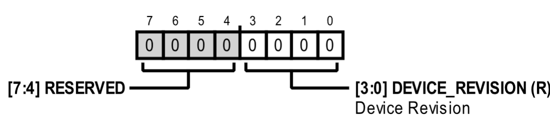

Figure 100. Address: 0x06, Reset: 0x00, Name: DEVICE_GRADE

Table 39. Bit Descriptions for DEVICE_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision. Indicates the device revision.	0x0	R

SCRATCH PAD REGISTER

Interface read/write test register.

REGISTER DETAILS

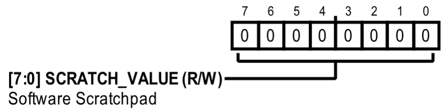

Figure 101. Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 40. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Use this register to test I3C communications with the device. Values written to this register have no impact on device behavior.	0x0	R/W

MIPI MANUFACTURER ID (LSBYTE) REGISTER

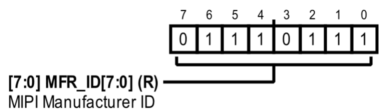

Figure 102. Address: 0x0C, Reset: 0x77, Name: MANUFACTURER_ID_L

Table 41. Bit Descriptions for MANUFACTURER_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	MFR_ID[7:0]	MIPI Manufacturer ID. The MFR_ID[15:0] field is the same value (0x0177) for all Analog Devices products.	0x77	R

MIPI MANUFACTURER ID (MSBYTE) REGISTER

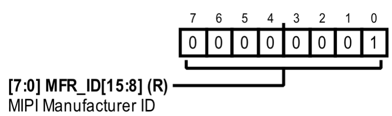

Figure 103. Address: 0x0D, Reset: 0x01, Name: MANUFACTURER_ID_H

Table 42. Bit Descriptions for MANUFACTURER_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	MFR_ID[15:8]	MIPI Manufacturer ID. The MFR_ID[15:0] field is the same value (0x0177) for all Analog Devices products.	0x1	R

RESERVED REGISTER

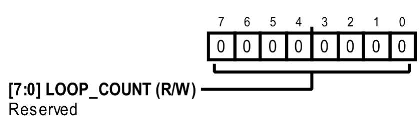

Figure 104. Address: 0x0E, Reset: 0x00, Name: LOOP_COUNT

Table 43. Bit Descriptions for LOOP_COUNT

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Reserved. This bit field must be set to 0x00.	0x0	R/W

REGISTER DETAILS

RESERVED REGISTER

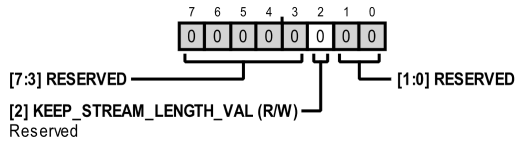

Figure 105. Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

Table 44. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	Reserved. This bit must be set to 0.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

INTERFACE CONFIGURATION C REGISTER

Additional interface configuration settings.

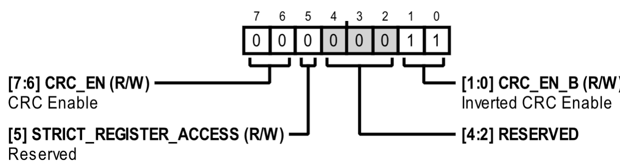

Figure 106. Address: 0x10, Reset: 0x03, Name: INTERFACE_CONFIG_C

Table 45. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_EN	CRC Enable. Set CRC_EN to 0x1 and CRC_EN_B to 0x2 in the same register write to enable interface CRC. 0x0: CRC Disabled. 0x1: CRC Enabled. Enables CRC if CRC_EN_B = 0x2.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Reserved. This bit must be set to 0.	0x0	R/W
[4:2]	RESERVED	Reserved.	0x0	R
[1:0]	CRC_EN_B	Inverted CRC Enable. To enable CRC, write as the inverted value of CRC_ENABLE.	0x3	R/W

INTERFACE STATUS REGISTER

Status bits indicating errors in register reads and/or writes in configuration mode. The interface status bits are active high and are cleared by writing a 1 to their corresponding bit locations.

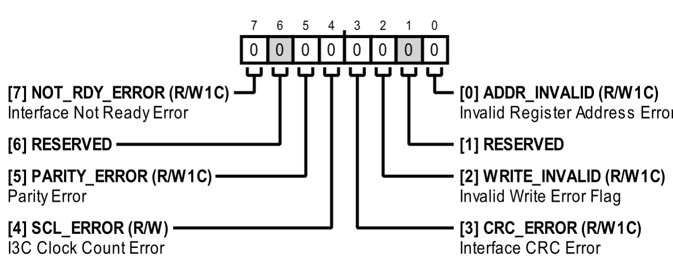

Figure 107. Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS

REGISTER DETAILS

Table 46. Bit Descriptions for INTERFACE_STATUS

Bits	Bit Name	Description	Reset	Access
7	NOT_RDY_ERROR	Interface Not Ready Error. This error bit is set if the user attempts to execute an I3C transaction before the completion of digital initialization. For example, before a device reset is complete.	0x0	R/W1C
6	RESERVED	Reserved.	0x0	R
5	PARITY_ERROR	Parity Error. This error bit is set when the parity bit in an I3C write transaction does not match the parity of the accompanying data.	0x0	R/W1C
4	SCL_ERROR	I3C Clock Count Error. This error bit is set when an incorrect number of serial clock periods is received in an I3C read/write transaction.	0x0	R/W
3	CRC_ERROR	Interface CRC Error. This error bit is set when the device receives an invalid CRC checksum value on SDA during a register read/write. This error bit is only active when CRC is enabled.	0x0	R/W1C
2	WRITE_INVALID	Invalid Write Error Flag. This error bit is set to 1 when the I3C controller attempts a register write to a register that contains exclusively read-only bits.	0x0	R/W1C
1	RESERVED	Reserved.	0x0	R
0	ADDR_INVALID	Invalid Register Address Error. This error bit is set to 1 when the I3C controller attempts to read from or write to an undefined register address.	0x0	R/W1C

ADC OPERATING MODE CONFIGURATION REGISTER

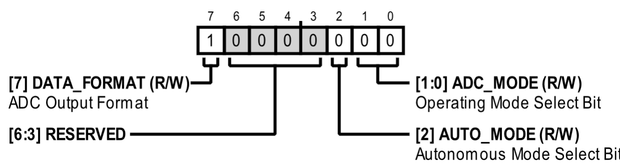

Figure 108. Address: 0x21, Reset: 0x80, Name: ADC_MODES

Table 47. Bit Descriptions for ADC_MODES

Bits	Bit Name	Description	Reset	Access
7	DATA_FORMAT	ADC Output Format. 0: Single-Ended Mode. ADC data are in straight binary (unsigned) format. 1: Differential Mode. ADC data are in twos complement (signed) format.	0x1	R/W
[6:3]	RESERVED	Reserved.	0x0	R
2	AUTO_MODE	Autonomous Mode Select Bit. 0: Monitor Mode. 1: Trigger Mode.	0x0	R/W
[1:0]	ADC_MODE	Operating Mode Select Bit. 0x0: Sample Mode. 0x1: Burst Averaging Mode. 0x3: Autonomous Mode. Select between persistent and nonpersistent autonomous mode via the AUTO_MODE bit.	0x0	R/W

ADC SETUP CONFIGURATION REGISTER

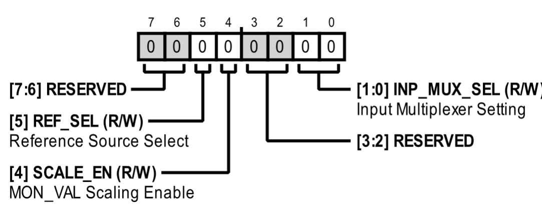

Figure 109. Address: 0x22, Reset: 0x00, Name: ADC_CONFIG

REGISTER DETAILS

Table 48. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REF_SEL	Reference Source Select. Selects which pin is used as the ADC reference source. 0: REF. 1: VDD.	0x0	R/W
4	SCALE_EN	MON_VAL Scaling Enable. MON_VAL scaling is enabled when SCALE_EN is set to 1 while the input multiplexer is configured to monitor the analog inputs (see the INP_MUX_SEL bit).	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	INP_MUX_SEL	Input Multiplexer Setting. 0x0: Analog Inputs. ADC connected to analog inputs (IN+ and IN−). 0x1: Invalid. 0x2: Invalid. 0x3: CLDO. ADC monitors CLDO. This setting is used to verify the CLDO supply voltage.	0x0	R/W

AVERAGING FILTER CONFIGURATION REGISTER

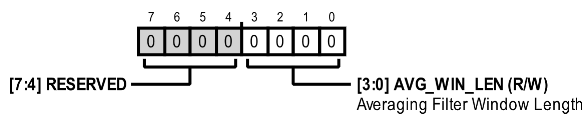

Figure 110. Address: 0x23, Reset: 0x00, Name: AVG_CONFIG

Table 49. Bit Descriptions for AVG_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	AVG_WIN_LEN	Averaging Filter Window Length. Sets the averaging ratio for averaging and burst averaging modes. The averaging ratio ranges from 2 to 4096 in powers of 2. 0x0: 2. 0x1: 4. 0x2: 8. 0x3: 16. 0x4: 32. 0x5: 64. 0x6: 128. 0x7: 256.	0x0	R/W

GENERAL PURPOSE PIN CONFIGURATION REGISTER

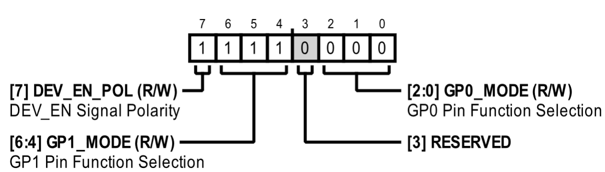

Figure 111. Address: 0x24, Reset: 0xF0, Name: GP_CONFIG

Table 50. Bit Descriptions for GP_CONFIG

Bits	Bit Name	Description	Reset	Access
7	DEV_EN_POL	DEV_EN Signal Polarity. Sets the polarity of the DEV_EN signal for compatibility with active high and active low amplifier enable pins. 0: DEV_EN Active Low.	0x1	R/W

REGISTER DETAILS

Table 50. Bit Descriptions for GP_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
		1: DEV_EN Active High. Default		
[6:4]	GP1_MODE	GP1 Pin Function Selection. 0x0: Disabled/High-Z. 0x1: GP1_INTR Signal. 0x2: Data Ready Signal. 0x3: DEV_EN Signal. 0x5: Static Logic Low (GND). 0x6: Static Logic High (VIO). 0x7: DEV_RDY Signal (Default).	0x7	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	GP0_MODE	GP0 Pin Function Selection. 0x0: Disabled/High-Z (Default). 0x1: GP0_INTR Signal. 0x2: Data Ready Signal. 0x3: DEV_EN Signal. 0x5: Static Logic Low (GND). 0x6: Static Logic High (VIO).	0x0	R/W

INTERRUPT CONFIGURATION REGISTER

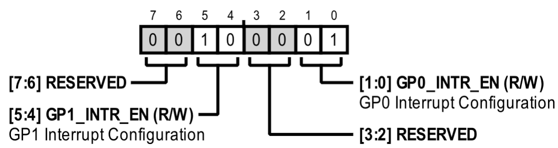

Figure 112. Address: 0x25, Reset: 0x21, Name: INTR_CONFIG

Table 51. Bit Descriptions for INTR_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	GP1_INTR_EN	GP1 Interrupt Configuration. Selects which of the threshold detection interrupt signals are passed through to the GP1_INTR output signal. 0x0: Neither Interrupt. 0x1: MIN_INTR. 0x2: MAX_INTR. Default. 0x3: Either Interrupt. GP1 outputs the logical OR of MIN_INTR and MAX_INTR signals.	0x2	R/W
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	GP0_INTR_EN	GP0 Interrupt Configuration. Selects which of the threshold detection interrupt signals are passed through to the GP0_INTR output signal. 0x0: Neither Interrupt. 0x1: MIN_INTR. Default. 0x2: MAX_INTR. 0x3: Either Interrupt. GP0 outputs the logical OR of MIN_INTR and MAX_INTR signals.	0x1	R/W

REGISTER DETAILS

TIMER CONFIGURATION REGISTER

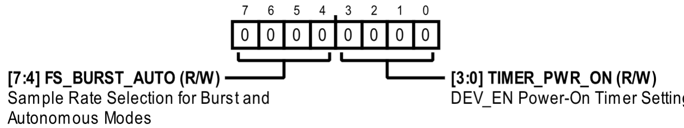

Figure 113. Address: 0x27, Reset: 0x00, Name: TIMER_CONFIG

Table 52. Bit Descriptions for TIMER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:4]	FS_BURST_AUTO	Sample Rate Selection for Burst and Autonomous Modes. 0x0: 2MSPS. 0x1: 1MSPS. 0x2: 300kSPS. 0x3: 100kSPS. 0x4: 33.3kSPS. 0x5: 10kSPS. 0x6: 3kSPS. 0x7: 1kSPS. 0x8: 500SPS. 0x9: 333SPS. 0xA: 250SPS. 0xB: 200SPS. 0xC: 166SPS. 0xD: 140SPS. 0xE: 125SPS. 0xF: 111SPS.	0x0	R/W
[3:0]	TIMER_PWR_ON	DEV_EN Power-On Timer Setting. Selects the delay between DEV_EN assertion and ADC sampling instant when DEV_EN is selected for either GP0 or GP1 pins. 0x0: 500ns. 0x1: 1µs. 0x2: 3.3µs. 0x3: 10µs. 0x4: 30µs. 0x5: 100µs. 0x6: 330µs. 0x7: 1000µs. 0x8: 2000µs. 0x9: 3000µs. 0xA: 4000µs. 0xB: 5000µs. 0xC: 6000µs. 0xD: 7000µs. 0xE: 8000µs. 0xF: 9000µs.	0x0	R/W

REGISTER DETAILS

MAXIMUM THRESHOLD CONFIGURATION REGISTER

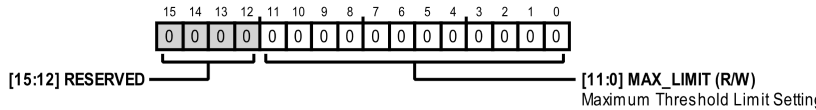

Figure 114. Address: 0x28, Reset: 0x0000, Name: MAX_LIMIT_REG

Table 53. Bit Descriptions for MAX_LIMIT_REG

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	MAX_LIMIT	Maximum Threshold Limit Setting. Sets the maximum threshold limit for autonomous modes. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R/W

MINIMUM THRESHOLD CONFIGURATION REGISTER

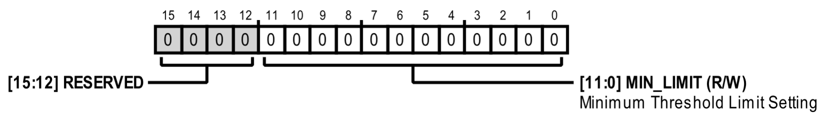

Figure 115. Address: 0x2A, Reset: 0x0000, Name: MIN_LIMIT_REG

Table 54. Bit Descriptions for MIN_LIMIT_REG

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	MIN_LIMIT	Minimum Threshold Limit Setting. Sets the minimum threshold limit for autonomous modes. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R/W

MAXIMUM THRESHOLD HYSTERESIS REGISTER

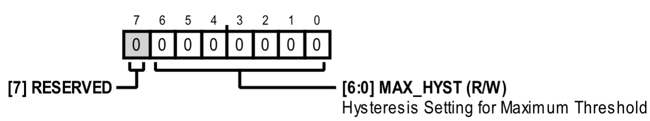

Figure 116. Address: 0x2C, Reset: 0x00, Name: MAX_HYST_REG

Table 55. Bit Descriptions for MAX_HYST_REG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	MAX_HYST	Hysteresis Setting for Maximum Threshold. Sets the hysteresis setting for self-clearing the MAX_INTR signal in monitor mode. Uses straight binary (unsigned) format.	0x0	R/W

MINIMUM THRESHOLD HYSTERESIS REGISTER

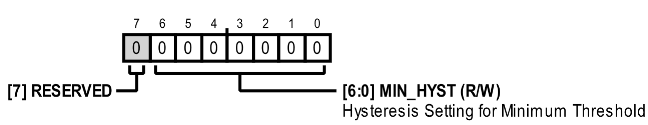

Figure 117. Address: 0x2D, Reset: 0x00, Name: MIN_HYST_REG

Table 56. Bit Descriptions for MIN_HYST_REG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 56. Bit Descriptions for MIN_HYST_REG (Continued)

Bits	Bit Name	Description	Reset	Access
[6:0]	MIN_HYST	Hysteresis Setting for Minimum Threshold. Sets the hysteresis setting for self-clearing the MIN_INTR signal in monitor mode. Uses straight binary (unsigned) format.	0x0	R/W

MON_VAL SCALING REGISTER

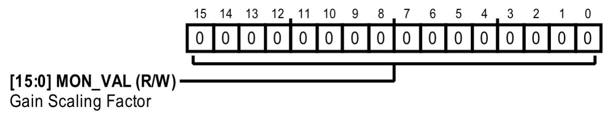

Figure 118. Address: 0x2E, Reset: 0x0000, Name: MON_VAL_REG

Table 57. Bit Descriptions for MON_VAL_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MON_VAL	Gain Scaling Factor. Sets the scaling factor for ADC results when using MON_VAL scaling. MON_VAL can be automatically generated or set manually.	0x0	R/W

INTERFACE ERROR IBI ENABLE REGISTER

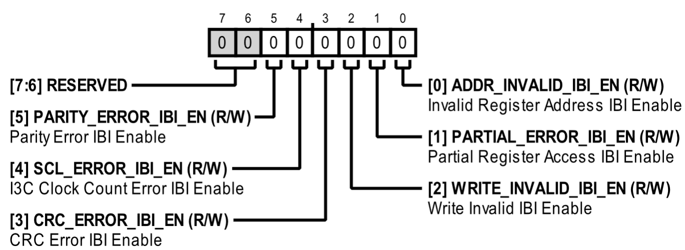

Figure 119. Address: 0x30, Reset: 0x00, Name: INTERFACE_IBI_EN

Table 58. Bit Descriptions for INTERFACE_IBI_EN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	PARITY_ERROR_IBI_EN	Parity Error IBI Enable. Set this bit to 1 to enable the PARITY_ERROR_IBI.	0x0	R/W
4	SCL_ERROR_IBI_EN	I3C Clock Count Error IBI Enable. Set this bit to 1 to enable the SCL_ERROR_IBI.	0x0	R/W
3	CRC_ERROR_IBI_EN	CRC Error IBI Enable. Set this bit to 1 to enable the CRC_ERROR_IBI.	0x0	R/W
2	WRITE_INVALID_IBI_EN	Write Invalid IBI Enable. Set this bit to 1 to enable the WRITE_INVALID_IBI.	0x0	R/W
1	PARTIAL_ERROR_IBI_EN	Partial Register Access IBI Enable. Set this bit to 1 to enable the PARTIAL_ERROR_IBI.	0x0	R/W
0	ADDR_INVALID_IBI_EN	Invalid Register Address IBI Enable. Set this bit to 1 to enable the ADDR_INVALID_IBI.	0x0	R/W

ADC IBI ENABLE REGISTER

If GRP_NOT_ASSIGNED is 0, GRP_ADDR contains the assigned group address. Otherwise, GRP_ADDR reads back all 1's. In other words, GRP_ADDR_REG either reads back 0xFF or the assigned group address.

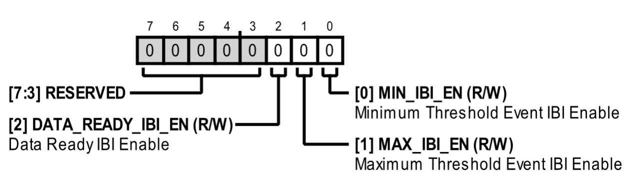

Figure 120. Address: 0x31, Reset: 0x00, Name: ADC_IBI_EN

REGISTER DETAILS

Table 59. Bit Descriptions for ADC_IBI_EN

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	DATA_READY_IBI_EN	Data Ready IBI Enable. If this IBI enable bit it set, an IBI will be triggered when the ADC result is ready after doing a conversion with CONV_TRIGGER.	0x0	R/W
1	MAX_IBI_EN	Maximum Threshold Event IBI Enable. If this IBI enable bit is set, the maximum threshold event will trigger an IBI. Only the first event that sets the MAX_THRESH_INTR bit will trigger an IBI. No IBI will be triggered for subsequent events after MAX_THRESH_INTR has been set.	0x0	R/W
0	MIN_IBI_EN	Minimum Threshold Event IBI Enable. If this IBI enable bit is set, the minimum threshold event will trigger an IBI. Only the first event that sets the MIN_THRESH_INTR bit will trigger an IBI. No IBI will be triggered for subsequent events after MIN_THRESH_INTR has been set.	0x0	R/W

FUSE CRC REGISTER

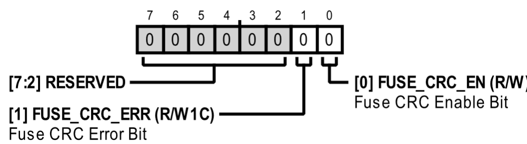

Figure 121. Address: 0x40, Reset: 0x00, Name: FUSE_CRC

Table 60. Bit Descriptions for FUSE_CRC

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	FUSE_CRC_ERR	Fuse CRC Error Bit. Indicates an invalid fuse map CRC check. If this bit is set following the fuse map CRC check, reset the device.	0x0	R/W1C
0	FUSE_CRC_EN	Fuse CRC Enable Bit. Setting this bit to 1 triggers a CRC check on the internal device fuse map. This bit self-clears when the fuse map CRC check is complete.	0x0	R/W

DEVICE STATUS REGISTER

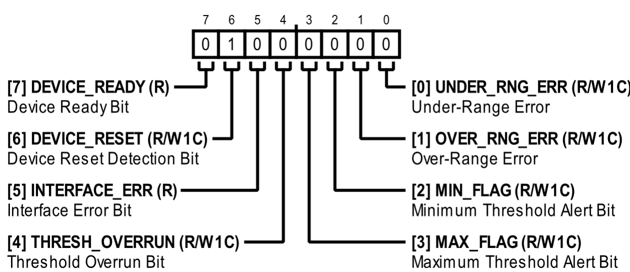

Figure 122. Address: 0x41, Reset: 0x40, Name: DEVICE_STATUS

Table 61. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	DEVICE_READY	Device Ready Bit. This bit is automatically set to 1 when the device reset and startup sequence is complete and is ready for serial communications from the digital host.	0x0	R
6	DEVICE_RESET	Device Reset Detection Bit. Indicates a device reset occurred. This bit is cleared by setting it to 1.	0x1	R/W1C
5	INTERFACE_ERR	Interface Error Bit. Indicates if one or more interface communication errors occurs. This bit is the logical OR of all bits in INTERFACE_STATUS_A register.	0x0	R
4	THRESH_OVERRUN	Threshold Overrun Bit. This bit is set to 1 when a threshold overrun event is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C
3	MAX_FLAG	Maximum Threshold Alert Bit. This bit is set to 1 when a maximum threshold violation is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C

REGISTER DETAILS

Table 61. Bit Descriptions for DEVICE_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
2	MIN_FLAG	Minimum Threshold Alert Bit. This bit is set to 1 when a minimum threshold violation is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C
1	OVER_RNG_ERR	Over-Range Error. Write 1 to clear.	0x0	R/W1C
0	UNDER_RNG_ERR	Under-Range Error. Write 1 to clear.	0x0	R/W1C

MAXIMUM INTERRUPT SAMPLE REGISTER

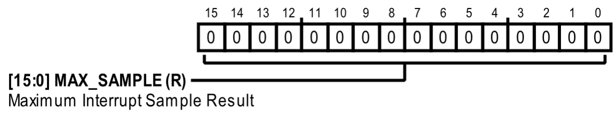

Figure 123. Address: 0x42, Reset: 0x0000, Name: MAX_SAMPLE_REG

Table 62. Bit Descriptions for MAX_SAMPLE_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MAX_SAMPLE	Maximum Interrupt Sample Result. Contains ADC result generated by maximum threshold interrupt in trigger mode. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R

MINIMUM INTERRUPT SAMPLE REGISTER

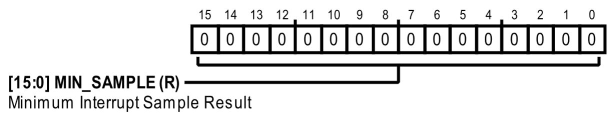

Figure 124. Address: 0x44, Reset: 0x0000, Name: MIN_SAMPLE_REG

Table 63. Bit Descriptions for MIN_SAMPLE_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MIN_SAMPLE	Minimum Interrupt Sample Result. Contains ADC result generated by minimum threshold interrupt in trigger mode. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R

TARGET ADDRESS REGISTER

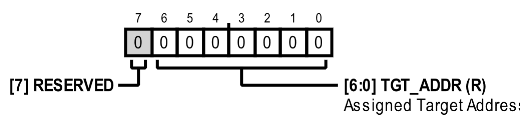

Figure 125. Address: 0x46, Reset: 0x00, Name: TGT_ADDR_REG

Table 64. Bit Descriptions for TGT_ADDR_REG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	TGT_ADDR	Assigned Target Address. Contains the Target address assigned to the AD4055 during dynamic address assignment (DAA).	0x0	R

GROUP ADDRESS REGISTER

If GRP_NOT_ASSIGNED is 0, GRP_ADDR contains the assigned group address. Otherwise, GRP_ADDR reads back all 1's. In other words, GRP_ADDR_REG either reads back 0xFF or the assigned group address.

REGISTER DETAILS

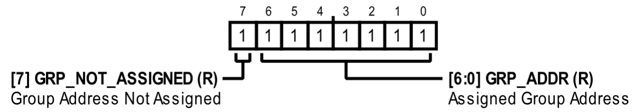

Figure 126. Address: 0x47, Reset: 0xFF, Name: GRP_ADDR_REG

Table 65. Bit Descriptions for GRP_ADDR_REG

Bits	Bit Name	Description	Reset	Access
7	GRP_NOT_ASSIGNED	Group Address Not Assigned. Indicates whether the device has been assigned a valid Group address with the SETGRPA CCC command. 0: Group Address Assigned. GRP_ADDR contains the assigned Group address for the device. 1: Group Not Assigned. GRP_NOT_ASSIGNED will be set to 0 after Group address is assigned with the SETGRPA CCC command.	0x1	R
[6:0]	GRP_ADDR	Assigned Group Address. Contains the Group address assigned to the AD4055 by the SETGRPA CCC command. If GRP_NOT_ASSIGNED is 0, GRP_ADDR contains the assigned group address. Otherwise, GRP_ADDR reads back all 1's.	0x7F	R

IBI STATUS REGISTER

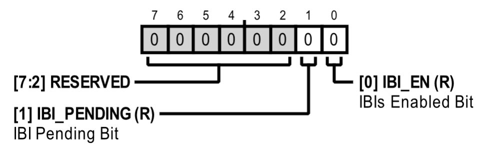

Figure 127. Address: 0x48, Reset: 0x00, Name: IBI_STATUS

Table 66. Bit Descriptions for IBI_STATUS

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	IBI_PENDING	IBI Pending Bit. Asserted while IBI is pending. Deasserted when Controller ACKs the IBI or when I3C peripheral or whole device is reset.	0x0	R
0	IBI_EN	IBIs Enabled Bit. Indicates if IBIs are enabled on the device. IBIs are enabled and disabled with the ENEC and DISEC CCC commands, respectively. Following the ENEC CCC, IBIs are enabled and IBI_EN reads back 1. Following the DISEC CCC, IBIs are disabled and IBI_EN reads back 0.	0x0	R

CONVERSION READ RESULT REGISTER

The AD4055 ADC core performs conversion(s) following I3C reads while the ADDR_PTR is pointing to the CONV_READ register address.

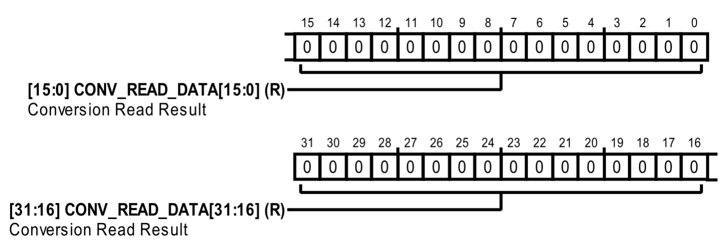

Figure 128. Address: 0x50, Reset: 0x00000000, Name: CONV_READ

Table 67. Bit Descriptions for CONV_READ

Bits	Bit Name	Description	Reset	Access
[31:0]	CONV_READ_DATA	Conversion Read Result. This bit field contains the most recent ADC result.	0x0	R

REGISTER DETAILS

CONVERSION TRIGGER REGISTER

The AD4055 ADC core performs conversion(s) following I3C writes which set the ADDR_PTR to the CONV_TRIGGER register address. By using I3C Group addressing, this register can be used to synchronize conversions across multiple AD4055 devices on the same I3C bus.

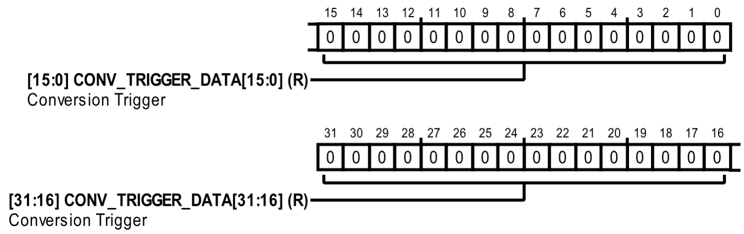

Figure 129. Address: 0x56, Reset: 0x00000000, Name: CONV_TRIGGER

Table 68. Bit Descriptions for CONV_TRIGGER

Bits	Bit Name	Description	Reset	Access
[31:0]	CONV_TRIGGER_DATA	Conversion Trigger. This bit field contains the most recent ADC result.	0x0	R

OUTLINE DIMENSIONS

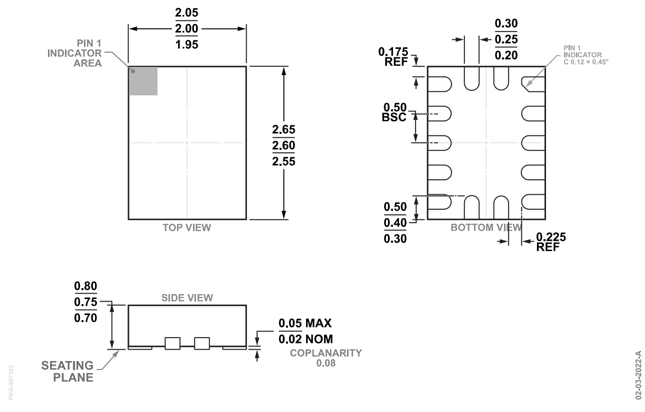

Figure 130. 14-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2.6 mm Body and 0.75 mm Packaging Height
(CP-14-7)
Dimensions shown in millimeters

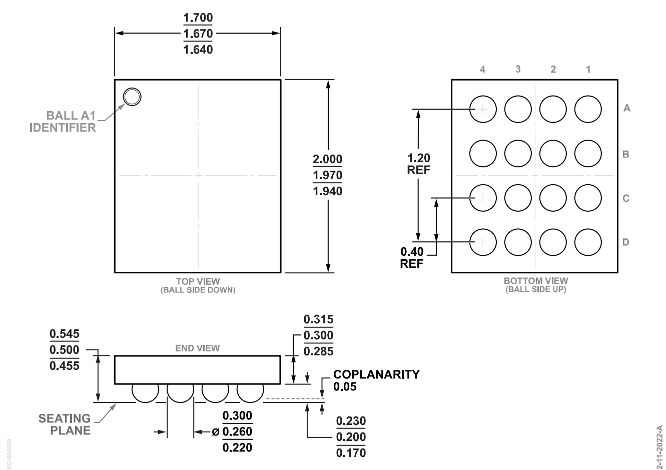

Figure 131. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4060BCPZ-RL7	−40°C to +125°C	14-Lead Lead Frame Chip Scale Package [LFCSP] (2.00 mm × 2.6 mm × 0.75 mm)	REEL, 3000	CP-14-7
AD4060BCBZ-RL7	−40°C to +125°C	16-Ball Wafer Level Chip Scale Package [WLCSP] (1.67 mm × 1.97 mm × 0.5 mm)	REEL, 3000	CB-16-26

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD4060-ARDZ	Evaluation Board

[1] Z = RoHS-Compliant Part.