

# AS5147U/AS5247U

## 14-Bit Dual-Die On-Axis Magnetic Rotary Position Sensor with Up to 14-Bit Binary Incremental Pulse Count

### General Description

The AS5147U/AS5247U is a high-resolution redundant rotary position sensor for fast absolute angle measurement over a full 360-degree range. This position sensor is equipped with a revolutionary integrated dynamic angle error compensation (DAEC™) with almost 0 latency at higher rotational speed. For increased signal quality at lower rotational speed, the dynamic filter system (DFS™) reduces transition noise.

The robust design of the device suppresses the influence of any homogenous external stray magnetic field. A standard 4-wire SPI serial interface with a CRC protection allows a host microcontroller to read 14-bit absolute angle position data from the AS5147U/AS5247U and to program non-volatile settings without a dedicated programmer.

Incremental movements are indicated on a set of ABI signals with a maximum resolution of 16989 steps / 4096 pulses per revolution.

Brushless DC (BLDC) motors are controlled through a standard UVW commutation interface with a programmable number of pole pairs from 1 to 7. The absolute angle position is also provided as PWM-encoded output signal.

The AS5147U/AS5247U supports embedded self-diagnostics for fulfilling up to ASIL D in safety relevant applications.

The AS5247U is using the **ams** stacked die technology in a TQFP-32 (7x7) package. The AS5147U sensor is available in a TSSOP14 Package.

*[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of this device are listed below:

**Figure 1:**  
Added Value of Using the AS5x47U

| Benefits  | Features   |
|---|--|
| <ul style="list-style-type: none"> <li>• Easy to use – saving costs on DSP</li> </ul>                           | <ul style="list-style-type: none"> <li>• DAEC <sup>™</sup> Dynamic angle error compensation</li> <li>• DFS <sup>™</sup> Dynamic filter system</li> </ul>                         |
| <ul style="list-style-type: none"> <li>• Higher durability and lower system costs (no shield needed)</li> </ul> | <ul style="list-style-type: none"> <li>• Magnetic stray field immunity</li> </ul>  |
| <ul style="list-style-type: none"> <li>• Enabler for safety critical applications</li> </ul>                    | <ul style="list-style-type: none"> <li>• Developed according ISO26262, diagnostics, dual redundant chip version ASIL-D capable, Safety Element out of Context (SEooC)</li> </ul> |
| <ul style="list-style-type: none"> <li>• Suitable for automotive applications</li> </ul>                        | <ul style="list-style-type: none"> <li>• AEC-Q100 Grade 0 qualified</li> </ul>   |
| <ul style="list-style-type: none"> <li>• Versatile choice of the interface</li> </ul>                           | <ul style="list-style-type: none"> <li>• Independent output interfaces: SPI, ABI, UVW, PWM</li> </ul>  |

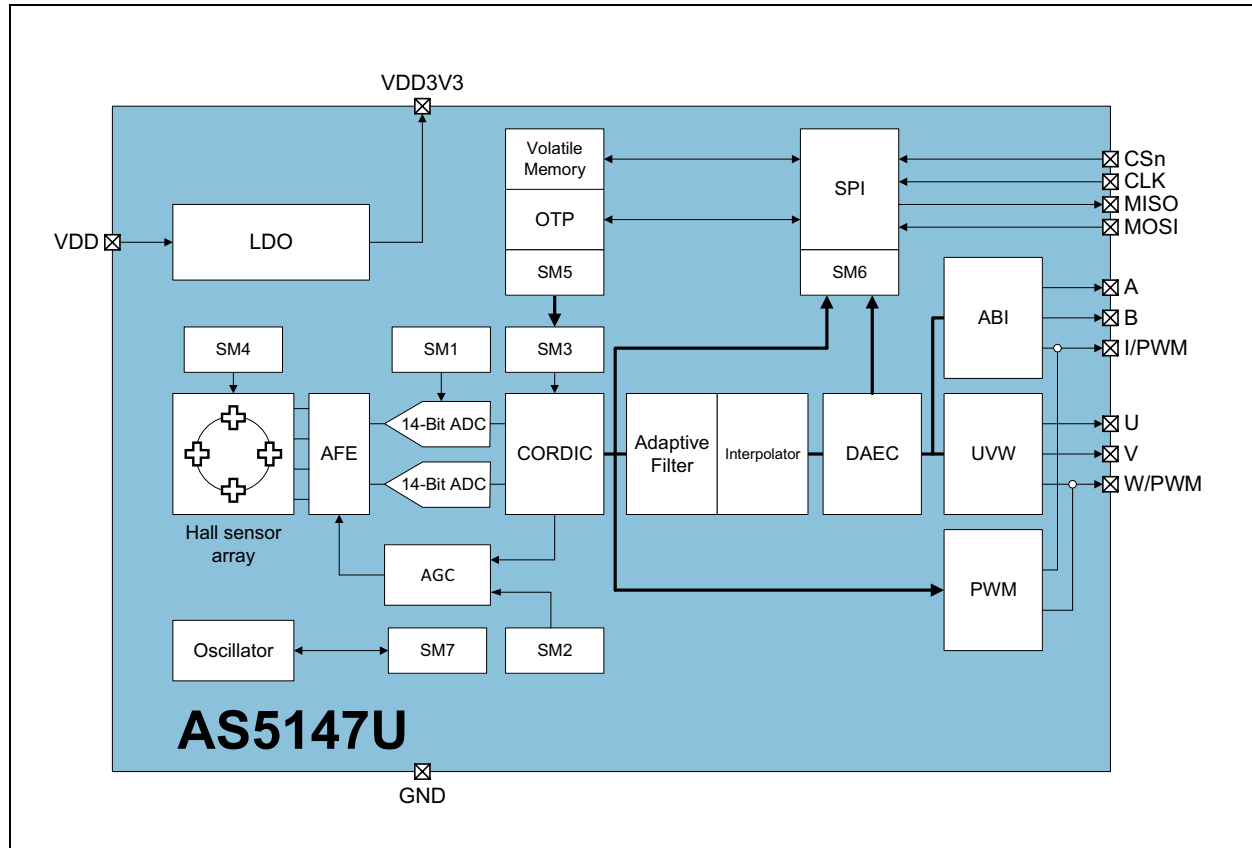
## Applications

The AS5x47U has been designed to support BLDC motor communication for the most challenging and safety-critical automotive applications (AEC-Q100 grade 0 automotive qualified – ISO26262 assessment) such as electric power steering (EPS), transmission (gearbox, actuator), brake (actuator) and starter/alternator.

## Block Diagram

The functional blocks of the AS5147U/AS5247U are shown below:

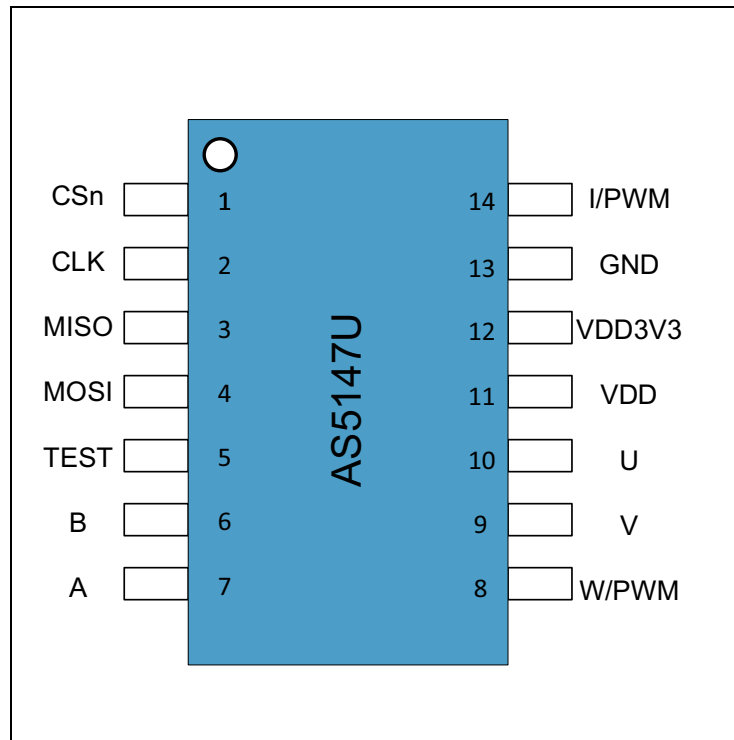
**Figure 2:**  
**AS5147U Block Diagram**



AS5247U uses 2xAS5147U in one package.

## Pin Assignment

**Figure 3:**  
TSSOP-14 Pin Assignment



**Figure 4:**  
AS5147U Pin Description

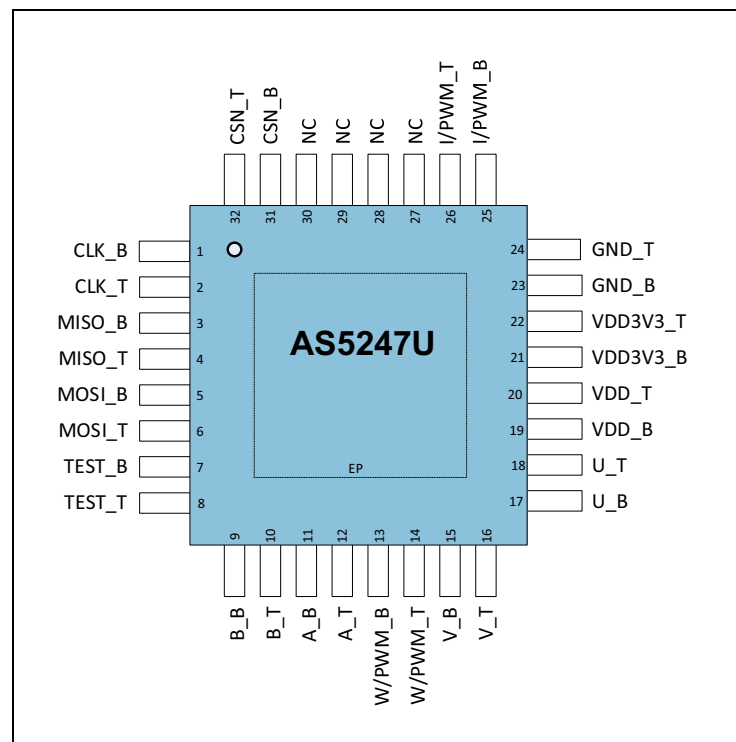
| Pin Number | Pin Name | Pin Type                     | Description   |
|------------|----------|------------------------------|---|
| 1          | CSn      | Digital input <sup>(1)</sup> | SPI chip select (active low) <sup>(2)</sup>               |
| 2          | CLK      | Digital input <sup>(1)</sup> | SPI clock <sup>(3)</sup>                                  |
| 3          | MISO     | Digital output               | SPI master data input, slave output <sup>(4)</sup>        |
| 4          | MOSI     | Digital input <sup>(1)</sup> | SPI master data output, slave input <sup>(3)</sup>        |
| 5          | TEST     |                              | Test pin (connect to ground)                              |
| 6          | B        | Digital output               | Incremental signal B <sup>(5)</sup>                       |
| 7          | A        | Digital output               | Incremental signal A <sup>(5)</sup>                       |
| 8          | W/PWM    | Digital output               | Commutation signal W or PWM-encoded output <sup>(5)</sup> |
| 9          | V        | Digital output               | Commutation signal V <sup>(5)</sup>                       |
| 10         | U        | Digital output               | Commutation signal U <sup>(5)</sup>                       |
| 11         | VDD      | Digital output               | 5V power supply voltage for on-chip regulator             |

| Pin Number | Pin Name | Pin Type       | Description  |
|------------|----------|----------------|--|
| 12         | VDD3V3   | Power supply   | 3.3V on-chip low-dropout (LDO) output. Requires an external decoupling capacitor (1μF) |
| 13         | GND      | Power supply   | Ground   |
| 14         | I/PWM    | Digital output | Incremental signal I (index) or PWM <sup>(5)</sup>                                     |

**Note(s):**

1. Floating state of a digital input is not allowed.
2. If SPI is not used, a pull-up resistor on CSn is required.
3. If SPI is not used, a pull-down resistor on CLK and MOSI is required.
4. If SPI is not used, the pin MISO can be left open.
5. If ABI, UVW or PWM is not used, the pins can be left open.

**Figure 5:**  
**TQFP32 Pin Assignment**



**Figure 6:**  
**AS5247U Pin Description**

| Pin Number | Pin Name | Pin Type                     | Description   |
|------------|----------|------------------------------|---|
| 1          | CLK_B    | Digital input                | SPI clock <sup>(3)</sup>  |
| 2          | CLK_T    | Digital input                | SPI clock <sup>(3)</sup>  |
| 3          | MISO_B   | Digital output               | SPI master data input, SPI slave output <sup>(4)</sup>                                  |
| 4          | MISO_T   | Digital output               | SPI master data input, SPI slave output <sup>(4)</sup>                                  |
| 5          | MOSI_B   | Digital input <sup>(1)</sup> | SPI master data output, SPI slave input <sup>(3)</sup>                                  |
| 6          | MOSI_T   | Digital input <sup>(1)</sup> | SPI master data output, SPI slave input <sup>(3)</sup>                                  |
| 7          | Test_B   |                              | Test pin (connect to ground)  |
| 8          | Test_T   |                              | Test pin (connect to ground)  |
| 9          | B_B      | Digital output               | Incremental signal B <sup>(5)</sup>   |
| 10         | B_T      | Digital output               | Incremental signal B <sup>(5)</sup>   |
| 11         | A_B      | Digital output               | Incremental signal A <sup>(5)</sup>   |
| 12         | A_T      | Digital output               | Incremental signal A <sup>(5)</sup>   |
| 13         | W/PWM_B  | Digital output               | Commutation signal W or PWM encoded output <sup>(5)</sup>                               |
| 14         | W/PWM_T  | Digital output               | Commutation signal W or PWM encoded output <sup>(5)</sup>                               |
| 15         | V_B      | Digital output               | Commutation signal V <sup>(5)</sup>   |
| 16         | V_T      | Digital output               | Commutation signal V <sup>(5)</sup>   |
| 17         | U_B      | Digital output               | Commutation signal U <sup>(5)</sup>   |
| 18         | U_T      | Digital output               | Commutation signal U <sup>(5)</sup>   |
| 19         | VDD_B    | Power supply                 | 5V power supply voltage for on-chip regulator   |
| 20         | VDD_T    | Power supply                 | 5V power supply voltage for on-chip regulator   |
| 21         | VDD3V3_B | Power supply                 | 3.3V on-chip low –dropout (LDO) output. Requires an external decoupling capacitor (1μF) |
| 22         | VDD3V3_T | Power supply                 | 3.3V on-chip low –dropout (LDO) output. Requires an external decoupling capacitor (1μF) |
| 23         | GND_B    | Power supply                 | Ground  |
| 24         | GND_T    | Power supply                 | Ground  |
| 25         | I/PWM_B  | Digital output               | Incremental Signal I (index) or PWM   |

| Pin Number | Pin Name | Pin Type                     | Description                                 |
|------------|----------|------------------------------|---|
| 26         | I/PWM_T  | Digital output               | Incremental Signal I (index) or PWM         |
| 27         | NC       | Not connected                | Connected to ground                         |
| 28         | NC       | Not connected                | Connected to ground                         |
| 29         | NC       | Not connected                | Connected to ground                         |
| 30         | NC       | Not connected                | Connected to ground                         |
| 31         | CSn_B    | Digital input <sup>(1)</sup> | SPI chip select (active low) <sup>(2)</sup> |
| 32         | CSn_T    | Digital input <sup>(1)</sup> | SPI chip select (active low) <sup>(2)</sup> |
| EP         | EP       | Not Connected                | Exposed pad; floating pin                   |

**Note(s):**

1. Floating state of a digital input is not allowed.
2. If SPI is not used, a pull-up resistor on CSn is required.
3. If SPI is not used, a pull-down resistor on CLK and MOSI is required.
4. If SPI is not used, the pin MISO can be left open.
5. If ABI, UVW or PWM is not used, the pins can be left open.

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Operational Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 7:**  
**Absolute Maximum Ratings**

| Symbol                                    | Parameter  | Min  | Max     | Units | Comments                                     |
|---|--|------|---------|-------|--|
| Electrical Parameters                     |  |      |         |       |  |
| VDD5                                      | DC Supply Voltage at VDD pin                       | -0.3 | 7.0     | V     | Not operational                              |
| VDD3                                      | DC Supply Voltage at VDD3V3 pin                    | -0.3 | 5.0     | V     | Not operational                              |
| V <sub>GND</sub>                          | DC Supply Voltage at GND pin                       | -0.3 | 0.3     | V     |  |
| V <sub>in</sub>                           | Input Pin Voltage                                  |      | VDD+0.3 | V     |  |
| I <sub>scr</sub>                          | Input Current (latch-up immunity)                  | -100 | 100     | mA    | AEC-Q100-004                                 |
| Total Power Dissipation                   |  |      |         |       |  |
| P <sub>T</sub>                            | Total Power Dissipation (all supplies and outputs) |      | 150     | mW    | AS5147U (Single Die)<br>x2 for AS5247U       |
| Electrostatic Discharge                   |  |      |         |       |  |
| ESD <sub>HBM</sub>                        | Electrostatic Discharge HBM                        | ±2   |         | kV    | AEC-Q100-002                                 |
| Temperature Ranges and Storage Conditions |  |      |         |       |  |
| T <sub>AMB</sub>                          | Operating Temperature Range                        | -40  | 150     | °C    | Ambient temperature                          |
| T <sub>aProg</sub>                        | Programming Temperature                            | 5    | 45      | °C    | Programming @ room temperature (25°C ± 20°C) |
| T <sub>STRG</sub>                         | Storage Temperature Range                          | -55  | 150     | °C    |  |
| T <sub>BODY</sub>                         | Package Body Temperature                           |      | 260     | °C    | IPC/JEDEC J-STD-020                          |
| RH <sub>NC</sub>                          | Relative Humidity (non-condensing)                 | 5    | 85      | %     |  |
| MSL                                       | Moisture Sensitivity Level                         | 3    |         |       | Represents a maximum floor lifetime of 168h  |



## Electrical Characteristics

All defined tolerances in this datasheet for external components need to be assured over the whole operation conditions range and even over lifetime.

Overall condition:  $T_{AMB} = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  components spec; unless otherwise noted.

**Figure 8:**  
**Operational Conditions**

| Symbol           | Parameter                    | Conditions  | Min              | Typ | Max              | Units |
|------------------|------------------------------|---|------------------|-----|------------------|-------|
| VDD5             | Positive supply voltage      | 5.0V operation mode   | 4.5              | 5.0 | 5.5              | V     |
| VDD3V3           | Positive supply voltage      | 3.3V operation mode; only from $-40^{\circ}\text{C}$ to $150^{\circ}\text{C}$ (Noisaset bit has to set) | 3.0              | 3.3 | 3.6              | V     |
| VDD_Burn         | Positive supply voltage      | Supply voltage required for programming in 3.3V operation   | 3.3              |     | 3.5              | V     |
| V <sub>REG</sub> | Regulated voltage            | Voltage at VDD3V3 pin if $VDD \neq VDD3V3$  | 3.2              | 3.4 | 3.6              | V     |
| I <sub>DD</sub>  | Supply current               | AS5147U<br>(AS5247U I <sub>DD</sub> x 2)  |                  |     | 16<br>(32)       | mA    |
| V <sub>IH</sub>  | High-level input voltage     |   | $0.7 \times VDD$ |     |                  | V     |
| V <sub>IL</sub>  | Low-level input voltage      |   |                  |     | $0.3 \times VDD$ | V     |
| V <sub>OH</sub>  | High-level output voltage    |   | $VDD - 0.5$      |     |                  | V     |
| V <sub>OL</sub>  | Low-level output voltage     |   |                  |     | $V_{GND} + 0.4$  | V     |
| C <sub>L</sub>   |                              |   |                  |     | 50               | pF    |
| I_Out_5V         | Output current 5 V operation |   |                  |     | 4                | mA    |
| I_Out_3V         | Output current 3 V operation |   |                  |     | 2                | mA    |

**Note(s):**

1. Only applicable for digital output pins I/PWM, A, B, U, V, W/PWM, MISO.

## Magnetic Characteristics

**Figure 9:**  
Magnetic Characteristics

| Symbol                        | Parameter                          | Conditions   | Min | Typ | Max | Unit |
|-------------------------------|------------------------------------|--|-----|-----|-----|------|
| B <sub>z</sub> <sup>(1)</sup> | Orthogonal magnetic field strength | Required orthogonal component of the magnetic field strength measured at the die surface along a circle of 1.1mm radius. | 35  |     | 70  | mT   |

**Note(s):**

1. Sensor can work with lower magnetic input field which influences spec parameters in terms of noise and accuracy. In case the sensor will be used in application with wider z distance, please contact the support team for detailed information.

## System Specifications

**Figure 10:**  
System Specifications

| Symbol                    | Parameter  | Conditions  | Min | Typ   | Max   | Units  |
|---------------------------|--|---|-----|-------|-------|--------|
| RES                       | Core and resolution on SPI   |   |     | 14    |       | bit    |
| RES_ABI                   | Resolution of the ABI interface  | Programmable with register setting (ABIRES)   | 25  |       | 4096  | steps  |
| INL <sub>OPT</sub> @ 25°C | Non-linearity, optimum placement of the magnet                                   |   |     | ±0.4  | ±0.8  | degree |
| INL <sub>OPT+TEMP</sub>   | Non-linearity @ displacement of magnet and temperature -40°C to 150°C            |   |     | ±0.6  | ±1    | degree |
| INL <sub>DIS+TEMP</sub>   | Non-linearity @ displacement of magnet and temperature -40°C to 150°C            | Assuming N35H magnet (D=8mm, H=3mm) 500µm displacement in x and y z-distance @ 2000µm                 |     |       | ±1.2  | degree |
| ONL                       | RMS output noise (1 sigma) on SPI, ABI and UVW. Not tested, guaranteed by design | Orthogonal component for the magnetic field within the specified range (B <sub>z</sub> ), NOISESET= 0 |     | 0.034 | 0.068 | degree |

| Symbol                    | Parameter  | Conditions  | Min | Typ   | Max   | Units         |
|---------------------------|--|---|-----|-------|-------|---------------|
| ONH                       | RMS output noise (1 sigma) on SPI, ABI and UVW. Not tested, guaranteed by design | Orthogonal component for the magnetic field within the specified range (Bz), NOISESET = 1 |     | 0.041 | 0.082 | degree        |
| $t_{\text{delay}}$        | System propagation delay –core   | Reading angle via SPI   | 90  |       | 110   | $\mu\text{s}$ |
| $t_{\text{delay\_DAEC}}$  | Residual system propagation delay after dynamic angle error correction           | At ABI, UVW and SPI   | 1.5 |       | 1.9   | $\mu\text{s}$ |
| $t_{\text{sampl}}$        | Refresh time of DAEC   | Refresh time at SPI (ANGLECOM),ABI,UVW  | 202 | 222   | 247   | ns            |
| $\text{DAE}_{1700}$       | Dynamic angle error  | At 1700 rpm constant speed  |     |       | 0.02  | degree        |
| $\text{DAE}_{\text{max}}$ | Dynamic angle error  | At 28000 rpm constant speed   |     |       | 0.32  | degree        |
| MS                        | Maximum speed  |   |     |       | 28000 | rpm           |

**Reference magnet:** N35H, 8mm diameter; 3mm thickness.  
Magnet in the Bz range.

## Timing Characteristics

**Figure 11:**  
Timing Specifications

| Symbol    | Parameter     | Conditions   | Min | Typ | Max | Units |
|-----------|---------------|--|-----|-----|-----|-------|
| $t_{pon}$ | Power-on time | Guaranteed by design. Time between $VDD > VDD_{min}$ and the first valid outcome |     |     | 10  | ms    |

## Detailed Description

The AS5147U/AS5247U is a Hall-effect magnetic sensor using a CMOS technology. The Hall sensors convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals from the Hall sensors are amplified and filtered by the analog front-end (AFE) before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC (coordinate rotation digital computer) block to compute the angle and magnitude of the magnetic vector. The intensity of the magnetic field (magnitude) used by the automatic gain control (AGC) to adjust the amplification level for compensation of the temperature and magnetic field variations.

The AS5147U/AS5247U generates continuously the angle information, which can be requested by the different interfaces of the device. The internal 14-bit resolution is available by readout register via the SPI interface. The resolution on the ABI output can be programmed for 10 to 14 bits.

The Dynamic Angle Error Compensation block corrects the calculated angle regarding latency by using a linear prediction calculation algorithm. At constant rotation speed the latency time is internally compensated by the AS5147U/AS5247U, reducing the dynamic angle error at the SPI, ABI and UVW outputs.

The adaptive filter block is implemented after the compensation block and reduces the transition noise at low rotation speed. The stable information is available on SPI, ABI and UVW.

AS5147U/AS5247U allows selecting between a UVW output interface and a PWM encoded interface on the W pin.

The non-volatile settings in the AS5147U/AS5247U is programmed through the SPI interface without any dedicated programmer.

The sensor can support high-speed application up to 28krpm. AS5147U/AS5247U is developed as SEooC, with assumed top level safety requirements, and supports together with the safety manual motor applications up to ASIL D.

## Power Management

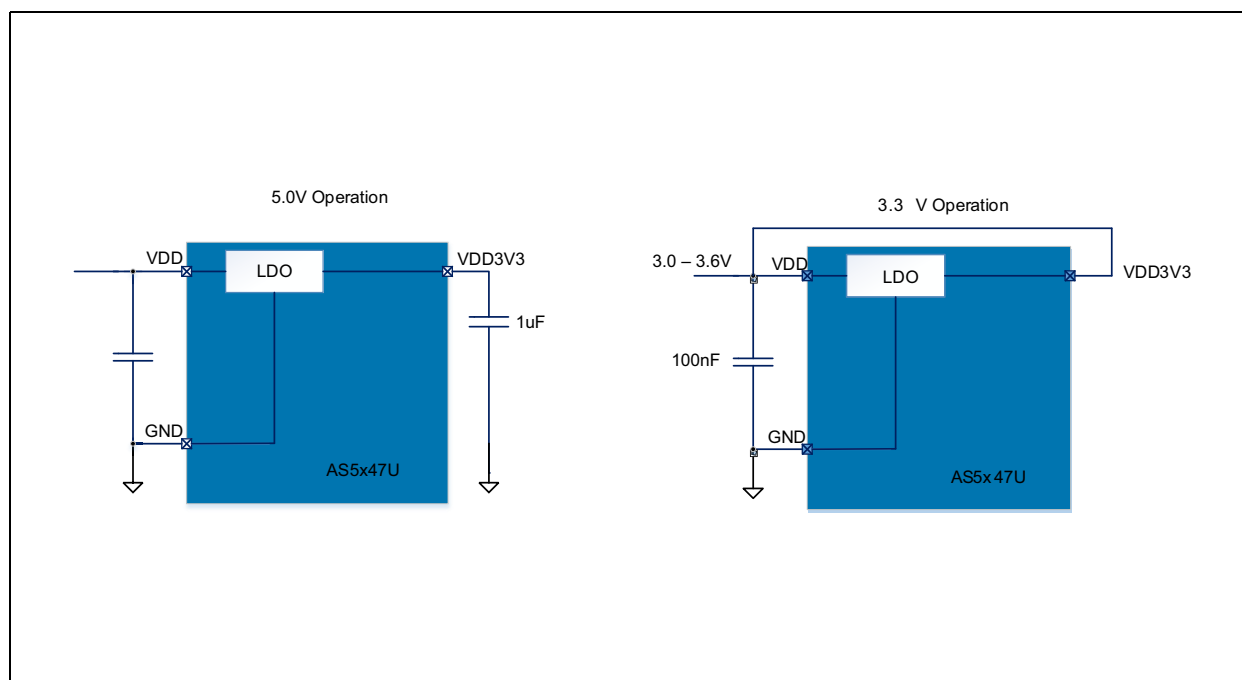
The AS5x47U can be either powered from a 5.0V supply using the on-chip low-dropout regulator or from a 3.3V voltage supply. The LDO regulator is not intended to power any other loads, and it needs a 1 $\mu$ F capacitor to ground located close to chip for decoupling as shown in Figure 13.

In 3.3V operation, VDD and VREG shall connected together. In this configuration, normal noise performance (ONL) is available at reduced maximum temperature (125°C) by clearing NOISESET to 0. When NOISESET is set to 1, the full temperature range is available with reduced noise performance (ONH).

**Figure 12:**  
Temperature Range and Output Noise in 3.3V and 5.0V Mode

| VDD (V) | NOISESET | Temperature Range (°C) | RMS Output Noise (degree) |
|---------|----------|------------------------|---------------------------|
| 5.0     | 0        | -40 to 150             | 0.068                     |
| 3.3     | 0        | -40 to 125             | 0.068                     |
| 3.3     | 1        | -40 to 150             | 0.082                     |

**Figure 13:**  
5.0V and 3.3V Power Supply Options



Setting valid for one sensor IC. Double setting necessary for AS5247U.

## Dynamic Angle Error Compensation

The AS5x47U uses 4 integrated Hall sensors which produce a voltage proportional to the orthogonal component of the magnetic field to the die. These voltage signals are amplified, filtered, and converted into the digital domain to allow the CORDIC digital block to calculate the angle of the magnetic vector. The propagation of these signals through the analog front-end and digital back-end generates a fixed delay between the time of measurement and the availability of the measured angle at the outputs. This latency generates a dynamic angle error represented by the product of the angular speed ( $\omega$ ) and the system propagation delay ( $t_{\text{delay}}$ ):

$$(EQ1) \quad DAE = \omega \times t_{\text{delay}}$$

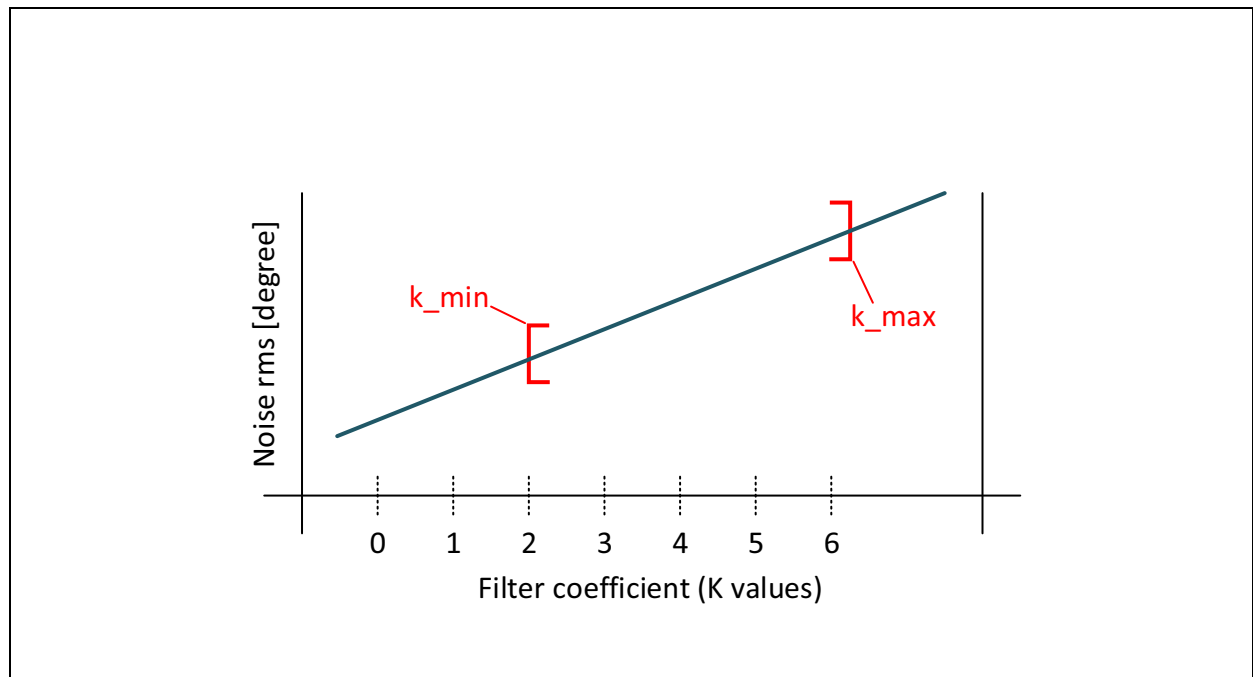
The dynamic angle compensation block calculates the current magnet rotation speed ( $\omega$ ) and multiplies it with the system propagation delay ( $t_{\text{delay}}$ ) to determine the correction angle to reduce this error. At constant speed, the residual system propagation delay is  $t_{\text{delay\_DAEC}}$ .

The angle represented on the PWM interface is not compensated by the Dynamic Angle Error Compensation algorithm. It is also possible to disable the Dynamic Angle Error Compensation with the DAECDIS setting. Disabling the Dynamic Angle Error Compensation gives a noise benefit of 0.016 degree rms. This setting can be advantageous for low speed (under 100 RPM) respectively static positioning applications.

## Adaptive Filter System

The AS5x47U uses an implemented adaptive filter system, which reduces the transition noise. The filter works dynamically depending on acceleration (positive and negative acceleration) of rotating system. It is able to match the right filter coefficients automatically. The filter coefficients (K value), which define also the limits in which the filters is acting, can be set in the OTP ( $K_{\text{min}} = 0x00$  and  $K_{\text{max}} = 0x00$  by default). In addition, there is the possibility to turn off the filter in the OTP.

**Figure 14:**  
Noise vs K Values



For detailed application information please refer to the  
Application Note: AS5x47U\_Adaptive\_Filter.

**Figure 15:**  
K Value Configuration

| K_Min [LSB] | Minimum K Value | K_Max [LSB] | Minimum K Value |
|-------------|-----------------|-------------|-----------------|
| 000         | 2               | 000         | 6               |
| 001         | 3               | 001         | 5               |
| 010         | 4               | 010         | 4               |
| 011         | 5               | 011         | 3               |
| 100         | 6               | 100         | 5               |
| 101         | 0               | 101         | 1               |
| 110         | 1               | 110         | 0               |
| 111         | 1               | 111         | 0               |



**Figure 16:**  
**Adaptive Filter System Setting**

| Symbol  | Parameter              | Min   | Typ | Max   | Unit | Notes   |
|---------|------------------------|-------|-----|-------|------|---|
| fcorner | Corner frequency       | 48    |     | 3059  | Hz   | Depending on K setting in the OTP               |
| ONFdyn  | Noise during rotation  | 0.019 |     | 0.086 | °    | RMS noise (depending on the selected K setting) |
| ONFstat | Noise when stand still | 0.011 |     | 0.084 | °    | Depending on K setting in the OTP               |

**Figure 17:**  
**Corner Frequency vs Noise**

| K Value | fcorner<br>Filter Corner<br>Frequency [Hz] | ONFdyn<br>Noise During<br>Rotation<br>[degree] | ONFstat<br>Noise When Stand Still<br>[degree] |
|---------|--|--|---|
| 0       | 48   | 0.019  | 0.011   |
| 1       | 97   | 0.028  | 0.017   |
| 2       | 194  | 0.036  | 0.032   |
| 3       | 387  | 0.048  | 0.044   |
| 4       | 773  | 0.062  | 0.059   |
| 5       | 1548                                       | 0.077  | 0.077   |
| 6       | 3095                                       | 0.086  | 0.084   |

## Speed Measurements

The AS5x47U features an average angular velocity calculation algorithm with 14-bit resolution. This angular velocity information is available over SPI and can be used without further averaging in the ECU is needed.

**Figure 18:**  
Angular Velocity Measurement Parameter

| Symbol       | Parameter                      | Min    | Typ    | Max   | Unit    | Notes  |
|--------------|--------------------------------|--------|--------|-------|---------|--|
| $V_{Res}$    | Velocity signal resolution     |        | 14     |       | bit     | Two's complement value   |
| $V_{Range}$  | Measurement range (default)    | -28000 |        | 28000 | rpm     |  |
| $V_{SENS}$   | Velocity sensitivity (default) |        | 24.141 |       | °/s/bit | 14-bit resolution  |
| $V_{ERROR}$  | Velocity total error           |        |        | ±5    | %       | Based on actual rotation speed                                     |
| $F_{Cutoff}$ | Cut off frequency              | 16.9   | 68.4   | 231   | Hz      | Depending on K value (see <a href="#">Adaptive Filter System</a> ) |

**Figure 19:**  
Angular Velocity Measurement Filter Parameters

| Filter Setting | Typ   | Unit | Notes     |
|----------------|-------|------|-----------|
| K=0            | 5.8   | °/s  | RMS noise |
| K=1            | 6     |      |           |
| K=2            | 8.4   |      |           |
| K=3            | 19.8  |      |           |
| K=4            | 51.8  |      |           |
| K=5            | 121.9 |      |           |
| K=6            | 244.9 |      |           |

## SPI Interface (Slave)

The SPI interface shall connected to a host microcontroller (master) to read or write the volatile memory as well as to program the non-volatile OTP registers.

The AS5x47U SPI only supports slave operation mode. It communicates at clock rates up to 10 MHz.

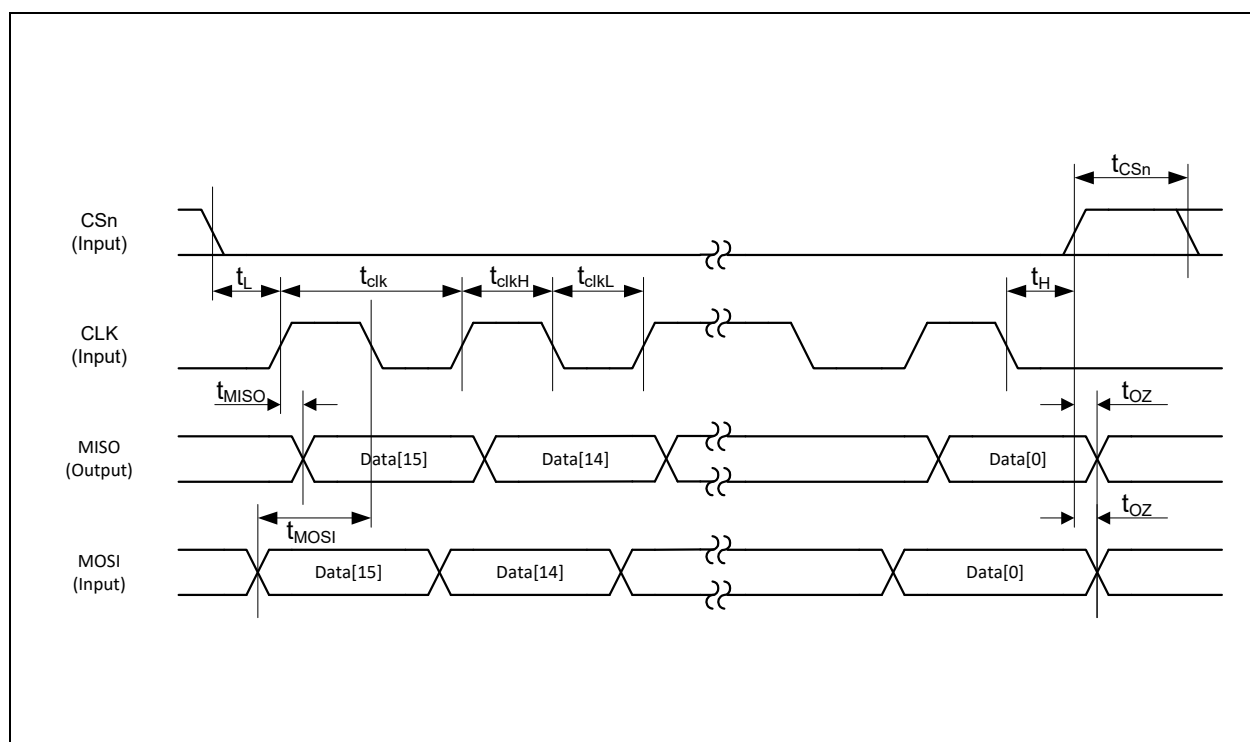
The AS5x47U SPI uses mode=1 (CPOL=0, CPHA=1) to exchange data. As shown in [Figure 20](#), a data transfer starts with the falling edge of CSn (CLK is low). The AS5x47U samples MOSI data on the falling edge of CLK. SPI commands are executed at the end of the frame (rising edge of CSn). The bit order is MSB first.

A CRC is protecting the SPI Data.

## SPI Timing

The AS5x47U SPI timing is shown in [Figure 20](#).

**Figure 20:**  
SPI Timing Diagram



**Figure 21:**  
**SPI Timing**

| Parameter  | Description  | Min                | Max | Units |
|------------|--|--------------------|-----|-------|
| $t_L$      | Time between CSn falling edge and CLK rising edge            | 350 <sup>(1)</sup> |     | ns    |
| $t_{CLK}$  | Serial clock period  | 100                |     | ns    |
| $t_{CLKL}$ | Low period of serial clock                                   | 50                 |     | ns    |
| $t_{CLKH}$ | High period of serial clock                                  | 50                 |     | ns    |
| $t_H$      | Time between last falling edge of CLK and rising edge of CSn | $t_{CLK}/2$        |     | ns    |
| $t_{XSSH}$ | High time of SS/ between two transmissions                   | 350 <sup>(1)</sup> |     | ns    |
| $t_{MOSI}$ | Data input valid to clock edge                               | 20                 |     | ns    |
| $t_{MISO}$ | CLK edge to data output valid                                |                    | 51  | ns    |
| $t_{OZ}$   | Time between CSn rising edge and MISO HiZ                    |                    | 10  | ns    |

**Note(s):**

1. Synchronization with the internal clock  $\rightarrow 2 * t_{CLK\_SYS} + 10ns$  ( $t_{CLK\_SYS}$  is 9MHz, typ.)

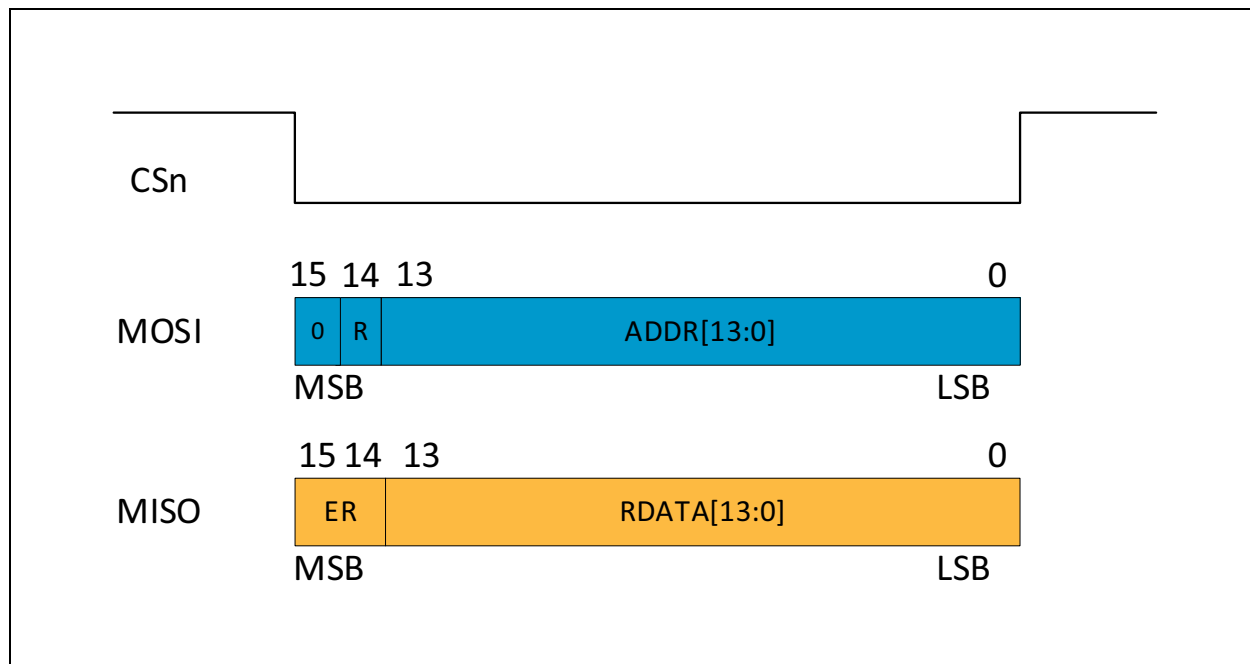
### SPI Transaction

AS5x47U provides two different SPI transactions

- 16-bit SPI frame without CRC (for high throughput)
- 24-bit SPI frames with CRC
- 32-bit SPI frames with CRC. The 32-bit SPI frames includes 8-bit PAD word.

For high-throughput requirements, the AS5x47U can handle 16-bit frames for read operations. This allows reading more than 400000 angle positions per second.

**Figure 22:**  
**16-Bit SPI Frame**



**Figure 23:**  
**16-Bit Command Frame**

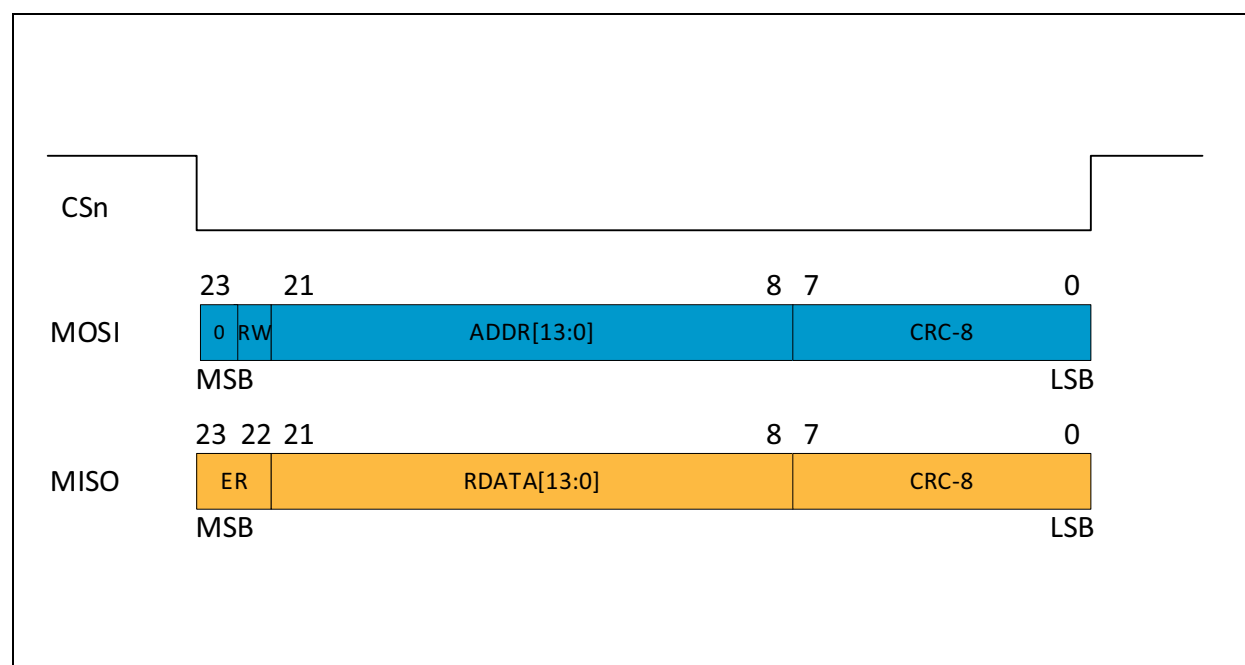
| Bit  | Name       | Description |
|------|------------|-------------|
| 15   | 0          | Do not Care |
| 14   | R          | 1: Read     |
| 13:0 | ADDR[13:0] | Address     |

**Figure 24:**  
**16-Bit Data Frame**

| Bit  | Name       | Description |
|------|------------|-------------|
| 15   | ER         | Warning Bit |
| 14   |            | Error Bit   |
| 13:0 | DATA[13:0] | Data        |

24-bit SPI frames and 32-bit SPI frames have CRC for increased reliability of communication over the SPI. A wrong setting of the calculation / setting of the CRC causes a CRC error, which sets the CRCERR bit in the error flag register.

**Figure 25:**  
**24-Bit SPI Frame**



**Figure 26:**  
**24-Bit Command Frame**

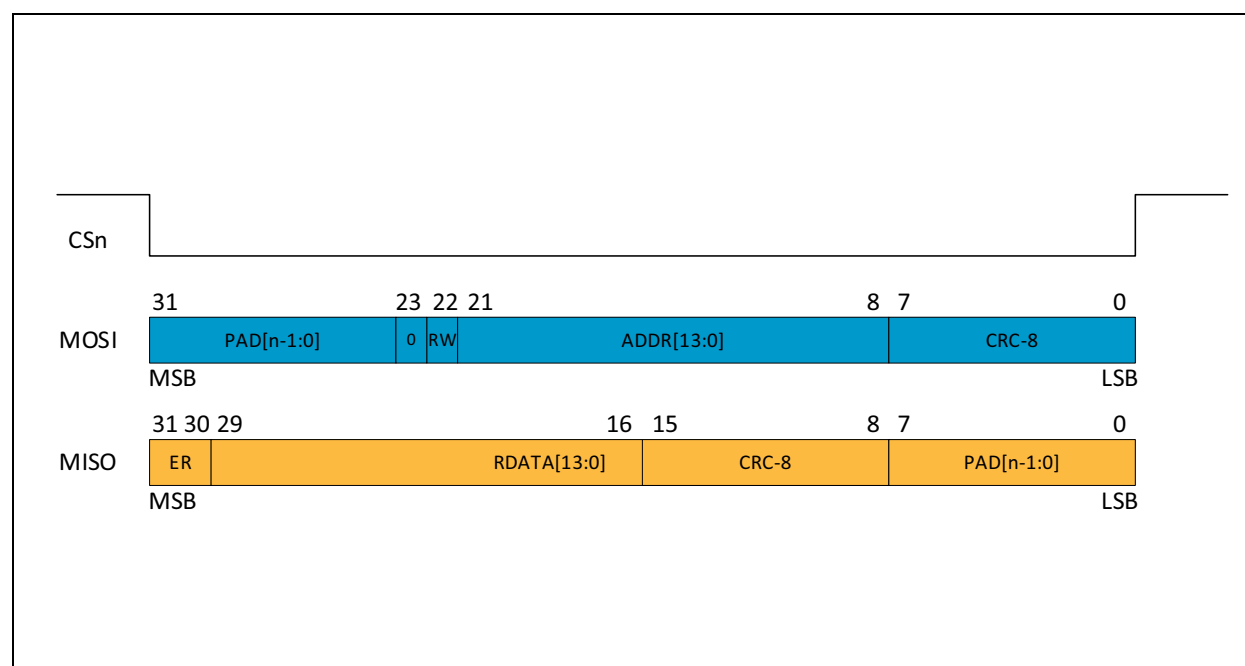
| Bit  | Name       | Description         |
|------|------------|---------------------|
| 23   | 0          | Do not Care         |
| 22   | RW         | 0: Write<br>1: Read |
| 21:8 | ADDR[13:0] | Address             |
| 7:0  | CRC        | Calculated CRC      |

**Figure 27:**  
**24-Bit Data Frame**

| Bit  | Name       | Description    |
|------|------------|----------------|
| 23   | ER         | Warning Bit    |
| 22   |            | Error Bit      |
| 21:8 | DATA[13:0] | Data           |
| 7:0  | CRC        | Calculated CRC |

The 32-bit frames have a “PAD Word”, which is applicable for operation in daisy chain mode. In automotive applications, the PAD Word can be used as additional communication protection.

**Figure 28:**  
**32-Bit SPI Frame**



**Figure 29:**  
**32-Bit Command Frame**

| Bit   | Name | Description         |
|-------|------|---------------------|
| 31:24 | PAD  | PAD Number          |
| 23    | 0    | Do Not care         |
| 22    | RW   | 0: Write<br>1: Read |

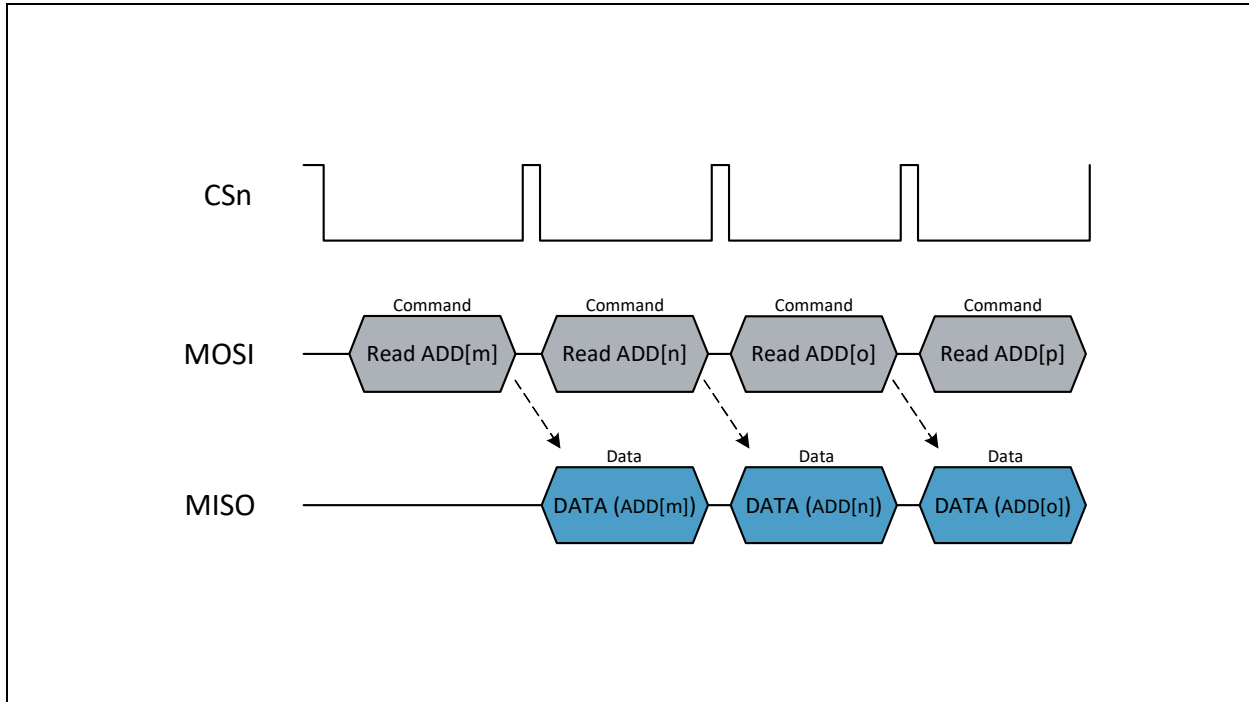
| Bit  | Name       | Description    |
|------|------------|----------------|
| 21:8 | ADDR[13:0] | Address        |
| 7:0  | CRC        | Calculated CRC |

Figure 30:  
32-Bit Data Frame

| Bit   | Name | Description    |
|-------|------|----------------|
| 31    | ER   | Warning Bit    |
| 30    |      | Error Bit      |
| 29:16 | Data | Data           |
| 15:8  | CRC  | Calculated CRC |
| 7:0   | PAD  | PAD Number     |

The data sent on the MISO pin. The CRC is calculated by the AS5147U/AS5247U. If an error or a warning is detected in the previous SPI command frame, the Error or Warning bit is set high. The SPI read is synchronized on the rising edge of CSn and the data is transmitted on MISO with the next read command, as shown in [Figure 31](#)

Figure 31:  
SPI Read

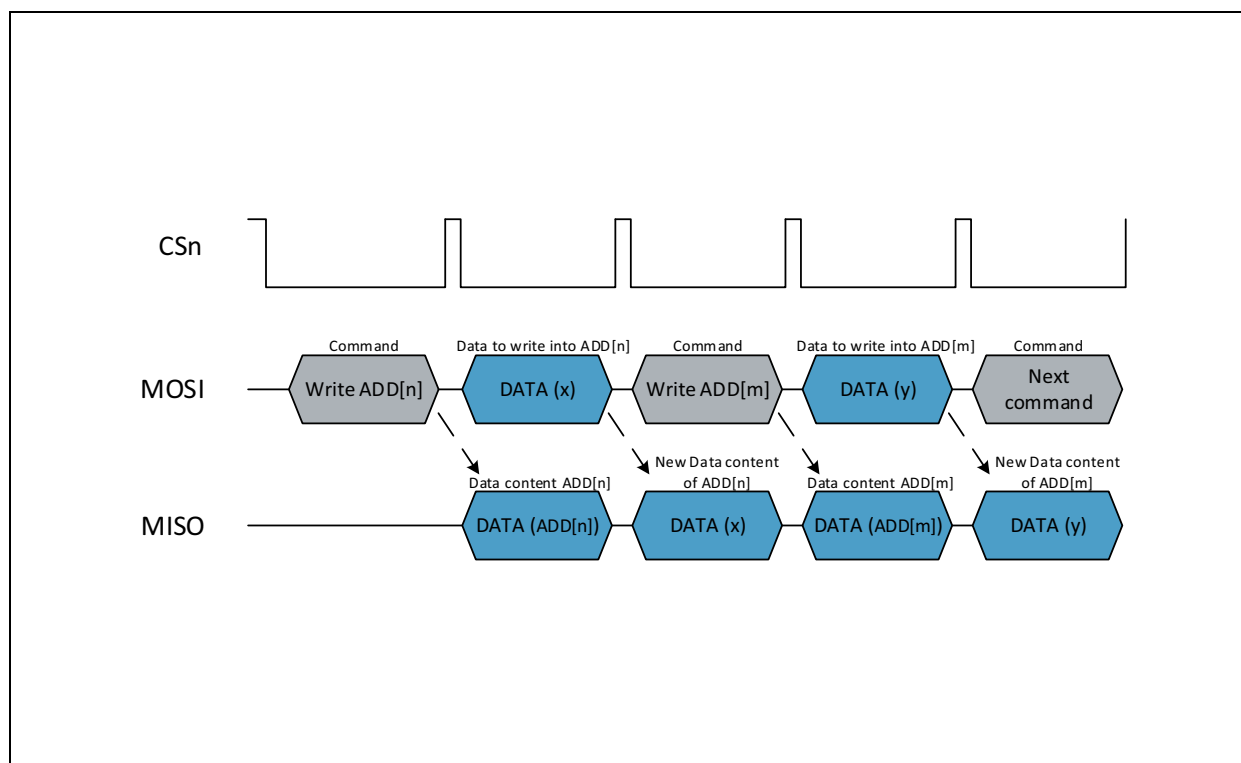


Recommended CRC calculation see chapter [CRC Checksum](#) In an SPI write transaction, the write command frame is followed by a write data frame at MOSI. The write data frame consists of



the new content of register which address is in the command frame. During the new content is transmitted on MOSI by the write data frame, the old content is send on MISO. At the next command on MOSI the actual content of the register is transmitted on MISO, as shown in [Figure 32](#).

**Figure 32:**  
**SPI Write**



### **PAD Word**

Any number of PAD [8\*n-1:0] bits can precede the MOSI data. The PAD word is used to allocate the data on MISO to the correct device.

### **CRC Checksum**

For secure and reliable data transmission, the 24-bit and 32-bit frames have a CRC for verification of correct transmission. The CRC is calculated out of the payload of SPI frames (e.g.: CRC is calculated out of bit 23:8 from 24-bit command frame)

The calculation of the CRC is based on Irreducible polynomial  $x^8 + x^4 + x^3 + x^2 + 1$  according to standard J1850.

The initialization CRC = 0xFF prevents that 0x000000 is a valid SPI command. This command would clear all sticky error flags.

## Volatile Registers

The volatile registers are shown in [Figure 33](#). Each register has a 14-bit address.

**Figure 33:**  
Volatile Memory Register Description

| Address | Name         | Default   | Description  |
|---------|--------------|---|--|
| 0x0000  | NOP          | 0x0000  | No operation   |
| 0x0001  | ERRFL        | 0x0000  | Error register   |
| 0x0003  | PROG         | 0x0000  | Programming register                                     |
| 0x3FF5  | DIA          | 0xX3C2 or 0xXBC2 for 3.3V mode, 0xX3C3 or 0xXBC3 for 5 V mode | DIAGNOSTIC   |
| 0x3FF9  | AGC          | 0x0000  | AGC Value  |
| 0x3FFA  | Sin-data     | 0x0000  | Raw digital sine channel data                            |
| 0x3FFB  | Cos-data     | 0x0000  | Raw digital cosine channel data                          |
| 0x3FFC  | VEL          | 0x0000  | Velocity   |
| 0x3FFD  | MAG          | 0x0000  | CORDIC magnitude   |
| 0x3FFE  | ANGLEUNC     | 0x0000  | Measured angle without dynamic angle error compensation  |
| 0x3FFF  | ANGLECOM     | 0x0000  | Measured angle with dynamic angle error compensation     |
| 0x00D1  | ECC_Checksum | 0x000   | ECC checksum calculated based on actual register setting |

**Figure 34:**  
ERRFL (0x0001)

| Name               | Read/Write | Bit Position | Description   |
|--------------------|------------|--------------|---|
| CORDIC Overflow    | R          | 10           | Reading the Overflow bit of the CORDIC  |
| OffCompNotFinished | R          | 9            | In case the flag is 1 the internal offset compensation is not finished  |
| BRKHALL            | R          | 8            | Broken Hall element information   |
| WDTST              | R          | 7            | <b>Watchdog information.</b> In case the flag sets to 1, the internal oscillator or the watchdog is not working correctly |

| Name           | Read/Write | Bit Position | Description   |
|----------------|------------|--------------|---|
| CRC error      | R          | 6            | CRC error during SPI communication  |
| Command_ error | R          | 5            | SPI invalid command received  |
| Framing error  | R          | 4            | Framing if SPI communication wrong  |
| P2ram_error    | R          | 3            | ECC has detected 2 uncorrectable errors in P2RAM in customer area   |
| P2ram_warning  | R          | 2            | ECC is correcting one bit of P2RAM in customer area   |
| MagHalf        | R          | 1            | This flag sets to 1 in case the AGC Value reaches 255 LSB and the magnitude value is the half of the of the regulated magnitude value (between AGC = 0LSB and AGC = 255LSB) which is typical 4800LSB. |
| Agc-warning    | R          | 0            | Agc-warning=1. The flag sets to 1 in case the AGC Value reaches 0LSB or 255LSB. The detailed information which level is reached can be found in the diagnostic register.                              |

Reading the ERRFL register automatically clears its contents (ERRFL=0x0000). In case of an error flag, a read of the DIA register is mandatory

**Figure 35:**  
**PROG (0x0003)**

| Name    | Read/Write | Bit Position | Description   |
|---------|------------|--------------|---|
| PROGVER | R/W        | 6            | Program verify: Must be set to 1 for verifying the correctness of the OTP programming |
| PROGOTP | R/W        | 3            | Start OTP programming cycle   |
| OTPREF  | R/W        | 2            | Refreshes the non-volatile memory content with the OTP programmed content             |
| PROGEN  | R/W        | 0            | Program OTP enable: Enables reading / writing the OTP memory                          |

The PROG register is used for programming the OTP memory.

**Figure 36:**  
**DIA(0x3FF5)**

| Name       | Read/Write | Bit Position | Description                    |
|------------|------------|--------------|--------------------------------|
| SPI_cnt    | R          | 11:12        | SPI frame counter              |
| Fusa_error | R          | 10           | Error flag broken Hall element |

| Name              | Read/Write | Bit Position | Description  |
|-------------------|------------|--------------|--|
| AGC_finished      | R          | 9            | Initial AGC settling finished                          |
| Off comp finished | R          | 8            | Error flag offset compensation finished                |
| SinOff_fin        | R          | 7            | Sine offset compensation finished                      |
| CosOff_fin        | R          | 6            | Cosine offset compensation finished                    |
| MagHalf_flag      | R          | 5            | Error flag magnitude is below half of target value     |
| Comp_h            | R          | 4            | Warning flag AGC high                                  |
| Comp_l            | R          | 3            | Warning flag AGC low                                   |
| Cordic_overflow   | R          | 2            | Error flag CORDIC overflow                             |
| LoopsFinished     | R          | 1            | All magneto core loops finished                        |
| Vdd_mode          | R          | 0            | VDD supply mode:<br>0: VDD 3.0 Mode<br>1: VDD 5.0 Mode |

**Figure 37:**  
**AGC(0x3FF9)**

| Name | Read/Write | Bit Position | Description     |
|------|------------|--------------|-----------------|
| AGC  | R          | 7:0          | 8-bit AGC value |

**Figure 38:**  
**VEL(0x3FFC)**

| Name | Read/Write | Bit Position | Description                            |
|------|------------|--------------|--|
| Vel  | R          | 13:0         | Velocity value (14-bit signed integer) |

**Figure 39:**  
**MAG (0x3FFD)**

| Name | Read/Write | Bit Position | Description                  |
|------|------------|--------------|------------------------------|
| Mag  | R          | 13:0         | CORDIC magnitude information |

**Figure 40:**  
**ANGLEUNC (0x3FFE)**

| Name     | Read/Write | Bit Position | Description  |
|----------|------------|--------------|--|
| ANGLEUNC | R          | 13:0         | Angle information without dynamic angle error compensation |

**Figure 41:**  
**ECC\_s (0x3FD0)**

| Name  | Read/Write | Bit Position | Description             |
|-------|------------|--------------|-------------------------|
| ECC_s | R          | 6:0          | Calculated ECC checksum |

**Figure 42:**  
**ANGLECOM(0x3FFF)**

| Name     | Read/Write | Bit Position | Description   |
|----------|------------|--------------|---|
| ANGLECOM | R          | 13:0         | Angle information with dynamic angle error compensation |

### Non-Volatile Registers (OTP)

The OTP (One-Time Programmable) memory is used to store the absolute zero position of the sensor and the customer settings permanently in the sensor IC. SPI write/read access is possible several times for all non-volatile registers (soft write). Soft written register content will be lost after a hardware reset. The programming itself can be done just once. Therefore the content of the non-volatile registers is stored permanently in the sensor. The register content is still present after a hardware reset and cannot be overwritten. For a correct function of the sensor the OTP programming is not required. If no configuration or programming is done, the non-volatile registers are in the default state 0x0000.

**Figure 43:**  
**Non-Volatile Register Table**

| Address | Name      | Default | Description                         |
|---------|-----------|---------|-------------------------------------|
| 0x0015  | DISABLE   | 0x0000  | Outputs and filter disable register |
| 0x0016  | ZPOSM     | 0x0000  | Zero position MSB                   |
| 0x0017  | ZPOSL     | 0x0000  | Zero position LSB/ MAG diagnostic   |
| 0x0018  | SETTINGS1 | 0x0000  | Customer setting register 1         |
| 0x0019  | SETTINGS2 | 0x0000  | Customer setting register 2         |
| 0x001A  | SETTINGS3 | 0x0000  | Customer setting register 3         |
| 0x001B  | ECC       | 0x0000  | ECC Settings                        |

**Figure 44:**  
**DISABLE (0x0015)**

| Name           | Read/Write/Program | Bit Position | Description   |
|----------------|--------------------|--------------|---|
| UVW_off        | R/W/P              | 0            | 0: Normal mode (default)<br>1: Switch UVW output off (tristate)           |
| ABI_off        | R/W/P              | 1            | 0: Normal mode (default)<br>1: Switch ABI output off (tristate)           |
| BRKHALL_Set    | R/W/P              | 2:5          | 0: Broken Hall element mechanism off<br>>1: Broken Hall element threshold |
| FILTER_disable | RW                 | 6            | 0: Filter enabled (default)<br>1: Filter disabled                         |

**Figure 45:**  
**ZPOS (0x0016)**

| Name | Read/Write/Program | Bit Position | Description                                  |
|------|--------------------|--------------|--|
| ZPOS | R/W/P              | 7:0          | 8 most significant bits of the zero position |

**Figure 46:**  
**ZPOS (0x0017)**

| Name    | Read/Write/Program | Bit Position | Description  |
|---------|--------------------|--------------|--|
| ZPOS    | R/W/P              | 5:0          | 6 least significant bits of the zero position                |
| Dia1_en | R/W/P              | 6            | Default=0; Enables the safe states of SM1 and SM4 on ABI/UVW |
| Dia2_en | R/W/P              | 7            | Default=0; Enables the safe states of SM8 on ABI/UVW         |

**Figure 47:**  
**SETTINGS1 (0x0018)**

| Name    | Read/Write/Program | Bit Position | Description  |
|---------|--------------------|--------------|--|
| k_max   | R/W/P              | 2:0          | K max. for adaptive filter setting                     |
| K_min   | R/W/P              | 5:3          | K min. for adaptive filter setting                     |
| Dia3_en | R/W/P              | 6            | Default=0<br>Enables the safe states of SM2 on ABI/UVW |

**Figure 48:**  
**SETTINGS2 (0x0019)**

| Name        | Read/Write/Program | Bit Position | Description  |
|-------------|--------------------|--------------|--|
| IWIDTH      | R/W/P              | 0            | 0: 3 pulses<br>1: 1 pulse  |
| NOISESET    | R/W/P              | 1            | Noise setting for 3.3V operation at 150°C  |
| DIR         | R/W/P              | 2            | Rotation direction   |
| UVW_ABI     | R/W/P              | 3            | Defines the PWM output<br>(0=ABI is operating, W is used as PWM)<br>(1=UVW is operating, I is used as PWM) |
| DAECDIS     | R/W/P              | 4            | Disable dynamic angle error compensation<br>(0=DAE compensation ON,<br>1=DAE compensation OFF)             |
| ABI_DEC     | R/W/P              | 5            | ABI setting to decimal count   |
| Data_select | R/W/P              | 6            | This bit defines which data can be read from<br>address 16383dec (3FFFhex)<br>0-> ANGLECOM<br>1-> ANGLEUNC |
| PWMon       | R/W/P              | 7            | Enables PWM (setting of UVW_ABI bit<br>necessary)  |

**Figure 49:**  
**SETTINGS3 (0x001A)**

| Name   | Read/Write/Program | Bit Position | Description              |
|--------|--------------------|--------------|--------------------------|
| UVWPP  | R/W/P              | 2:0          | UVW number of pole pairs |
| HYS    | R/W/P              | 4:3          | Hysteresis               |
| ABIRES | R/W/P              | 7:5          | Resolution of ABI        |

**Figure 50:**  
**ECC (0x001B)**

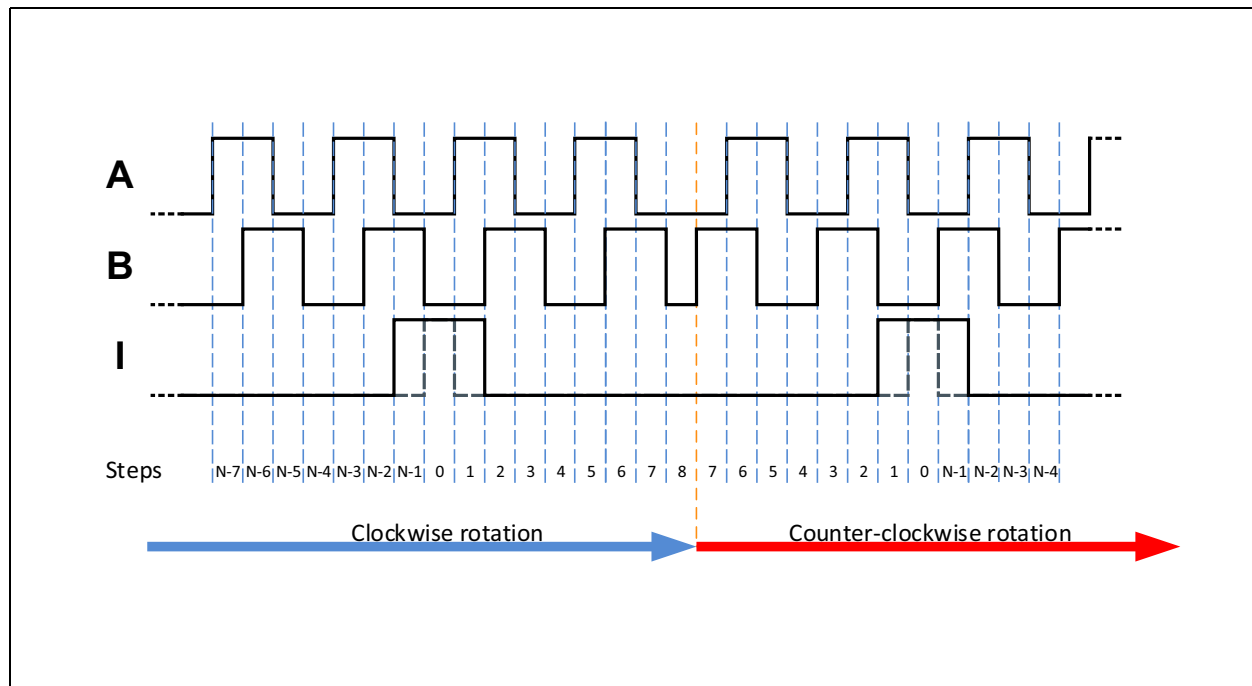
| Name      | Read/Write/Program | Bit Position | Description  |
|-----------|--------------------|--------------|--------------|
| Ecc_chsum | R/W/P              | 6:0          | ECC checksum |
| Ecc_en    | R/W/P              | 7            | Enables ECC  |

## ABI Incremental Interface

The AS5x47U can send the angle position to the host microcontroller through an incremental interface. This interface is available simultaneously with the other interfaces. By default, the incremental interface is set to work at a 12-bit resolution which corresponds to 4096 steps per revolution or 1024 pulses per revolution (ppr). This resolution can be changed with the OTP bits ABIRES. The phase shift between the A and B signals indicates the rotation direction: clockwise (A leads, B follows) or counterclockwise (B leads, A follows). During the start-up time, after power on to the chip, all three ABI signals are high. The DIR bit can be used to invert the sense of the rotation direction.

The IWIDTH setting programs the width of the index pulse from 3 LSB (default) to 1 LSB.

**Figure 51:**  
ABI Signals



N = 16384 for 14-bit resolution, N = 4096 for 12-bit resolution and N = 1024 for 10-bit resolution..

The [Figure 51](#) shows the ABI signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0).

The rotation direction of the magnet is defined as clockwise (DIR=0) when the view is from the topside of AS5x47U.



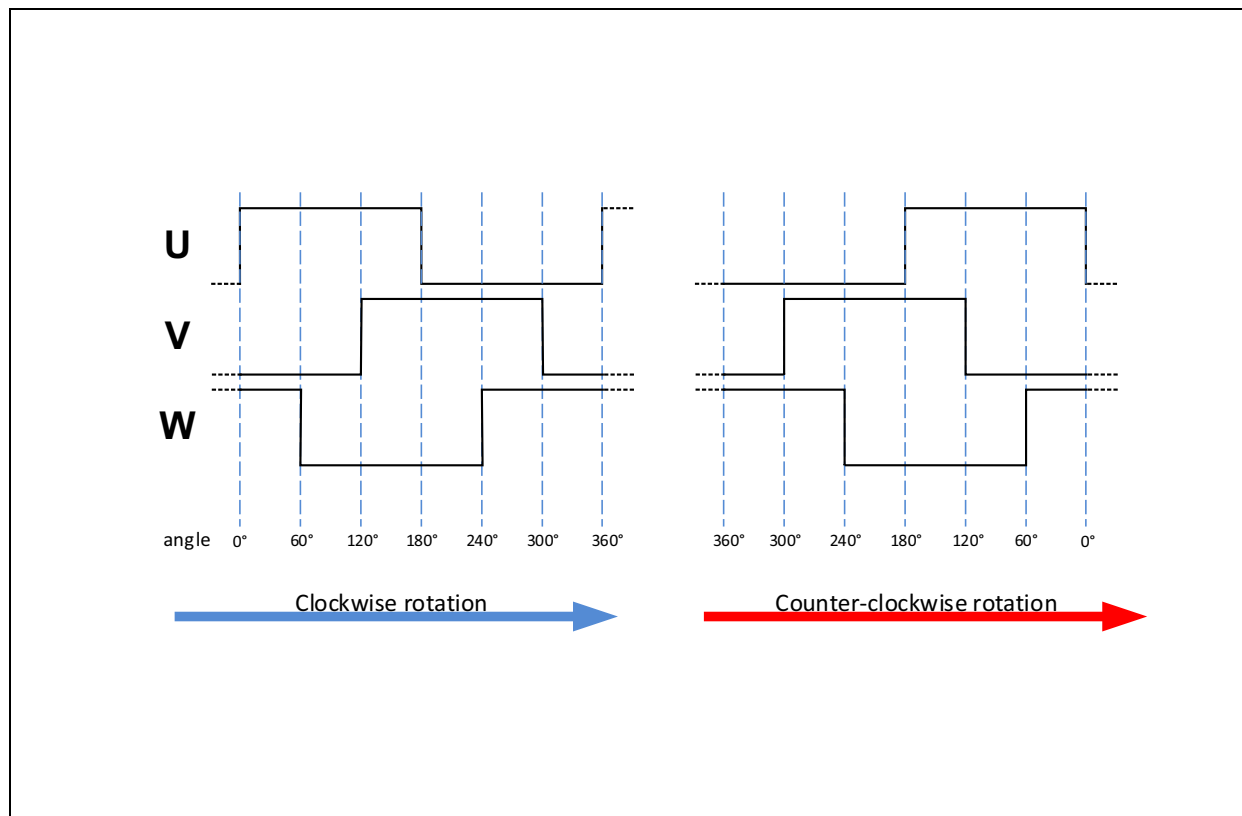
**Figure 52:**  
**ABI Settings**

| ABIRES [LSB]<br>SETTINGS3<br>(0x001A) | ABI_DEC<br>SETTINGS2<br>(0x0019) | ABI_Pulses | ABI Resolution [LSB] |
|---------------------------------------|----------------------------------|------------|----------------------|
| 100                                   | 0                                | 4096       | 16384                |
| 011                                   | 0                                | 2048       | 8192                 |
| 000                                   | 0                                | 1024       | 4096 (default value) |
| 001                                   | 0                                | 512        | 2048                 |
| 010                                   | 0                                | 256        | 1024                 |
| 000                                   | 1                                | 1000       | 4000                 |
| 001                                   | 1                                | 500        | 2000                 |
| 010                                   | 1                                | 400        | 1600                 |
| 011                                   | 1                                | 300        | 1200                 |
| 100                                   | 1                                | 200        | 800                  |
| 101                                   | 1                                | 100        | 400                  |
| 110                                   | 1                                | 50         | 200                  |
| 111                                   | 1                                | 25         | 100                  |

### UVW Commutation Interface

The AS5x47U can emulate the UVW signals generated by the three discrete Hall switches commonly used in BLDC motors. The UVWPP field in the SETTINGS3 register selects the number of pole pairs of the motor (from 1 to 7 pole pairs). The UVW signals are generated with 14-bit resolution. During the start-up time, after power on of the chip, the UVW signals are low.

**Figure 53:**  
UVW Signals



The Figure 53 shows the UVW signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0). The rotation direction of the magnet is defined as clockwise (DIR=0) when the view is from the topside of AS5x47U. With the bit DIR, it is possible to invert the rotation direction.

**Figure 54:**  
UVW Settings

| UVWPP [LSB] | Pole Pairs    |
|-------------|---------------|
| 000         | 1pp (default) |
| 001         | 2pp           |
| 010         | 3pp           |
| 011         | 4pp           |

| UVWPP [LSB] | Pole Pairs |
|-------------|------------|
| 100         | 5pp        |
| 101         | 6pp        |
| 110         | 7pp        |
| 111         | 7pp        |

### PWM

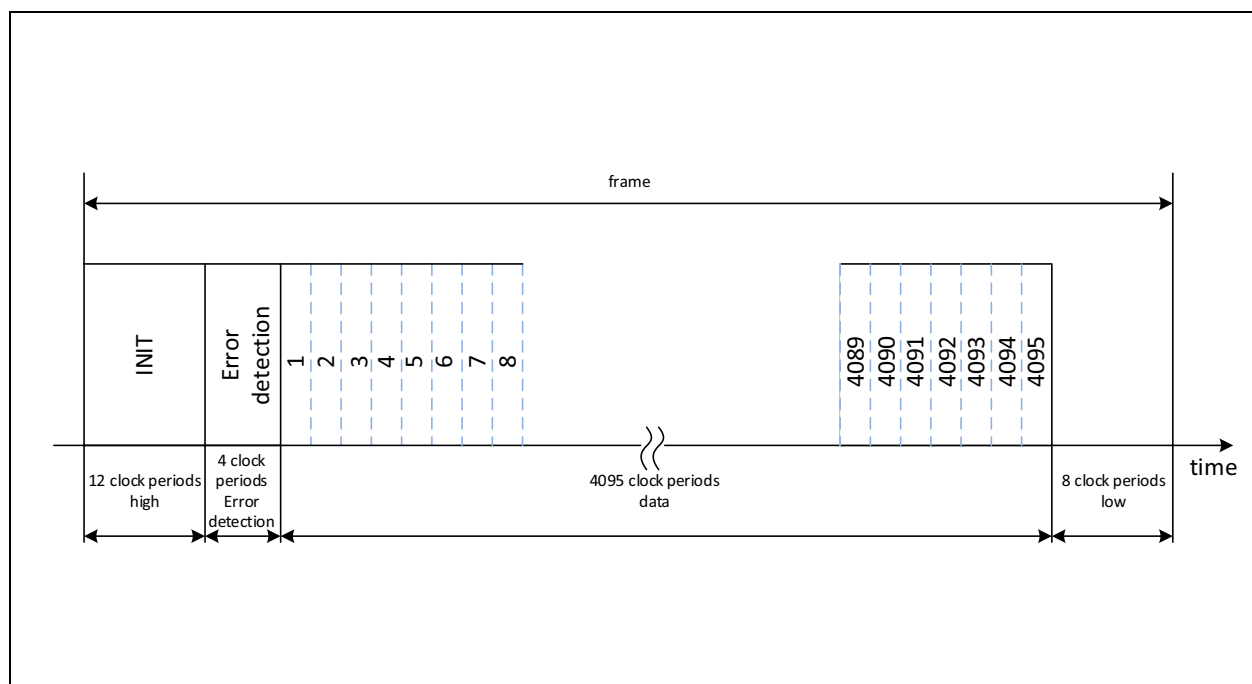
The PWM can be enabled with the bit setting PWMon. The PWM encoded signal is displayed on the pin W or the pin I. The bit setting UVW\_ABI defines which output is used as PWM. The PWM output consists of a frame of 4119 PWM clock periods, as shown in Figure 55. The PWM frame has the following sections:

- 12 PWM Clocks for INIT
- 4 PWM Clocks for error detection
- 4095 PWM clock periods of data
- 8 PWM clock periods low

The angle is represented in the data part of the frame with a 12-bit resolution. One PWM clock period represents 0.088 degree and has a typical duration of 444ns.

If the embedded diagnostic of the AS5x47U detects any error the PWM interface displays only 12 clock periods high (0.3% duty-cycle). Respectively the 4 clocks for error detection are forced to low.

**Figure 55:**  
Pulse Width Modulation Encoded Signal



## Hysteresis

The hysteresis can be programmed in the HYS bits of the SETTINGS3 register. The hysteresis can be 1, 2, or 3 LSB bits, in which the LSB is defined by the ABI resolution setting (ABIRES).

**Figure 56:**  
Hysteresis Settings

| HYS | Hysteresis Related to 11-Bit ABI Resolution |
|-----|---|
| 00  | 1   |
| 01  | 2   |
| 10  | 3   |
| 11  | 0   |

## Automatic Gain Control (AGC) and CORDIC Magnitude

The AS5x47U uses AGC to compensate for variations in the magnetic field strength due to changes of temperature, air gap between the chip and the magnet, and demagnetization of the magnet. The automatic gain control value can be read in the AGC field of the AGC register. Within the specified input magnetic field strength (Bz), the Automatic Gain Control keeps the CORDIC magnitude value (MAG) constant.

If magnetic field strength is out of specifications, the AGC has its limits reached and the Agc-warning bit is set. When the magnetic field strength is decreasing more then AGC can control, the CORDIC magnitude is also decreasing.

If the CORDIC magnitude decreases lower than half of the target magnet, the error flag MagHalf\_flag is set

## Functional Safety

### *Safety Manual*

The safety manual, available upon request, contains all the necessary information for the system integrator, to integrate AS5147U or AS5247U in a safety related item.

AS5147U and AS5247U are developed as Safety Element out of Context (SEooC).

The Safety manual includes the following information:

- Product development lifecycle
- Description of the technical safety concept

- Detail information of assumption of use of the element with respect to its intended use which includes
  - Device safe state information
  - Fault tolerant time interval
  - Coverage information

Additionally, beside the safety manual, a verification summary document is available upon request. This document includes all safety verification and the summary of the safety analyses information.

An additional document (Verification and Safety Analysis report) which is part of the safety manual includes the following information:

- Description of safety analysis at device level
- HW architectural metric results
- Description of verifications based on the ISO26262
- Detailed FMEDA

### **Safety Mechanism**

AS5147U and AS5247U provide several self-diagnostic features (Safety Mechanism) which increases the safety coverage.

**Figure 57:**  
**Safety Mechanism**

| SM  | Mechanism           | Programmable UVW/ABI            | SPI                 | PWM                   | UVW/ABI            |
|-----|---------------------|---------------------------------|---------------------|-----------------------|--------------------|
| SM1 | Offset compensation | Yes, with Dia1_en (default off) | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |
| SM2 | AGC                 | Yes, with Dia3_en (default off) | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |
| SM3 | CORDIC overflow     | -                               | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |
| SM4 | Broken Hall element | Yes, with Dia4_en (default off) | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |
| SM5 | ECC                 |                                 | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |
| SM6 | CRC error           | -                               | SPI only            | N/A                   | N/A                |
| SM7 | Watchdog            | -                               | No communication    | According chapter PWM | UVW:000<br>ABI:111 |
| SM8 | Magnitude half      | Yes, with Dia2_en (default off) | Bit in DIA register | According chapter PWM | UVW:000<br>ABI:111 |

If an error happens, depending on the OTP setting, the outputs are going into the defined safe states. Additionally, each SPI data frame indicates the failure with the error and warning flag.

In case UVW/ABI interface should provide in case of an error the safe state, a programming option is included.

A detailed information about the different safety mechanism are included in the safety manual.

### **Broken Hall Element Function**

The broken Hall element detection (SM4), detects an error in the Hall element and the complete analog chain.

Additionally this feature can detect an increase of the system INL.

The threshold of the safety mechanism is programmable in case the system INL is higher than expected. The threshold value according the safety manual is 1024 LSB. A change of this threshold might be an influence on the safety requirement. The safety mechanism is disable in default use.

**Figure 58:**  
**BRK Threshold Settings**

| BRKHALL_SET [LSB]<br>DISABLE<br>(0x0015) | SM4 Threshold |
|--|---------------|
| 0000                                     | SM4 Off       |
| 0001                                     | 256           |
| 0010                                     | 512           |
| 0011                                     | 768           |
| 0100                                     | 1024          |
| 1000                                     | 2048          |
| 1111                                     | 3840          |

The threshold information shall be programmed into the BRKHALL\_SET, if the safety mechanism is used.

Detailed information about "System INL vs. Threshold" is available upon request.

### **ECC**

The ECC (Error Code Correction) is a mechanism which protects the customer settings.

The ECC protection is active whenever ECC\_en=1. ECC\_en is the error corrected counterpart of the P2RAM bit en and is found in register ECC\_STATUS. Whenever a bit error occurs, this is reported by the status register ERRFL [2:3]. Single bit errors are corrected immediately and do not influence the correct operation of the sensor. If either a single or double errors are detected, the next SPI MISO frame will report this to the software by setting flags error=1 (double bit error) or

warning=1 (single bit error). Warning and error are sticky flags, which guarantees that spurious P2RAM errors are certainly reported.

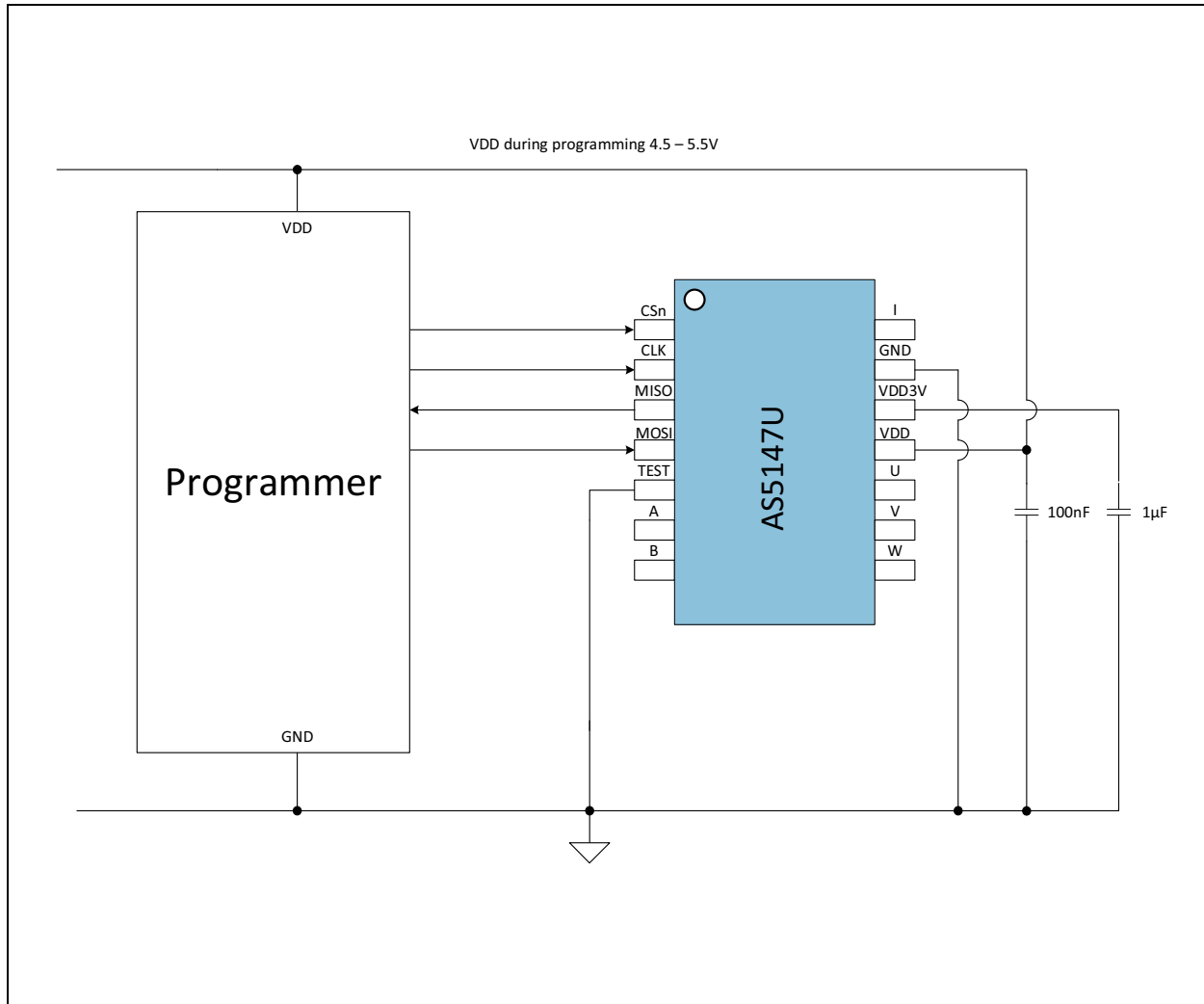
The ECC protection is activated with the following steps:

- Writing uses data into the register and set ECC\_en to high.
- Reading ECC\_s from register 0x3FD0 and set the value into ECC\_chsum. Do not overwrite the ECC\_en.
- Programming the part.

## Application Information

### Burn and Verification of the OTP Memory

**Figure 59:**  
Minimum Programming Diagram for the AS5147U with 5V Supply Voltage

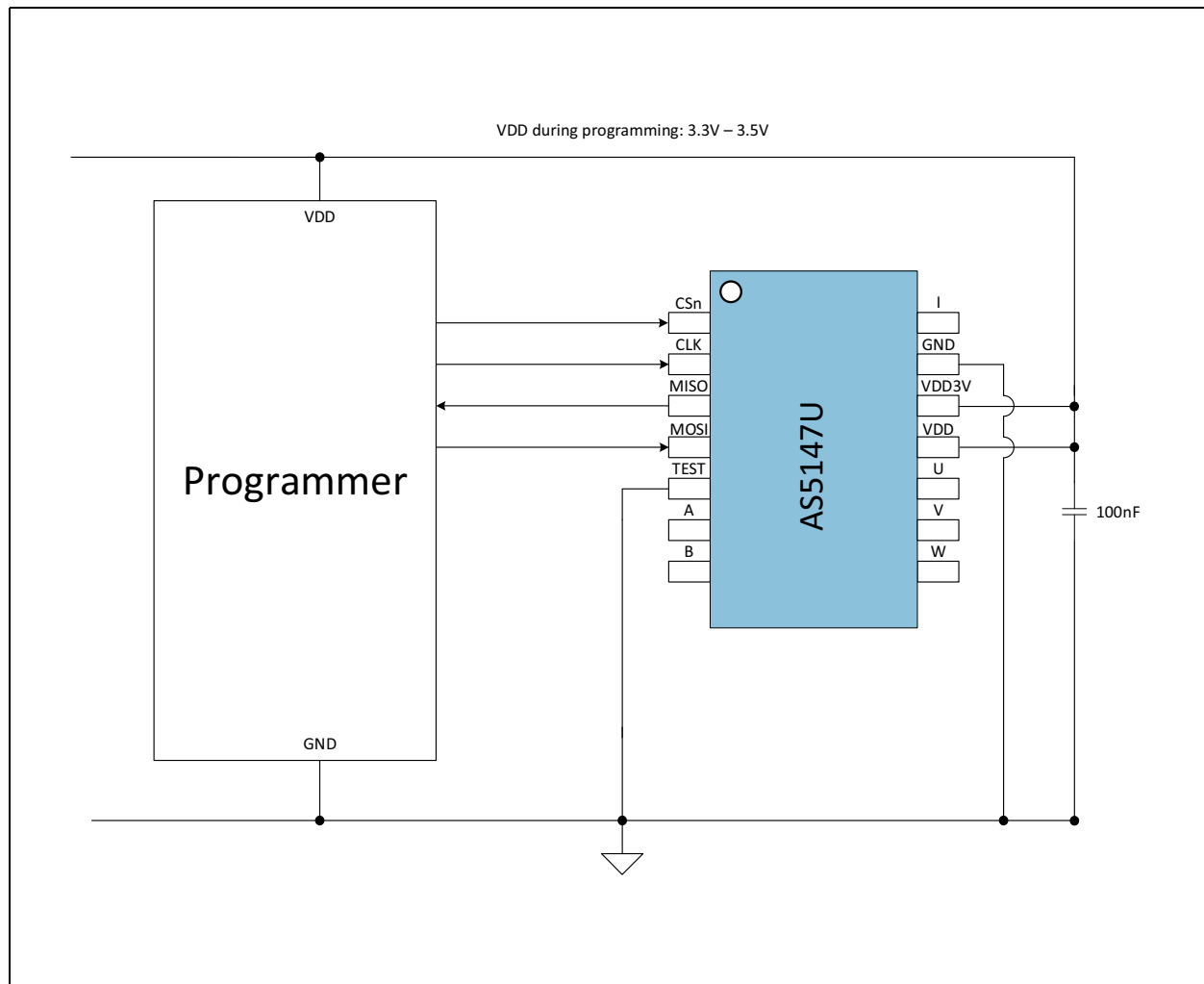


**Note(s):**

1. In terms of EMC and for remote application, additional circuits are necessary.



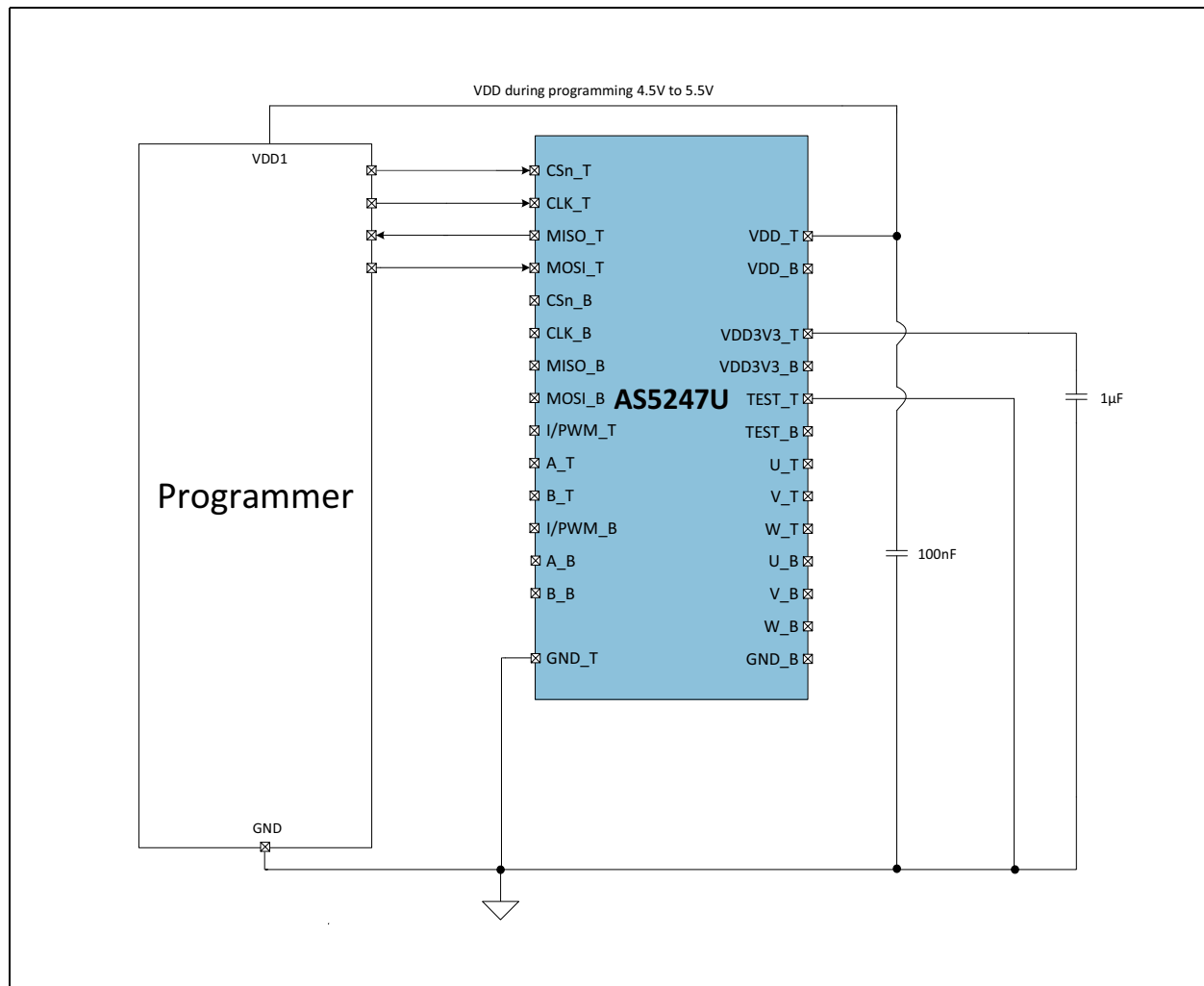
**Figure 60:**  
**Minimum Programming Diagram for the AS5147U with 3.3V Supply Voltage**



**Note(s):**

1. In terms of EMC and for remote application, additional circuits are necessary.

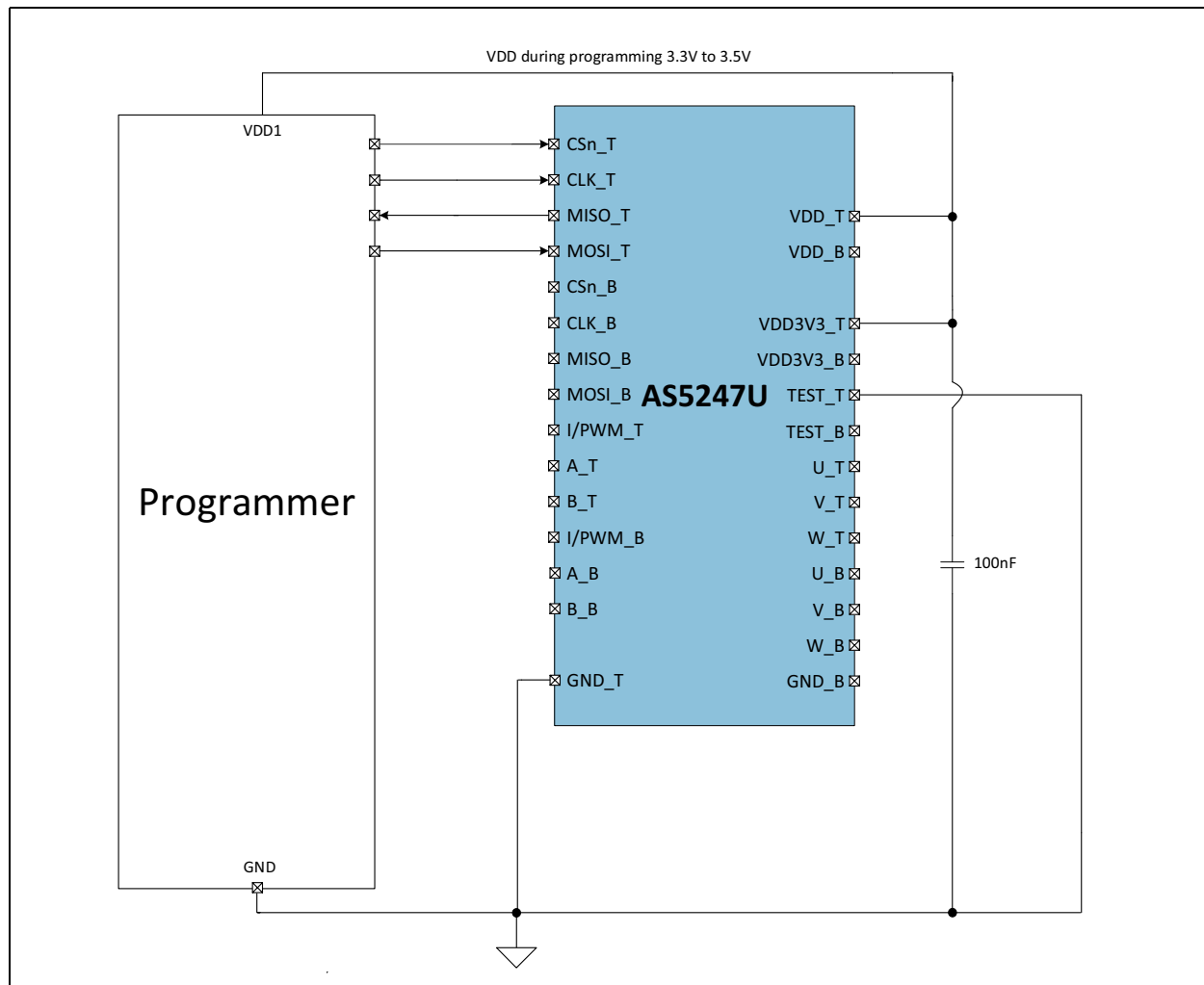
**Figure 61:**  
**Minimum Programming Diagram for AS5247U with 5V Supply Voltage**



**Note(s):**

1. In terms of EMC and for remote application, additional circuits are necessary.
2. Diagram shows only the connection to top die of AS5247U. For programming of bottom die the following pins have to be connected instead of the connection in the drawing: CSn\_B, CLK\_B, MISO\_B, MOSI\_B, GND\_B, VDD\_B, VDD3V3\_B, TEST\_B

**Figure 62:**  
**Minimum Programming Diagram for AS5247U with 3.3V Supply Voltage**



**Note(s):**

1. In terms of EMC and for remote application, additional circuits are necessary.
2. Diagram shows only the connection to topdie of AS5247U. For programming of bottom die the following pins have to be connected instead of the connection in the drawing: CSn\_B, CLK\_B, MISO\_B, MOSI\_B, GND\_B, VDD\_B, VDD3V3\_B, TEST\_B.

**Figure 63:**  
**Programming Parameter**

| Symbol      | Parameter               | Conditions  | Min | Typ | Max | Units |
|-------------|-------------------------|---|-----|-----|-----|-------|
| $T_{aProg}$ | Programming temperature | Programming @ room temperature (25°C ± 20°C)            | 5   |     | 45  | °C    |
| $V_{DD}$    | Positive supply voltage | 5 V operation mode. Supply voltage during programming   | 4.5 | 5   | 5.5 | V     |
| $V_{DD}$    | Positive supply voltage | 3.3 V operation mode. Supply voltage during programming | 3.3 |     | 3.5 | V     |
| $I_{Prog}$  | Current for programming | Max current during OTP burn procedure.                  |     |     | 100 | mA    |

**Note(s):**

1. Programming parameter valid for AS5147U and AS5247U

**Step-by-step procedure to permanently program the non-volatile memory (OTP):**

The programming can either be performed in 5V operation using the internal LDO (1μF on regulator output pin), or in 3V operation but using a supply voltage between 3.3V and 3.5V.

1. Power on cycle
2. Write the SETTINGS1 and SETTINGS2 and SETTINGS3 registers with the custom settings for this application
3. Place the magnet at the desired zero position
4. Read out the measured angle from the ANGLECOM register
5. Write ANGLECOM [5:0] into the ZPOSL register and ANGLECOM[13:6] into the ZPOSM register
6. Read Reg(0x0015) to Reg(0x001A)
7. Set ECC\_en in register ECC to 1 (ECC protection enabled)
8. Read ECC\_s (0x3FD0) to get the correct ECC key
9. Write ECC\_s key into ECC register
10. Set ECC\_en in register ECC to 1 (ECC protection enabled)
11. Read Reg(0x0015) to Reg(0x001B) → read register step1
12. Comparison of written content (settings and angle) with content of read register step1
13. If point 11 is correct, enable OTP read / write by setting PROGEN = 1 in the PROG register
14. Start the OTP burn procedure by setting PROGOTP = 1 in the PROG register
15. Read the PROG register until it reads 0x0001 (programming procedure complete)

16. Clear the memory content by writing 0x00 in the whole non-volatile memory
17. Set the PROGVER = 1 to set the guard band for the guard band test.<sup>1</sup>
18. Refresh the non-volatile memory content with the OTP content by setting OTPREF = 1
19. Read Reg(0x0015) to Reg(0x001B) → Read register step2
20. Comparison of written content (settings and angle) with content of read register step2. If a deviation in the comparison occurs, the guard band test was not successful. Reprogramming is not allowed.  
Mandatory: guard band test
21. New power on cycle
22. Read Reg(0x0016) to Reg(0x001B) → read register step3
23. Comparison of written content (settings and angle) with content of read register step3. If a deviation in the comparison occurs, the power on test was not successful. Reprogramming is not allowed.
24. If point 19 is correct, the programming was successful.
25. Repeat point 1 to point 20 in case an AS5247U is used.

---

1. Guard band test:

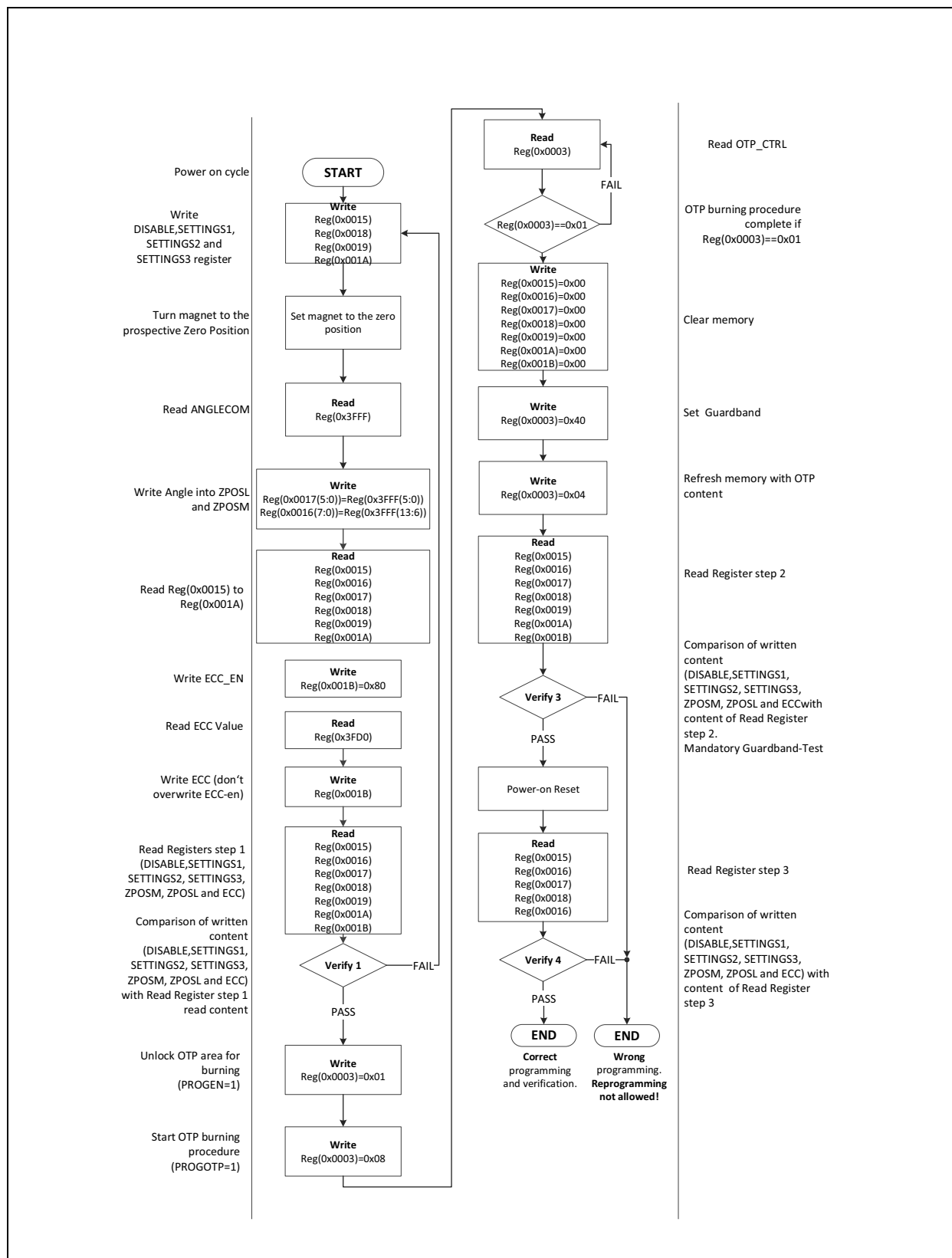
Restricted to temperature range: 25 °C ± 20 °C

Right after the programming procedure (max. 1 hour with same conditions 25°C ± 20 °C), same VDD voltage.

The guard band test is only for the verification of the burned OTP fuses during the programming sequence.

A use of the guard band in other cases is not allowed.

**Figure 64:**  
**OTP Memory Burn and Verification Flowchart**

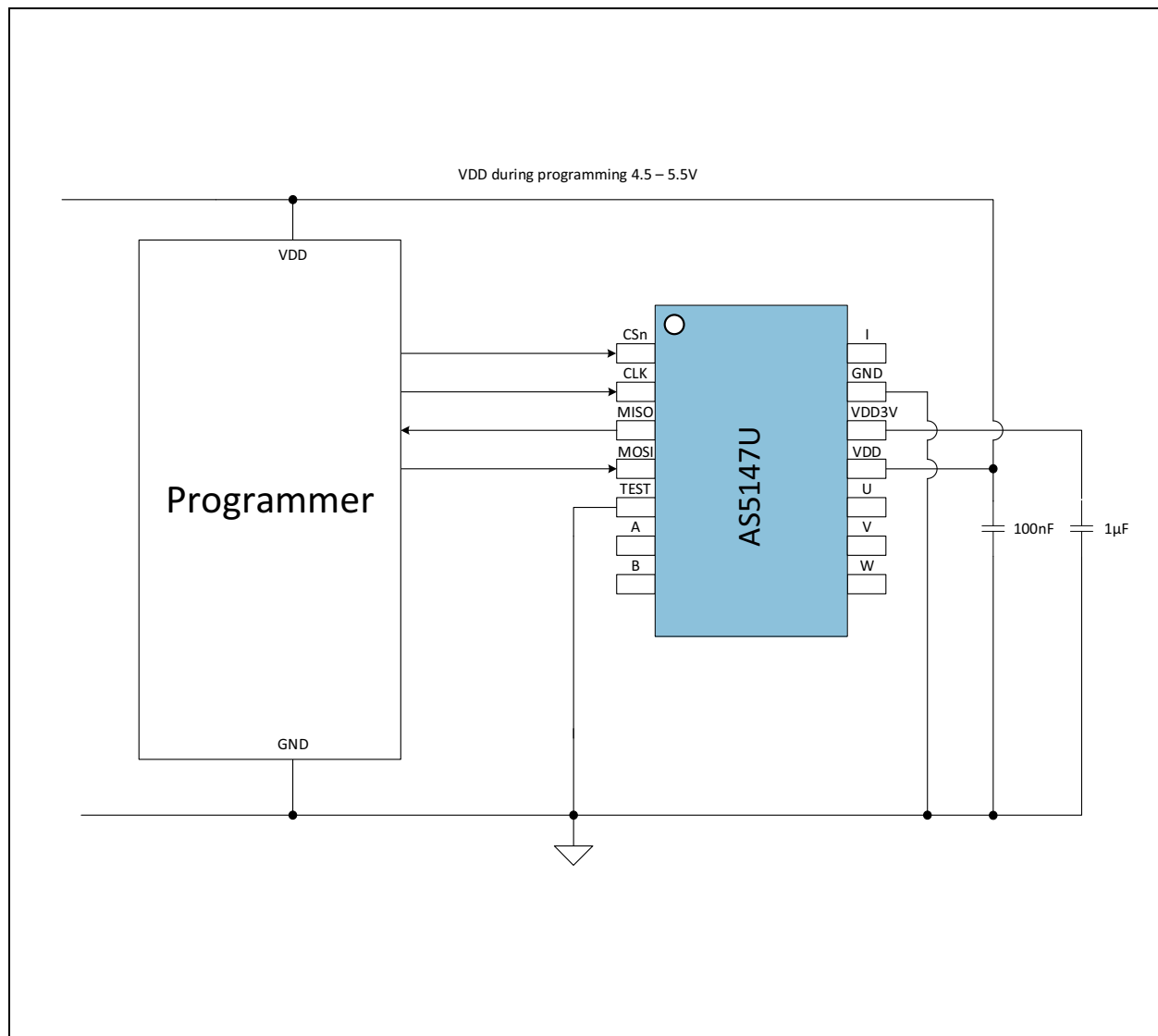


**Note(s):**

1. This procedure has to be done twice, for the top die and for the bottom die.
2. Device with wrong programming must not be used. Scrapping mandatory.

### Circuit Diagram

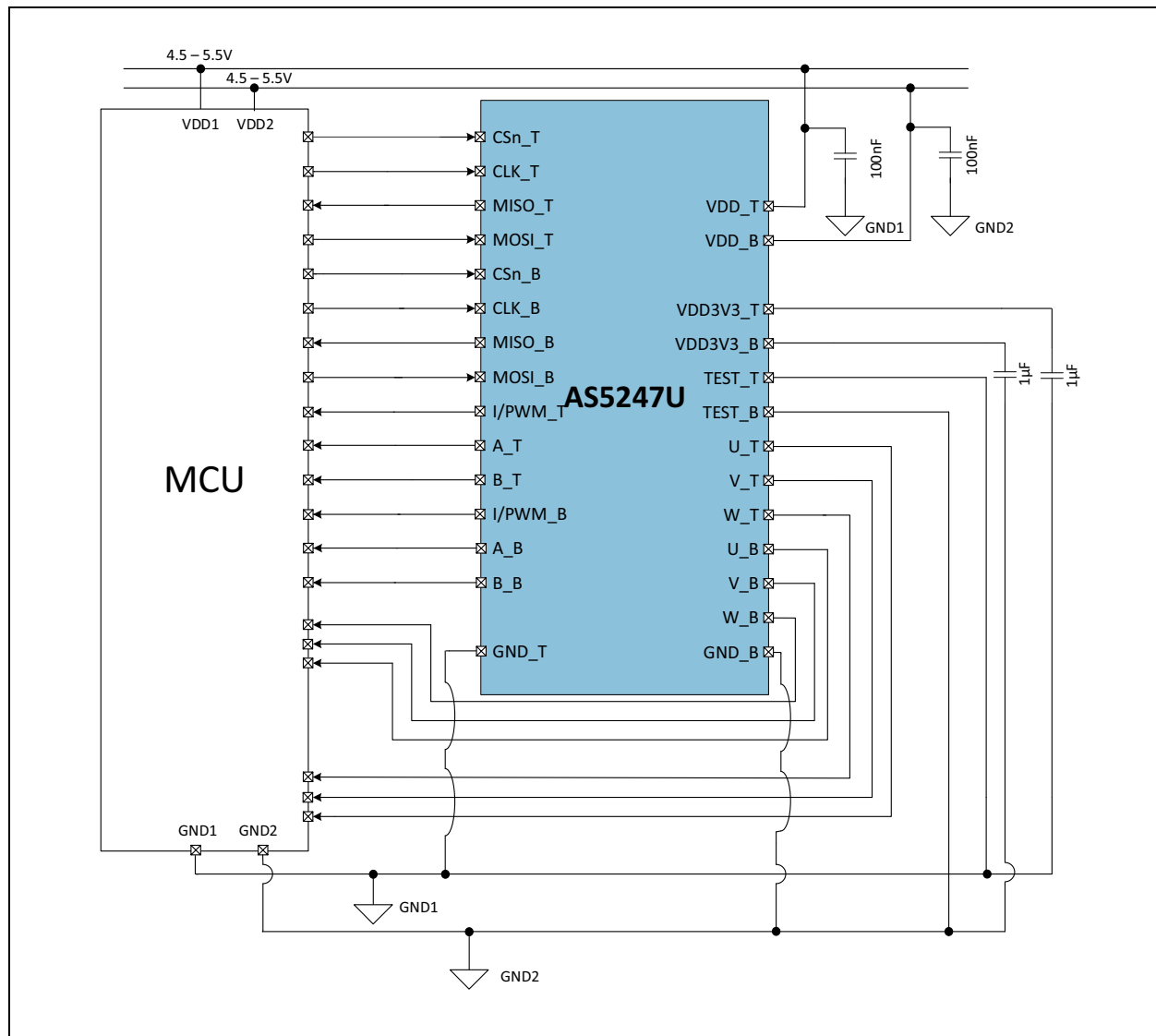
**Figure 65:**  
**Minimum Circuit Diagram for the AS5147U**



**Note(s):**

1. In terms of EMC and for remote application, additional protection circuit is necessary.

**Figure 66:**  
**Minimum Circuit Diagram for the AS5247U**



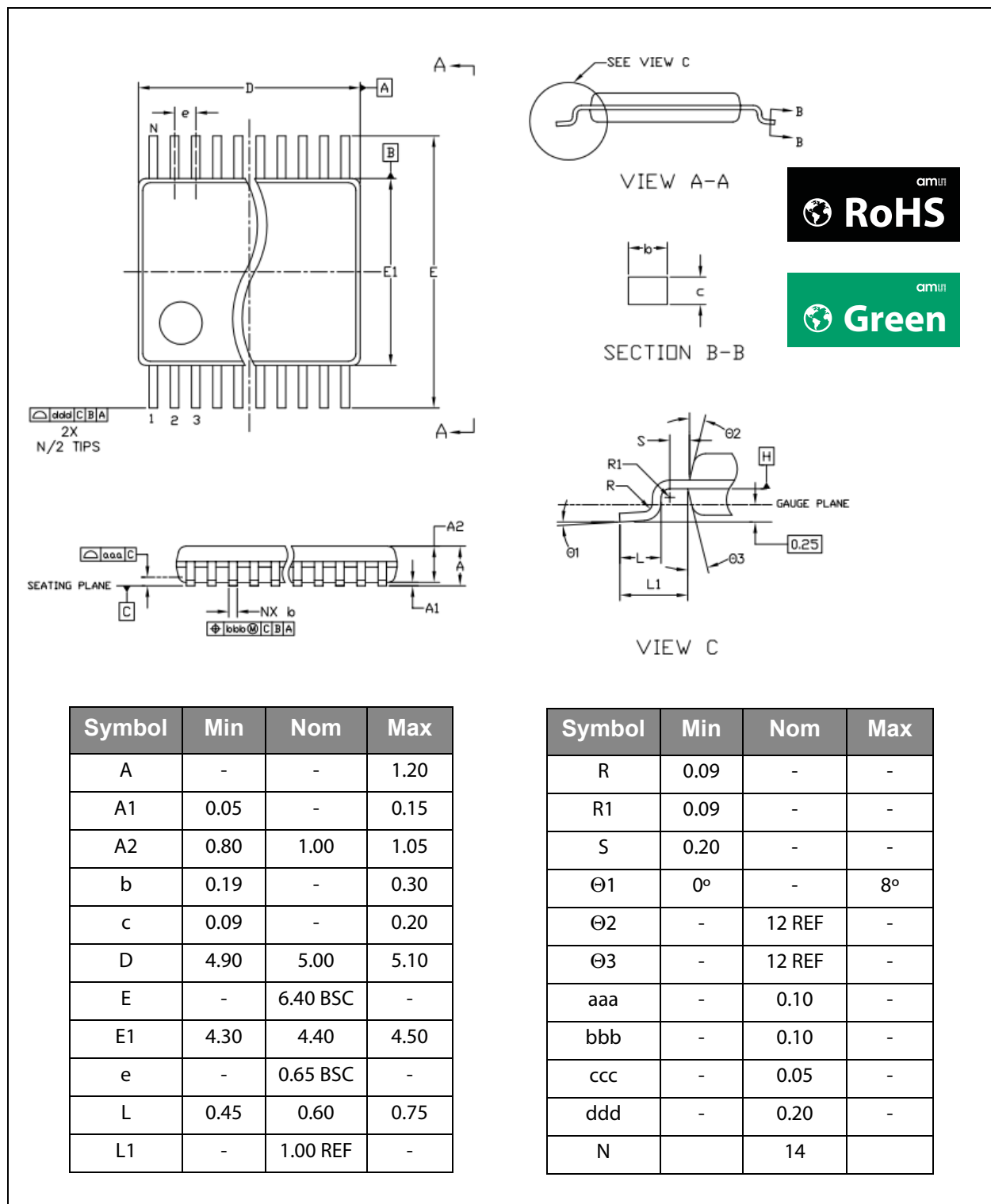
**Note(s):**

1. This application block diagram is showing the AS5247U using in a full redundant application. In terms of EMC and for remote application, additional protection circuit is necessary.



## Package Drawings & Markings

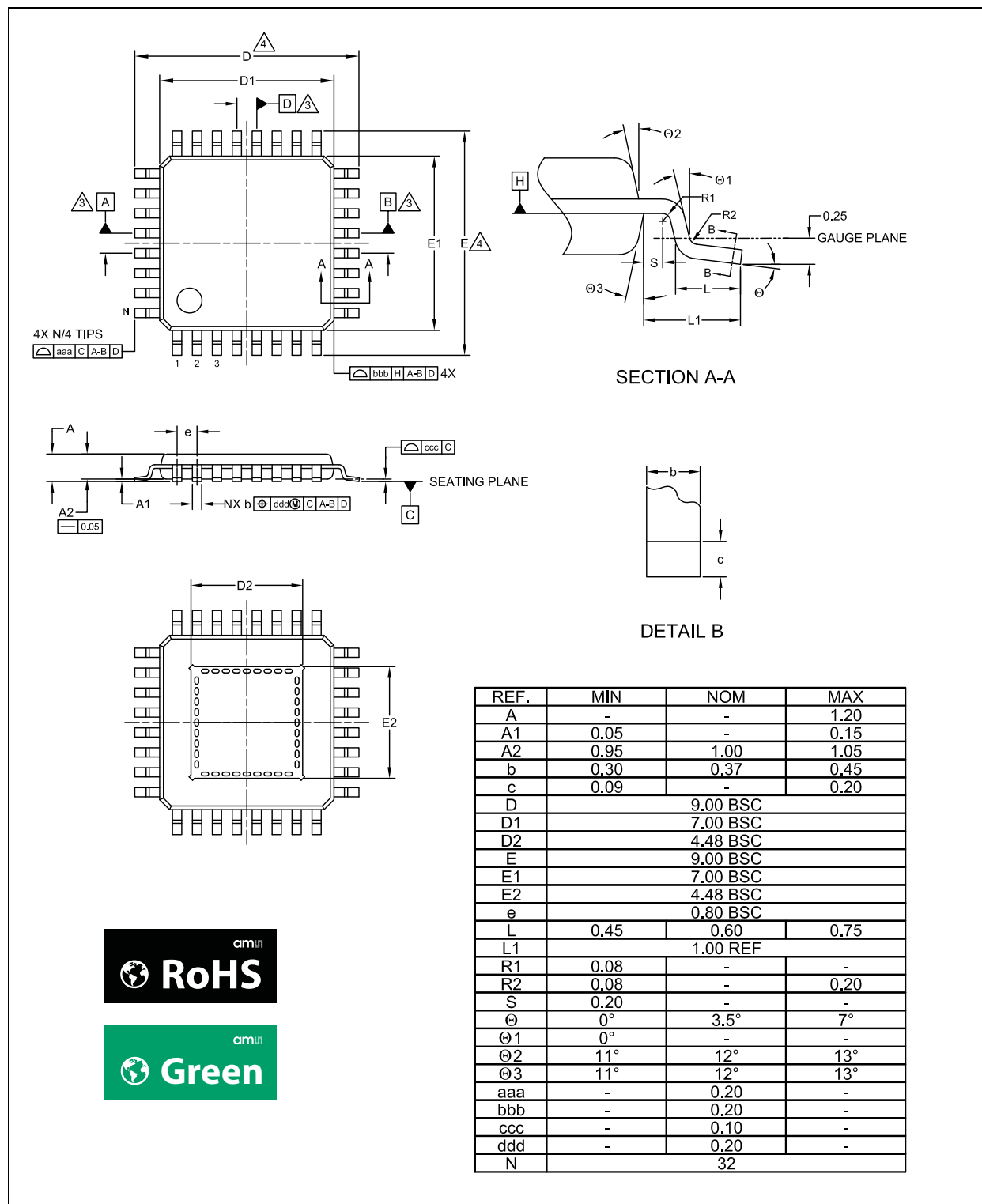
**Figure 67:**  
**TSSOP14 Package Outline Drawing AS5147U**



**Note(s):**

1. Dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. N is the total number of terminals.

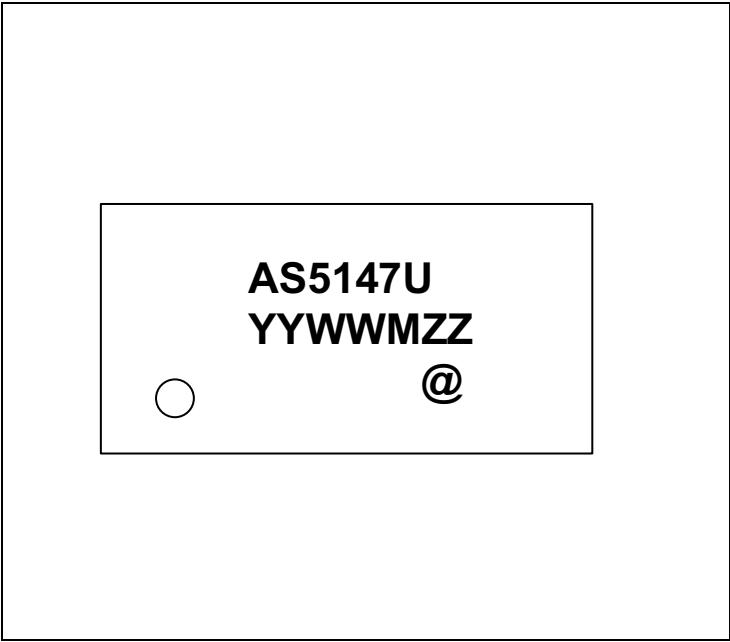
**Figure 68:**  
**TQFP32 Packaging Outline Drawing AS5247U**



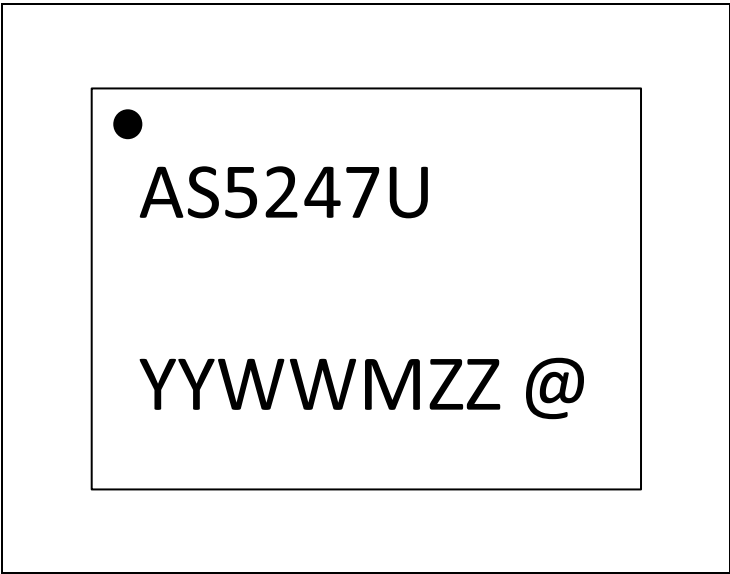
**Note(s):**

1. Dimensioning and tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters (angles in degrees).
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. N is the total number of terminals.

**Figure 69:**  
**AS5147U Package Marking**



**Figure 70:**  
**AS5247U Package Marking**

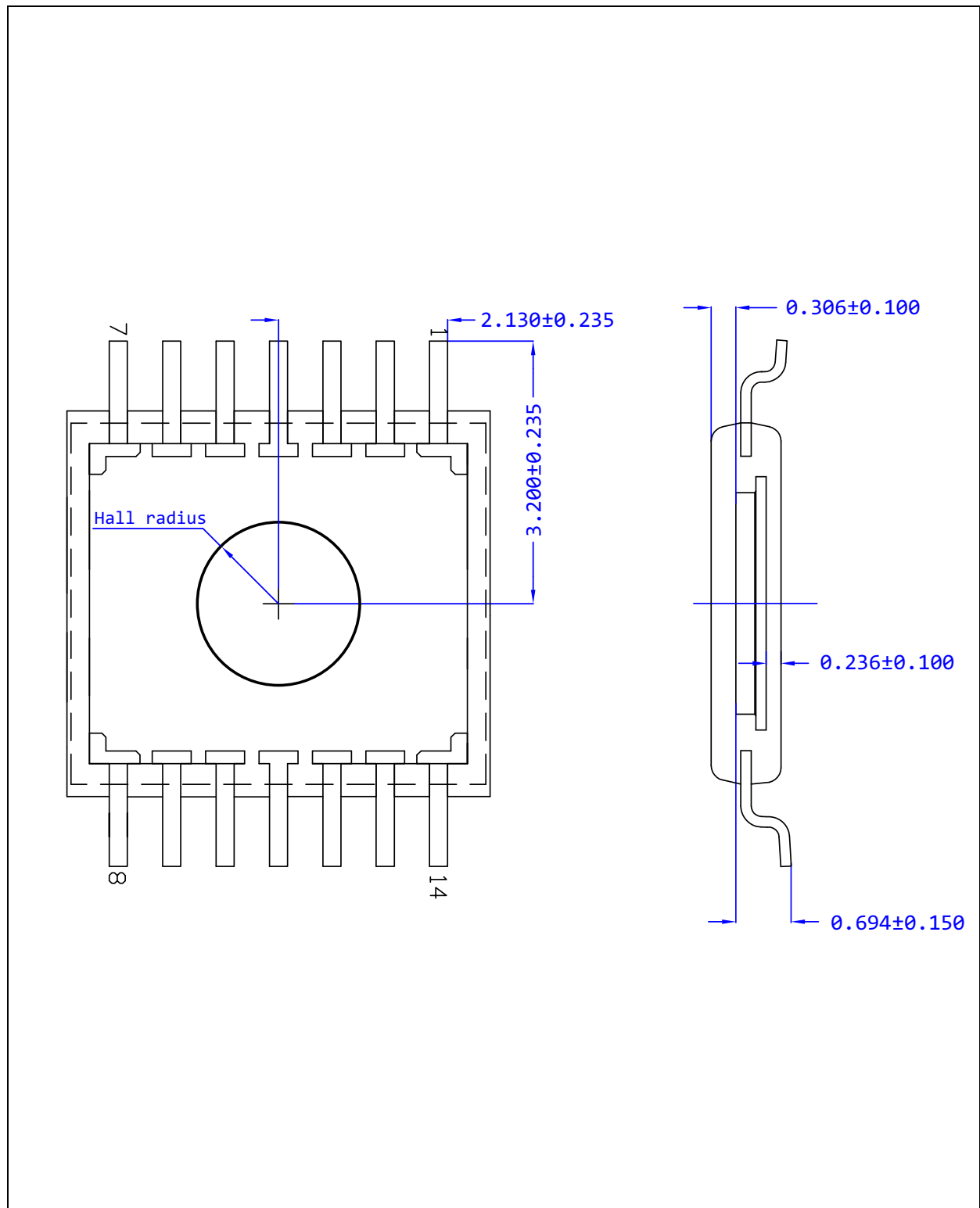


**Figure 71:**  
**Packaging Code**

| YY  | WW                 | M                | ZZ                              | @                 |
|---|--------------------|------------------|---------------------------------|-------------------|
| Last two digits of the manufacturing year | Manufacturing week | Plant identifier | Free choice / traceability code | Sublot identifier |

## Mechanical Data

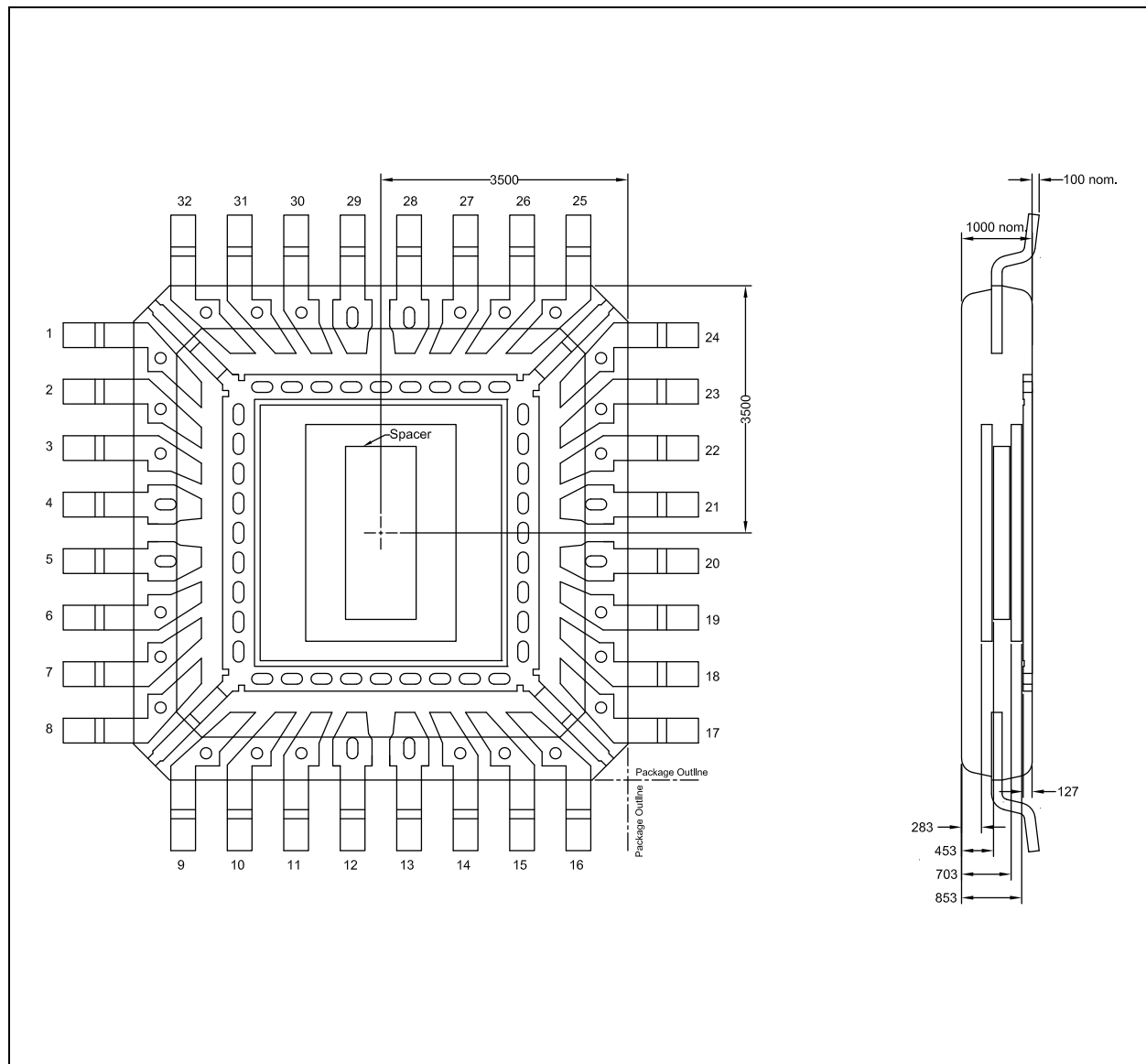
Figure 72:  
TSSOP14 Die Placement and Hall Array Position



**Note(s):**

1. Dimensions are in mm.
2. The Hall array center is located in the center of the IC package. Hall array radius is 1.1mm.
3. Die thickness is 203µm nominal.

**Figure 73:**  
**TQFP32 Die Placement and Hall Array Position**



**Note(s):**

1. All dimensions are in  $\mu\text{m}$ .
2. Die thickness: 150  $\mu\text{m}$  nom.
3. Adhesive thickness: 15  $\mu\text{m}$  nom.
4. Spacer thickness: 230  $\mu\text{m}$  typ.
5. The Hall array center is located in the center of the IC package. Hall array radius is 1.1 mm.

## Ordering & Contact Information

**Figure 74:**  
Ordering Information

| Ordering Code | Package | Marking | Delivery Form               | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5147U-HTSM  | TSSOP14 | AS5147U | 7" Tape & Reel in dry pack  | 500 pcs/reel      |
| AS5147U-HTST  | TSSOP14 | AS5147U | 13" Tape & Reel in dry pack | 4500 pcs/reel     |
| AS5247U-HTQT  | TQFP32  | AS5247U | 13" Tape & Reel in dry pack | 2000 pcs/reel     |

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| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice  |
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| Changes from 1-01 (2018-Nov-07) to current revision 1-04 (2020-Feb-12) | Page |
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| <b>1-01 (2018-Nov-07) to 1-02 (2020-Jan-27)</b>                        |      |
| Updated figure 68  | 50   |
| <b>1-02 (2020-Jan-27) to 1-03 (2020-Jan-29)</b>                        |      |
| Updated figure 5   | 5    |
| Updated figure 6   | 6    |
| <b>1-03 (2020-Jan-29) to 1-04 (2020-Feb-12)</b>                        |      |
| Updated figure 6   | 6    |
| Updated figure 68  | 50   |
| Updated figure 73  | 53   |

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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