


Features

- Superior circuit protection
- Overcurrent and overvoltage protection
- Blocks surges up to rated limits
- High-speed performance
- Small SMT package
- Agency listing: 

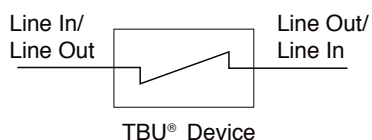
Applications

- Voice / VDSL cards
- Protection modules and dongles
- Process control equipment
- Test and measurement equipment
- General electronics

TBU-CA Series - TBU® High-Speed Protectors

General Information

The TBU-CA Series of Bourns® TBU® products are low capacitance single bidirectional high-speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.



Agency Listing

Description	
UL	File Number: E315805

The TBU® high-speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during surge events. The TBU® device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.

Absolute Maximum Ratings (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Number	Value	Unit
V _{imp}	Peak impulse voltage withstand with duration less than 10 ms	TBU-CA025-xxx-WH	250	V
		TBU-CA040-xxx-WH	400	
		TBU-CA050-xxx-WH	500	
		TBU-CA065-xxx-WH	650	
		TBU-CA085-xxx-WH	850	
V _{rms}	Continuous A.C. RMS voltage	TBU-CA025-xxx-WH	100	V
		TBU-CA040-xxx-WH	200	
		TBU-CA050-xxx-WH	250	
		TBU-CA065-xxx-WH	300	
		TBU-CA085-xxx-WH	425	
T _{op}	Operating temperature range		-55 to +125	°C
T _{stg}	Storage temperature range		-65 to +150	°C
T _{jmax}	Maximum Junction Temperature		+125	°C
ESD	HBM ESD protection per IEC 61000-4-2		±2	kV

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WARNING Cancer and Reproductive Harm - www.P65Warnings.ca.gov

*RoHS Directive 2002/95/EC Jan. 27, 2003 including annex and RoHS Recast 2011/65/EU June 8, 2011. Specifications are subject to change without notice. Users should verify actual device performance in their specific applications. The products described herein and this document are subject to specific legal disclaimers as set forth on the last page of this document, and at www.bourns.com/docs/legal/disclaimer.pdf

TBU-CA Series - TBU® High-Speed Protectors

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Electrical Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Number	Min.	Typ.	Max.	Unit
I _{trigger}	Current required for the device to go from operating state to protected state	TBU-CAxxx-050-WH	50	75	100	mA
		TBU-CAxxx-100-WH	100	150	200	
		TBU-CAxxx-200-WH	200	300	400	
		TBU-CAxxx-300-WH	300	450	600	
		TBU-CAxxx-500-WH	500	750	1000	
R _{device}	Series resistance of the TBU device	V _{imp} = 250 V I _{trigger} (min.) = 50 mA		13.3	15.3	Ω
		V _{imp} = 250 V I _{trigger} (min.) = 100 mA		7.1	8.2	
		V _{imp} = 250 V I _{trigger} (min.) = 200 mA		4.2	4.8	
		V _{imp} = 250 V I _{trigger} (min.) = 300 mA		3.2	3.8	
		V _{imp} = 250 V I _{trigger} (min.) = 500 mA		2.6	3.0	
		V _{imp} = 400 V I _{trigger} (min.) = 50 mA		14.3	16.5	
		V _{imp} = 400 V I _{trigger} (min.) = 100 mA		8.1	9.4	
		V _{imp} = 400 V I _{trigger} (min.) = 200 mA		5.2	6.0	
		V _{imp} = 400 V I _{trigger} (min.) = 300 mA		4.3	5.0	
		V _{imp} = 400 V I _{trigger} (min.) = 500 mA		3.6	4.2	
		V _{imp} = 500 V I _{trigger} (min.) = 50 mA		15.7	18.0	
		V _{imp} = 500 V I _{trigger} (min.) = 100 mA		9.5	10.9	
		V _{imp} = 500 V I _{trigger} (min.) = 200 mA		6.6	7.5	
		V _{imp} = 500 V I _{trigger} (min.) = 300 mA		5.6	6.5	
		V _{imp} = 500 V I _{trigger} (min.) = 500 mA		5.0	5.7	
		V _{imp} = 650 V I _{trigger} (min.) = 50 mA		17.7	20.3	
		V _{imp} = 650 V I _{trigger} (min.) = 100 mA		11.5	13.2	
		V _{imp} = 650 V I _{trigger} (min.) = 200 mA		8.6	9.8	
		V _{imp} = 650 V I _{trigger} (min.) = 300 mA		7.6	8.8	
		V _{imp} = 650 V I _{trigger} (min.) = 500 mA		7.0	8.0	
		V _{imp} = 850 V I _{trigger} (min.) = 50 mA		21.4	24.5	
		V _{imp} = 850 V I _{trigger} (min.) = 100 mA		15.2	17.4	
		V _{imp} = 850 V I _{trigger} (min.) = 200 mA		12.3	14.0	
		V _{imp} = 850 V I _{trigger} (min.) = 300 mA		11.3	13.0	
		V _{imp} = 850 V I _{trigger} (min.) = 500 mA		10.7	12.2	
t _{block}	Time for the device to go from normal operating state to protected state				1	μs
I _Q	Current through the triggered TBU® device with 50 Vdc circuit voltage		0.25	0.50	1.00	mA
V _{reset}	Voltage below which the triggered TBU® device will transition to normal operating state		12	16	20	V
R _{th(j-l)}	Junction to package pads - FR4 using recommended pad layout			98		°C/W
R _{th(j-l)}	Junction to package pads - FR4 using heat sink on board (6 cm ²) (1 in ²)			40		°C/W

Environmental Characteristics

Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

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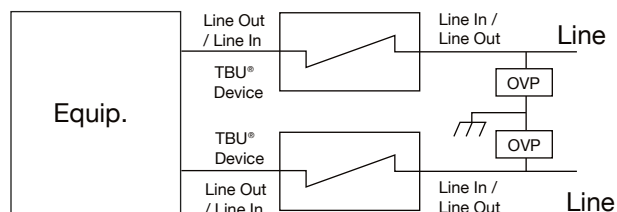
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TBU-CA Series - TBU® High-Speed Protectors

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Reference Application

The TBU® devices are general use protectors used in a wide variety of applications. The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV.



Basic TBU Operation

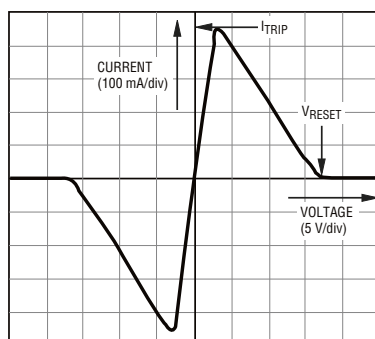
The TBU® device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU® device operates in approximately 1 μ s - once line current exceeds the TBU® device's trigger current $I_{trigger}$. When operated, the TBU® device will limit the current to less than the $I_{trigger}$ value within the t_{block} duration. If voltage above V_{reset} is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

After the surge, the TBU® device resets when the voltage across the TBU® device falls to the V_{reset} level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below V_{reset} (such as unpowered signal lines).

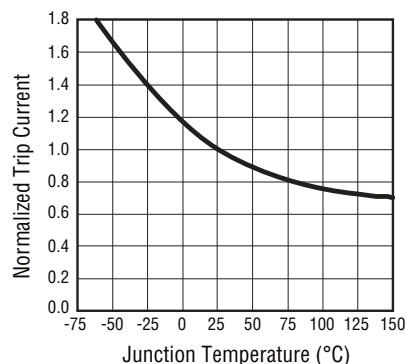
If the line has a normal DC bias above V_{reset} , the voltage across the TBU® device may not fall below V_{reset} after the surge. In such cases, special care needs to be taken to ensure that the TBU® device will reset, with software monitoring as one method used to accomplish this. Bourns application engineers can provide further assistance.

Performance Graphs

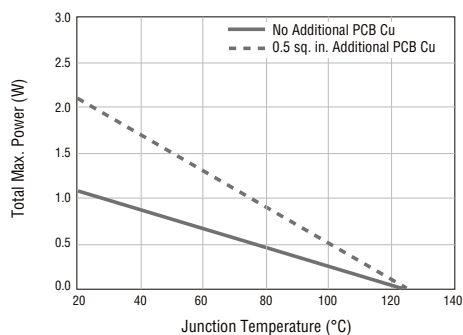
Typical V-I Characteristics (TBU-CA050-300-WH)



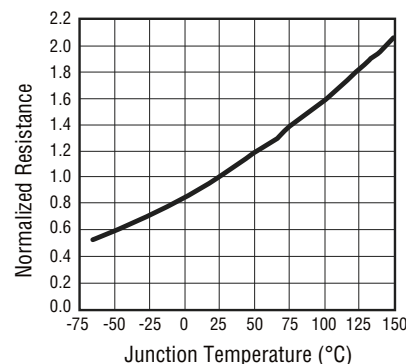
Typical Trigger Current vs. Temperature



Power Derating Curve



Typical Resistance vs. Temperature



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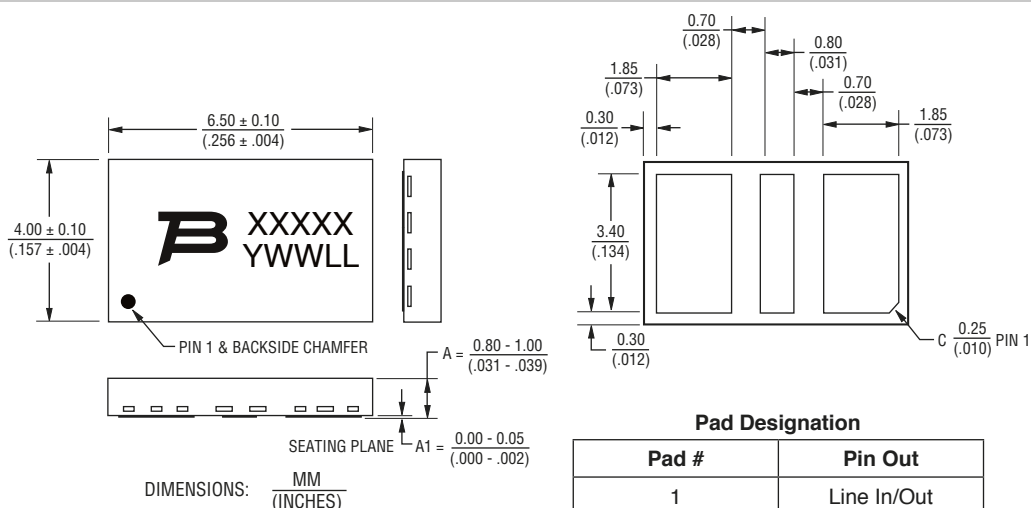
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TBU-CA Series - TBU® High-Speed Protectors

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Product Dimensions

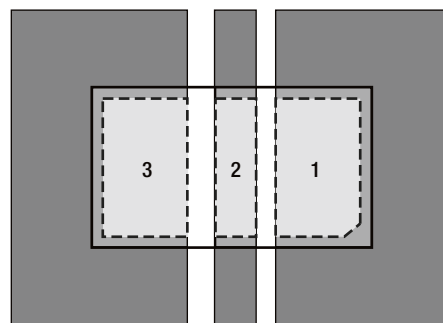


Pad Designation

Pad #	Pin Out
1	Line In/Out
2	NU
3	Line Out/In

Recommended Pad Layout

TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should be soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.



Dark grey areas show added PCB copper area for better thermal resistance.

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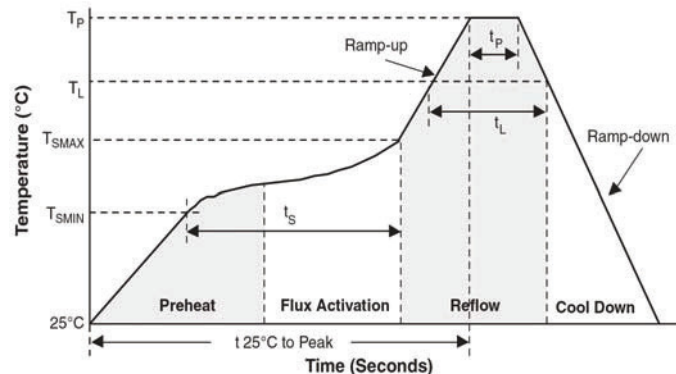
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Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (T _{smax} to T _p)	3 °C/sec. max.
Preheat <ul style="list-style-type: none"> - Temperature Min. (T_{smin}) - Temperature Max. (T_{smax}) - Time (t_{smin} to t_{smax}) 	150 °C 200 °C 60-180 sec.
Time maintained above: <ul style="list-style-type: none"> - Temperature (T_L) - Time (t_L) 	217 °C 60-150 sec.
Peak/Classification Temperature (T _p)	260 °C
Time within 5 °C of Actual Peak Temp. (t _p)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



How to Order

TBU - CA 085 - 500 - WH

TBU® Product _____

Series _____
CA = Bi-Series

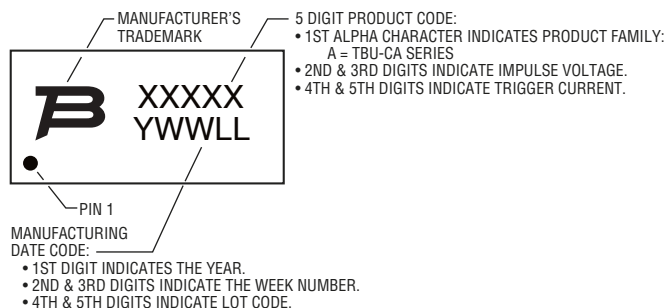
Impulse Voltage Rating _____
025 = 250 V
040 = 400 V
050 = 500 V
065 = 650 V
085 = 850 V

Trigger Current _____
050 = 50 mA
100 = 100 mA
200 = 200 mA
300 = 300 mA
500 = 500 mA

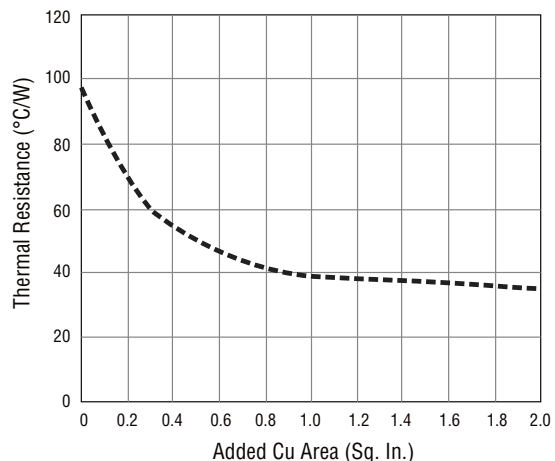
Hold to Trip Ratio Suffix _____
W = Hold to Trip Ratio

Package Suffix _____
H = DFN Package

Typical Part Marking



Thermal Resistance vs Additional PCB Cu Area



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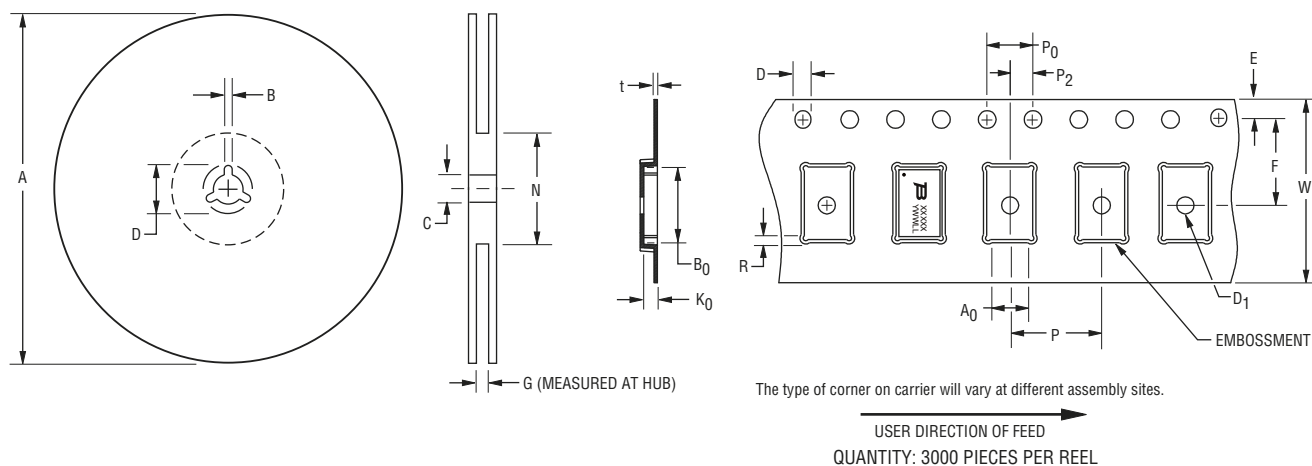
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Packaging Specifications



A		B		C		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
326 (12.835)	330 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

A0		B0		D		D1		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
4.3 (.169)	4.5 (.177)	6.7 (.264)	6.9 (.272)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)

K0		P		P0		P2		R		t	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.0 (.039)	1.2 (.047)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0 (0)	0.5 (.020)	0.25 (.010)	0.35 (.014)

W	
Min.	Max.
15.7 (.618)	16.3 (.642)

DIMENSIONS: $\frac{\text{MM}}{(\text{INCHES})}$

REV. 03/18

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